# SNx4LVC00A Quadruple 2-Input Positive-NAND Gates

## 1 Features

- ESD protection exceeds JESD 22
  - 2000V Human-Body Model
  - 1000V Charged-Device Model
- SN74LVC00A operates from 1.65V to 3.6V
- SN54LVC00A operates from 2V to 3.6V
- SNx4LVC00A specified from –40°C to +85°C and –40°C to +125°C
- SN54LVC00A specified from –55°C to +125°C
- Inputs accept voltages to 5.5V
- Max $t_{pd}$ of 4.3ns at 3.3V
- Typical $V_{OLP}$ (output ground bounce) < 0.8V at $V_{CC}$ = 3.3V, $T_A$ = 25°C
- Typical $V_{OHV}$ (output $V_{OH}$ undershoot) > 2V at $V_{CC}$ = 3.3V, $T_A$ = 25°C
- Latch-up performance exceeds 250 mA per JESD 17
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## 2 Applications

- AV Receivers
- Audio Docks: Portable
- Blu-Ray Players and Home Theater
- MP3 Players or Recorders
- Personal Digital Assistants (PDAs)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drives (SSDs): Client and Enterprise
- TVs: LCD, Digital, and High-Definition (HDTV)
- Tablets: Enterprise
- Video Analytics: Server
- Wireless Headsets, Keyboards, and Mice

## 3 Description

The SN54LVC00A quadruple 2-input positive-NAND gate is designed for 2.7V to 3.6V $V_{CC}$ operation, and the SN74LVC00A quadruple 2-input positive-NAND gate is designed for 1.65V to 3.6V $V_{CC}$ operation.

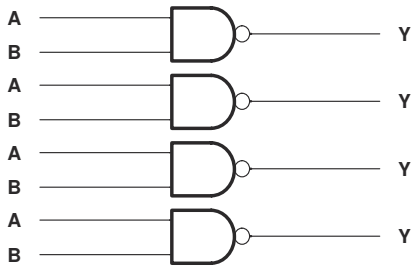
The SNx4LVC00A devices perform the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V system environment.

**Device Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE(3) |
|---|---|---|---|
| SNx4LVC00A | BQA (WQFN, 14) | 3mm × 2.5mm | 3mm × 2.5mm |
| | D (SOIC, 14) | 8.65mm × 6mm | 8.65 mm × 3.91 mm |
| | DB (SSOP, 14) | 6.2mm × 7.8mm | 6.20 mm × 5.30 mm |
| | NS (SOP, 14) | 10.2mm × 7.8mm | 10.30 mm × 5.30 mm |
| | PW (TSSOP, 14) | 5mm × 4.4mm | 5.00 mm × 4.40 mm |
| | RGY (VQFN, 14) | 3.5mm × 3.5mm | 3.50 mm × 3.50 mm |
| | FK (LCCC, 20) | 8.9mm x 8.9mm | 8.89 mm × 8.89 mm |
| | J (CDIP, 14) | 19.55mm x 7.9mm | 19.55 mm x 6.7mm |
| | W (CFP, 14) | 9.21mm x 9mm | 9.21mm x 6.28mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Simplified Schematic**

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## 4 Pin Configuration and Functions

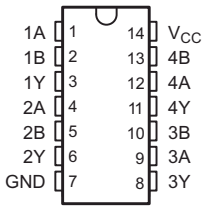
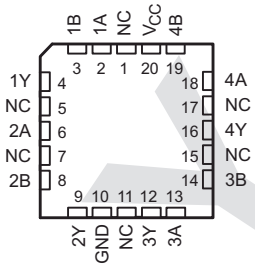



**Figure 4-1. SN54LVC00A J or W Package; SN74LVC00A D, DB, NS, or PW Package 14-Pin CDIP, CFP SOIC, SSOP, SO, or TSSOP (Top View)**




NC - No internal connection

**Figure 4-2. SN54LVC00A FK Package 20-Pin LCCC (Top View)**

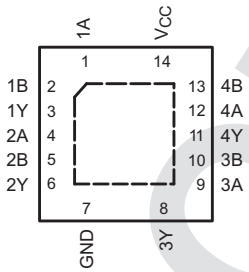



**Figure 4-3. SN74LVC00A BQA or RGY Package 14-Pin WQFN or VQFN (Top View)**

**Table 4-1. Pin Functions**

| PIN | | | | | TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|
| NAME | SN74LVC00A | | SN54LVC00A | | | |
| | D, DB, NS, PW | BQA, RGY | J, W | FK | | |
| 1A | 1 | 1 | 1 | 2 | I | Gate 1 input |
| 1B | 2 | 2 | 2 | 3 | I | Gate 1 input |
| 1Y | 3 | 3 | 3 | 4 | O | Gate 1 output |
| 2A | 4 | 4 | 4 | 6 | I | Gate 2 input |
| 2B | 5 | 5 | 5 | 8 | I | Gate 2 input |
| 2Y | 6 | 6 | 6 | 9 | O | Gate 2 output |
| GND | 7 | 7 | 7 | 10 | I | Ground Pin |
| 3Y | 8 | 8 | 8 | 12 | O | Gate 3 output |
| 3A | 9 | 9 | 9 | 13 | I | Gate 3 input |
| 3B | 10 | 10 | 10 | 14 | I | Gate 3 input |
| 4Y | 11 | 11 | 11 | 16 | O | Gate 4 output |
| 4A | 12 | 12 | 12 | 18 | I | Gate 4 input |
| 4B | 13 | 13 | 13 | 19 | I | Gate 4 input |
| $V_{CC}$ | 14 | 14 | 14 | 20 | — | Positive supply |
| NC | — | — | — | 1 | — | No Connection |
| | | | | 5 | | |
| | | | | 7 | | |
| | | | | 11 | | |
| | | | | 15 | | |
| | | | | 17 | | |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage(2) | | –0.5 | 6.5 | V |
| $V_O$ | Output voltage (2) (3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| $V_{CC}$ | Continuous current through GND | | | ±100 | mA |
| $P_{tot}$ | Power dissipation(4) (5) | $T_A$ = –40°C to +125°C | | 500 | mW |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CC}$ is provided in the *Recommended Operating Conditions* table.
(4) For the D package: above 70°C, the value of $P_{tot}$ derates linearly with 8 mW/K.
(5) For the DB, NS, and PW packages: above 60°C, the value of $P_{tot}$ derates linearly with 5.5 mW/K.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions, SN54LVC00A

over operating free-air temperature range (unless otherwise noted)(1)

| | | | SN54LVC00A –55°C to +125°C | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $V_{CC}$ | Supply voltage | Operating | 2 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | V |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2.7 V | | –12 | mA |
| | | $V_{CC}$ = 3 V | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2.7 V | | 12 | mA |
| | | $V_{CC}$ = 3 V | | 24 | |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

## 5.4 Recommended Operating Conditions, SN74LVC00A

over operating free-air temperature range (unless otherwise noted)(1)

| | | | SN74LVC00A | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | –40°C to 85°C | | –40°C to 125°C | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 3.6 | 1.65 | 3.6 | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | 1.5 | | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | | 0.65 × $V_{CC}$ | | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | 1.7 | | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | 2 | | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | 0.35 × $V_{CC}$ | | 0.35 × $V_{CC}$ | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | | 0.7 | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | | 0.8 | | 0.8 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | –4 | | –4 | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | –8 | | –8 | | –8 | |
| | | $V_{CC}$ = 2.7 V | | –12 | | –12 | | –12 | |
| | | $V_{CC}$ = 3 V | | –24 | | –24 | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | | 4 | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | | 8 | | 8 | |
| | | $V_{CC}$ = 2.7 V | | 12 | | 12 | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | | 24 | | 24 | |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

## 5.5 Thermal Information

| THERMAL METRIC(1) | | SN74LVC00A | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BQA (WQFN) | D (SOIC) | DB (SSOP) | NS (SOP) | PW (TSSOP) | RGY (VQFN) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 102.3 | 127.8 | 140.4 | 123.8 | 150.8 | 92.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.6 Electrical Characteristics, SN54LVC00A

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | SN54LVC00A –55°C to +125°C | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –100 µA | | 2.7 V to 3.6 V | $V_{CC}$ – 0.2 | | V |
| | $I_{OH}$ = –12 mA | | 2.7 V | 2.2 | | |
| | | | 3 V | 2.4 | | |
| | $I_{OH}$ = –24 mA | | 3 V | 2.2 | | |
| $V_{OL}$ | $I_{OL}$ = 100 µA | | 2.7 V to 3.6 V | | 0.2 | V |
| | $I_{OL}$ = 12 mA | | 2.7 V | | 0.4 | |
| | $I_{OL}$ = 24 mA | | 3 V | | 0.55 | |
| $I_I$ | $V_I$ = 5.5 V or GND | | 3.6 V | | ±5 | µA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, | $I_O$ = 0 | 3.6 V | | 10 | µA |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V, | Other inputs at $V_{CC}$ or GND | 2.7 V to 3.6 V | | 500 | µA |

## 5.7 Electrical Characteristics, SN74LVC00A

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | SN74LVC00A $T_A$ = 25°C | | | –40°C to +85°C | | –40°C to +125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –100 µA | 1.65 V to 3.6 V | $V_{CC}$ – 0.2 | | | $V_{CC}$ – 0.2 | | $V_{CC}$ – 0.3 | | V |
| | $I_{OH}$ = –4 mA | 1.65 V | 1.29 | | | 1.2 | | 1.05 | | |
| | $I_{OH}$ = –8 mA | 2.3 V | 1.9 | | | 1.7 | | 1.55 | | |
| | $I_{OH}$ = –12 mA | 2.7 V | 2.2 | | | 2.2 | | 2.05 | | |
| | | 3 V | 2.4 | | | 2.4 | | 2.25 | | |
| | $I_{OH}$ = –24 mA | 3 V | 2.3 | | | 2.2 | | 2 | | |
| $V_{OL}$ | $I_{OL}$ = 100 µA | 1.65 V to 3.6 V | | | 0.1 | | 0.2 | | 0.3 | V |
| | $I_{OL}$ = 4 mA | 1.65 V | | | 0.24 | | 0.45 | | 0.6 | |
| | $I_{OL}$ = 8 mA | 2.3 V | | | 0.3 | | 0.7 | | 0.85 | |
| | $I_{OL}$ = 12 mA | 2.7 V | | | 0.4 | | 0.4 | | 0.6 | |
| | $I_{OL}$ = 24 mA | 3 V | | | 0.55 | | 0.55 | | 0.8 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 3.6 V | | | ±1 | | ±5 | | ±20 | µA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 3.6 V | | | 1 | | 10 | | 40 | µA |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | 2.7 V to 3.6 V | | | 500 | | 500 | | 5000 | µA |
| $C_i$ | $V_I = V_{CC}$ or GND | 3.3 V | | 5 | | | | | | pF |

## 5.8 Switching Characteristics, SN54LVC00A

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | SN54LVC00A –55°C to +125°C | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| $t_{pd}$ | A or B | Y | 2.7 V | | 5.1 | ns |
| | | | 3.3 V ± 0.3 V | 1 | 4.3 | |

## 5.9 Switching Characteristics, SN74LVC00A

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | SN74LVC00A | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | –40°C to +85°C | | –40°C to +125°C | | |
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | Y | 1.8 V ± 0.15 V | 1 | 6 | 12 | 1 | 12.5 | 1 | 14 | ns |
| | | | 2.5 V ± 0.2 V | 1 | 4.6 | 5.9 | 1 | 6.4 | 1 | 7.9 | |
| | | | 2.7 V | 1 | 4.3 | 4.9 | 1 | 5.1 | 1 | 6.5 | |
| | | | 3.3 V ± 0.3 V | 1 | 3.5 | 4.1 | 1 | 4.3 | 1 | 5.5 | |
| $t_{sk(o)}$ | | | 3.3 V ± 0.3 V | | | | | 1 | | 1.5 | ns |

## 5.10 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per gate | f = 10 MHz | 1.8 V | 18 | pF |
| | | | 2.5 V | 18 | |
| | | | 3.3 V | 19 | |

## 5.11 Typical Characteristics

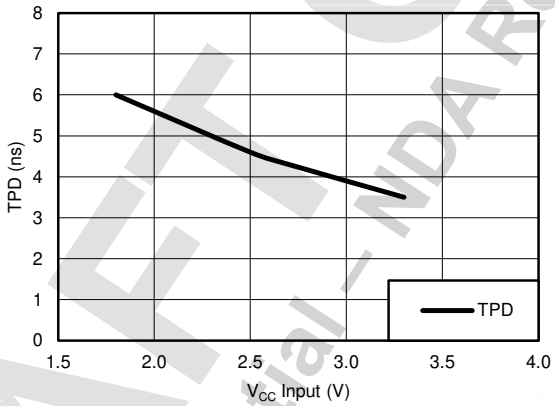
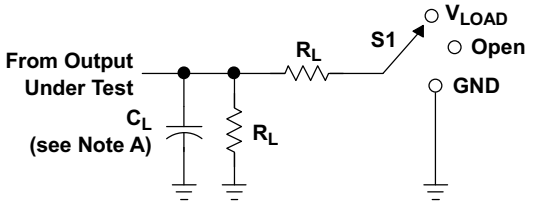



**Figure 5-1. TPD vs $V_{CC}$ ($T_A$ = 25°C)**

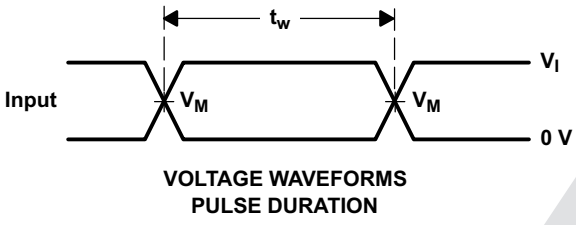
# 6 Parameter Measurement Information



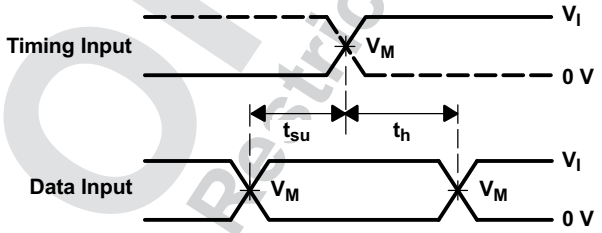

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

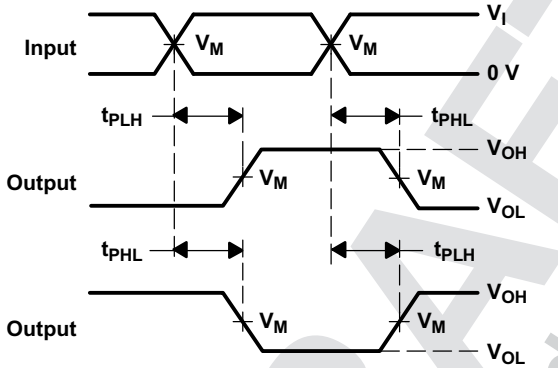
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V ± 0.3 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



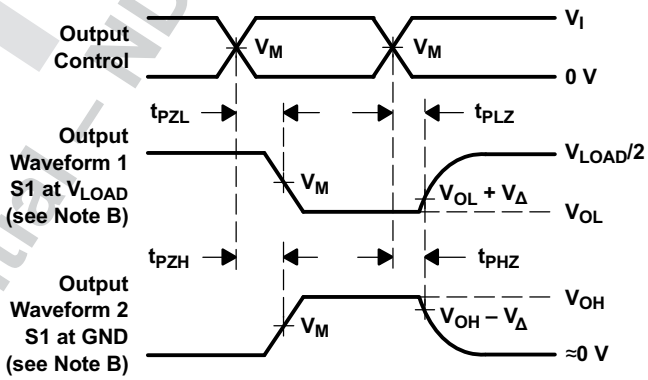

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 6-1. Load Circuit and Voltage Waveforms**

# 7 Detailed Description

## 7.1 Overview

The maximum sink and source current is 24 mA.

Inputs can be driven from 1.8-V, 2.5-V, 3.3-V (LVTTL), or 5-V (CMOS) devices. This feature allows the use of this device as translators in a mixed-system environment.

## 7.2 Functional Block Diagram

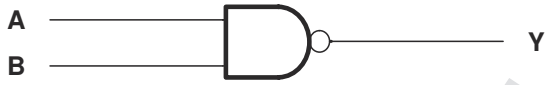



**Figure 7-1. Logic Diagram, Each Gate (Positive Logic)**

## 7.3 Feature Description

### *7.3.1 Balanced High-Drive CMOS Push-Pull Outputs*

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the *Section 5.1* must be followed at all times.

### *7.3.2 Standard CMOS Inputs*

Standard CMOS inputs are high impedance and are typically modelled as a resistor in parallel with the input capacitance given in the *Section 5.6* and *Section 5.7*. The worst case resistance is calculated with the maximum input voltage, given in the *Section 5.1*, and the maximum input leakage current, given in the *Section 5.6* and *Section 5.7*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in *Section 5.3* and *Section 5.4* to avoid excessive currents and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be utilized to condition the input signal prior to the standard CMOS input.

### *7.3.3 Clamp Diodes*

The inputs and outputs to this device have negative clamping diodes.

**CAUTION**

Voltages beyond the values specified in the *Section 5.1* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

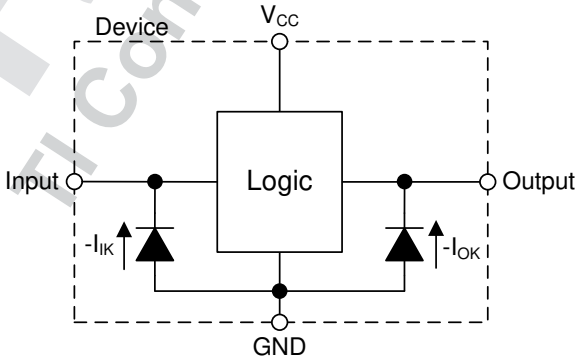



**Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output**

### 7.3.4 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Section 5.1*.

## 7.4 Device Functional Modes

Table 7-1 lists the functional modes of SN54LVC00A and SN74LVC00A.

**Table 7-1. Function Table (Each Gate)**

| INPUTS | | OUTPUT Y |
|---|---|---|
| A | B | |
| H | H | L |
| L | X | H |
| X | L | H |

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

SN74LVC00A is a high-drive CMOS device that can be used for a multitude of buffer-type functions. It can produce 24 mA of drive current at 3.3 V. Therefore, this device is ideal for driving multiple inputs and for high-speed applications up to 100 MHz. The inputs and outputs are 5.5-V tolerant allowing the device to allowing the device to perform mixed-voltage input down translation. For example the A input can be 3.3 V and the B input can be 5 V, while $V_{CC}$ = 2.5 V and the device will operate properly to output a 2.5 V signal.

## 8.2 Typical Application

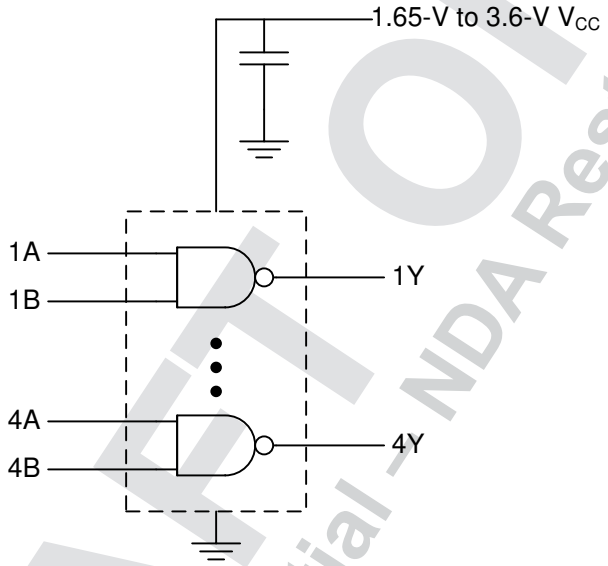



**Figure 8-1. Typical NAND Gate Application and Supply Voltage**

### *8.2.1 Design Requirements*

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

### *8.2.2 Detailed Design Procedure*

1. Recommended Input Conditions
   - Rise time and fall time specs: See (Δt/ΔV) in the *Section 5.4* table.
   - Specified high and low levels: See ($V_{IH}$ and $V_{IL}$) in the *Section 5.4* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC}$.
2. Recommended Output Conditions
   - Load currents should not exceed 25 mA per output and 50 mA total for the part.
   - Outputs should not be pulled above 5.5 V.

### 8.2.3 Application Curve

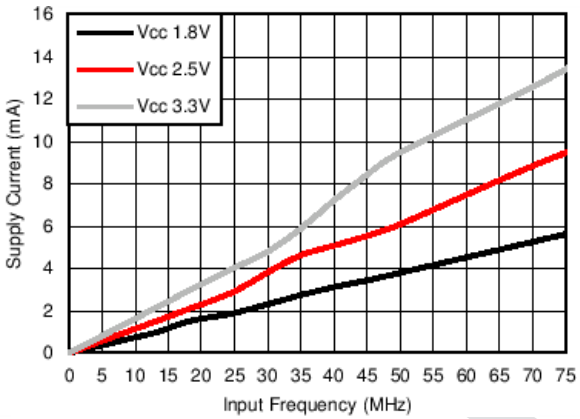



**Figure 8-2. $I_{CC}$ vs Frequency**

## Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Section 5.4* table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended; if there are multiple $V_{CC}$ pins, then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 8.3 Layout

### 8.3.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Section 8.3.2 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

### 8.3.2 Layout Example

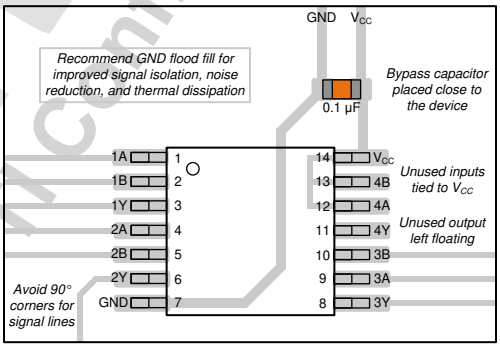



**Figure 8-3. Layout Diagram for the SNx4LVC00A**

# 9 Device and Documentation Support

## 9.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 9-1. Related Links**

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54LVC00A | Click here | Click here | Click here | Click here | Click here |
| SN74LVC00A | Click here | Click here | Click here | Click here | Click here |

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### *9.3.1 Community Resources*

## 9.4 Trademarks

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## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 10

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision T (May 2024) to Revision U (July 2024) | Page |
|---|---|
| • Updated RθJA values: D = 86 to 127.8, all values in °C/W | 5 |
| • Added *Typical Characteristics* | 7 |

| Changes from Revision S (March 2024) to Revision T (May 2024) | Page |
|---|---|
| • Updated RθJA values: DB = 96 to 140.4, NS = 76 to 123.8, PW = 113 to 150.8, RGY = 47 to 92.1; Updated DB, NS, PW, and RGY packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W | 5 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9753301Q2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9753301Q2A SNJ54LVC 00AFK | Samples |
| 5962-9753301QCA | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9753301QC A SNJ54LVC00AJ | Samples |
| 5962-9753301QDA | ACTIVE | CFP | W | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9753301QD A SNJ54LVC00AW | Samples |
| 5962-9753301VDA | ACTIVE | CFP | W | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9753301VD A SNV54LVC00AW | Samples |
| SN74LVC00ABQAR | ACTIVE | WQFN | BQA | 14 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC00A | Samples |
| SN74LVC00AD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC00A | Samples |
| SN74LVC00ADBR | ACTIVE | SSOP | DB | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC00A | Samples |
| SN74LVC00ADBRG4 | ACTIVE | SSOP | DB | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC00A | Samples |
| SN74LVC00ADE4 | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC00A | Samples |
| SN74LVC00ADR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC00A | Samples |
| SN74LVC00ADRG4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC00A | Samples |
| SN74LVC00ADT | ACTIVE | SOIC | D | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC00A | Samples |
| SN74LVC00ANSR | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC00A | Samples |
| SN74LVC00ANSRG4 | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC00A | Samples |
| SN74LVC00APW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC00A | Samples |
| SN74LVC00APWE4 | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC00A | Samples |
| SN74LVC00APWG4 | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC00A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC00APWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LC00A | Samples |
| SN74LVC00APWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC00A | Samples |
| SN74LVC00APWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC00A | Samples |
| SN74LVC00APWT | ACTIVE | TSSOP | PW | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC00A | Samples |
| SN74LVC00ARGYR | ACTIVE | VQFN | RGY | 14 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC00A | Samples |
| SNJ54LVC00AFK | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9753301Q2A SNJ54LVC 00AFK | Samples |
| SNJ54LVC00AJ | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9753301QC A SNJ54LVC00AJ | Samples |
| SNJ54LVC00AW | ACTIVE | CFP | W | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9753301QD A SNJ54LVC00AW | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN54LVC00A, SN54LVC00A-SP, SN74LVC00A :**

- Catalog : SN74LVC00A, SN54LVC00A
- Automotive : SN74LVC00A-Q1, SN74LVC00A-Q1
- Enhanced Product : SN74LVC00A-EP, SN74LVC00A-EP
- Military : SN54LVC00A
- Space : SN54LVC00A-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

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