SN74AHC1G86B-EP Enhanced Product, Single 2-Input Exclusive-OR Gate

1 Features

- Operating range 2V to 5.5V V_{CC}
- Low delay, 4.3ns typ. (25°C, 5V)
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- Enable or disable a digital signal
- Controlling an indicator LED

3 Description

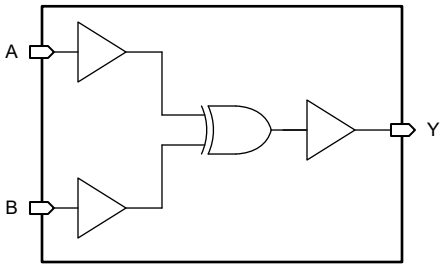
The SN74AHC1G86B-EP is a 2-input XOR Gate which performs the Boolean function Y = A ⊕ B in positive logic..

This device contains four independent 2-input XOR Gates with Schmitt-trigger inputs. Each gate performs the Boolean function Y = A ⊕ B in positive logic.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74AHC1G86B-EP	DCK (SC-70, 5)	2.0mm × 2.1mm	2.0mm × 1.25mm

(1) For more information, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

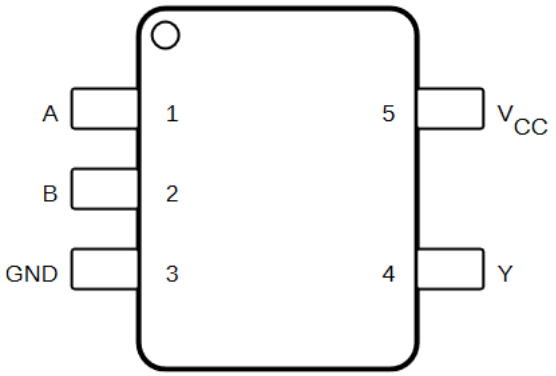


Figure 4-1. DCK Package 5-Pin SC70 (Top View)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A	1	I	Input A
B	2	I	Input B
GND	3	—	Ground Pin
Y	4	O	Output
V_{CC}	5	—	Supply Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage range		-0.5	7	V
V_O	Output voltage range		-0.5	V_{CC} + 0.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state		-0.5	4.6	V
I_{IK}	Input clamp current(2)	V_I < 0	–20		mA
I_{OK}	Output clamp current(2)	V_O < 0 or V_O > V_{CC}	–20	20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}	–25	25	mA
I_O	Continuous output current through V_{CC} or GND		–50	50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage		2	5.5	V
V_{IH}	high-level input voltage	V_{CC}= 2V	1.5		V
V_{IH}	high-level input voltage	V_{CC}= 3V	2.1		V
V_{IH}	high-level input voltage	V_{CC}= 5.5V	3.85		V
V_{IL}	low-level input voltage	V_{CC}= 2V		0.5	V
V_{IL}	low-level input voltage	V_{CC}= 3V		0.9	V
V_{IL}	low-level input voltage	V_{CC}= 5.5V		1.65	V
V_I	input voltage		0	5.5	V
V_O	output voltage		0	V_{CC}	V
I_{OH}	high-level output current	V_{CC}= 2V		-50	µA
I_{OH}	high-level output current	V_{CC}= 3.3V ± 0.3V		-4	mA
I_{OH}	high-level output current	V_{CC}= 5V ± 0.5V		-8	mA
I_{OL}	low-level output current	V_{CC}= 2V		50	µA
I_{OL}	low-level output current	V_{CC}= 3.3V ± 0.3V		4	mA
I_{OL}	low-level output current	V_{CC}= 5V ± 0.5V		8	mA
Δt/Δv	input transition rise or fall rate	V_{CC}= 3.3V ± 0.3V		100	nS/V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
Δt/Δv	input transition rise or fall rate	V_{CC}= 5V ± 0.5V		20	nS/V
T_A	Operating free-air temperature		-55	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DCK (SC-70)	5	329.6	244.7	217.7	142.1	216.7	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{T+}	Positive-going input threshold voltage	Vcc = 3V	1.2		2.20	1.2		2.20	V
V_{T+}	Positive-going input threshold voltage	Vcc = 4.5V	1.75		3.15	1.75		3.15	V
V_{T+}	Positive-going input threshold voltage	Vcc = 5.5V	2.15		3.85	2.15		3.85	V
V_{T-}	Negative-going input threshold voltage	Vcc = 3V	0.9		1.9	0.9		1.9	V
V_{T-}	Negative-going input threshold voltage	Vcc = 4.5V	1.35		2.75	1.35		2.75	V
V_{T-}	Negative-going input threshold voltage	Vcc = 5.5V	1.65		3.35	1.65		3.35	V
ΔV_T	Hysteresis (V_{T+} − V_{T-})	Vcc = 3V	0.3		1.2	0.3		1.2	V
ΔV_T	Hysteresis (V_{T+} − V_{T-})	Vcc = 4.5V	0.4		1.4	0.4		1.4	V
ΔV_T	Hysteresis (V_{T+} − V_{T-})	Vcc = 5.5V	0.5		1.6	0.5		1.6	V
V_{OH}	I_{OH}= –50μA	Vcc = 2V	1.9			1.9			V
V_{OH}	I_{OH}= –50μA	Vcc = 3V	2.9			2.9			V
V_{OH}	I_{OH}= –50μA	Vcc = 4.5V	4.4			4.4			V
V_{OH}	I_{OH}= –4mA	Vcc = 3V	2.58			2.48			V
V_{OH}	I_{OH}= –8mA	Vcc = 4.5V	3.94			3.8			V
V_{OL}	I_{OH}= 50μA	Vcc = 2V			0.1			0.1	V
V_{OL}	I_{OH}= 50μA	Vcc = 3V			0.1			0.1	V
V_{OL}	I_{OH}= 50μA	Vcc = 4.5V			0.1			0.1	V
V_{OL}	I_{OH}= 4mA	Vcc = 3V			0.36			0.44	V
V_{OL}	I_{OH}= 8mA	Vcc = 4.5V			0.36			0.44	V
I_I	V_I= 5.5V or GND	0 V to 5.5V	-0.1		0.1	-1		1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5V	-0.25		0.25	-2.5		2.5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5V			1			4	μA
Ci	V_I = V_{CC} or GND	5V		1.7	10				pF
C_O	V_O = V_{CC} or GND	5V		3					pF
C_{PD}	Power dissipation capacitance	5V	5	14	22.4				pF

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-55°C to 125°C			UNIT
					MIN	TYP	MAX	
T_{PLH}	A or B	Y	CL = 15pF	3.3V ± 0.3V	1	5	9.5	nS
T_{PLH}	A or B	Y	CL = 50pF	3.3V ± 0.3V	1	7.5	13	nS
T_{PLH}	A or B	Y	CL = 15pF	5V ± 0.5V	1	3.6	7	nS
T_{PLH}	A or B	Y	CL = 50pF	5V ± 0.5V	1	5.1	7	nS
T_{PHL}	A or B	Y	CL = 15pF	3.3V ± 0.3V	1	5	9.5	nS
T_{PHL}	A or B	Y	CL = 50pF	3.3V ± 0.3V	1	7.5	13	nS
T_{PHL}	A or B	Y	CL = 15pF	5V ± 0.5V	1	3.6	7	nS
T_{PHL}	A or B	Y	CL = 50pF	5V ± 0.5V	1	5.1	7	nS
T_{PLH}	A or B	Y	CL = 15pF	3.3V ± 0.3V	1	3.6	8.5	nS
T_{PLH}	A or B	Y	CL = 50pF	3.3V ± 0.3V	1.5	6.5	12.5	nS
T_{PLH}	A or B	Y	CL = 15pF	5V ± 0.5V	1	2.5	6.5	nS
T_{PLH}	A or B	Y	CL = 50pF	5V ± 0.5V	1.5	4.6	8.5	nS
T_{PHL}	A or B	Y	CL = 15pF	3.3V ± 0.3V	1	3.6	8.5	nS
T_{PHL}	A or B	Y	CL = 50pF	3.3V ± 0.3V	1.5	6.5	12.5	nS
T_{PHL}	A or B	Y	CL = 15pF	5V ± 0.5V	1	2.5	6.5	nS
T_{PHL}	A or B	Y	CL = 50pF	5V ± 0.5V	1.5	4.6	8.5	nS
T_{PLH}	A or B	Y	CL = 15pF	3.3V ± 0.3V	1	7	14	nS
T_{PLH}	A or B	Y	CL = 50pF	3.3V ± 0.3V	1	9.5	17.5	nS
T_{PLH}	A or B	Y	CL = 15pF	5V ± 0.5V	1	4.8	8.6	nS
T_{PLH}	A or B	Y	CL = 50pF	5V ± 0.5V	1	6.3	11	nS
T_{PHL}	A or B	Y	CL = 15pF	3.3V ± 0.3V	1	7	14	nS
T_{PHL}	A or B	Y	CL = 50pF	3.3V ± 0.3V	1	9.5	17.5	nS
T_{PHL}	A or B	Y	CL = 15pF	5V ± 0.5V	1	4.8	8.6	nS
T_{PHL}	A or B	Y	CL = 50pF	5V ± 0.5V	1	6.3	11	nS

5.7 Typical Characteristics

T_A = 25°C (unless otherwise noted)

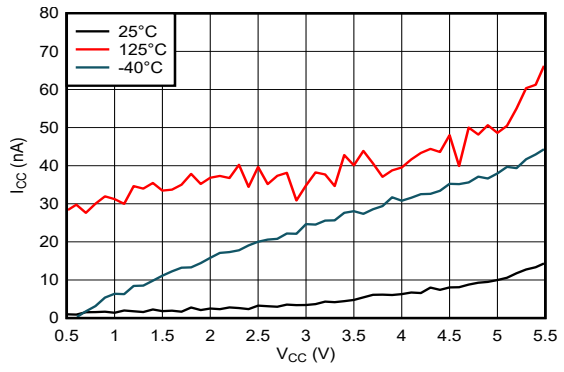


Figure 5-1. Supply Current Across Supply Voltage

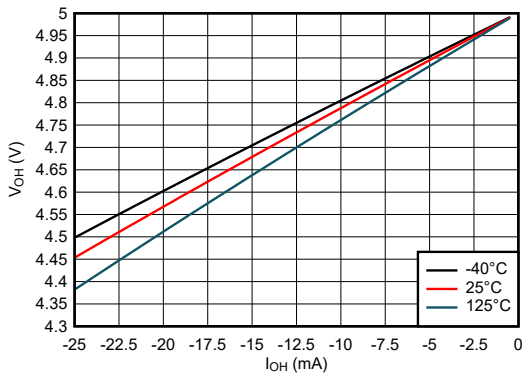


Figure 5-2. Output Voltage vs Current in HIGH State; 5V Supply

5.7 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

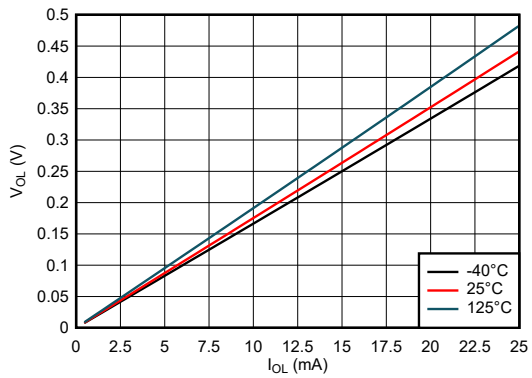


Figure 5-3. Output Voltage vs Current in LOW State; 5V Supply

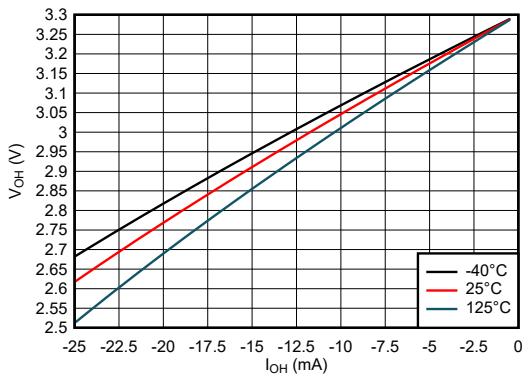


Figure 5-4. Output Voltage vs Current in HIGH State; 3.3V Supply

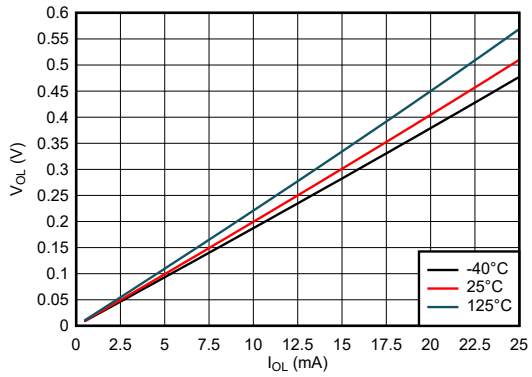


Figure 5-5. Output Voltage vs Current in LOW State; 3.3V Supply

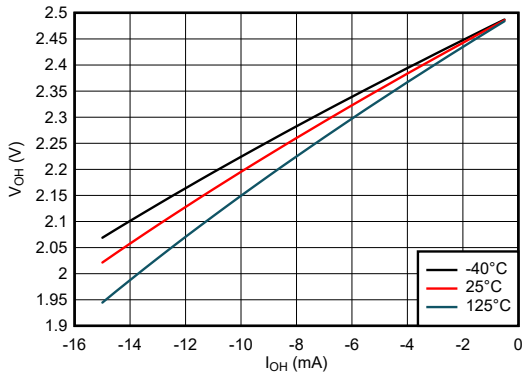


Figure 5-6. Output Voltage vs Current in HIGH State; 2.5V Supply

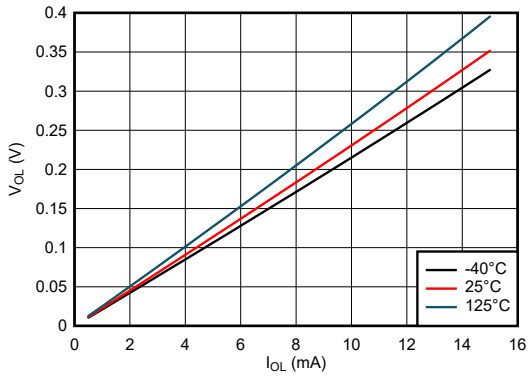
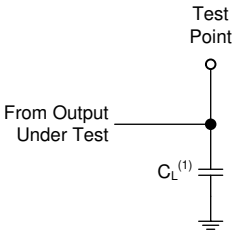


Figure 5-7. Output Voltage vs Current in LOW State; 2.5V Supply

6 Parameter Measurement Information

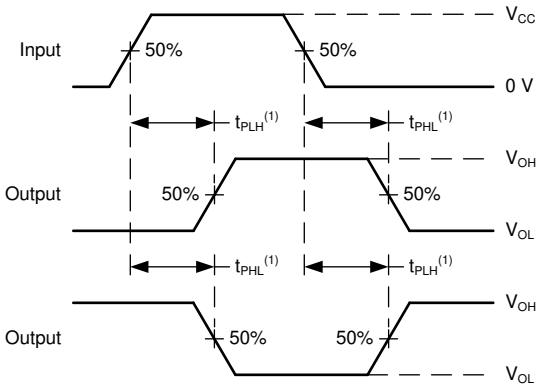
Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns.

The outputs are measured individually with one input transition per measurement.



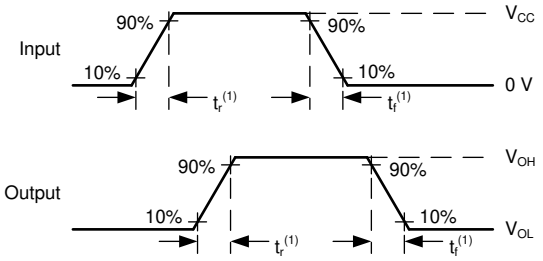
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-3. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN74AHC1G86 is a single 2-input exclusive-OR gate. The device performs the Boolean function Y = A × B or Y = $\overline{A}$B + A $\overline{B}$ in positive logic.

A common application is as a true or complementary element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

7.2 Functional Block Diagram

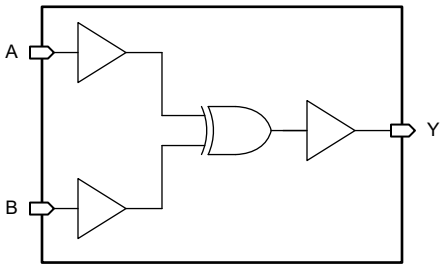


Figure 7-1. Exclusive-OR Logic

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10kΩ resistor, however, is recommended and will typically meet all requirements.

7.3.3 Clamp Diode Structure

As Figure 7-2 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

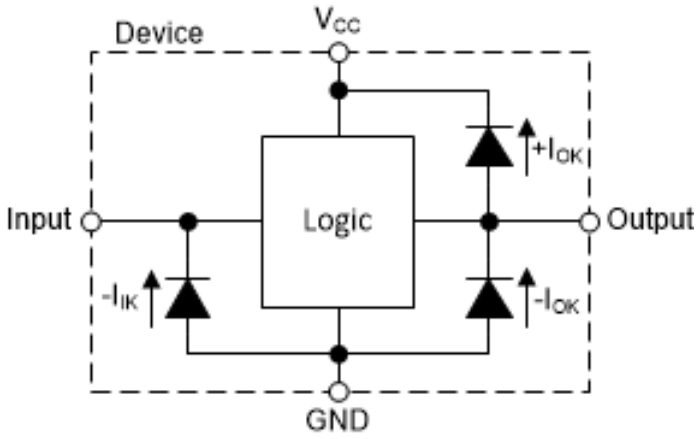


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

SN74AHC1G86B-EP is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid V_{CC} making it Ideal for down translation.

8.2 Typical Application

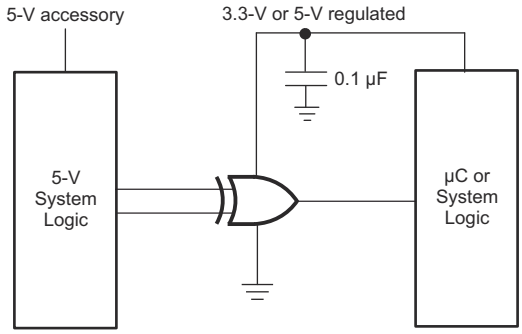


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AHC1G86B-EP plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AHC1G86B-EP plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74AHC1G86B-EP can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74AHC1G86B-EP can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AHC1G86B-EP (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74AHC1G86B-EP has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AHC1G86B-EP to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

8.2.3 Application Curves

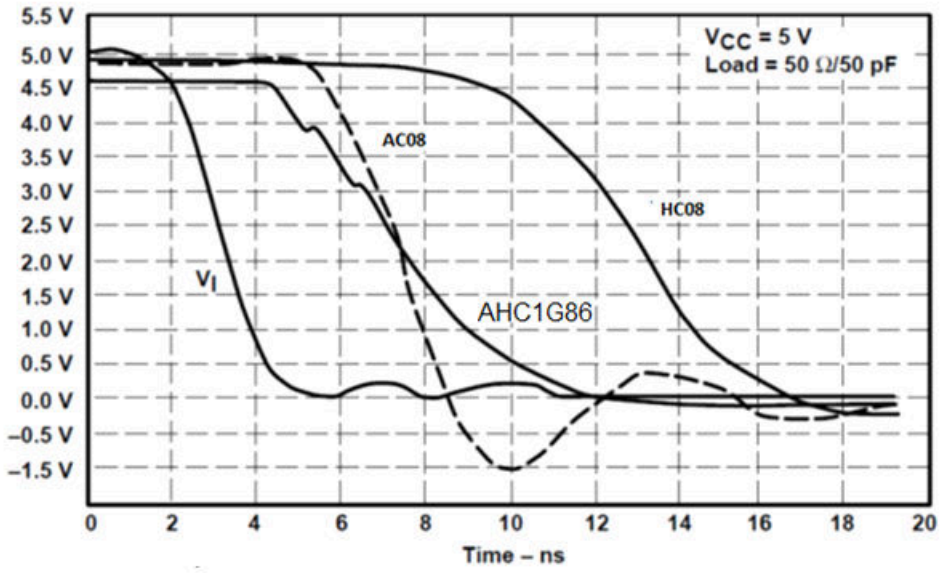


Figure 8-2. Switching Characteristics Comparison

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For the SN74AHC1G86B-EP, a 0.1µF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width

- Lengths less than 12cm to minimize transmission line effects
- Avoid 90° corners for signal traces
- Use an unbroken ground plane below signal traces
- Flood fill areas around signal traces with ground
- For traces longer than 12cm
  - Use impedance controlled traces
  - Source-terminate using a series damping resistor near the output
  - Avoid branches; buffer signals that must branch separately

8.4.2 Layout Example

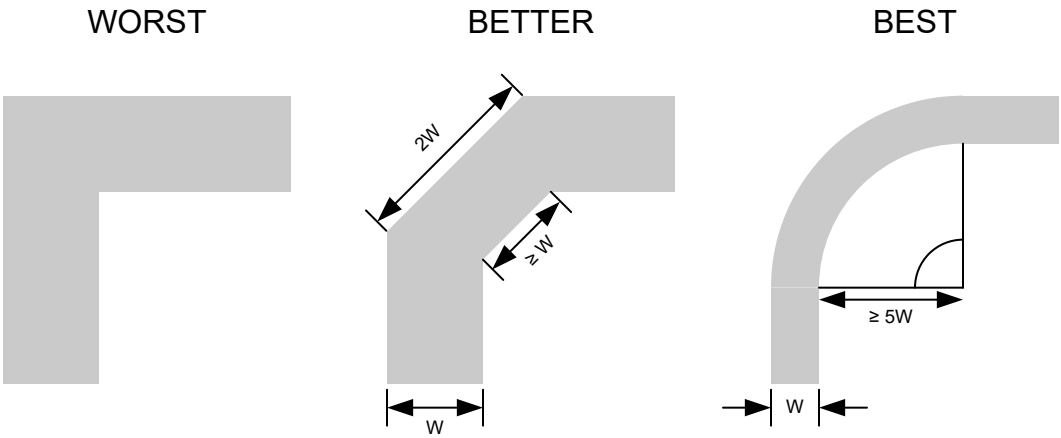


Figure 8-3. Example Trace Corners for Improved Signal Integrity

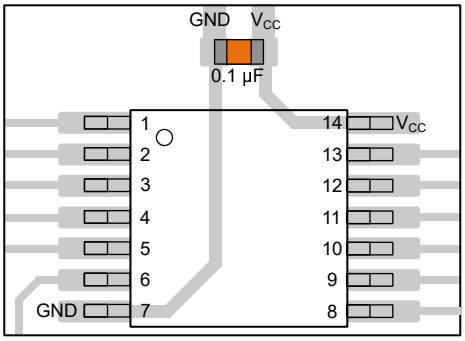


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

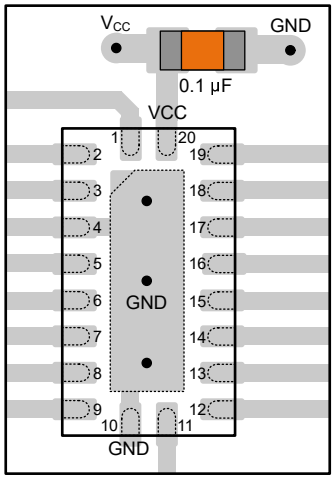


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

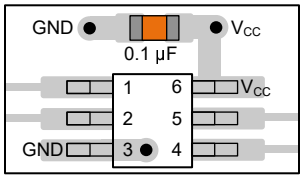


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

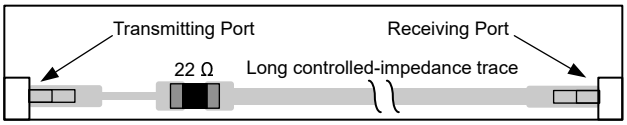


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
March 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC1G86MDCKREP	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CGB	Samples
V62/08612-01XE	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CGB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74AHC1G86-EP :

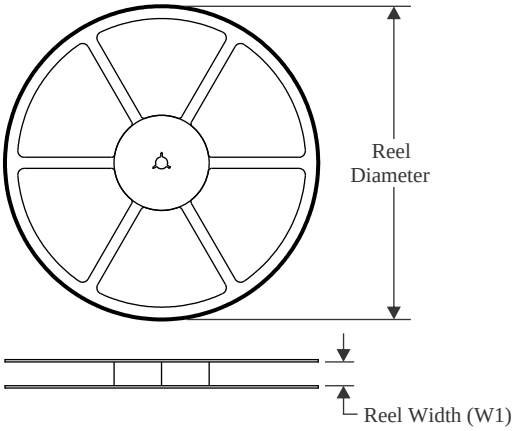
- Catalog : SN74AHC1G86
- Automotive : SN74AHC1G86-Q1

NOTE: Qualified Version Definitions:

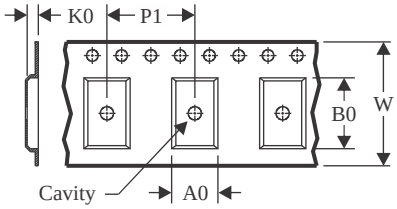
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

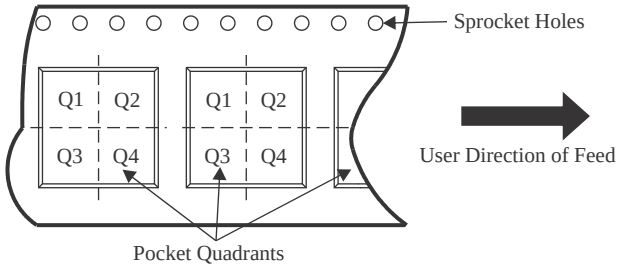


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

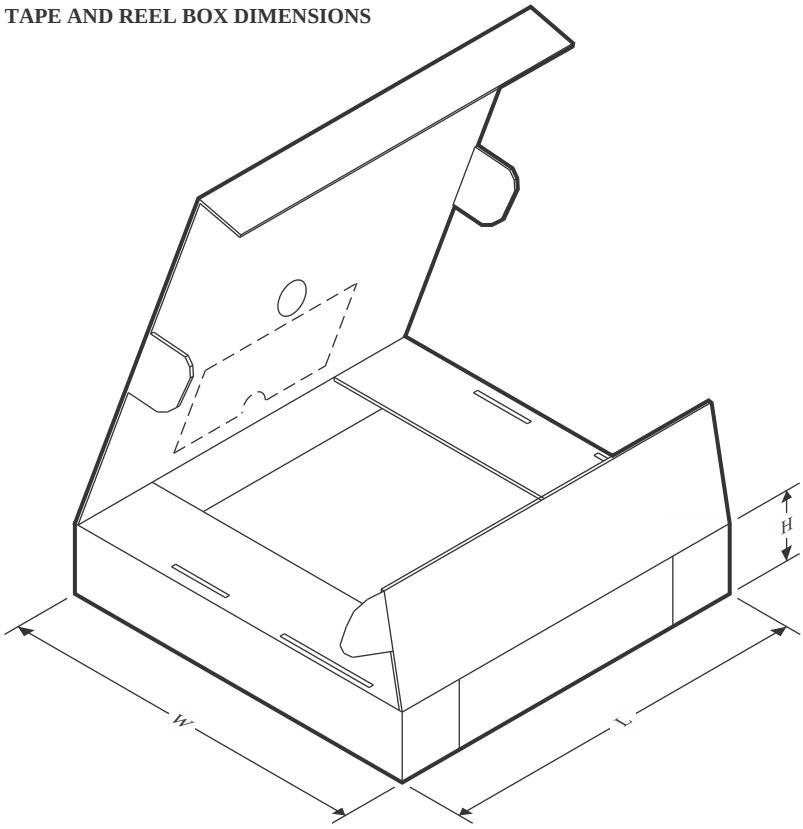
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G86MDCKREP	SC70	DCK	5	3000	180.0	8.4	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

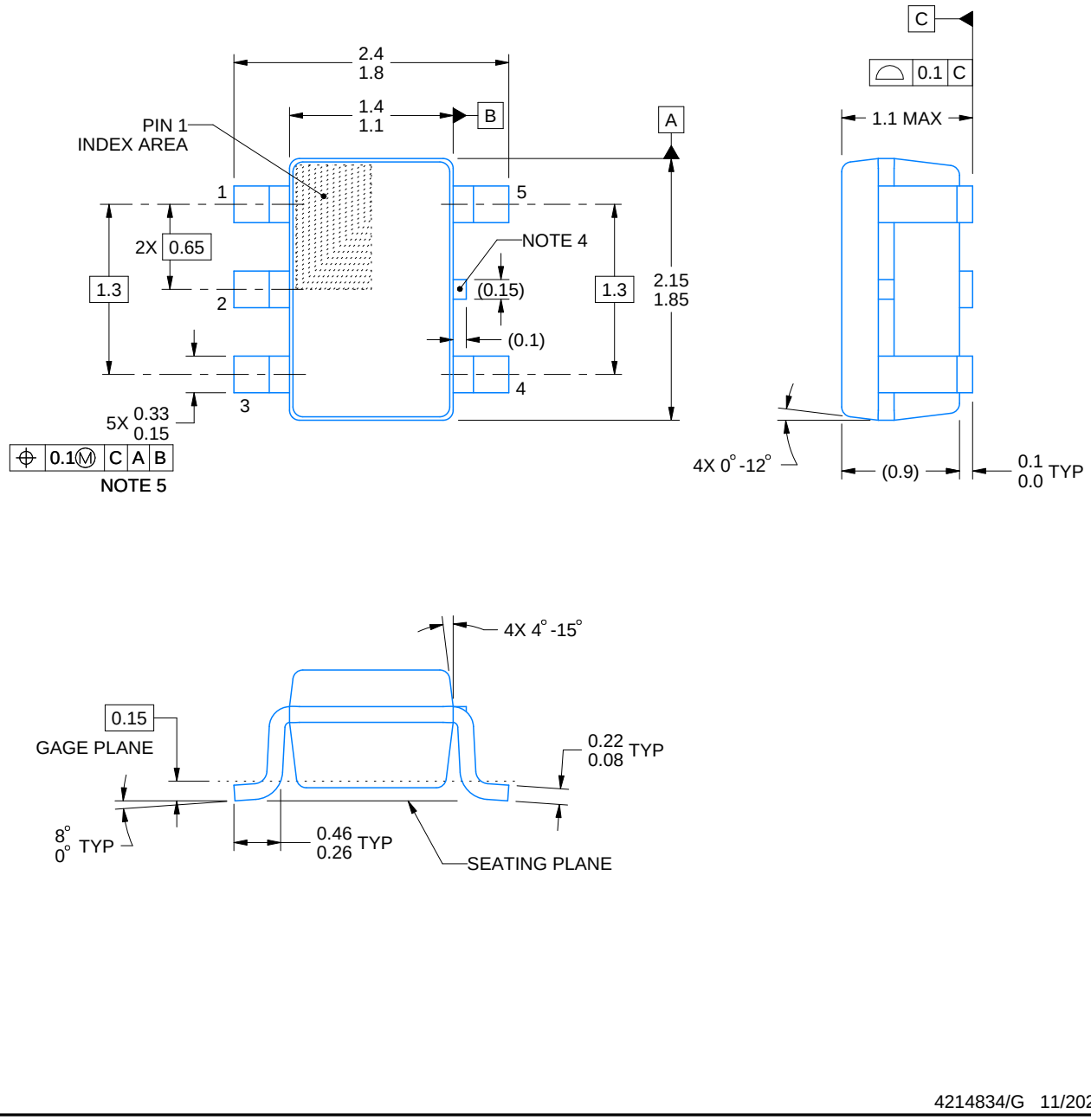
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G86MDCKREP	SC70	DCK	5	3000	202.0	201.0	28.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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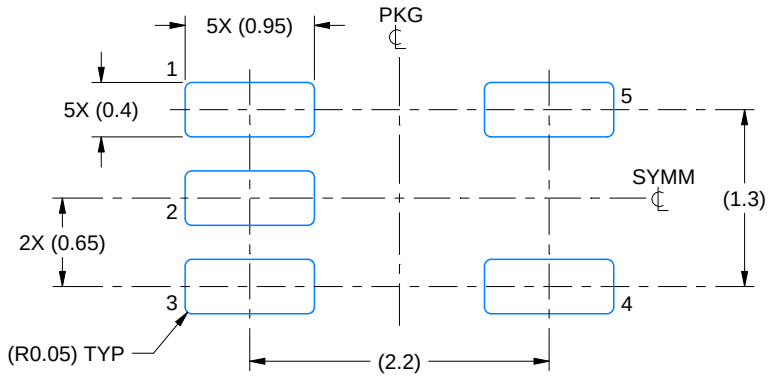
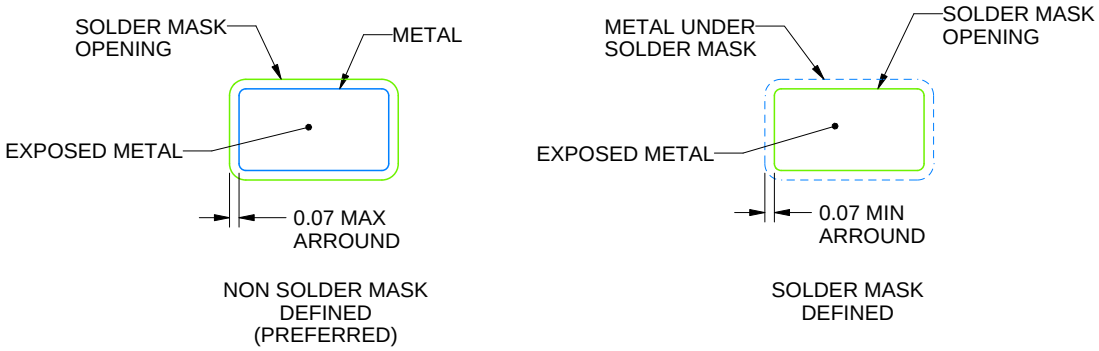
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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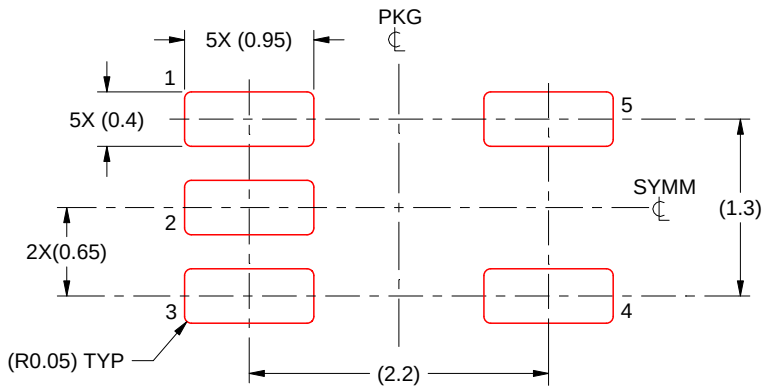
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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