# SNxAHCT74 Dual Positive-Edge-Triggered D-Type Flip-Flops With Clear And Preset

## 1 Features

- Operating range of 4.5 V to 5.5 V
- Low power consumption, 10-µA maximum $I_{CC}$
- ±8-mA output drive at 5 V
- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250 mA per JESD 17

## 2 Applications

- Convert a momentary switch to a toggle switch
- Hold a signal during controller reset
- Input slow edge-rate signals
- Operate in noisy environments
- Divide a clock signal by two

## 3 Description

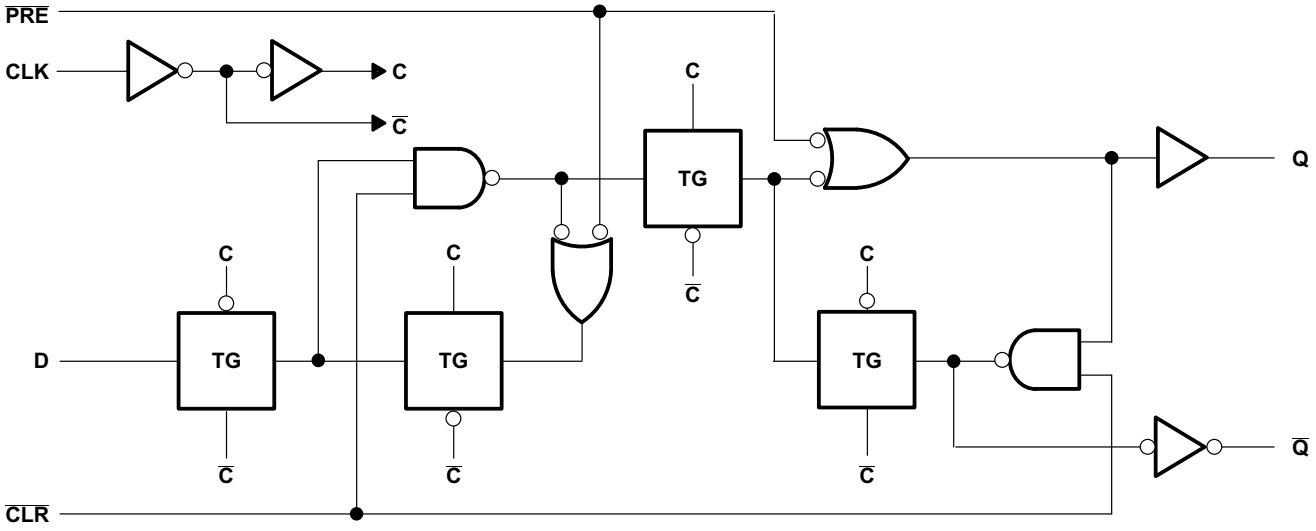
The ’AHCT74 dual positive-edge-triggered devices are D-type flip-flops.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

**Device Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE (NOM)(3) |
|---|---|---|---|
| SN54AHCT74 | J (CDIP, 14) | 21.3 mm × 7.6 mm | 19.56 mm × 6.67 mm |
| | W (CFP, 14) | 13.1 mm × 6.92 mm | 13.1 mm × 6.92 mm |
| | FK (LCCC, 20) | 8.9 mm × 8.9 mm | 8.9 mm × 8.9 mm |
| SN74AHCT74 | N (PDIP , 14) | 19.3 mm × 8 mm | 19.3 mm × 6.35 mm |
| | D (SOIC, 14) | 8.7 mm × 6 mm | 8.7 mm × 3.91 mm |
| | NS (SOP, 14) | 10.3 mm × 7.8 mm | 10.3 mm × 5.3 mm |
| | DB (SSOP, 14) | 6.2 mm × 7.8 mm | 6.2 mm × 5.3 mm |
| | PW (TSSOP, 14) | 5 mm × 6.4 mm | 5 mm × 4.4 mm |
| | DGV (TVSOP, 14) | 3.6 mm × 6.4 mm | 3.6 mm × 4.4 mm |
| | RGY (VQFN, 14) | 3.5 mm × 3.5 mm | 3.50 mm × 3.50 mm |
| | BQA (WQFN, 14) | 3 mm × 2.5 mm | 3.00 mm × 2.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Logic Diagram, Each Flip-Flop (Positive Logic)**

# Table of Contents



## 4 Revision History

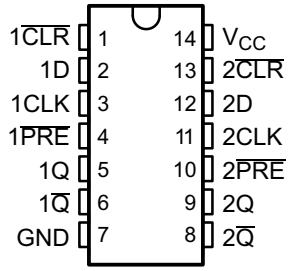
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision Q (July 2023) to Revision R (October 2023) | Page |
|---|---|
| • Updated title and format of *Device Information* table | 1 |
| • Updated RθJA values: D = 86 to 124.5, all values in °C/W | 5 |

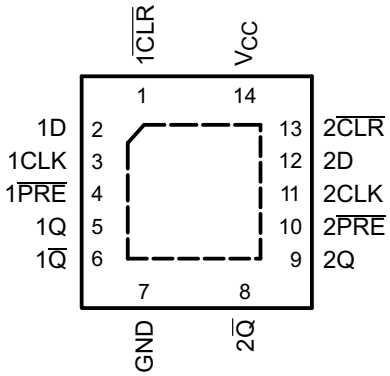
| Changes from Revision P (May 2023) to Revision Q (July 2023) | Page |
|---|---|
| • Updated thermal values for PW package from RθJA = 113 to 147.7, all values in °C/W | 5 |

## 5 Pin Configuration and Functions

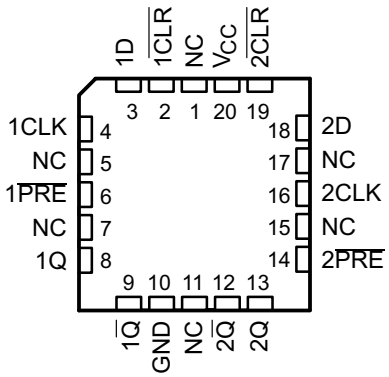
SN54AHCT74 . . . J or W PACKAGE
SN74AHCT74 . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)




SN74AHCT74 . . . RGY PACKAGE
(TOP VIEW)




SN54AHCT74 . . . FK PACKAGE
(TOP VIEW)




NC − No internal connection

**Figure 5-1. Title**

**Table 5-1. Pin Functions**

| PIN | | | | | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|---|---|
| NAME | SN74AHCT74 | | SN54AHCT74 | | | |
| | D, DB, DGV, N, NS, PW | RGY, BQA | J, W | FK | | |
| 1$\overline{CLR}$ | 1 | 1 | 1 | 2 | I | 1A Input |
| 1D | 2 | 2 | 2 | 3 | I | 1B Input |
| 1CLK | 3 | 3 | 3 | 4 | O | 1Y Output |
| 1$\overline{PRE}$ | 4 | 4 | 4 | 6 | I | 2A Input |
| 1Q | 5 | 5 | 5 | 8 | I | 2B Input |
| 1$\overline{Q}$ | 6 | 6 | 6 | 9 | O | 2Y Output |
| 2$\overline{Q}$ | 8 | 8 | 8 | 12 | O | 3Y Output |
| 2Q | 9 | 9 | 9 | 13 | I | 3A Input |
| 2$\overline{PRE}$ | 10 | 10 | 10 | 14 | I | 3B Input |
| 2CLK | 11 | 11 | 11 | 16 | O | 4Y Output |
| 2D | 12 | 12 | 12 | 18 | I | 4A Input |
| 2$\overline{CLR}$ | 13 | 13 | 13 | 19 | I | 4B Input |
| GND | 7 | 7 | 7 | 10 | — | Ground Pin |
| NC | — | — | — | 1, 5, 7, 11, 15, 17 | — | No Connection |
| $V_{CC}$ | 14 | 14 | 14 | 20 | — | Power Pin |
| Thermal Pad | — | PAD | — | — | — | Thermal Pad |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ (2) | Input voltage range | | –0.5 | 7 | V |
| $V_O$ (2) | Output voltage range | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current, | ($V_I$ < 0) | | -20 | mA |
| $I_{OK}$ | Output clamp current | ($V_O$ < 0 or $V_O$ > $V_{CC}$) | | ±20 | mA |
| $I_O$ | Continuous output current | ($V_O$ = 0 to $V_{CC}$) | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

| | | SN54AHCT74 | | SN74AHCT74 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level Input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| Δt/Δv | Input Transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 6.4 Thermal Information

| THERMAL METRIC[1] | | SNx4AHCT74 | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | D | DB | DGV | N | NS | PW | RGY | BQA | |
| | | 14 PINS | | | | | | | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 124.5 | 96 | 127 | 80 | 76 | 147.7 | 47 | 88.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –55°C TO 125°C | | $T_A$ = –40°C TO 85°C | | $T_A$ = –40°C TO 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | Recommended | | |
| | | | | | | SN54AHCT74 | | SN74AHCT74 | | SN74AHCT74 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OH}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1[1] | | ±1 | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 20 | | 20 | | 20 | µA |
| $\Delta I_{CC}$ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2 | 10 | | | | 10 | | | pF |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at VCC = 0 V.

## 6.6 Timing Requirements

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Section 6.6)

| PARAMETER | | | $T_A$ = 25°C | | $T_A$ = –55°C TO 125°C | | $T_A$ = –40°C TO 85°C | | $T_A$ = –40°C TO 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | Recommended | | |
| | | | | | SN54AHCT74 | | SN54AHCT74 | | SN54AHCT74 | | |
| | | | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ low | 5 | | 5 | | 5 | | 5 | | ns |
| | | CLK | 5 | | 5 | | 5 | | 5 | | |
| $t_{su}$ | Setup time before CLK↑ | Data | 5 | | 5 | | 5 | | 5 | | ns |
| | | $\overline{PRE}$ or $\overline{CLR}$ inactive | 3.5 | | 3.5 | | 3.5 | | 3.5 | | |
| $t_h$ | Hold time, data after CLK↑ | | 0 | | 0 | | 0 | | 0 | | ns |

## 6.7 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | $T_A$ = –55°C TO 125°C | | $T_A$ = –40°C TO 85°C | | $T_A$ = –40°C TO 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | Recommended | | |
| | | | | | | | SN54AHCT74 | | SN54AHCT74 | | SN54AHCT74 | | |
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 100[1] | 160[1] | | 90 | | 80 | | 80 | | ns |
| | | | $C_L$ = 50pF | 80 | 140 | | 65 | | 65 | | 65 | | |

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | $T_A$ = –55°C TO 125°C | | $T_A$ = –40°C TO 85°C | | $T_A$ = –40°C TO 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | SN54AHCT74 | | SN54AHCT74 | | Recommended SN54AHCT74 | | |
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 7.6[1] | 10.4[1] | 1[1] | 12[1] | 1 | 12 | 1 | 12 | ns |
| $t_{PHL}$ | | | | | 7.6[1] | 10.4[1] | 1[1] | 12[1] | 1 | 12 | 1 | 12 | |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | $C_L$ = 15 pF | | 5.8[1] | 7.8[1] | 1[1] | 9[1] | 1 | 9 | 1 | 9.0 | ns |
| $t_{PHL}$ | | | | | 5.8[1] | 7.8[1] | 1[1] | 9[1] | 1 | 9 | 1 | 9.0 | |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 8.1 | 11.4 | 1 | 13 | 1 | 13 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 8.1 | 11.4 | 1 | 13 | 1 | 13 | 1 | 13 | |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | $C_L$ = 50 pF | | 6.3 | 8.8 | 1 | 10 | 1 | 10 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 6.3 | 8.8 | 1 | 10 | 1 | 10 | 1 | 10 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.8 Noise Characteristics

$V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C[1]

| PARAMETER | | SN54AHCT74 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.8 | V |

(1) Characteristics are for surface-mount packages only.

## 6.9 Operating Characteristics

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 32 | pF |

## 6.10 Typical Characteristics

$T_A$ = 25°C (unless otherwise noted)

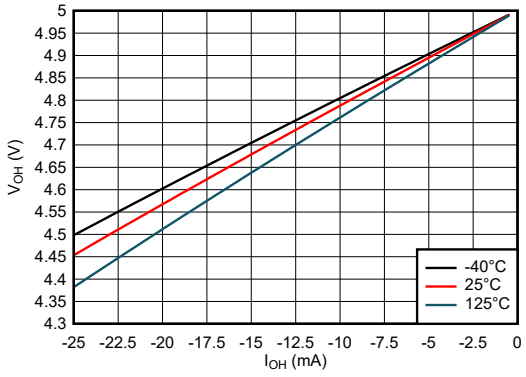



**Figure 6-1. Output Voltage vs Current in HIGH State; 5-V Supply**

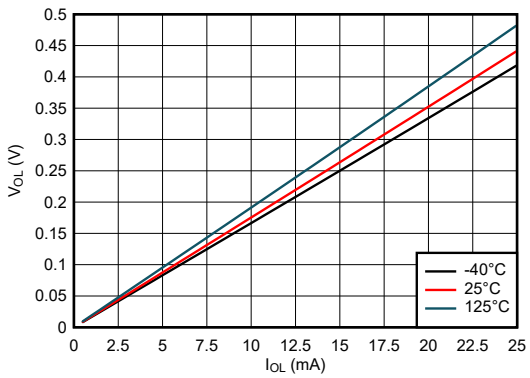
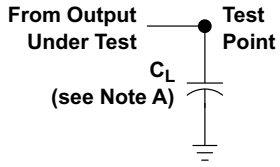
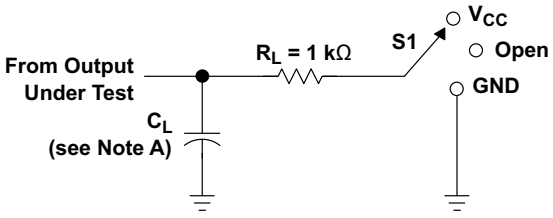



**Figure 6-2. Output Voltage vs Current in LOW State; 5-V Supply**

## 7 Parameter Measurement Information

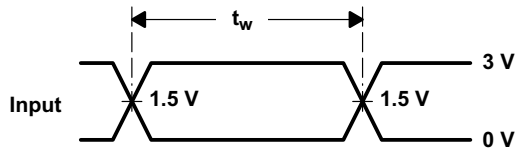



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

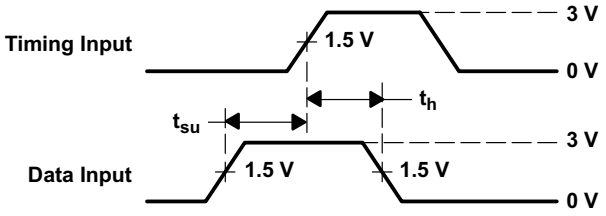



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

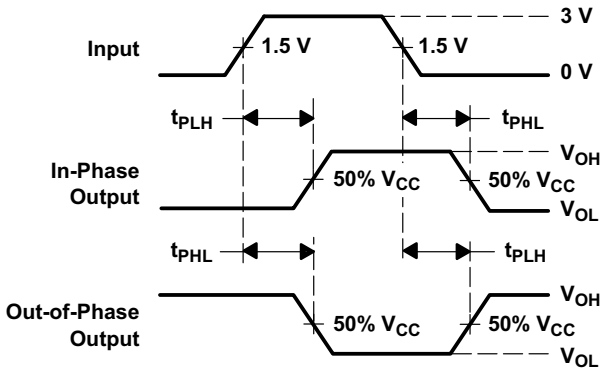
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |



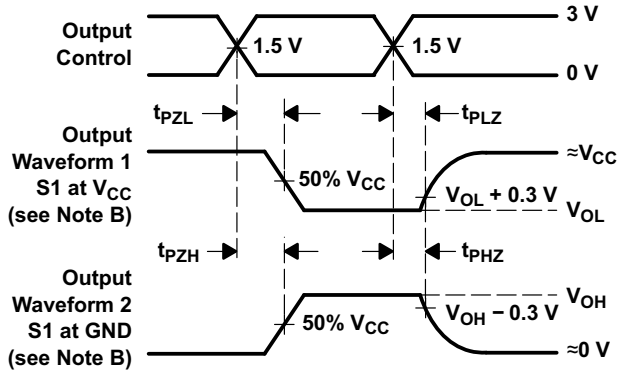

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

**Figure 7-1. Load Circuit and Voltage Waveforms**

# 8 Detailed Description

## 8.1 Overview

The ’AHCT74 dual positive-edge-triggered devices are D-type flip-flops.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

## 8.2 Functional Block Diagram

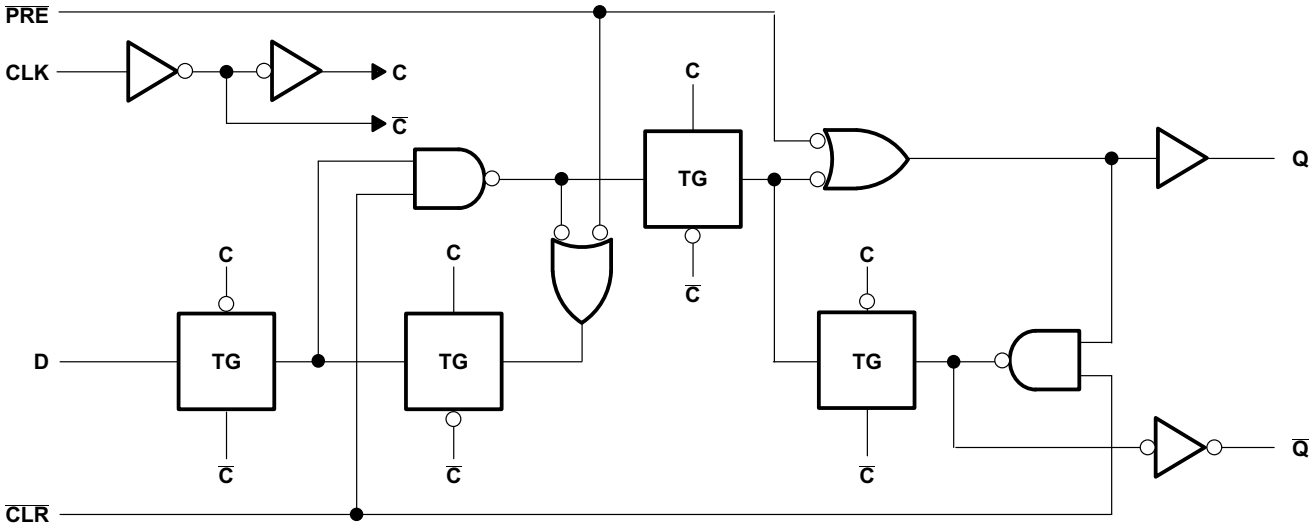



**Figure 8-1.**

## 8.3 Feature Description

### 8.3.1 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at $V_{CC}$ or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-kΩ resistor is recommended and will typically meet all requirements.

### 8.3.2 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

### 8.3.3 Clamp Diode Structure

As Figure 8-2 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

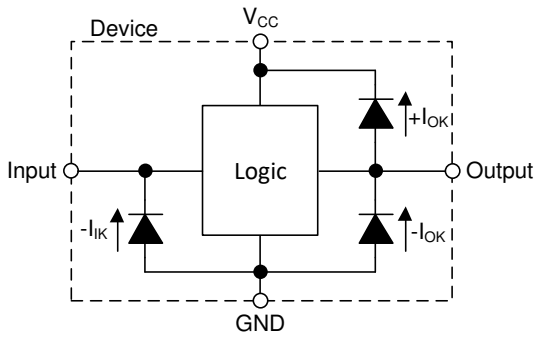



**Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output**

## 8.4 Device Functional Modes

**Table 8-1. Functional Table (Each Flip-Flop)**

| INPUTS | | | | OUTPUT | |
|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H(1) | H(1) |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q}_0$ |

(1) This configuration is non-stable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

Toggle switches are typically large, mechanically complex and relatively expensive. It is desirable to use a momentary switch instead because they are small, mechanically simple and low cost. Some systems require a toggle switch's functionality but are space or cost constrained and must use a momentary switch instead. External Schmitt-trigger buffers are used to remove noisy inputs into the (CLK) and (D) inputs.

If the data input (D) of the SNx4AHCT74 is tied to the inverted output ($\overline{Q}$), then each clock pulse will cause the value at the output (Q) to toggle. The momentary switch can be debounced and directly connected to the clock input (CLK) to toggle the output.

## 9.2 Typical Application

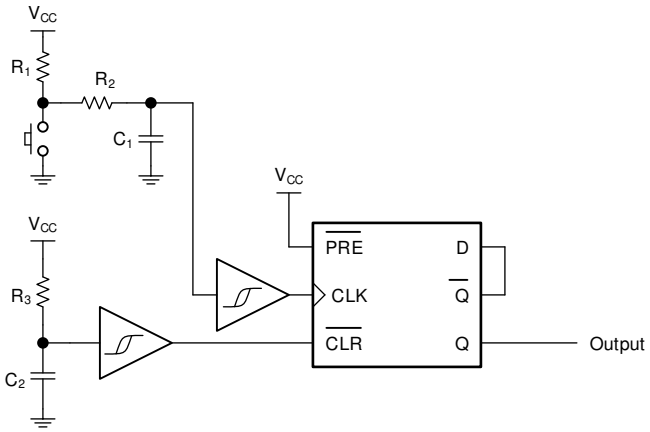



**Figure 9-1. Typical Application Block Diagram**

### 9.2.1 Design Requirements

#### *9.2.1.1 Input Considerations*

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SNx4AHCT74 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

#### *9.2.1.2 Output Considerations*

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

#### 9.2.1.3 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SNx4AHCT74 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SNx4AHCT74 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SNx4AHCT74 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OL}$. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

**CAUTION**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SNx4AHCT74 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than ($V_{CC} / I_{O(max)}$) Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

### 9.2.3 Application Curves

Figure 9-2 shows an example of a single button press bouncing and causing the output to toggle multiple times. This will cause issues in the desired application. Figure 9-3 shows 4 button presses with an added debounce circuit, fixing the unwanted toggling and allowing for proper toggle switch operation.

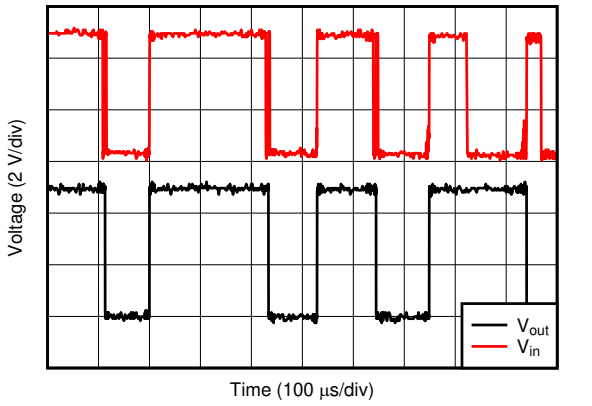



**Figure 9-2. Circuit Response Without RC Debounce**
**$V_{in}$: = CLK Input, $V_{out}$ := Q Output**

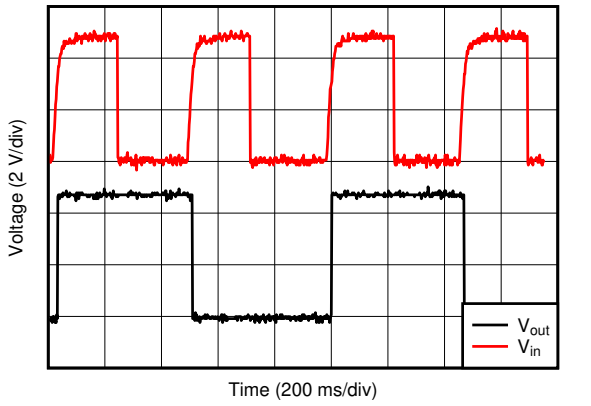



**Figure 9-3. Circuit Response with RC Debounce**
**$V_{in}$: = CLK Input, $V_{out}$ := Q Output**

## 9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

## 9.4 Layout

### 9.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

#### *9.4.1.1 Layout Example*

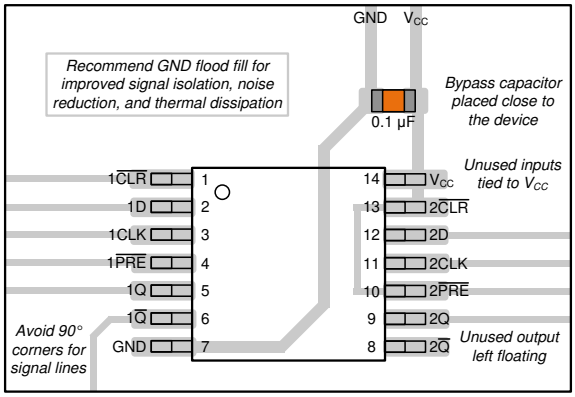



**Figure 9-4. Layout Example of the SNx4AHCT74**

# 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9686101Q2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9686101Q2A SNJ54AHCT 74FK | Samples |
| 5962-9686101QCA | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9686101QC A SNJ54AHCT74J | Samples |
| 5962-9686101QDA | ACTIVE | CFP | W | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9686101QD A SNJ54AHCT74W | Samples |
| SN74AHCT74BQAR | ACTIVE | WQFN | BQA | 14 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT74 | Samples |
| SN74AHCT74D | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI | -40 to 125 | AHCT74 | |
| SN74AHCT74DBR | ACTIVE | SSOP | DB | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB74 | Samples |
| SN74AHCT74DGVR | ACTIVE | TVSOP | DGV | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB74 | Samples |
| SN74AHCT74DR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT74 | Samples |
| SN74AHCT74N | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | SN74AHCT74N | Samples |
| SN74AHCT74NSR | ACTIVE | SOP | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT74 | Samples |
| SN74AHCT74PW | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI | -40 to 125 | HB74 | |
| SN74AHCT74PWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | HB74 | Samples |
| SN74AHCT74PWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB74 | Samples |
| SN74AHCT74RGYR | ACTIVE | VQFN | RGY | 14 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HB74 | Samples |
| SNJ54AHCT74FK | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9686101Q2A SNJ54AHCT 74FK | Samples |
| SNJ54AHCT74J | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9686101QC A SNJ54AHCT74J | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SNJ54AHCT74W | ACTIVE | CFP | W | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9686101QDA SNJ54AHCT74W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN54AHCT74, SN74AHCT74 :**

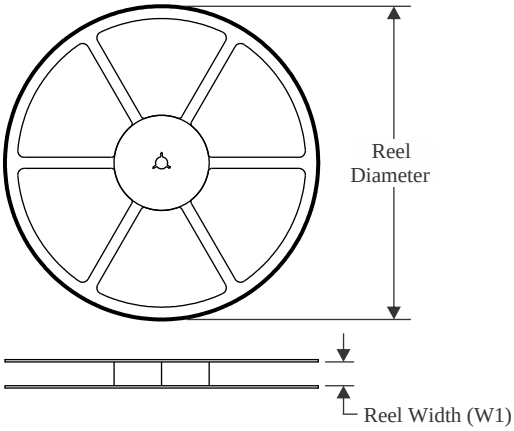
- Catalog : SN74AHCT74
- Enhanced Product : SN74AHCT74-EP, SN74AHCT74-EP
- Military : SN54AHCT74

NOTE: Qualified Version Definitions:

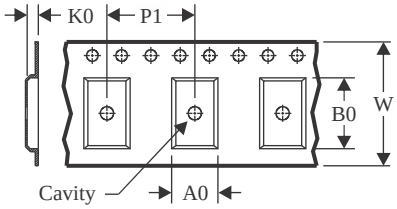
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

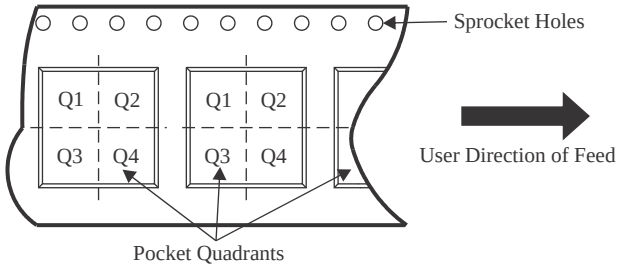



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

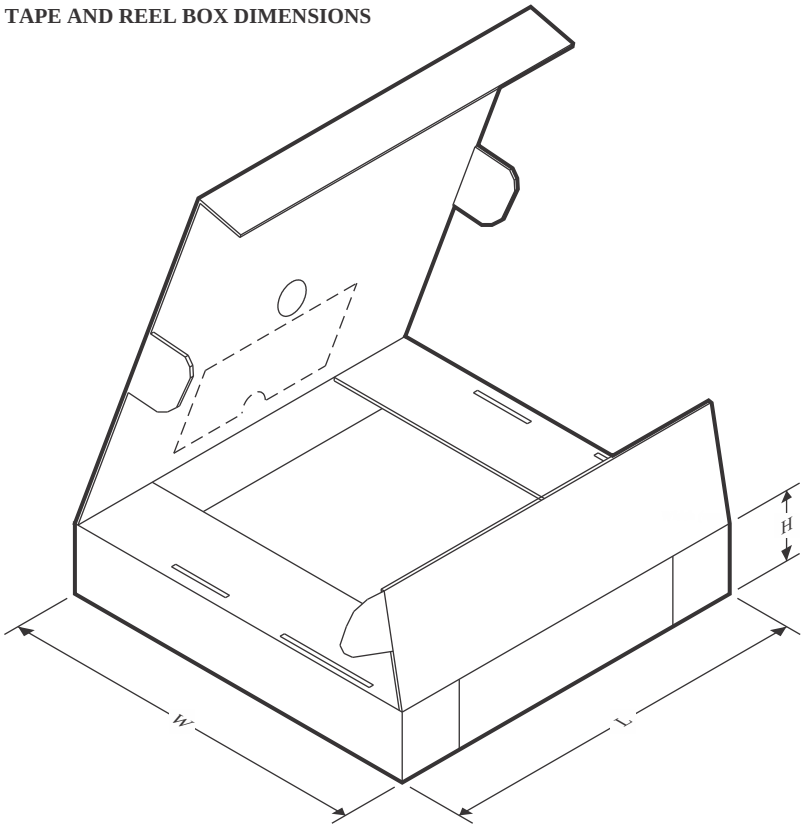
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AHCT74BQAR | WQFN | BQA | 14 | 3000 | 180.0 | 12.4 | 2.8 | 3.3 | 1.1 | 4.0 | 12.0 | Q1 |
| SN74AHCT74DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74AHCT74DGVR | TVSOP | DGV | 14 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHCT74DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74AHCT74DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74AHCT74NSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHCT74PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHCT74PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHCT74RGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

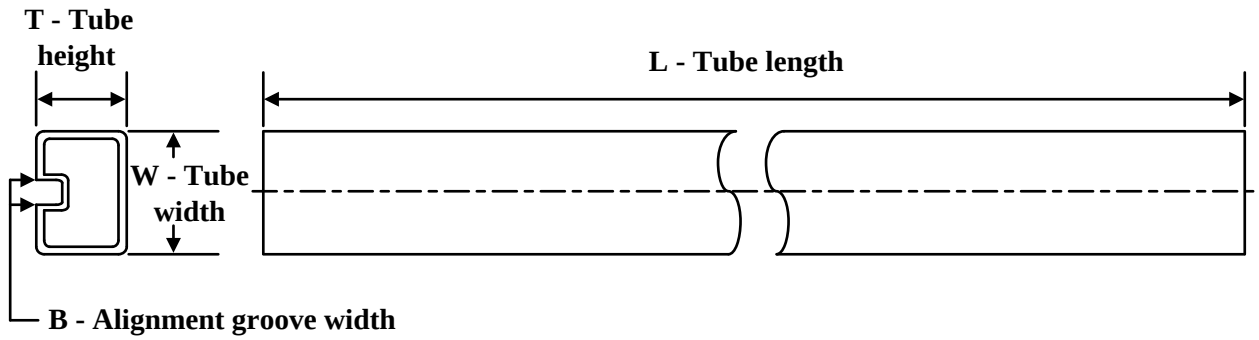
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AHCT74BQAR | WQFN | BQA | 14 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AHCT74DBR | SSOP | DB | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHCT74DGVR | TVSOP | DGV | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHCT74DR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74AHCT74DR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74AHCT74NSR | SOP | NS | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHCT74PWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHCT74PWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHCT74RGYR | VQFN | RGY | 14 | 3000 | 356.0 | 356.0 | 35.0 |

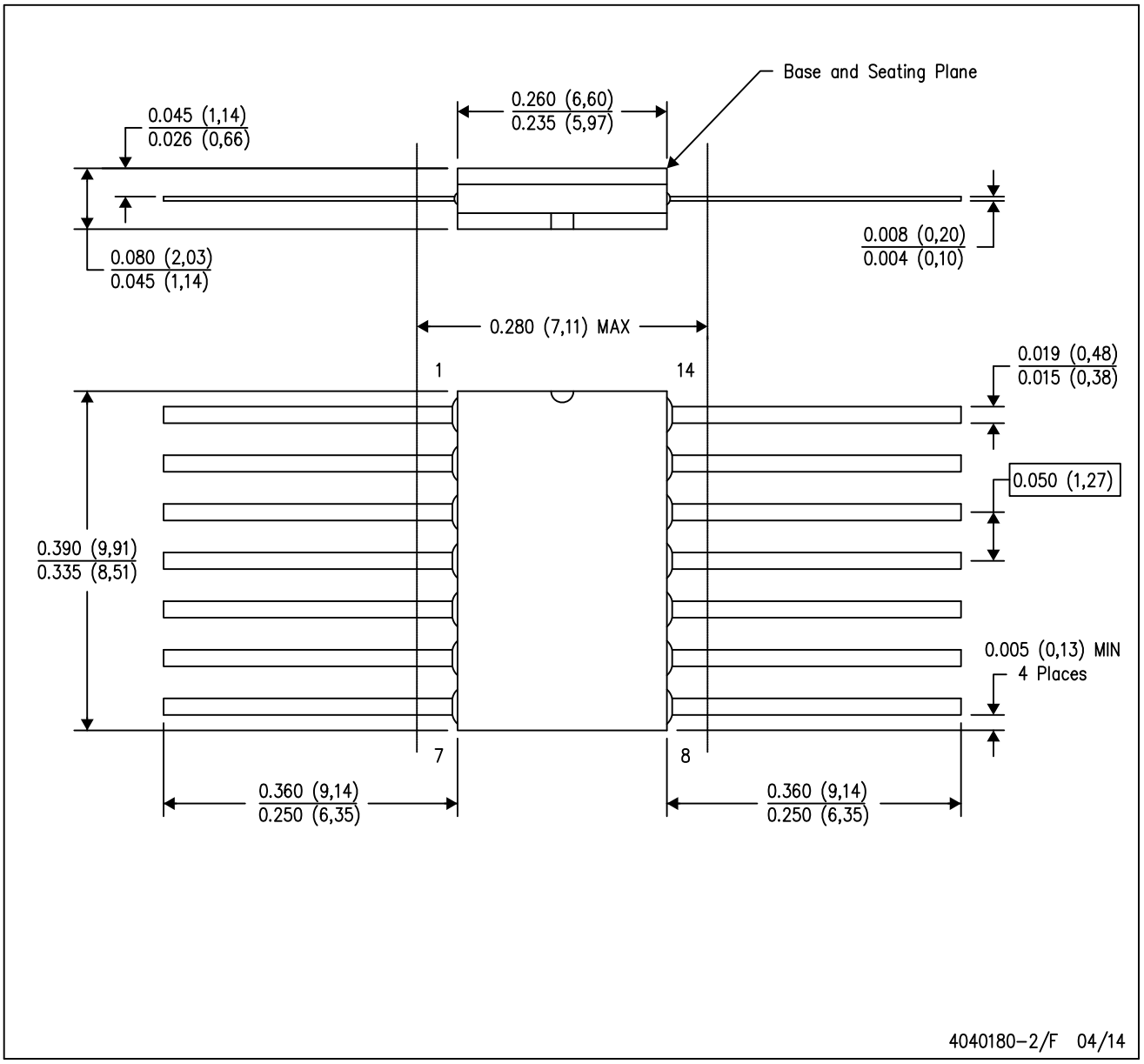
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9686101Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9686101QDA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74AHCT74N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AHCT74N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54AHCT74FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AHCT74W | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |

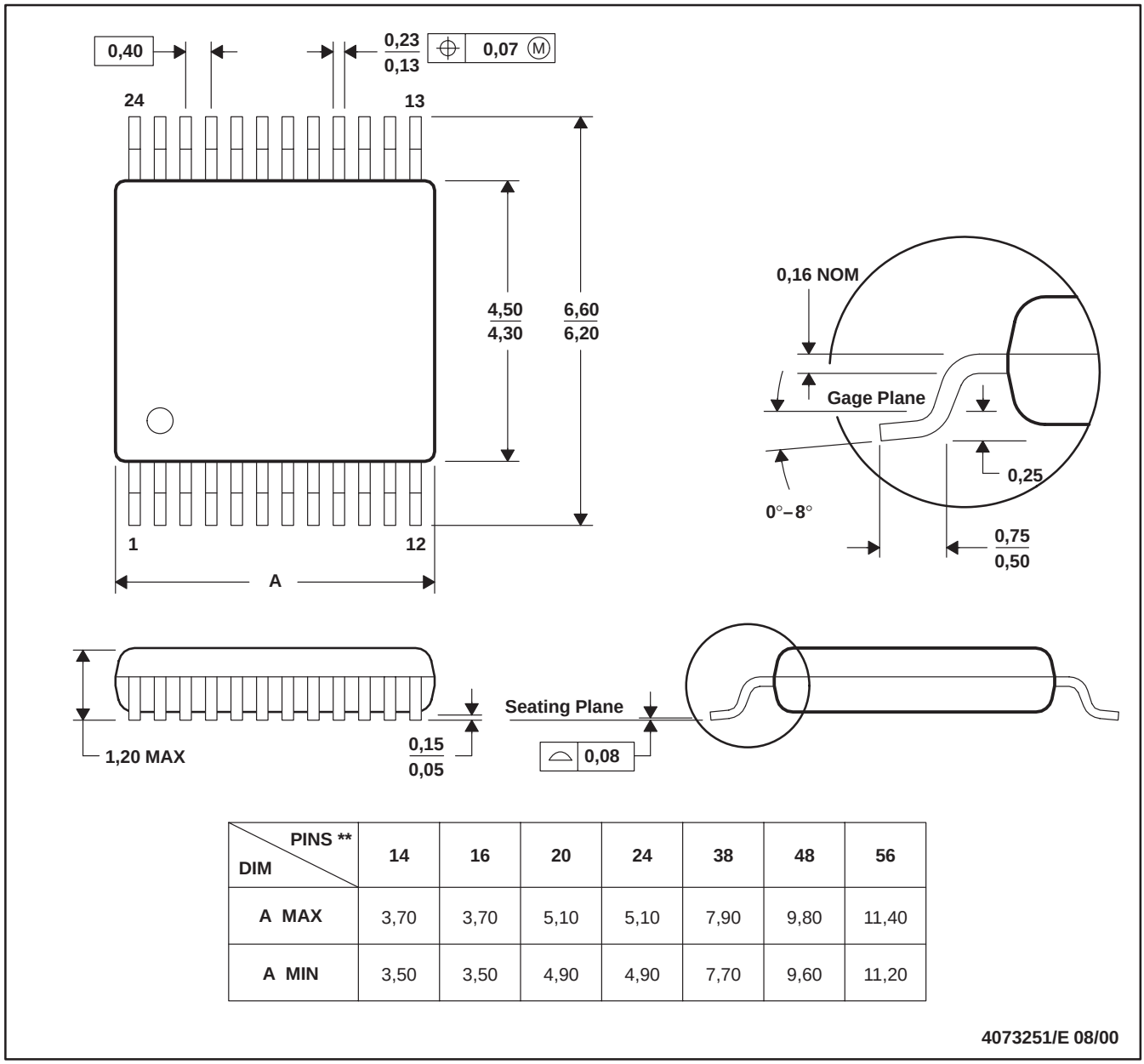
W (R–GDFP–F14) CERAMIC DUAL FLATPACK




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

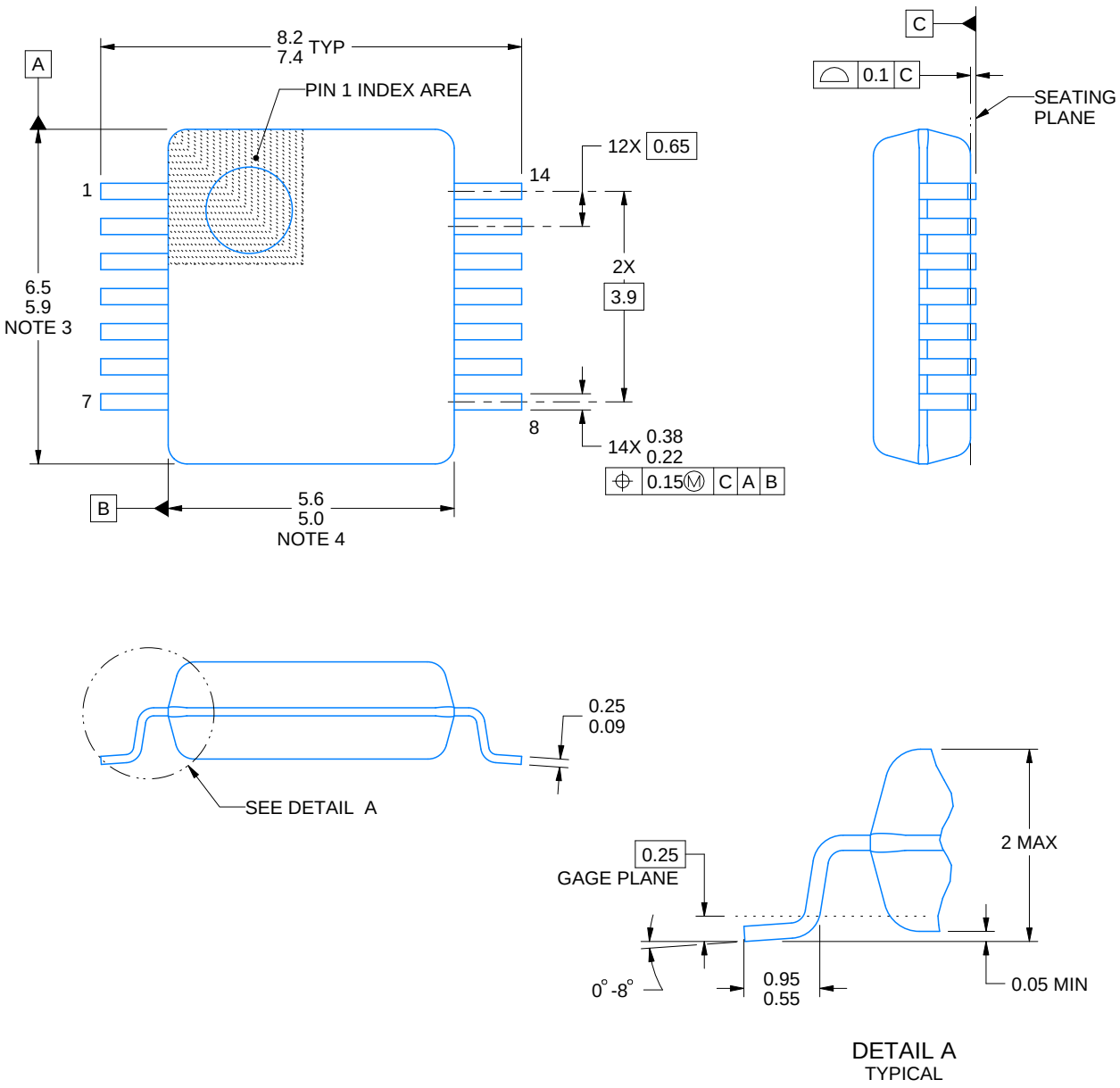
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

# PACKAGE OUTLINE

## DB0014A

## SSOP - 2 mm max height

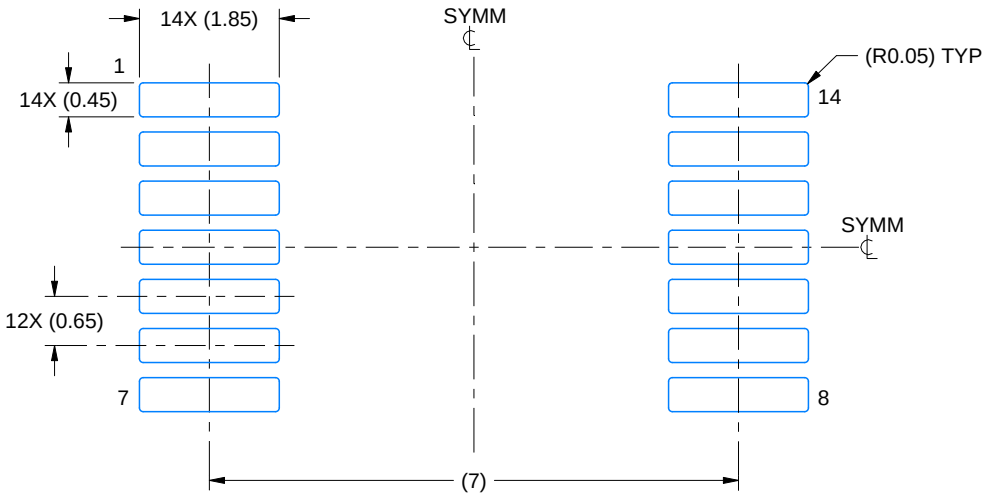
SMALL OUTLINE PACKAGE



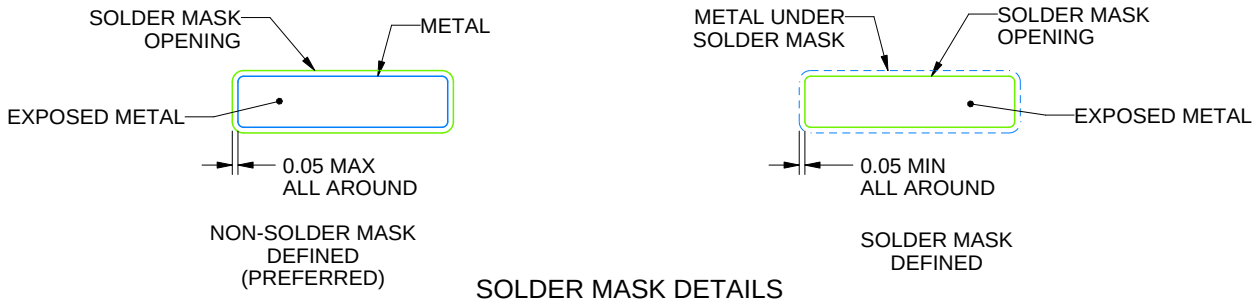

4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

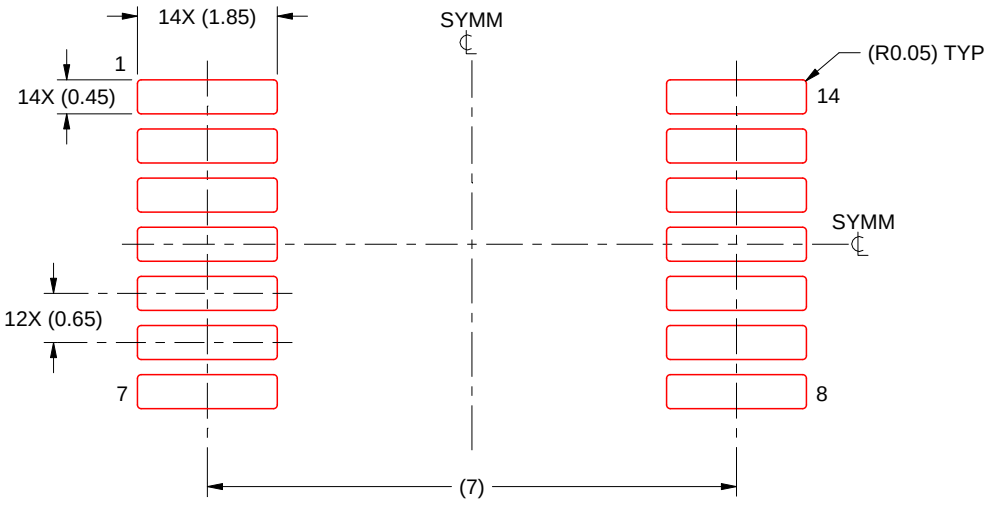



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

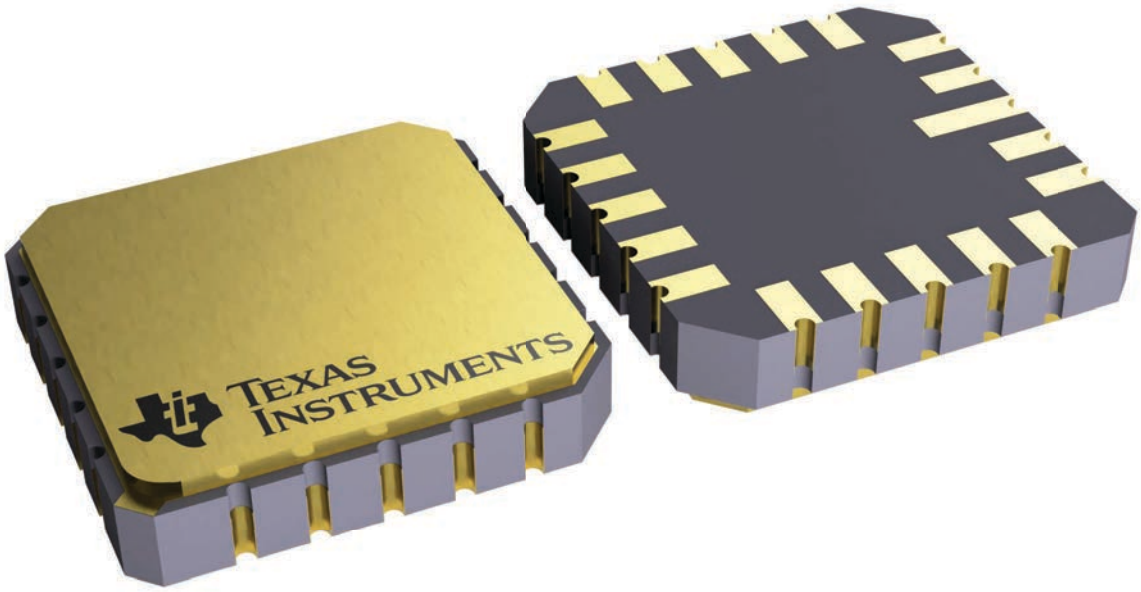
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

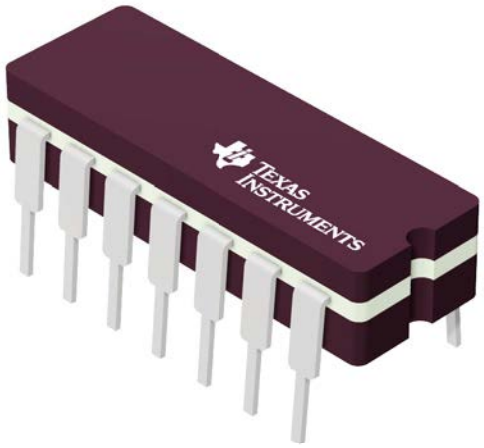



4229370VA\

# GENERIC PACKAGE VIEW

## J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

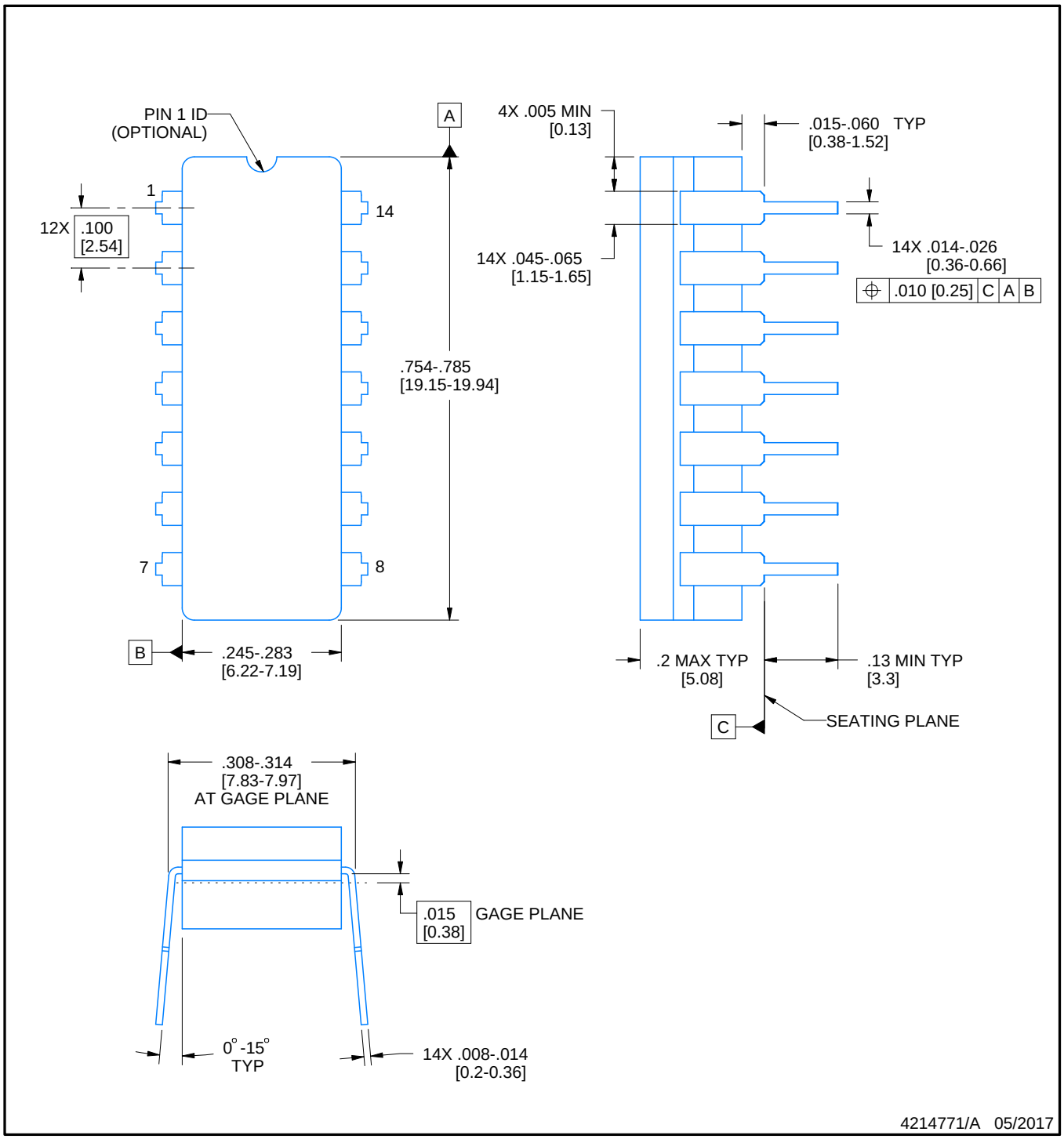
4040083-5/G

# PACKAGE OUTLINE

## J0014A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




NOTES:

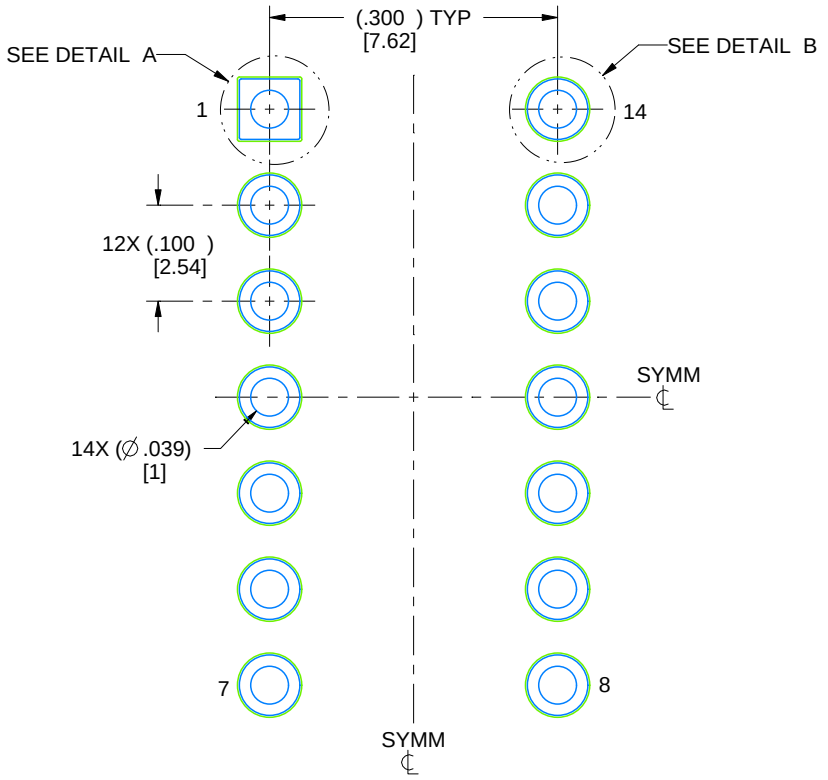
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

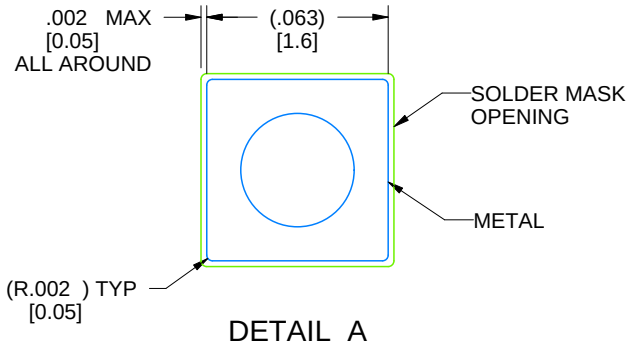
## J0014A

## CDIP - 5.08 mm max height

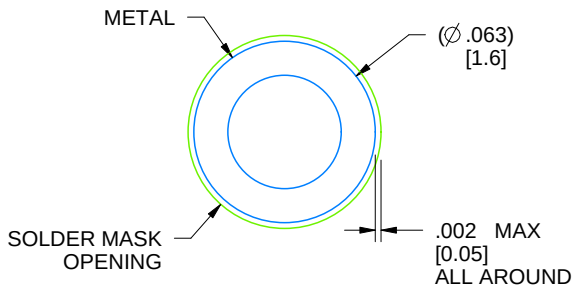
CERAMIC DUAL IN LINE PACKAGE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X




DETAIL A
SCALE: 15X



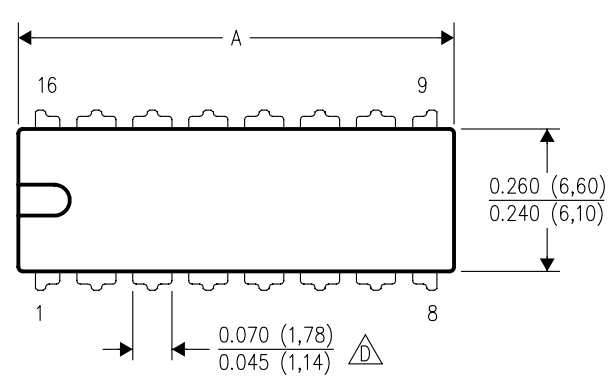

DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

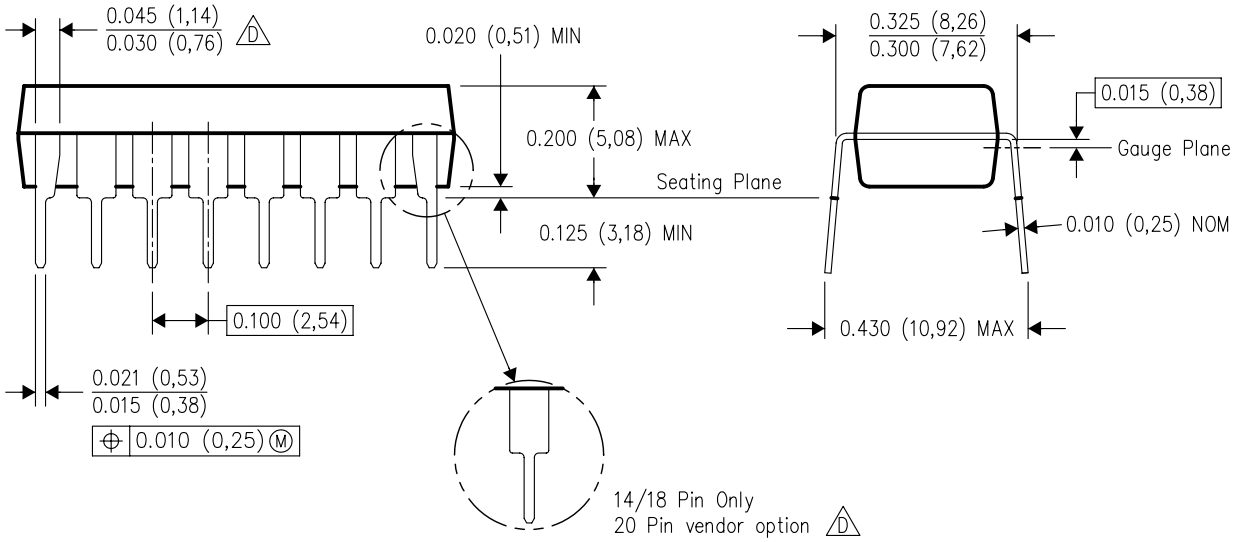
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

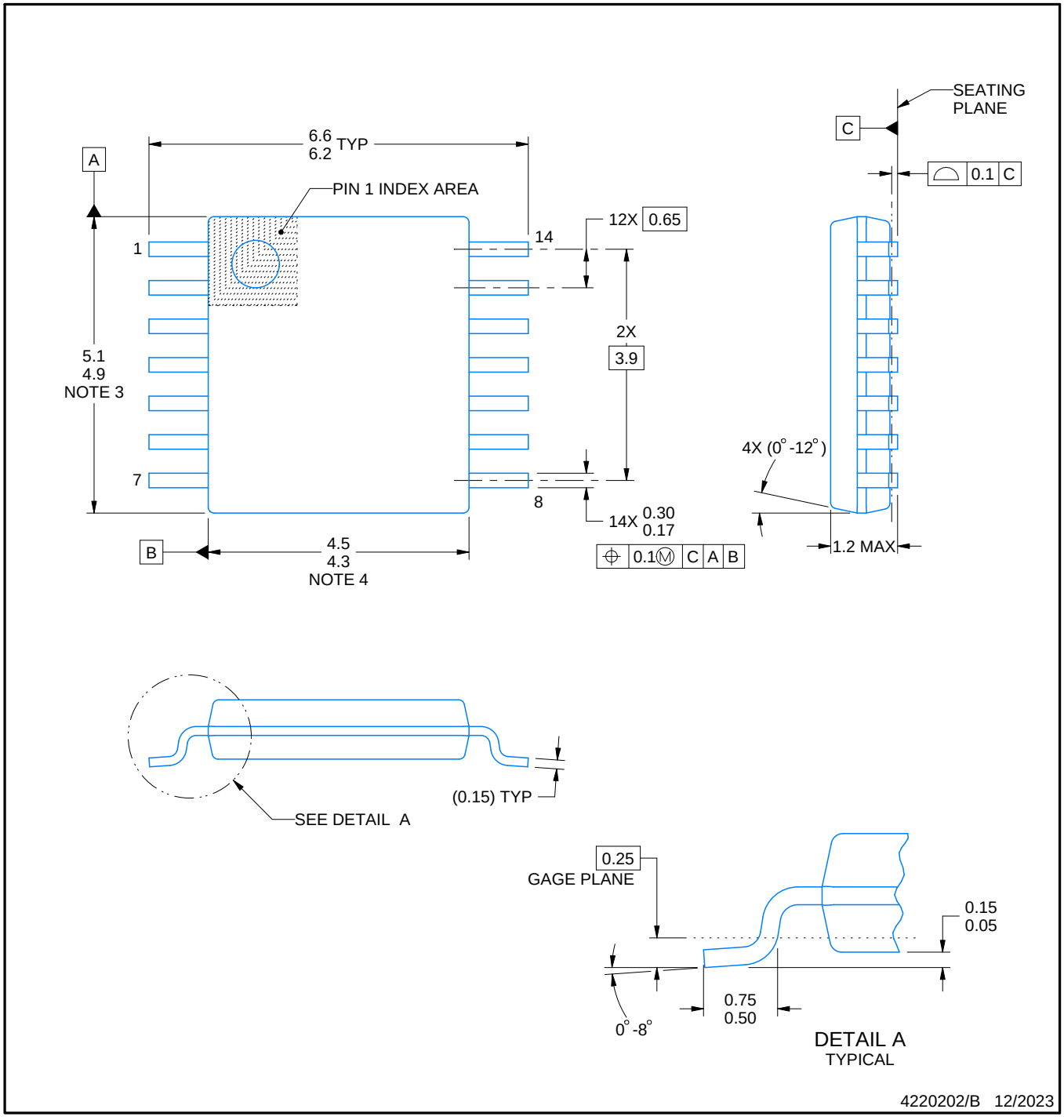
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

# PACKAGE OUTLINE

## PW0014A

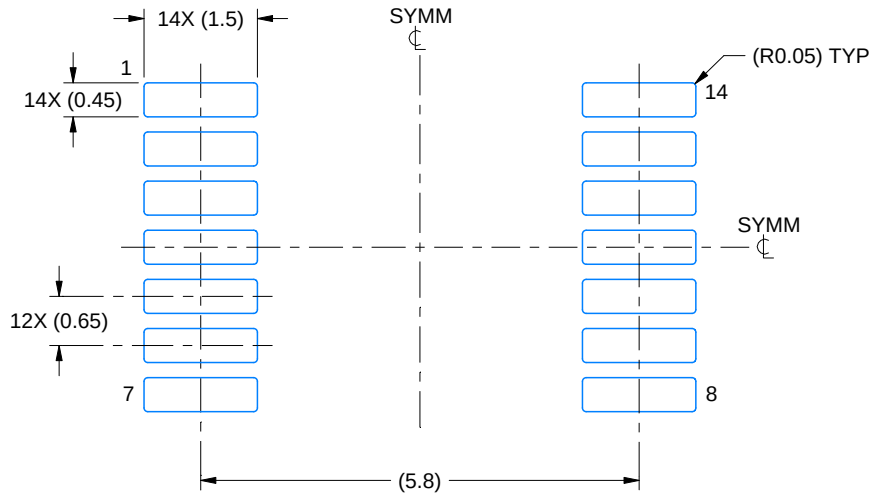
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

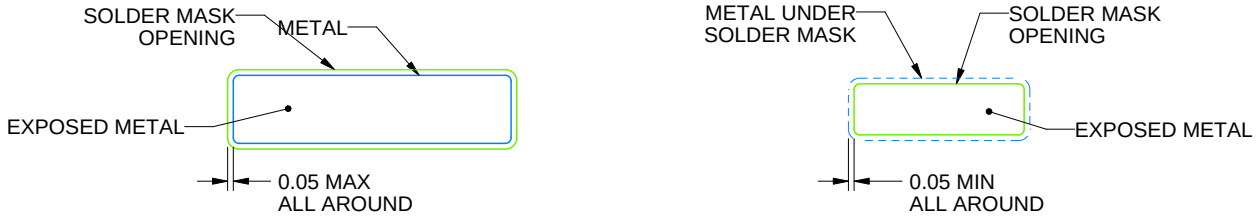



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

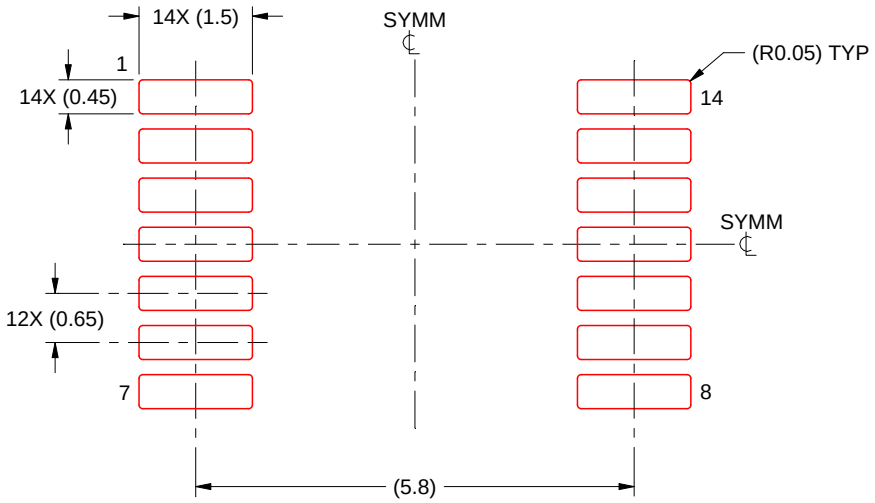



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

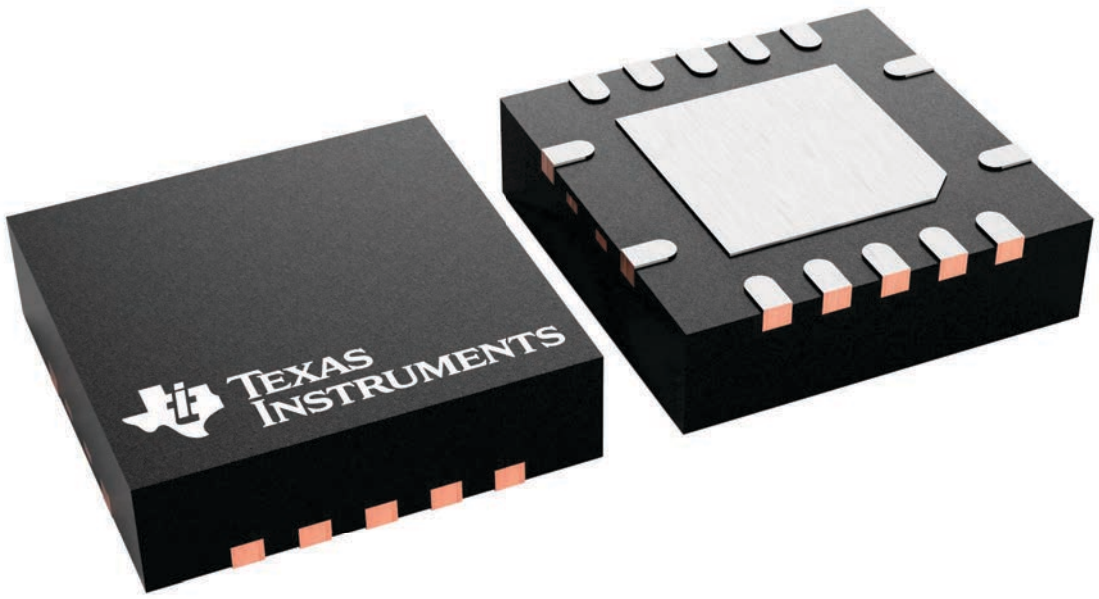
## RGY 14

## VQFN - 1 mm max height

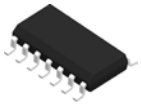
**3.5 x 3.5, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4231541/A

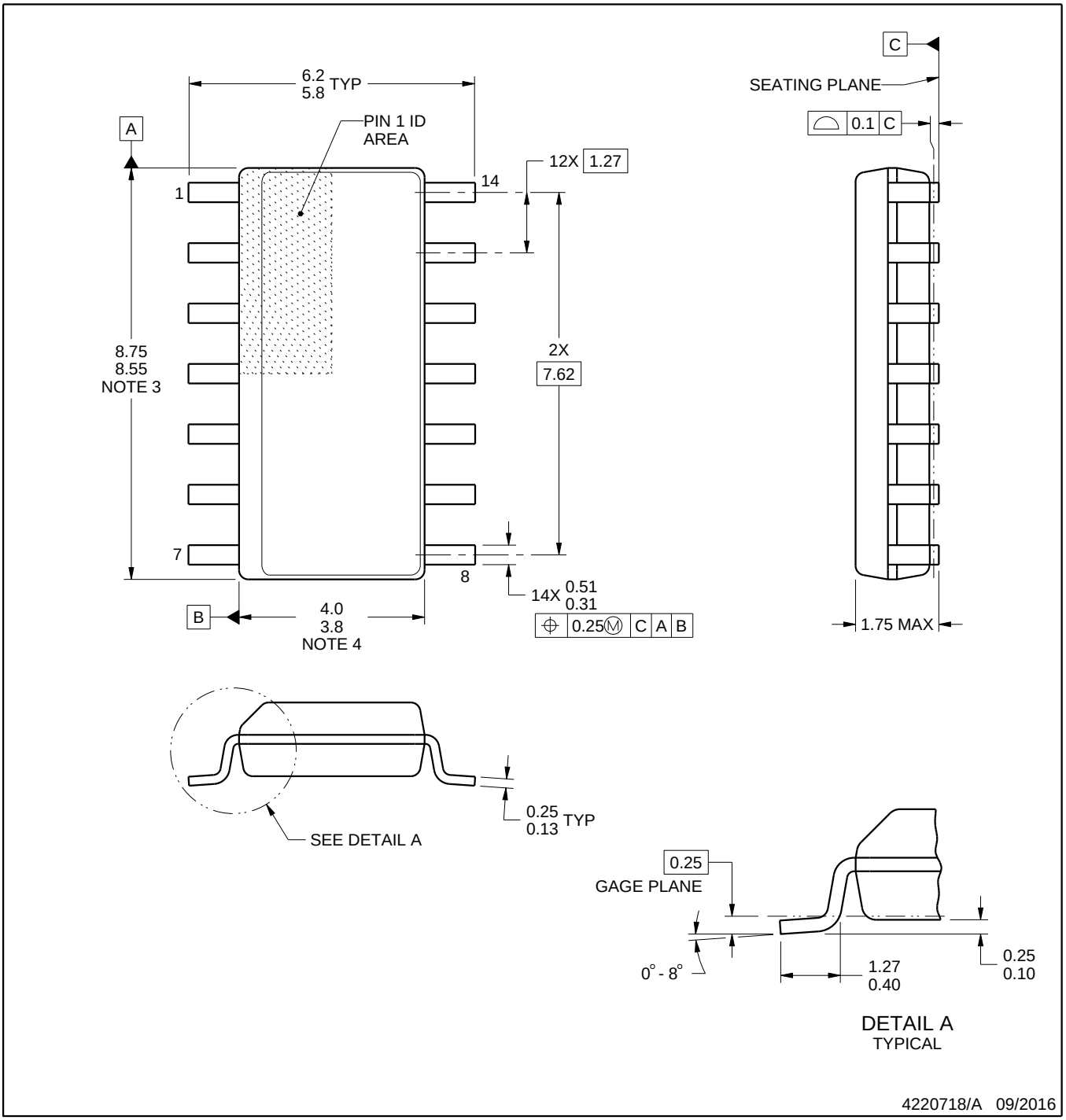


# PACKAGE OUTLINE

## D0014A

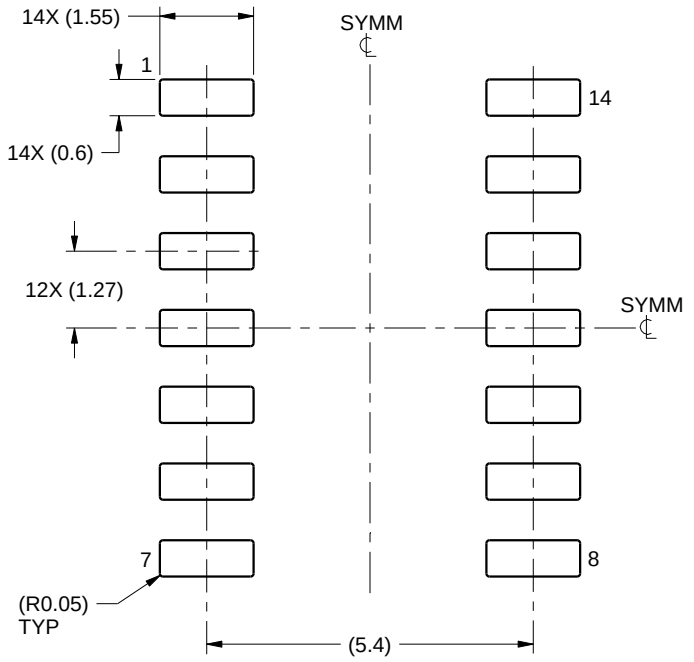
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

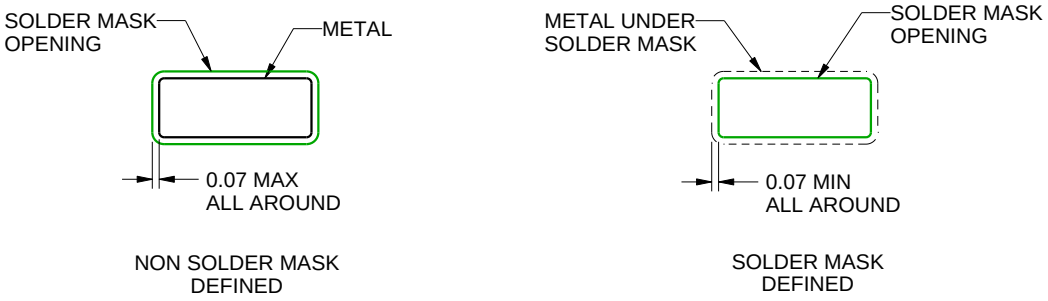



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

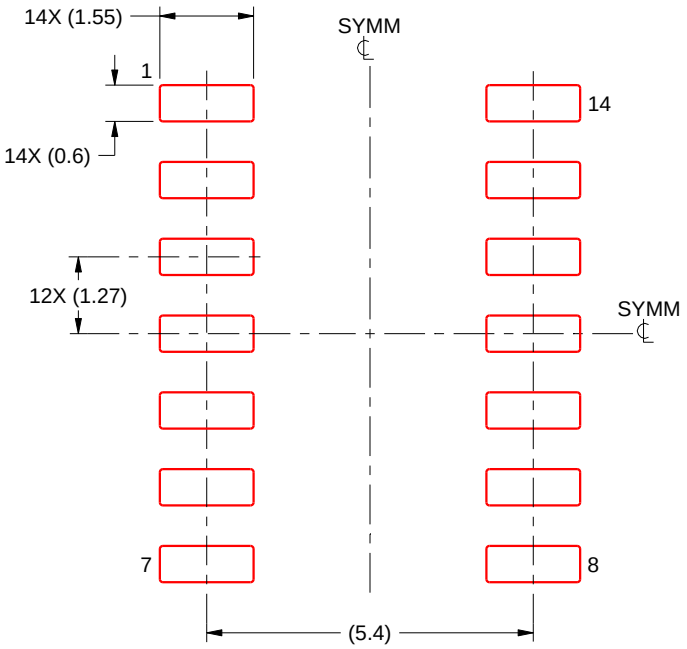
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

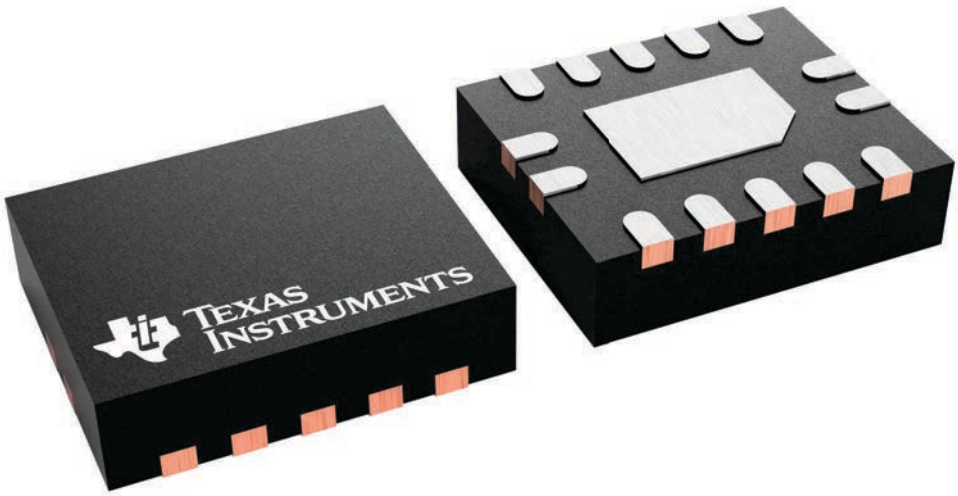
## BQA 14

## WQFN - 0.8 mm max height

**2.5 x 3, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

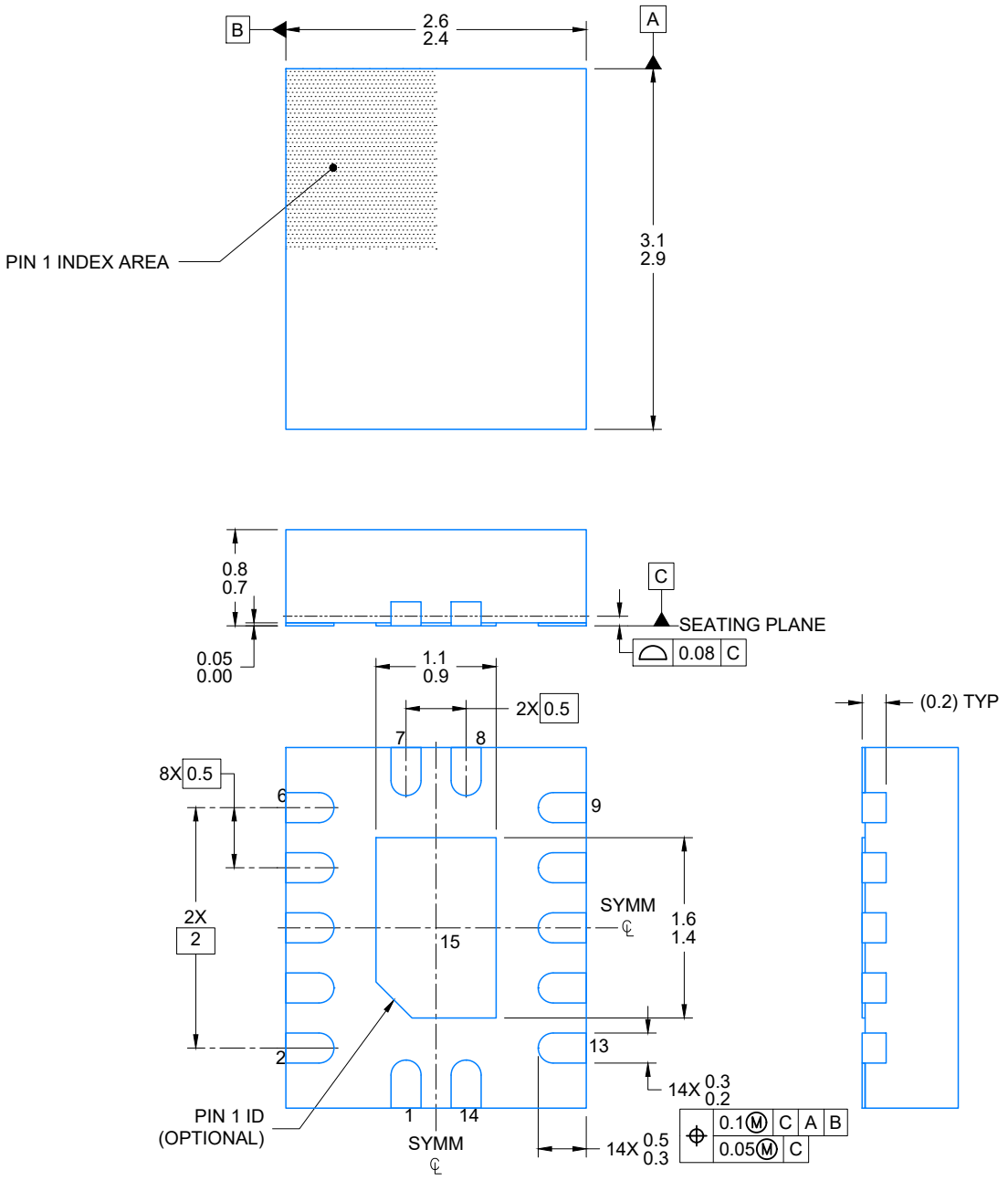


# PACKAGE OUTLINE

## BQA0014A

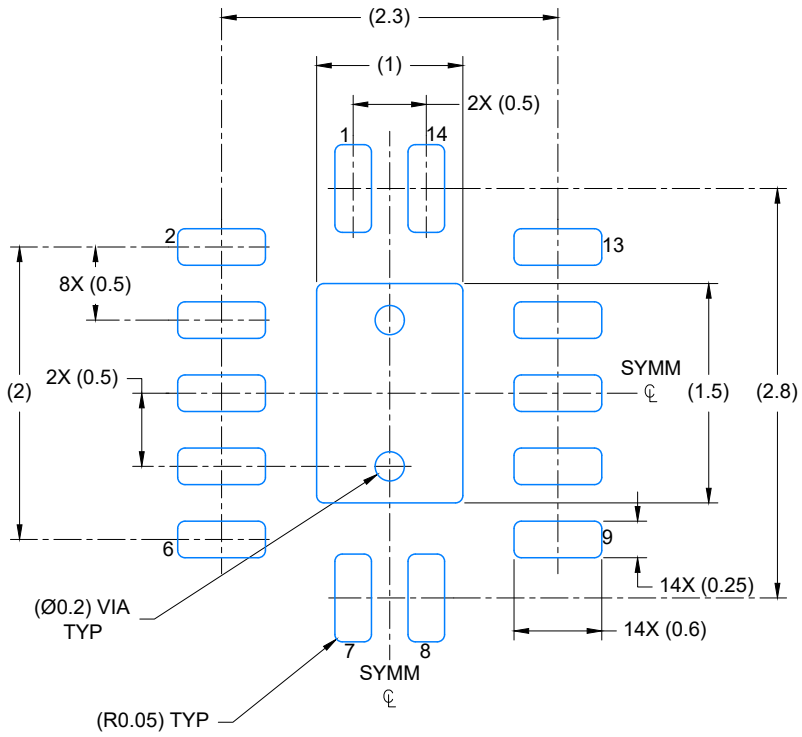
### WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

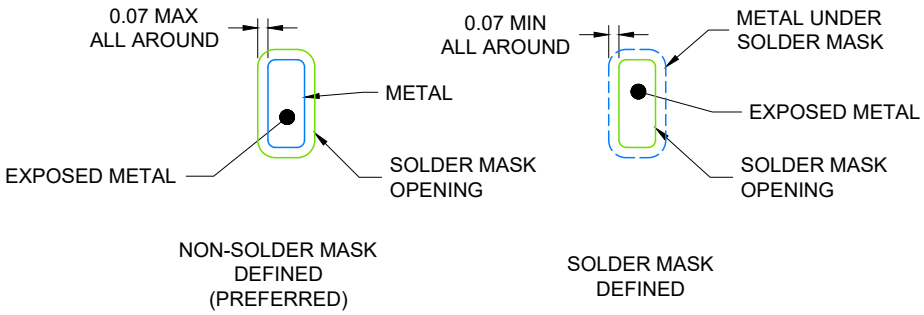



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



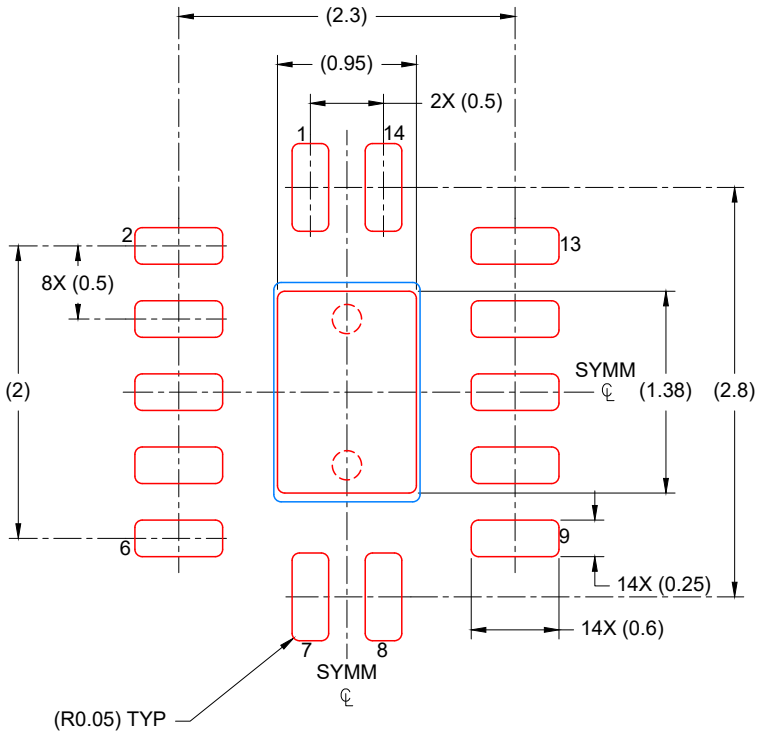

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

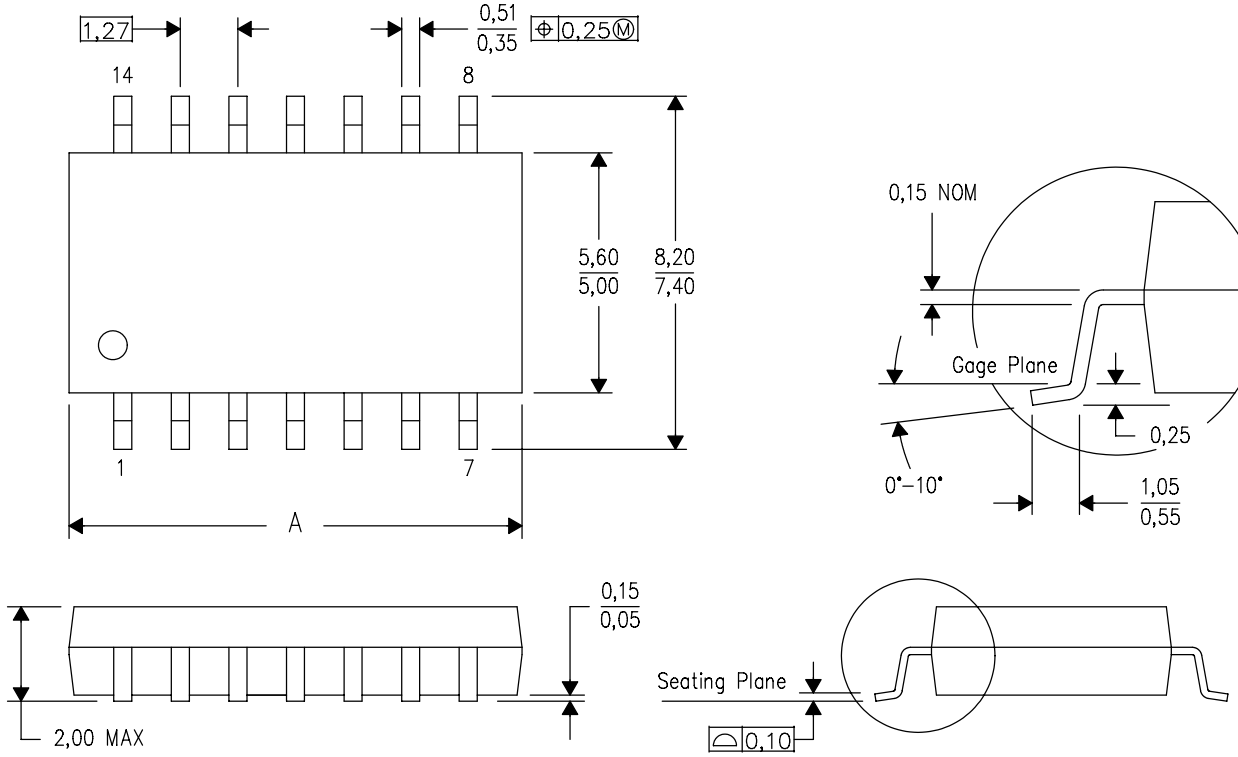
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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