SN75ALS194 Quadruple Differential Line Drivers

1 Features

- Meet or exceed the requirements of ANSI standard EIA/TIA-422-B and ITU recommendation V.11
- Designed to operate up to 20 Mbaud
- 3-state TTL-compatible outputs
- Single 5V supply operation
- High output impedance in power-off condition
- Two pairs of drivers, independently enabled
- Designed as improved replacements for the MC3487

2 Applications

- Factory automation
- ATM and cash counters
- Smart grid
- AC and servo motor drives

3 Description

These four differential line drivers are designed for data transmission over twisted-pair or parallel-wire transmission lines. They meet the requirements of ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11 and are compatible with 3-state TTL circuits. Advanced low-power Schottky technology provides high speed without the usual power penalty. Standby supply current is typically only 26mA. Typical propagation delay time is less than 10ns, and enable/disable times are typically less than 16ns.

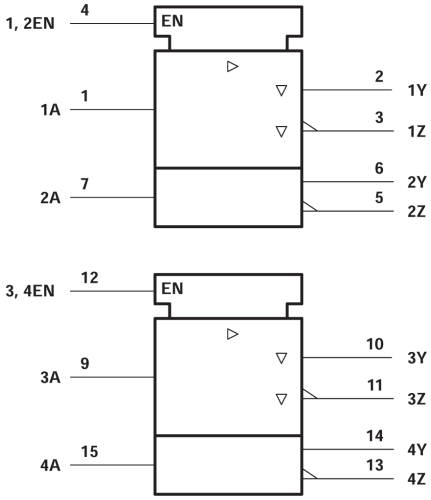
High-impedance inputs keep input currents low: less than 1μA for a high level and less than 100μA for a low level. The driver circuits can be enabled in pairs by separate active-high enable inputs. The SN75ALS194 is capable of data rates in excess of 20 megabits per second and is designed to operates with the SN75ALS195 quadruple line receiver.

The SN75ALS194 is characterized for operation from 0°C to 70°C.

Package Information

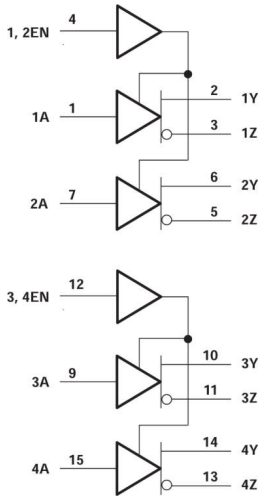
PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN75ALS194	NS (SOP, 16)	10.2mm × 7.8mm
	D (SOIC, 16)	9.9mm × 6mm
	N (PDIP, 16)	19.3mm × 9.4mm

(1) For more information, Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Pin numbers shown are for the D, J, N, and W packages.

Logic Symbol[1]



Logic Diagram (Positive Logic)

[1] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Table of Contents

4 Pin Configuration and Functions

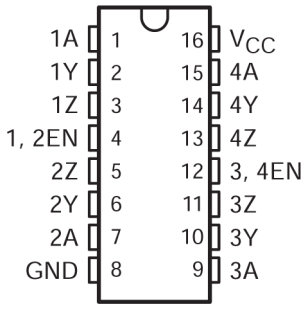


Figure 4-1. D, N, or NS Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A	1	I	Single Ended Data Input for Channel 1
1Y	2	O	Non-Inverting Output for Differential Driver on Channel 1
1Z	3	O	Inverting Output of Differential Driver on Channel 1
1, 2EN	4	I	Channel 1 and 2 Enable
2Z	5	O	Inverting Output of Differential Driver on Channel 2
2Y	6	O	Non-Inverting Output for Differential Driver on Channel 2
2A	7	I	Single Ended Data Input for Channel 2
GND	8	GND	Device GND
3A	9	I	Single Ended Data Input for Channel 3
3Y	10	O	Non-Inverting Output for Differential Driver on Channel 3
3Z	11	O	Inverting Output of Differential Driver on Channel 3
3, 4EN	12	I	Channel 3 and 4 Enable
4Z	13	O	Inverting Output of Differential Driver on Channel 4
4Y	14	O	Non-Inverting Output for Differential Driver on Channel 4
4A	15	I	Single Ended Data Input for Channel 4
V_{CC}	16	PWR	Device VCC (4.75V to 5.25V)

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage, (see (2))			7	V
V_I	Input voltage			5.5	V
V_O	Output voltage			7	V
	Continuous total dissipation			See *Dissipation Ratings* table	
T_A	Operating free-air temperature range:	SN75ALS194	0	70	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds:	D or N package		260	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal

5.2 Dissipation Ratings

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 125°CPOWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
N	1150 mW	9.2 mW/°C	736 mW	N/A

5.3 Recommended Operating Conditions

(1)		SN75ALS194			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	All inputs, T_A = 25°C	2			V
	A inputs, T_A = Full range	2			
	EN inputs, T_A = Full range	2			
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}				-20	mA
Low-level output current, I_{OL}	T_A = 25°C			48	mA
	T_A = Full range			48	
Operating free-air temperature, T_A		0		70	°C

(1) Full range is TA = 0°C to 70°C for SN75ALS194.

5.4 Thermal Information

THERMAL METRIC(1)		D (SOIC)	N (PDIP)	NS (SOP)	UNIT
		16-PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	60.6	88.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	48.1	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	40.6	50.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	27.5	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	40.3	50.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = –18mA			–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = –20mA	SN75ALS194	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = MAX			0.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100W,	See Figure 5-1	1/2 V_{OD1} or 2(3)			V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(4)					±0.4	V
V_{OC}	Common-mode output voltage					±3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(4)					±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6V			100	mA
			V_O = –0.25V			–100	
I_{OZ}	High-impedance-state output current	V_{CC} = MAX, Output enables at 0.8V	V_O = 2.7V			100	
			V_O = 0.5V			–100	mA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			100	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			50	mA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5V			–200	mA
I_{OS}	Short-circuit output current(5)	V_{CC} = MAX,	V_I = 2V	–40		–140	mA
I_{CC}	Supply current (all drivers)	V_{CC} = MAX,	All outputs disabled		26	45	mA

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) All typical values are at V_{CC} = 5V, TA = 25°C.
(3) The minimum V_{OD2} with a 100Ω load is either 1/2V_{OD1} or 2V, whichever is greater.
(4) Δ | V_{OD} | and Δ | V_{OC} | are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(5) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

5.6 Switching Characteristics

V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN75ALS194			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	C 15 F L = 15pF, See Figure 6-1		6	13	ns
t_{PHL}	Propagation delay time, high- to low-level output			9	14	ns
	Output-to-output skew			3.5	6	ns
$t_{t(OD)}$	Differential output transition time	C_L = 15pF, See Figure 6-2		8	14	ns
t_{PZH}	Output enable time to high level	C_L = 15pF, See Figure 6-3		9	12	ns
t_{PZL}	Output enable time to low level			12	20	ns
t_{PHZ}	Output disable time from high level			9	14	ns
t_{PLZ}	Output disable time from low level			12	15	ns

Table 5-1. Symbol Equivalents

DATA SHEET PARAMETER	EIA/TIA-422-B
V_O	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)
$\Delta \lvert V_{OD} \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$
V_{OC}	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$

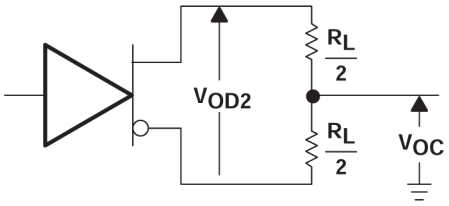


Figure 5-1. Driver V_{OD} And V_{OC}

5.7 Typical Characteristics

Data for temperatures below 0°C and above 70°C are applicable to the SN55ALS194 circuits only.
The A input is connected to V_{CC} during the testing of the Y outputs and to GND during the testing of the Z outputs.
The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

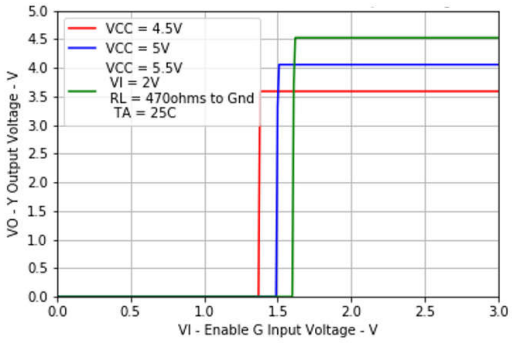


Figure 5-2. Y Output Voltage vs Data Input Voltage

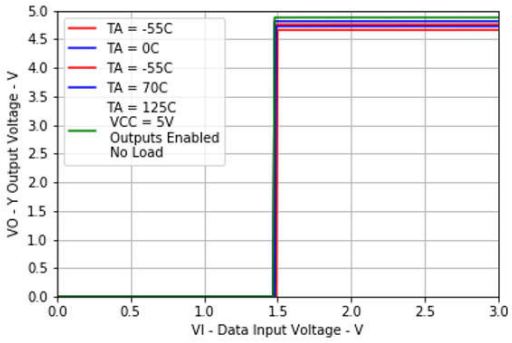


Figure 5-3. Y Output Voltage vs Data Input Voltage

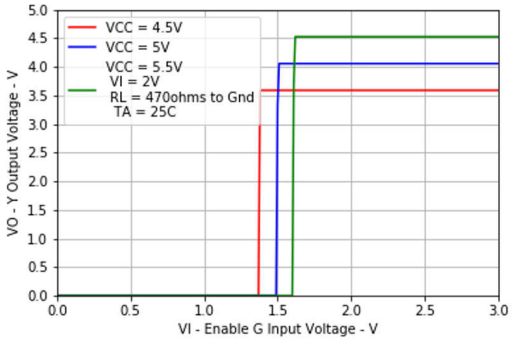


Figure 5-4. Y Output Voltage vs Enable G Input Voltage

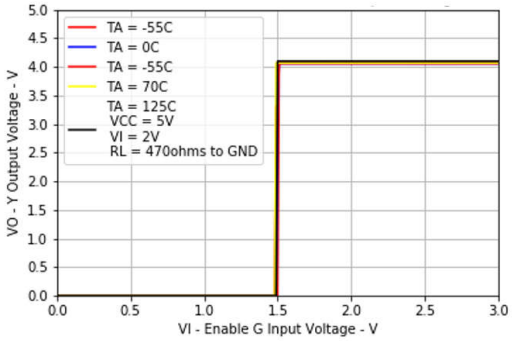


Figure 5-5. Y Output Voltage vs Enable G Input Voltage

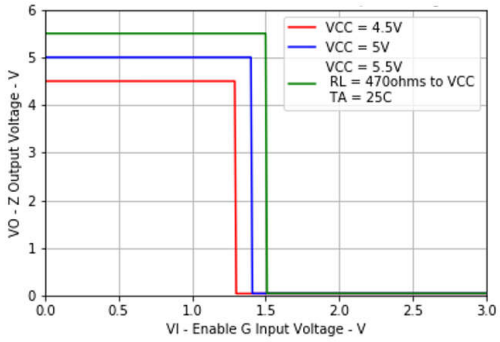


Figure 5-6. Z Output Voltage vs Enable G Input Voltage

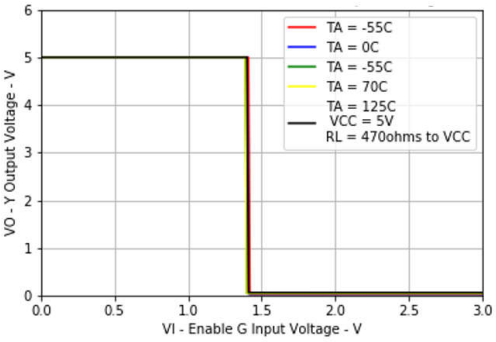


Figure 5-7. Z Output Voltage vs Enable G Input Voltage

5.7 Typical Characteristics (continued)

Data for temperatures below 0°C and above 70°C are applicable to the SN55ALS194 circuits only.
The A input is connected to V_{CC} during the testing of the Y outputs and to GND during the testing of the Z outputs.
The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

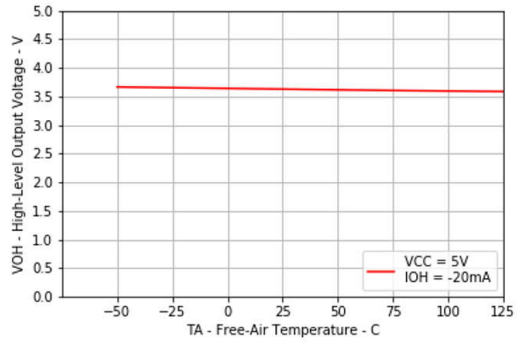


Figure 5-8. High-level Output Voltage vs Free-air Temperature

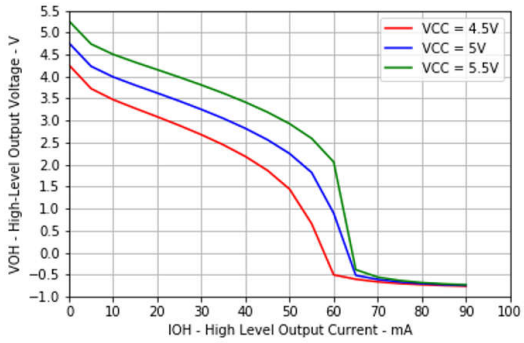


Figure 5-9. High-level Output Voltage vs High-level Output Current

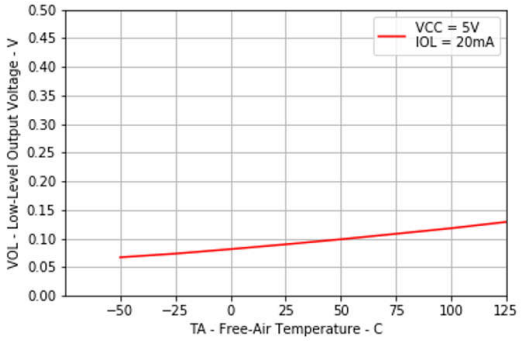


Figure 5-10. Low-level Output Voltage vs Free-air Temperature

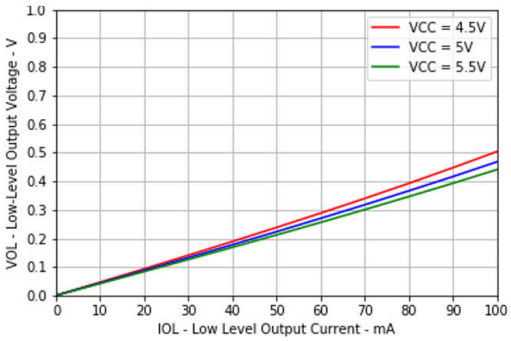


Figure 5-11. Low-level Output Voltage vs Low-level Output Current

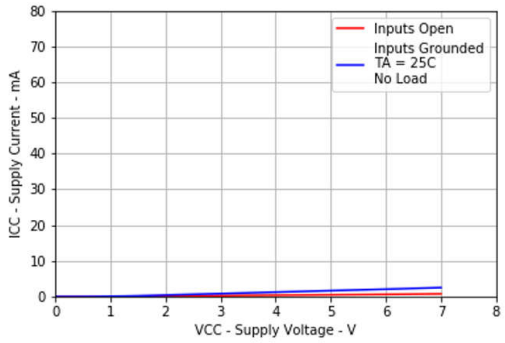


Figure 5-12. Supply Current vs Supply Voltage

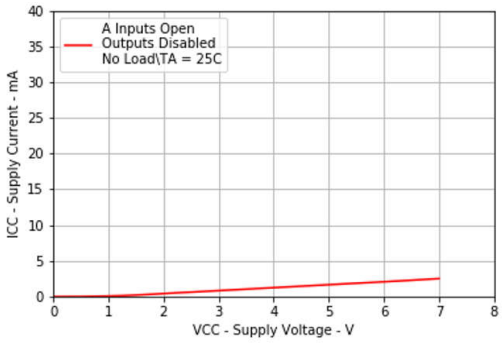


Figure 5-13. Supply Current vs Supply Voltage

5.7 Typical Characteristics (continued)

Data for temperatures below 0°C and above 70°C are applicable to the SN55ALS194 circuits only.
The A input is connected to V_{CC} during the testing of the Y outputs and to GND during the testing of the Z outputs.
The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

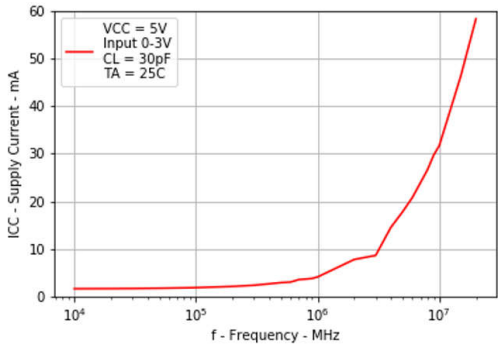
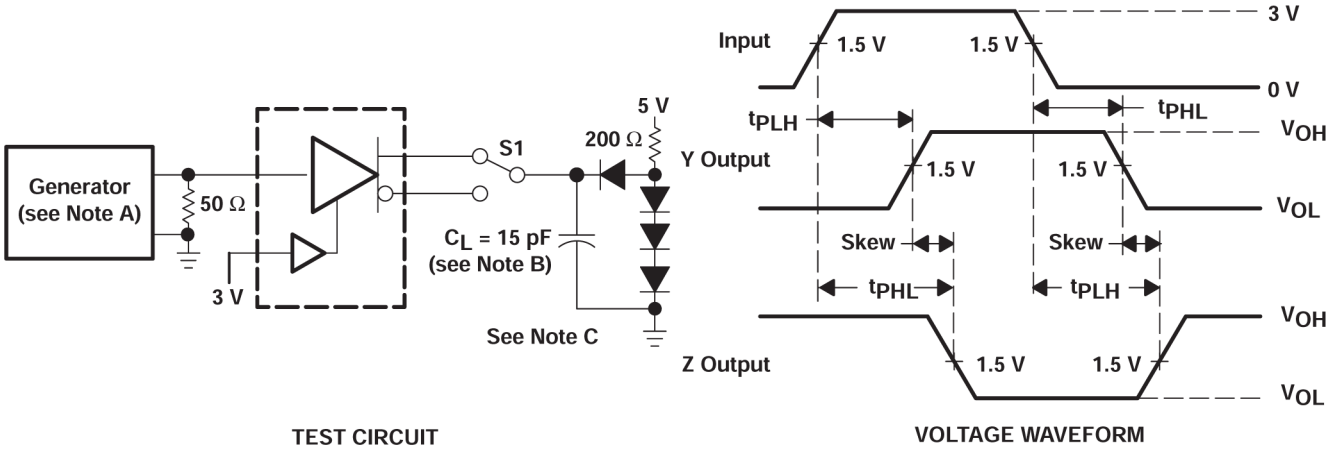


Figure 5-14. Supply Current vs Frequency

6 Parameter Measurement Information

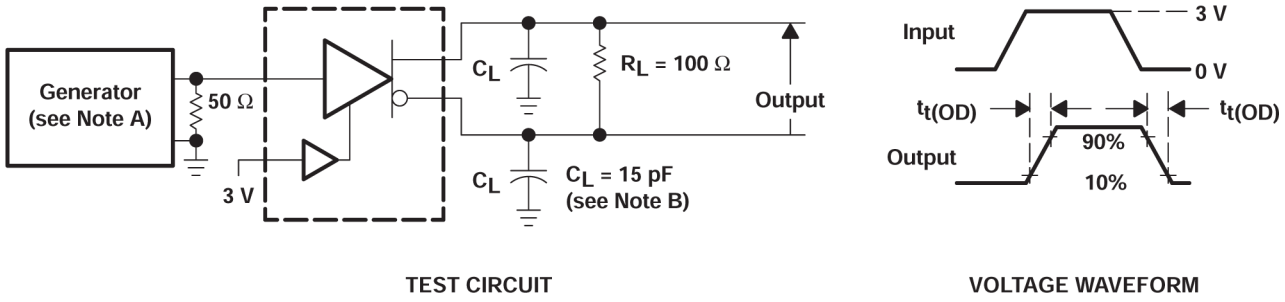


A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5ns$, $t_f \le 5ns$, PRR ≤ 1MHz, duty cycle ≤ 50%, $Z_O \approx 50\Omega$.

B. C_L includes probe and stray capacitance.

C. All diodes are 1N916 or 1N3064.

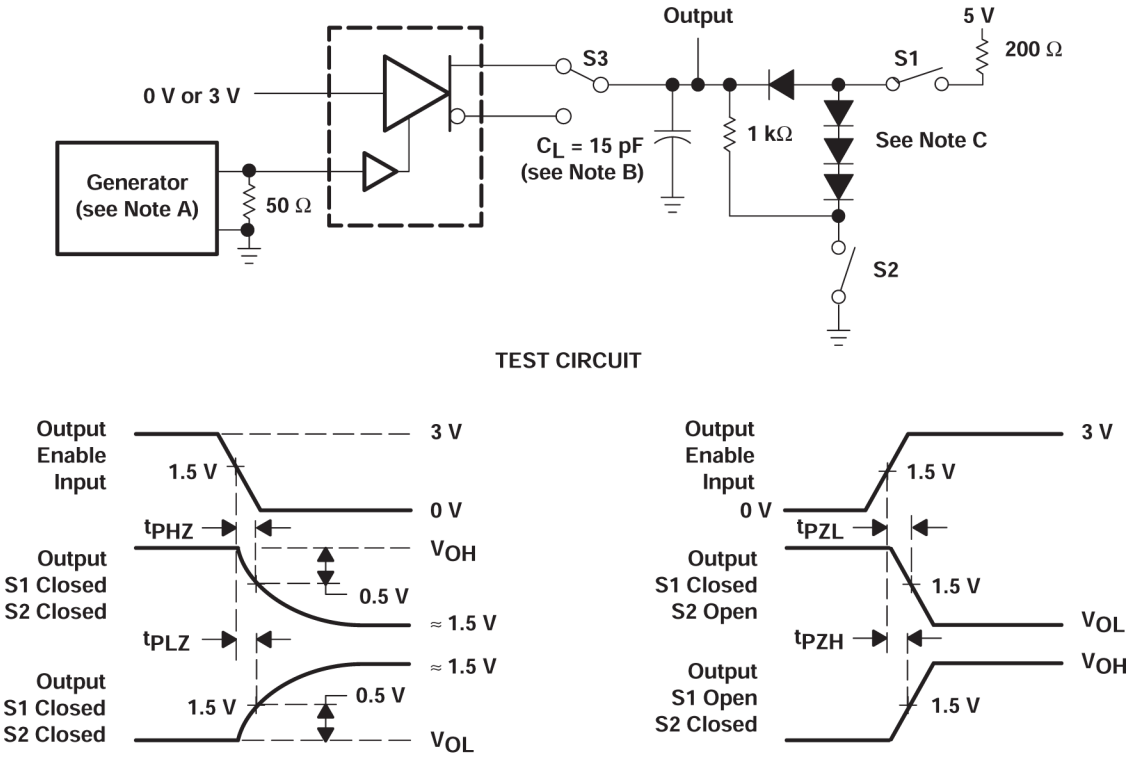
Figure 6-1. Test Circuit and Voltage Waveform



A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5ns$, $t_f \le 5ns$, PRR ≤ 1MHz, duty cycle ≤ 50%, $Z_O \approx 50\Omega$.

B. C_L includes probe and stray capacitance.

Figure 6-2. Differential-Output Test Circuit and Voltage Waveform



A. The input pulse is supplied by a generator having the following characteristics: t_r ≤ 5ns, t_f ≤ 5ns, PRR ≤ 1MHz, duty cycle ≤ 50%, Z_O ≈ 50Ω.

B. C_L includes probe and stray capacitance.

C. All diodes are 1N916 or 1N3064.

Figure 6-3. Driver Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Device Functional Modes

Function Table (Each Driver)

INPUTS A(1)	OUTPUT EN	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

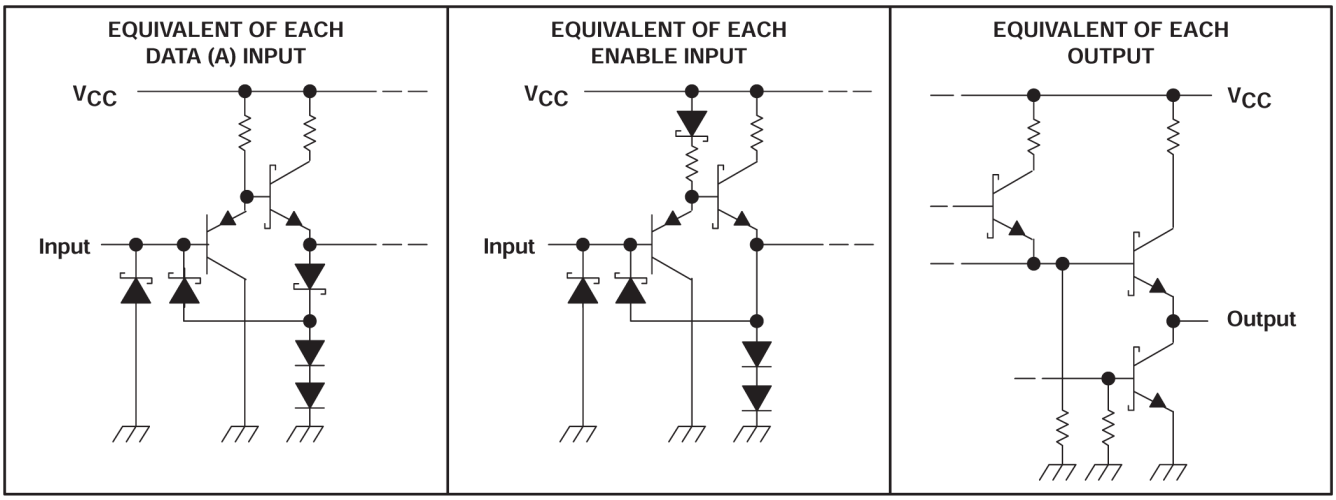


Figure 7-1. Schematics of Inputs and Outputs

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 1995) to Revision E (March 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS194D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	75ALS194	
SN75ALS194DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS194	Samples
SN75ALS194N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS194N	Samples
SN75ALS194NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS194	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

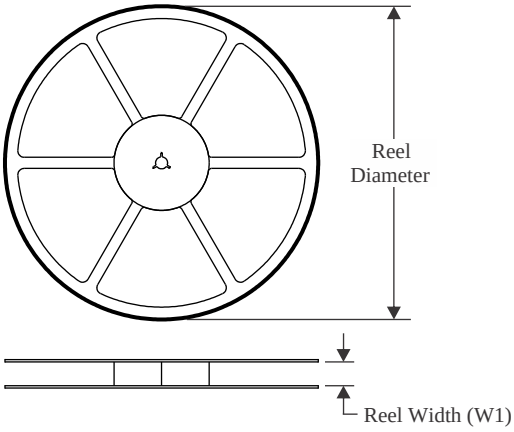
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

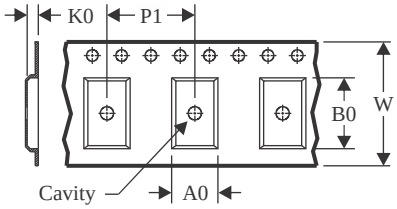
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

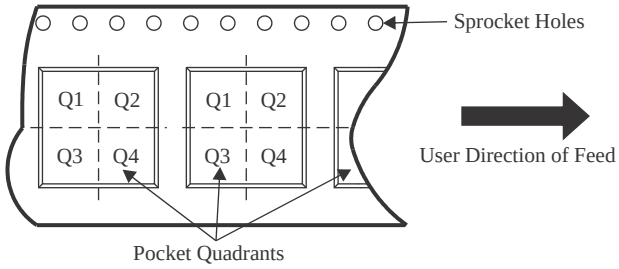


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

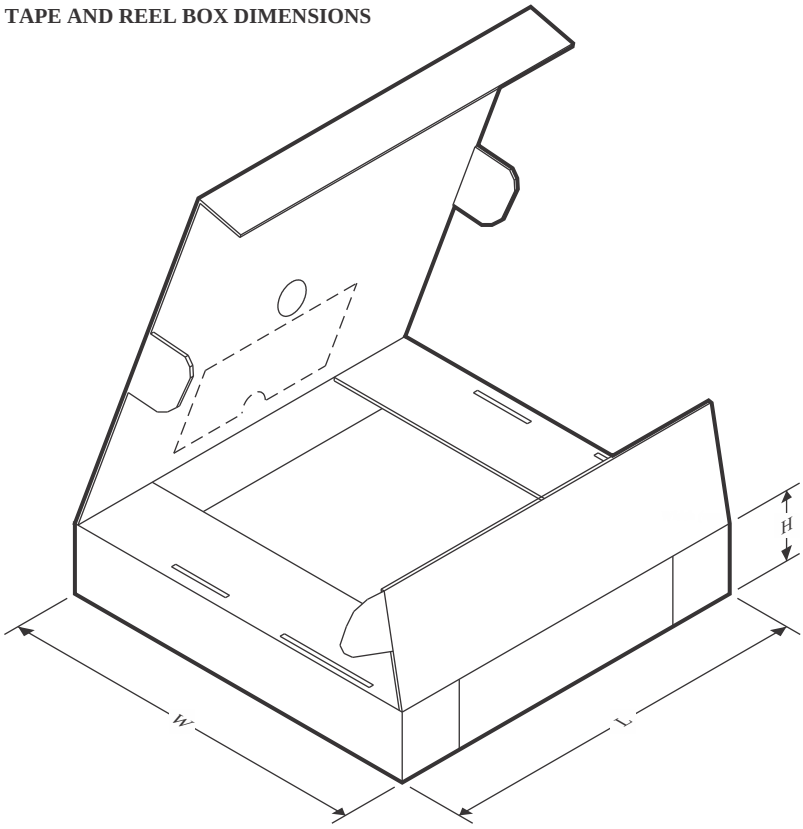
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS194DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75ALS194DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75ALS194NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75ALS194NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

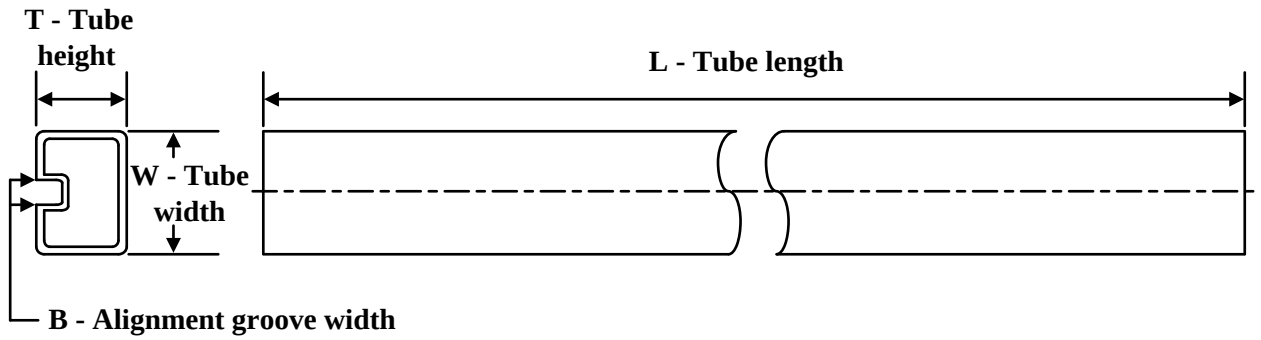
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS194DR	SOIC	D	16	2500	353.0	353.0	32.0
SN75ALS194DR	SOIC	D	16	2500	340.5	336.1	32.0
SN75ALS194NSR	SO	NS	16	2000	356.0	356.0	35.0
SN75ALS194NSR	SO	NS	16	2000	353.0	353.0	32.0

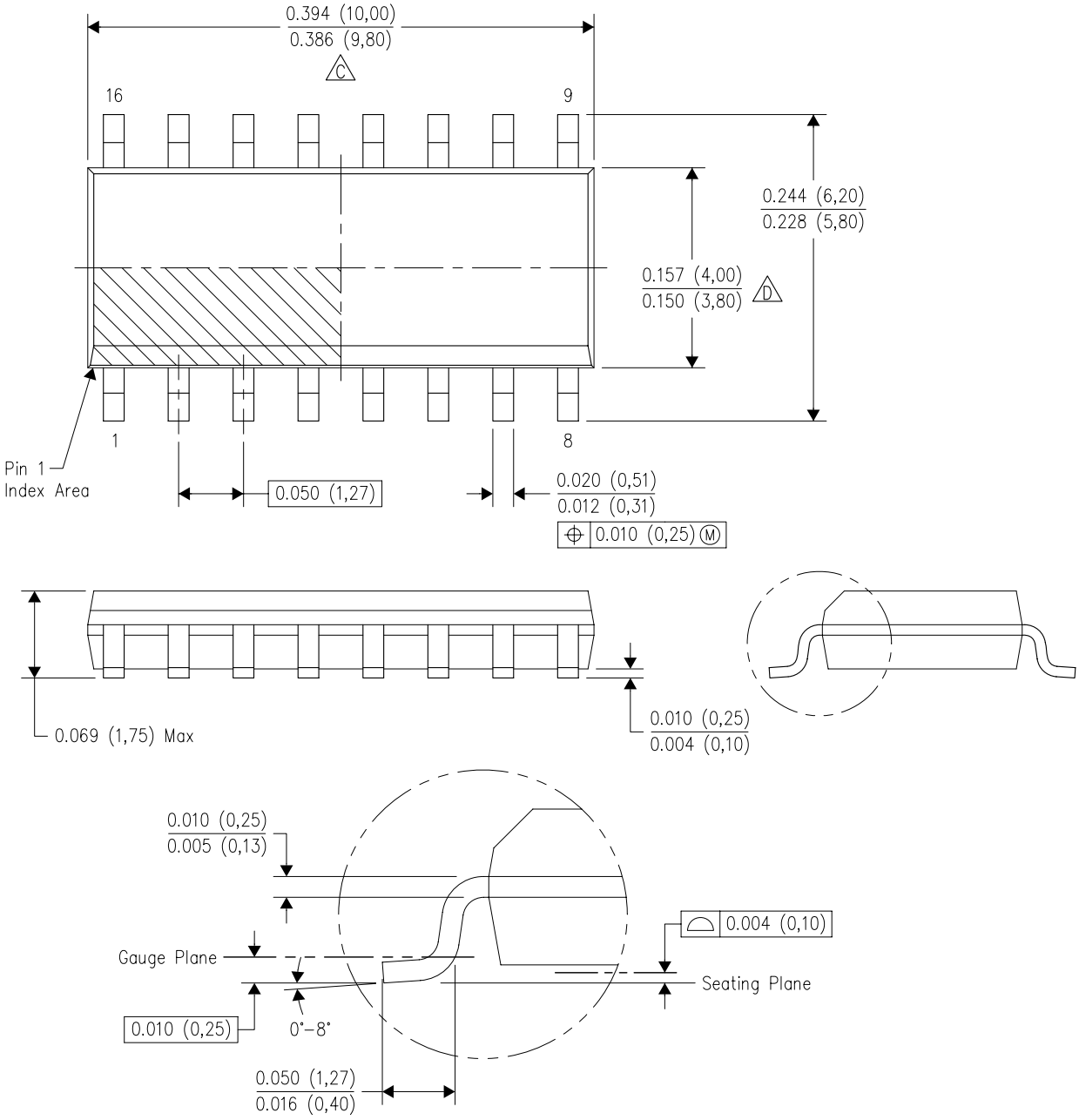
TUBE



*All dimensions are nominal

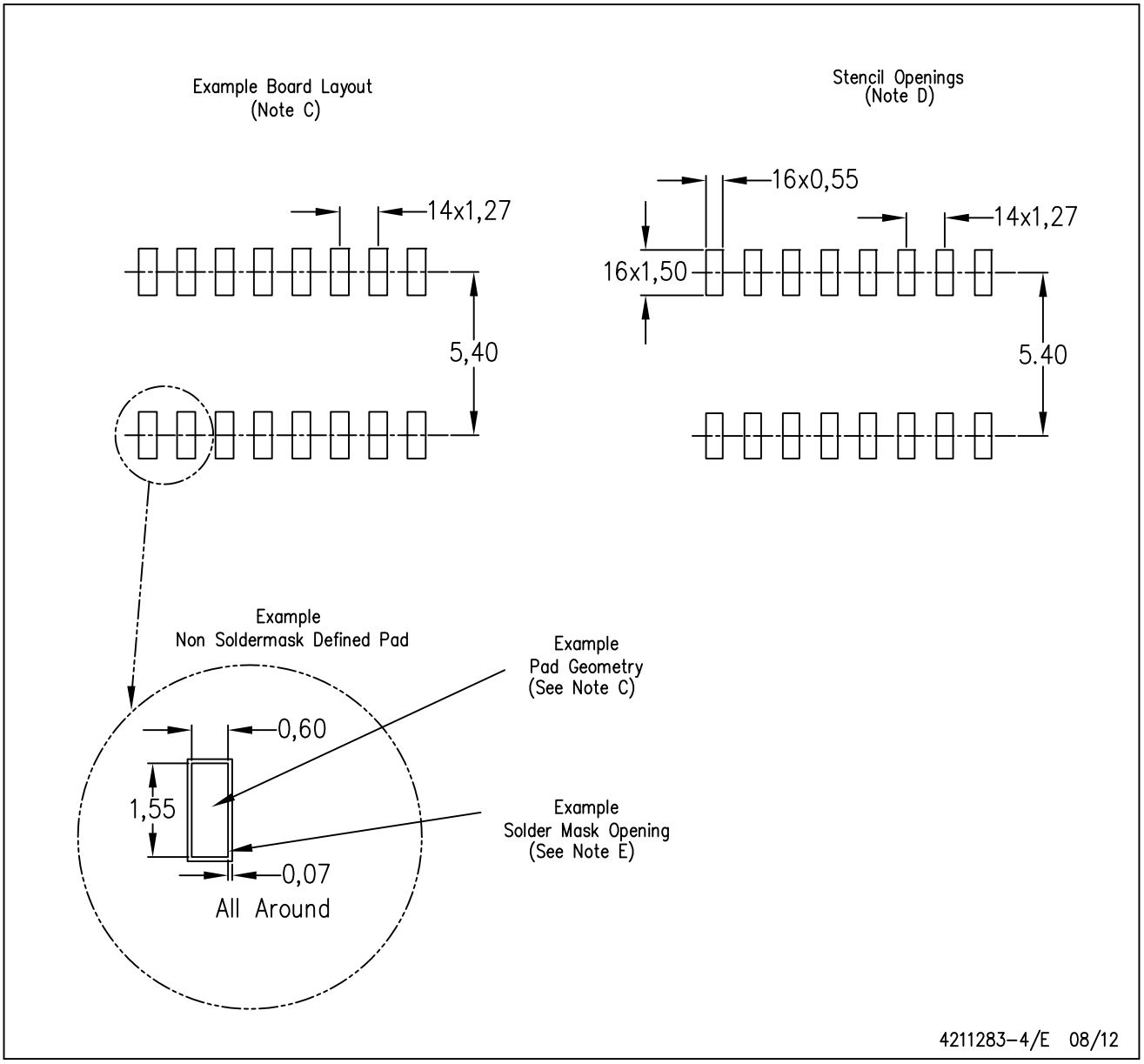
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS194N	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

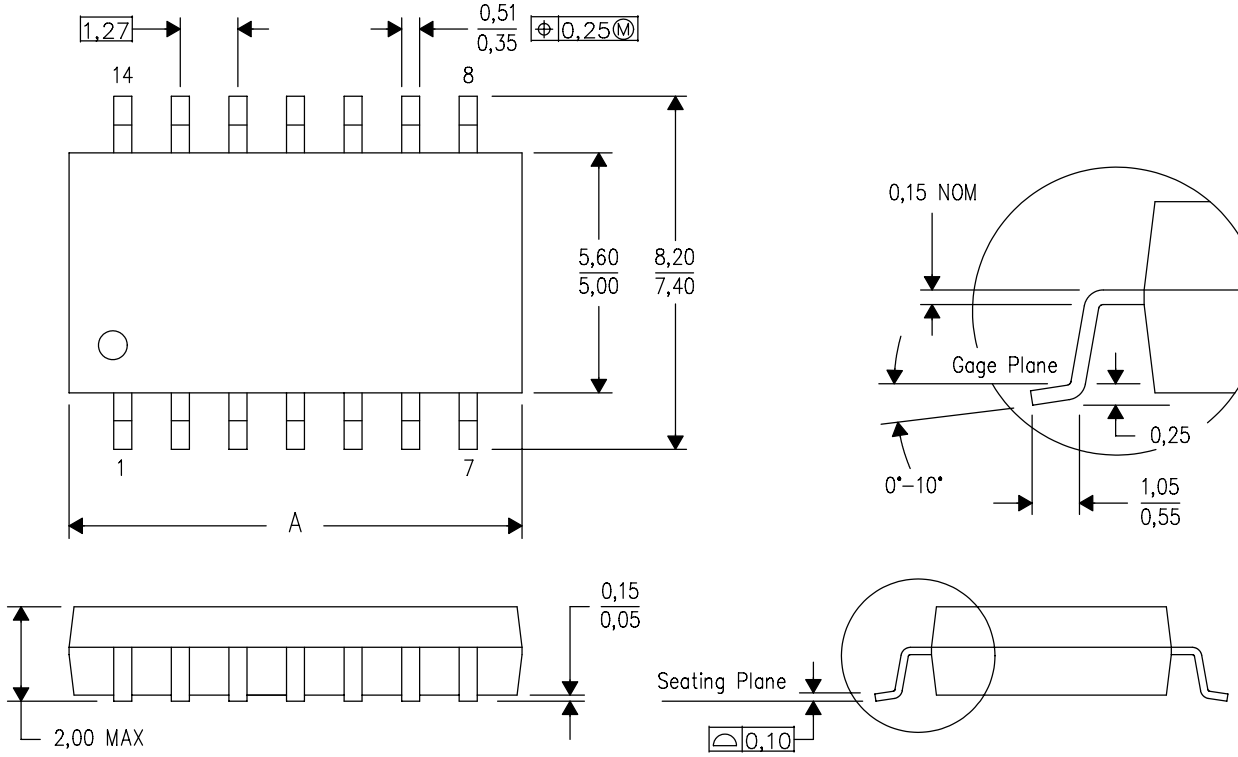


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

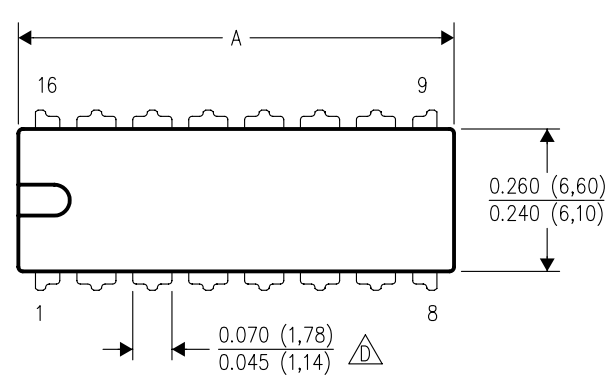
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

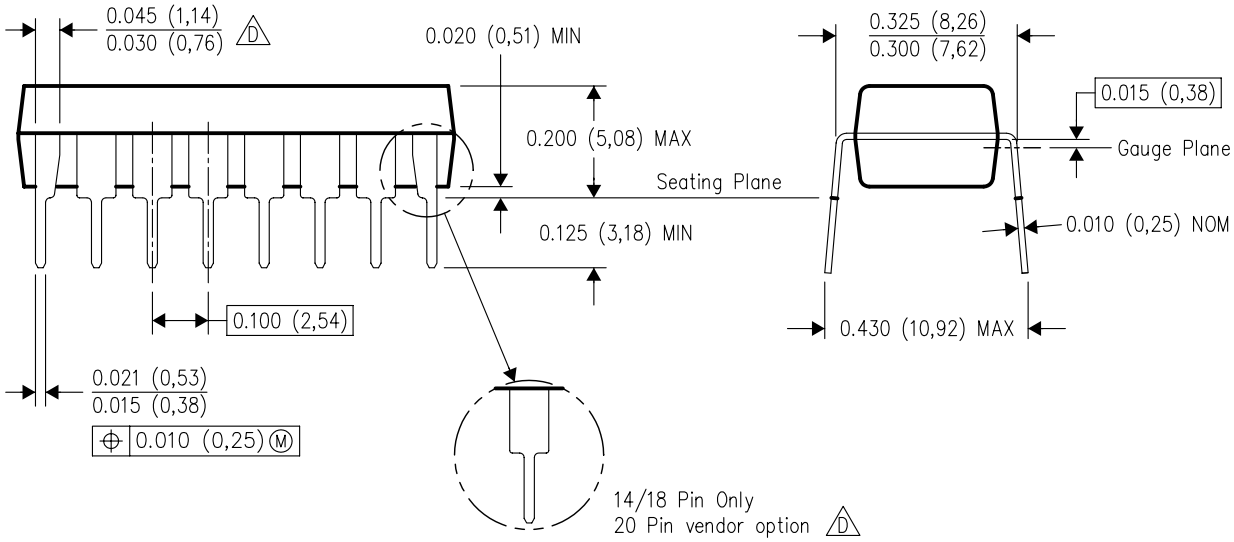
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

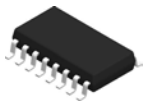


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

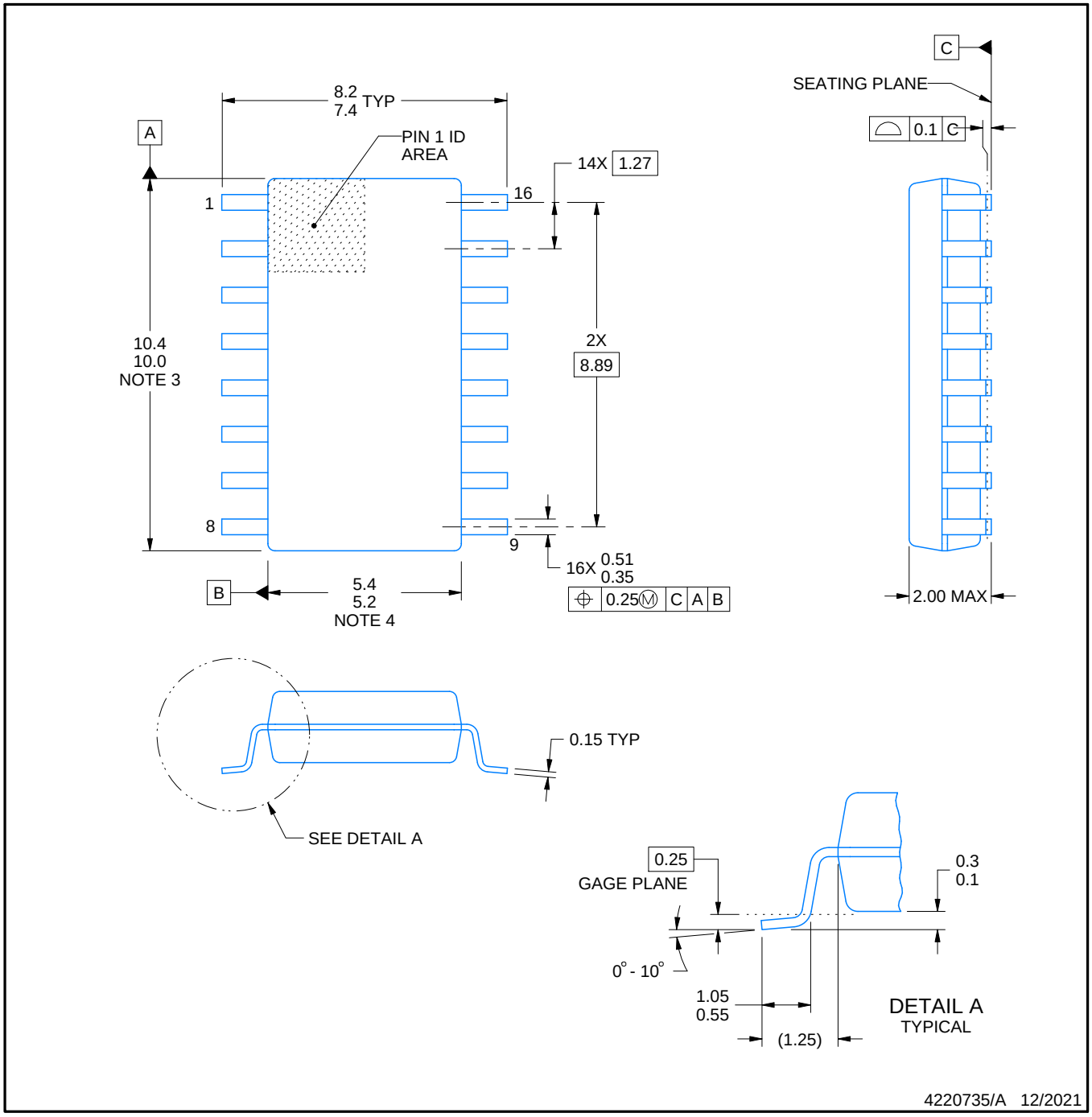


PACKAGE OUTLINE

NS0016A

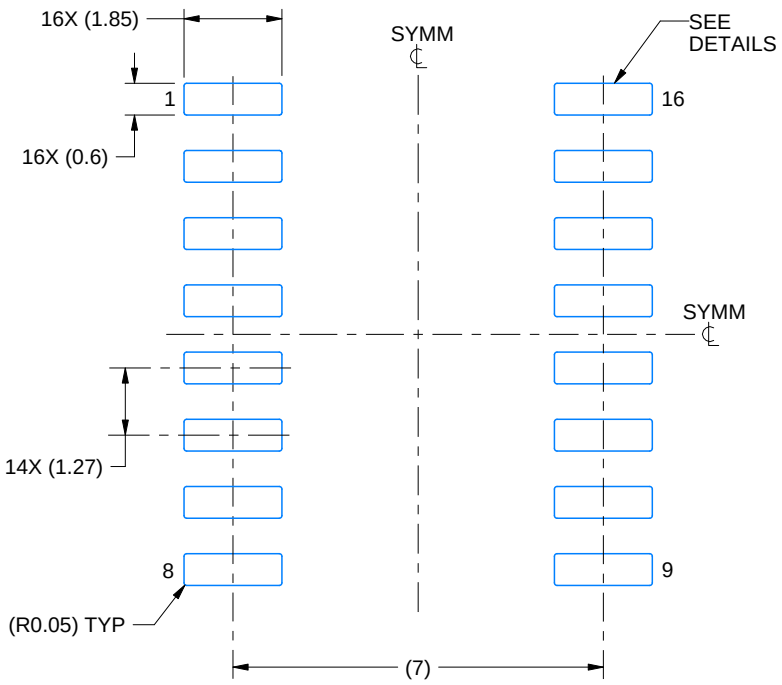
SOP - 2.00 mm max height

SOP

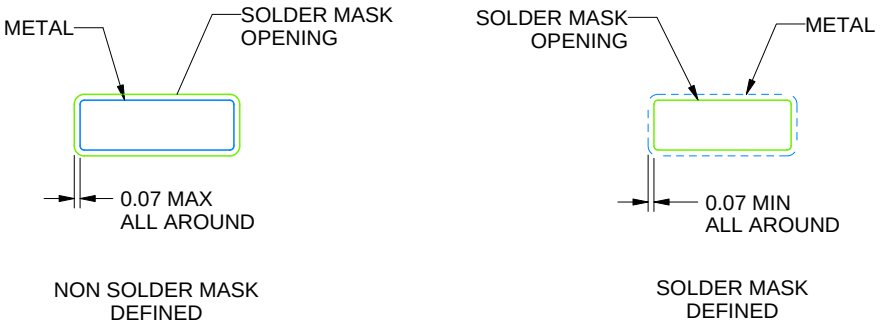


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

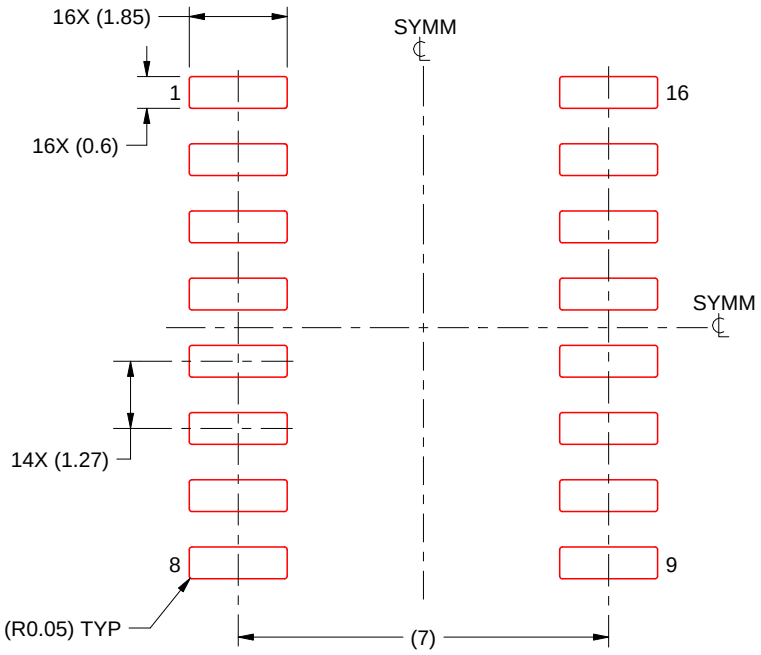
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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