

I²C CONTROLLED 18 CHANNEL GPIO EXPANDER

 Check for Samples: [TCA6418E](#)

FEATURES

- **Operating Power-Supply Voltage Range of 1.65 V to 3.6 V**
- **18 GPIOs Configurable as Inputs or Outputs**
- **ESD Protection Exceeds JESD 22 on Non-GPIO Pins**
 - **2000-V Human Body Model (A114-A)**
 - **1000-V Charged Device Model (C101)**
- **Low Standby (Idle) Current Consumption: 3 μ A**
- **Supports 1-MHz Fast Mode Plus I²C Bus**
- **Open-Drain Active-Low Interrupt Output, Asserted When Key is Pressed or Key is Released**
- **Selectable Debounce Time of 50 μ s**
- **Schmitt-Trigger Action Allows Slow Input Transition and Better Switching Noise Immunity at the SCL and SDA Inputs: Typical V_{hys} at 1.8 V is 0.18 V**
- **Latch-Up Performance Exceeds 200 mA Per JESD 78, Class II**
- **Very Small Package**
 - **WCSP (YFP): 2 mm \times 2 mm; 0.4 mm pitch**

APPLICATIONS

- **Smart Phones**
- **PDA's**
- **GPS Devices**
- **MP3 Players**
- **Digital Cameras**

DESCRIPTION/ORDERING INFORMATION

The TCA6418E is a 18 channel GPIO expansion device with integrated ESD protection. It can operate from 1.65 V to 3.6 V and has 18 general purpose inputs/outputs (GPIO) that can be used via the I²C interface [serial clock (SCL), serial data (SDA)].

The major benefit of this device is it frees up the processor from having to individually monitor changes in multiple inputs and also frees up the GPIOs on the processor to drive other outputs.. This provides power and bandwidth savings. The TCA6418E is also ideal for usage with processors that have limited GPIOs.

ORDERING INFORMATION⁽¹⁾

| T _A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|---------------|-----------------------|------------------|
| –40°C to 85°C | WCSP – YFP | Tape and reel | TCA6418EYFPR | AZ2 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

YFP PACKAGE

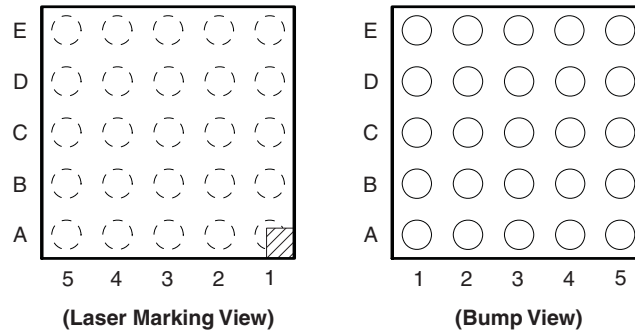


Table 1. YFP Package Terminal Assignments

| | | | | | |
|----------|---------------------------|----------|----------|----------|----------|
| E | $\overline{\text{INT}}$ | GND | GPIO13 | GPIO8 | GPIO4 |
| D | SCL | GPIO17 | GPIO12 | GPIO7 | GPIO3 |
| C | SDA | GPIO16 | GPIO11 | GPIO6 | GPIO2 |
| B | V_{CC} | GPIO15 | GPIO10 | GND | GPIO1 |
| A | $\overline{\text{RESET}}$ | GPIO14 | GPIO9 | GPIO5 | GPIO0 |
| | 5 | 4 | 3 | 2 | 1 |

TERMINAL FUNCTIONS

| TERMINAL | | TYPE | DESCRIPTION |
|---------------|---------------------------|------|---|
| NO. | NAME | | |
| WCSP (YFP) | | | |
| A1 | GPIO0 | I/O | GPIO port |
| B1 | GPIO1 | I/O | GPIO port |
| C1 | GPIO2 | I/O | GPIO port |
| D1 | GPIO3 | I/O | GPIO port |
| E1 | GPIO4 | I/O | GPIO port |
| A2 | GPIO5 | I/O | GPIO port |
| B2 | GND | - | Ground |
| C2 | GPIO6 | I/O | GPIO port |
| D2 | GPIO7 | I/O | GPIO port |
| E2 | GPIO8 | I/O | GPIO port |
| A3 | GPIO9 | I/O | GPIO port |
| B3 | GPIO10 | I/O | GPIO port |
| C3 | GPIO11 | I/O | GPIO port |
| D3 | GPIO12 | I/O | GPIO port |
| E3 | GPIO13 | I/O | GPIO port |
| A4 | GPIO14 | I/O | GPIO port |
| B4 | GPIO15 | I/O | GPIO port |
| C4 | GPIO16 | I/O | GPIO port |
| D4 | GPIO17 | I/O | GPIO port |
| E4 | GND | - | Ground |
| A5 | $\overline{\text{RESET}}$ | I | Active-low reset input. Connect to V_{CC} through a pullup resistor, if no active connection is used. |
| B5 | V_{CC} | Pwr | Supply voltage of 1.65 V to 3.6 V |
| C5 | SDA | I/O | Serial data bus. Connect to V_{CC} through a pullup resistor. |
| D5 | SCL | I | Serial clock bus. Connect to V_{CC} through a pullup resistor. |
| E5 | $\overline{\text{INT}}$ | O | Active-low interrupt output. Open drain structure. Connect to V_{CC} through a pullup resistor. |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|------------------|---|--------------------|---------------------------------------|-----|------|
| V _{CC} | Supply voltage range | | -0.5 | 4.6 | V |
| V _I | Input voltage range ⁽²⁾ | | -0.5 | 4.6 | V |
| V _O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | | -0.5 | 4.6 | V |
| | Output voltage range in the high or low state ⁽²⁾ | | -0.5 | 4.6 | |
| I _{IK} | Input clamp current | V _I < 0 | | ±20 | mA |
| I _{OK} | Output clamp current | V _O < 0 | | ±20 | mA |
| I _{OL} | Continuous output Low current | P port, SDA | V _O = 0 to V _{CC} | 50 | mA |
| | | INT | | 25 | |
| I _{OH} | Continuous output High current | P port | V _O = 0 to V _{CC} | 50 | |
| T _{stg} | Storage temperature range | | -65 | 150 | °C |

- (1) Stresses beyond those listed under [ABSOLUTE MAXIMUM RATINGS](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [RECOMMENDED OPERATING CONDITIONS](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| | | | VALUE | UNIT |
|-----------------|--|-------------|-------|------|
| θ _{JA} | Package thermal impedance ⁽¹⁾ | YFP package | 98.8 | °C/W |

- (1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

| | | | MIN | MAX | UNIT |
|-----------------|--------------------------------|---------------------------|-----------------------|-----------------------|------|
| V _{CC} | Supply voltage | | 1.65 | 3.6 | V |
| V _{IH} | High-level input voltage | SCL, SDA, GPIO0-17, RESET | 0.7 × V _{CC} | 3.6 | V |
| V _{IL} | Low-level input voltage | SCL, SDA, GPIO0-17, RESET | -0.5 | 0.3 × V _{CC} | V |
| I _{OH} | High-level output current | GPIO0-17 | | 10 | mA |
| I _{OL} | Low-level output current | GPIO0-17 | | 25 | mA |
| T _A | Operating free-air temperature | | -40 | 85 | °C |

ELECTRICAL CHARACTERISTICS

 over recommended operating free-air temperature range, $V_{CC} = 1.65\text{ V to }3.6\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CCP} | MIN | TYP | MAX | UNIT |
|-----------|---|--|-----------------|----------------------------|-----|------|---------------|
| V_{IK} | Input diode clamp voltage | $I_I = -18\text{ mA}$ | 1.65 V to 3.6 V | -1.2 | | | V |
| V_{POR} | Power-on reset voltage | $V_I = V_{CCP}$ or GND, $I_O = 0$ | 1.65 V to 3.6 V | | 1 | 1.4 | V |
| V_{OH} | GPIO0-17 high-level output voltage | $I_{OH} = -1\text{ mA}$ | 1.65 V | 1.25 | | | V |
| | | $I_{OH} = -8\text{ mA}$ | 1.65 V | 1.2 | | | |
| | | | 2.3 V | 1.8 | | | |
| | | $I_{OH} = -10\text{ mA}$ | 3 V | 2.6 | | | |
| | | | 1.65 V | 1.1 | | | |
| | | | 2.3 V | 1.7 | | | |
| V_{OL} | GPIO0-17 low-level output voltage | $I_{OL} = 1\text{ mA}$ | 1.65 V | | | 0.4 | V |
| | | $I_{OL} = 8\text{ mA}$ | 1.65 V | | | 0.45 | |
| | | | 2.3 V | | | 0.25 | |
| | | $I_{OL} = 10\text{ mA}$ | 3 V | | | 0.25 | |
| | | | 1.65 V | | | 0.6 | |
| | | | 2.3 V | | | 0.3 | |
| I_{OL} | SDA | $V_{OL} = 0.4\text{ V}$ | 1.65 V to 3.6 V | 3 | | | mA |
| | $\overline{\text{INT}}$ | $V_{OL} = 0.4\text{ V}$ | 1.65 V to 3.6 V | 3 | | | |
| I_I | SCL, SDA, GPIO0-17, $\overline{\text{RESET}}$ | $V_I = V_{CC1}$ or GND; Pull-downs disabled for GPIO0-17 | 1.65 V to 3.6 V | | | 1 | μA |
| r_{INT} | GPIO0-17 | | | | 55 | | k Ω |
| I_{CC} | | V_I on SDA, GPIO0-17, = V_{CC} or GND, $I_O = 0$, I/O = inputs, | 1.65 V to 3.6 V | $f_{SCL} = 0\text{ kHz}$ | | 13 | μA |
| | | | | $f_{SCL} = 400\text{ kHz}$ | | 25 | |
| | | | | $f_{SCL} = 1\text{ MHz}$ | | 35 | |
| C_1 | SCL | $V_I = V_{CC1}$ or GND | 1.65 V to 3.6 V | | 6 | 8 | pF |
| C_{io} | SDA | $V_{IO} = V_{CC}$ or GND | 1.65 V to 3.6 V | | 10 | 12.5 | pF |
| | GPIO0-17 | | | | 5 | 6 | |

I²C INTERFACE TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 12](#))

| | STANDARD MODE I ² C BUS | | FAST MODE I ² C BUS | | FAST MODE PLUS (FM+) I ² C BUS | | UNIT |
|--|---------------------------------------|------|-----------------------------------|-----|--|------|------|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| f_{scl} I ² C clock frequency | 0 | 100 | 0 | 400 | 0 | 1000 | kHz |
| t_{sch} I ² C clock high time | 4 | | 0.6 | | 0.26 | | μs |
| t_{scl} I ² C clock low time | 4.7 | | 1.3 | | 0.5 | | μs |
| t_{sp} I ² C spike time | | 50 | | 50 | | 50 | ns |
| t_{sds} I ² C serial data setup time | 250 | | 100 | | 50 | | ns |
| t_{sdh} I ² C serial data hold time | 0 | | 0 | | 0 | | ns |
| t_{icr} I ² C input rise time | | 1000 | $20 + 0.1C_b^{(1)}$ | 300 | | 120 | ns |
| t_{icf} I ² C input fall time | | 300 | $20 + 0.1C_b^{(1)}$ | 300 | | 120 | ns |
| t_{ocf} I ² C output fall time; 10 pF to 400 pF bus | | 300 | $20 + 0.1C_b^{(1)}$ | 300 | | 120 | μs |
| t_{buf} I ² C bus free time between Stop and Start | 4.7 | | 1.3 | | 0.5 | | μs |
| t_{sts} I ² C Start or repeater Start condition setup time | 4.7 | | 0.6 | | 0.26 | | μs |
| t_{sth} I ² C Start or repeater Start condition hold time | 4 | | 0.6 | | 0.26 | | μs |
| t_{sps} I ² C Stop condition setup time | 4 | | 0.6 | | 0.26 | | μs |
| $t_{vd(data)}$ Valid data time; SCL low to SDA output valid | | 1 | | 0.9 | | 0.45 | μs |
| $t_{vd(ack)}$ Valid data time of ACK condition; ACK signal from SCL low to SDA (out) low | | 1 | | 0.9 | | 0.45 | μs |

(1) C_b = total capacitance of one bus line in pF

RESET TIMING REQUIREMENTS

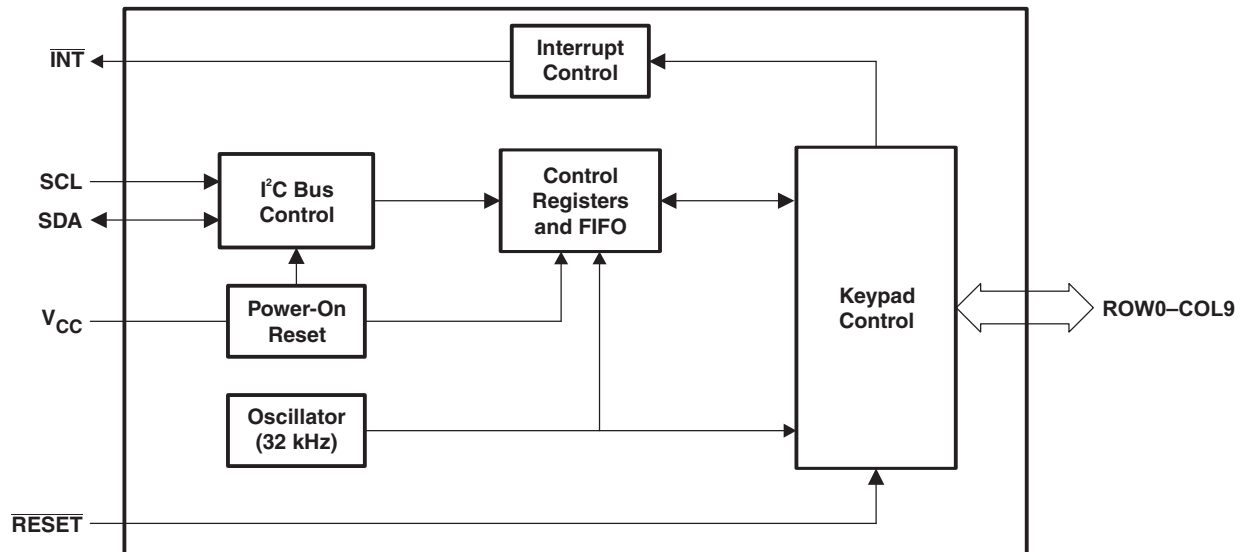
over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 15](#))

| | STANDARD MODE, FAST MODE, FAST MODE PLUS (FM+) I ² C BUS | | UNIT |
|-------------------------------|--|-----|------|
| | MIN | MAX | |
| t_W Reset pulse duration | 120 ⁽¹⁾ | | μs |
| t_{REC} Reset recovery time | 120 ⁽¹⁾ | | μs |
| t_{RESET} Time to reset | 120 ⁽¹⁾ | | μs |

(1) The GPIO debounce circuit uses each GPIO input which passes through a two-stage register circuit. Both registers are clocked by the same clock signal, presumably free-running, with a nominal period of 50μs. When an input changes state, the new state is clocked into the first stage on one clock transition. On the next same-direction transition, if the input state is still the same as the previously clocked state, the signal is clocked into the second stage, and then on to the remaining circuits. Since the inputs are asynchronous to the clock, it will take anywhere from zero to 50 μsec after the input transition to clock the signal into the first stage. Therefore, the total debounce time may be as long as 100 μsec. Finally, to account for a slow clock, the spec further guard-banded at 120 μsec.

SWITCHING CHARACTERISTICS

| PARAMETER | | FROM | TO | STANDARD MODE, FAST MODE, FAST MODE PLUS (FM+) I ² C BUS | | UNIT |
|-----------------|----------------------------|----------|-------------------------|---|-----|------|
| | | | | MIN | MAX | |
| t _{IV} | Interrupt valid time | GPIO0-17 | $\overline{\text{INT}}$ | 40 | 120 | μs |
| | | | | 0 | 1 | |
| t _{IR} | Interrupt reset delay time | SCL | $\overline{\text{INT}}$ | | 1 | μs |
| t _{PV} | Output data valid | SCL | GPIO0-17 | | 400 | ns |
| t _{PS} | Input data setup time | GPIO | SCL | 0 | | ns |
| t _{PH} | Input data hold time | | | | | |
| | | GPIO | SCL | 300 | | ns |

LOGIC DIAGRAM (POSITIVE LOGIC)


At power on, the GPIOs are configured as inputs with internal 50-kΩ pulldown resistors enabled; however, the system master can enable the GPIOs to function as inputs or outputs.

The system master can reset the TCA6418E in the event of a timeout or other improper operation by asserting a low in the $\overline{\text{RESET}}$ input, while keeping the V_{CC} at its operating level.

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_{W} . The TCA6418E registers and I²C/SMBus state machine are changed to their default state once $\overline{\text{RESET}}$ is low (0). When $\overline{\text{RESET}}$ is high (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pullup resistor to V_{CC} , if no active connection is used.

The power-on reset puts the registers in their default state and initializes the I²C/SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without de-powering the part.

The open-drain interrupt ($\overline{\text{INT}}$) output is used to indicate to the system master that an input state has changed. $\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote input can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C bus. Thus, the TCA6418E can remain a simple slave device.

Power-On Reset

When power (from 0 V) is applied to V_{CC} , an internal power-on reset holds the TCA6418E in a reset condition until V_{CC} reaches V_{POR} . At that time, the reset condition is released, and the TCA6418E registers and I²C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered below 0.2 V and back up to the operating voltage for a power-reset cycle.

Power-On Reset Requirements

In the event of a glitch or data corruption, TCA6418E can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Figure 1](#) and [Figure 2](#).

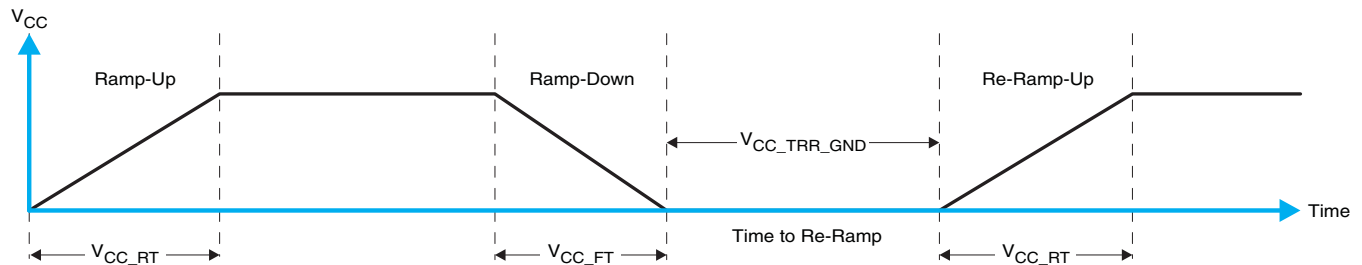


Figure 1. V_{CC} is Lowered Below 0.2 V or 0 V and Then Ramped Up to V_{CC}

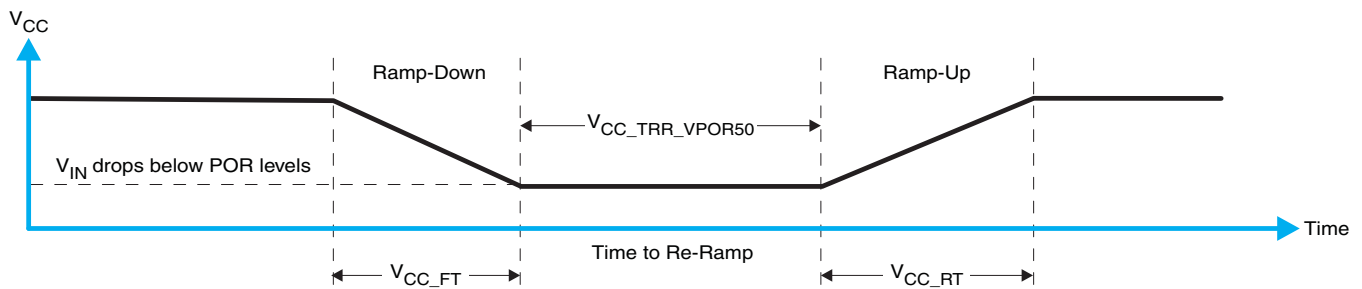


Figure 2. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

[Table 2](#) specifies the performance of the power-on reset feature for TCA6418E for both types of power-on reset.

Table 2. RECOMMENDED SUPPLY SEQUENCING AND RAMP RATES⁽¹⁾

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|----------------------|---|------------------------------|-------|-----|-------|---------|
| V_{CC_FT} | Fall rate | See Figure 1 | 1 | 100 | | ms |
| V_{CC_RT} | Rise rate | See Figure 1 | 0.01 | 100 | | ms |
| $V_{CC_TRR_GND}$ | Time to re-ramp (when V_{CC} drops to GND) | See Figure 1 | 0.001 | | | ms |
| $V_{CC_TRR_POR50}$ | Time to re-ramp (when V_{CC} drops to $V_{POR_MIN} - 50$ mV) | See Figure 2 | 0.001 | | | ms |
| V_{CC_GH} | Level that V_{CCP} can glitch down to, but not cause a functional disruption when $V_{CCX_GW} = 1$ μ s | See Figure 3 | | | 1.2 | V |
| V_{CC_GW} | Glitch width that will not cause a functional disruption when $V_{CCX_GH} = 0.5 \times V_{CCx}$ | See Figure 3 | | | | μ s |
| V_{PORF} | Voltage trip point of POR on falling V_{CC} | | 0.767 | | 1.144 | V |
| V_{PORR} | Voltage trip point of POR on rising V_{CC} | | 1.033 | | 1.428 | V |

(1) $T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 3 and Table 2 provide more information on how to measure these specifications.

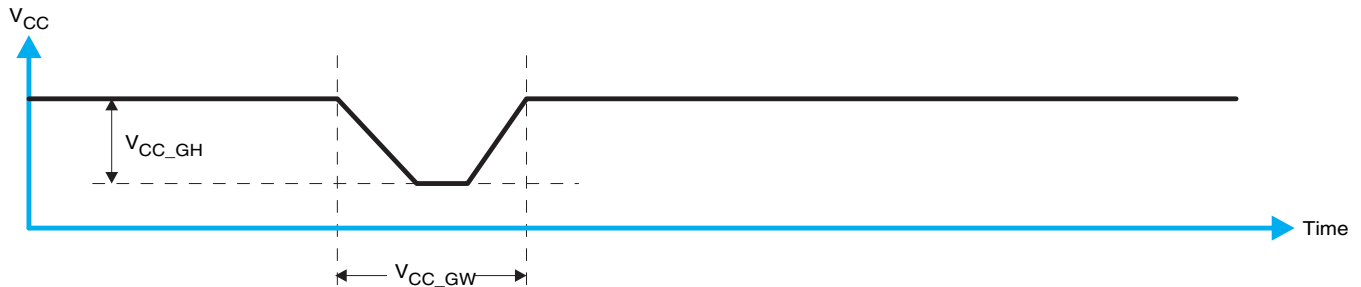


Figure 3. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 4 and Table 2 provide more details on this specification.

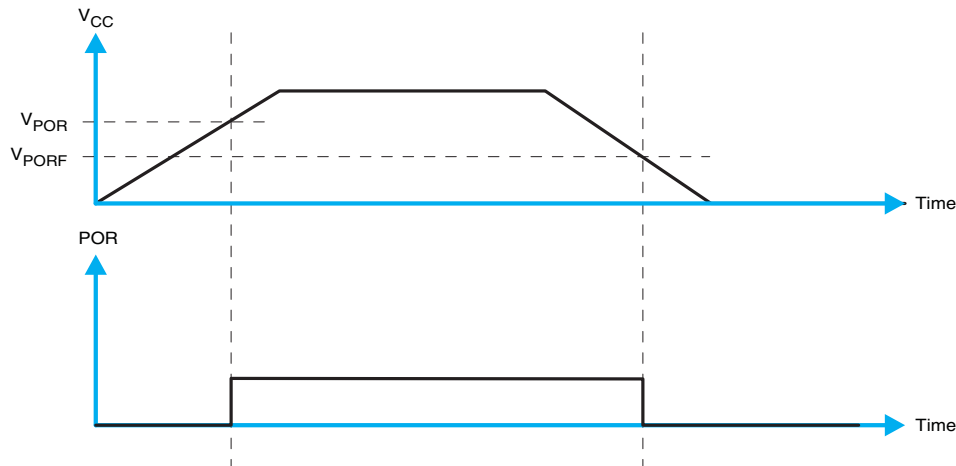


Figure 4. V_{POR}

For proper operation of the power-on reset feature, use as directed in the figures and table above.

Interrupt Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} , the signal \overline{INT} is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as \overline{INT} .

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the input port register.

The \overline{INT} output has an open-drain structure and requires a pullup resistor to V_{CC} depending on the application. For more information on the interrupt output feature, see [Control Register and Command Byte](#) and [Typical Applications](#).

I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high (see [Figure 5](#)). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address (ADDR) input of the slave device must not be changed between the Start and the Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see [Figure 6](#)).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see [Figure 5](#)).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see [Figure 7](#)). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

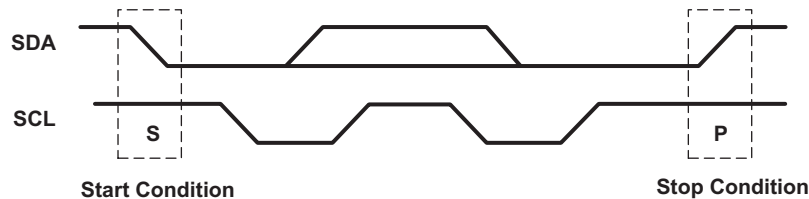


Figure 5. Definition of Start and Stop Conditions

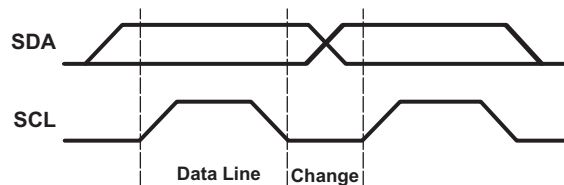


Figure 6. Bit Transfer

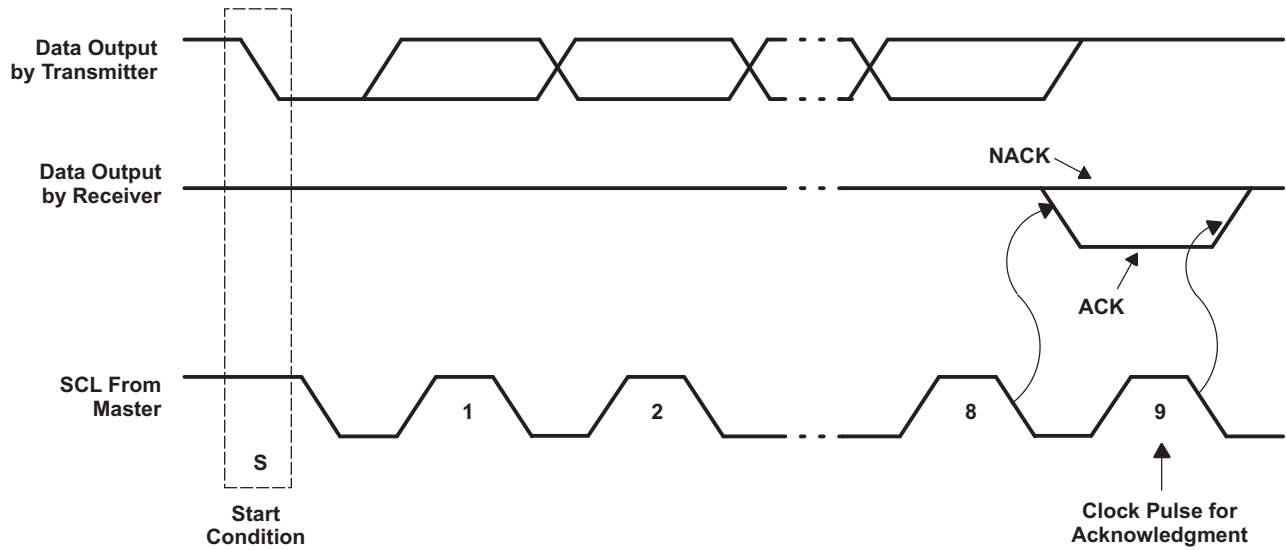


Figure 7. Acknowledgment on the I²C Bus

Device Address

The address of the TCA6418E is shown in [Table 3](#).

Table 3.

| BYTE | BIT | | | | | | | |
|--------------------------------|---------|---|---|---|---|---|---|---------|
| | 7 (MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) |
| I ² C slave address | 0 | 1 | 1 | 0 | 1 | 0 | 0 | R/W |

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte, which is stored in the control register in the TCA6418E. The command byte indicates the register that will be updated with information. All registers can be read and written to by the system master.

Table 4 shows all the registers within this device and their descriptions. The default value in all registers is 0.

Table 4. Register Descriptions

| ADDRESS | REGISTER NAME | REGISTER DESCRIPTION | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---------------------------|-------------|-------------|-------------|-------------|-------------|-----------------|-------------|-------------|
| 0x00 | Reserved | Reserved | | | | | | | | |
| 0x01 | Reserved | Reserved | | | | | | | | |
| 0x02 | INT_STAT | Interrupt status register | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | GPI_IN T | N/A 0 |
| 0x03 | Reserved | Reserved | | | | | | | | |
| 0x04 | Reserved | Reserved | | | | | | | | |
| 0x05 | Reserved | Reserved | | | | | | | | |
| 0x06 | Reserved | Reserved | | | | | | | | |
| 0x07 | Reserved | Reserved | | | | | | | | |
| 0x08 | Reserved | Reserved | | | | | | | | |
| 0x09 | Reserved | Reserved | | | | | | | | |
| 0x0A | Reserved | Reserved | | | | | | | | |
| 0x0B | Reserved | Reserved | | | | | | | | |
| 0x0C | Reserved | Reserved | | | | | | | | |
| 0x0D | Reserved | Reserved | | | | | | | | |
| 0x0E | Reserved | Reserved | | | | | | | | |
| 0x0F | Reserved | Reserved | | | | | | | | |
| 0x10 | Reserved | Reserved | | | | | | | | |
| 0x11 | GPIO_INT_STAT1 | GPIO interrupt status | GPIO0 0 | GPIO1 0 | GPIO2 0 | GPIO3 0 | GPIO4 0 | GPIO 5 0 | GPIO6 0 | GPIO7 0 |
| 0x12 | GPIO_INT_STAT2 | GPIO interrupt status | GPIO15 0 | GPIO14 0 | GPIO13 0 | GPIO12 0 | GPIO11 0 | GPIO 10 0 | GPIO9 0 | GPIO8 0 |
| 0x13 | GPIO_INT_STAT3 | GPIO interrupt status | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | GPIO17 0 | GPIO16 0 |
| 0x14 | GPIO_DAT_STAT1 (read twice to clear) | GPIO data status | GPIO0 0 | GPIO1 0 | GPIO2 0 | GPIO3 0 | GPIO4 0 | GPIO 5 0 | GPIO6 0 | GPIO7 0 |
| 0x15 | GPIO_DAT_STAT2 (read twice to clear) | GPIO data status | GPIO15 0 | GPIO14 0 | GPIO13 0 | GPIO12 0 | GPIO11 0 | GPIO 10 0 | GPIO9 0 | GPIO8 0 |
| 0x16 | GPIO_DAT_STAT3 (read twice to clear) | GPIO data status | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | GPIO17 0 | GPIO16 0 |
| 0x17 | GPIO_DAT_OUT1 | GPIO data out | GPIO0 0 | GPIO1 0 | GPIO2 0 | GPIO3 0 | GPIO4 0 | GPIO 5 0 | GPIO6 0 | GPIO7 0 |
| 0x18 | GPIO_DAT_OUT2 | GPIO data out | GPIO15 0 | GPIO14 0 | GPIO13 0 | GPIO12 0 | GPIO11 0 | GPIO 10 0 | GPIO9 0 | GPIO8 0 |
| 0x19 | GPIO_DAT_OUT3 | GPIO data out | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | GPIO17 0 | GPIO16 0 |
| 0x1A | GPIO_INT_EN1 | GPIO interrupt enable | GPIO0 0 | GPIO1 0 | GPIO2 0 | GPIO3 0 | GPIO4 0 | GPIO 5 0 | GPIO6 0 | GPIO7 0 |

Table 4. Register Descriptions (continued)

| ADDRESS | REGISTER NAME | REGISTER DESCRIPTION | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------------|--|-------------|-------------|-------------|-------------|-------------|-----------------|-------------|-------------|
| 0x1B | GPIO_INT_EN2 | GPIO interrupt enable | GPIO15 0 | GPIO14 0 | GPIO13 0 | GPIO12 0 | GPIO11 0 | GPIO 10 0 | GPIO9 0 | GPIO8 0 |
| 0x1C | GPIO_INT_EN3 | GPIO interrupt enable | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | GPIO17 0 | GPIO16 0 |
| 0x1D | Reserved | Reserved | | | | | | | | |
| 0x1E | Reserved | Reserved | | | | | | | | |
| 0x1F | Reserved | Reserved | | | | | | | | |
| 0x20 | Reserved | Reserved | | | | | | | | |
| 0x21 | Reserved | Reserved | | | | | | | | |
| 0x22 | Reserved | Reserved | | | | | | | | |
| 0x23 | GPIO_DIR1 | GPIO data direction 0: input 1: output | GPIO0 0 | GPIO1 0 | GPIO2 0 | GPIO3 0 | GPIO4 0 | GPIO 5 0 | GPIO6 0 | GPIO7 0 |
| 0x24 | GPIO_DIR2 | GPIO data direction 0: input 1: output | GPIO15 0 | GPIO14 0 | GPIO13 0 | GPIO12 0 | GPIO11 0 | GPIO 10 0 | GPIO9 0 | GPIO8 0 |
| 0x25 | GPIO_DIR3 | GPIO data direction 0: input 1: output | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | GPIO17 0 | GPIO16 0 |
| 0x26 | GPIO_INT_LVL 1 | GPIO edge/level detect 0: low 1: high | GPIO0 0 | GPIO1 0 | GPIO2 0 | GPIO3 0 | GPIO4 0 | GPIO 5 0 | GPIO6 0 | GPIO7 0 |
| 0x27 | GPIO_INT_LVL 2 | GPIO edge/level detect 0: low 1: high | GPIO15 0 | GPIO14 0 | GPIO13 0 | GPIO12 0 | GPIO11 0 | GPIO 10 0 | GPIO9 0 | GPIO8 0 |
| 0x28 | GPIO_INT_LVL 3 | GPIO edge/level detect 0: low 1: high | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | GPIO17 0 | GPIO16 0 |
| 0x29 | DEBOUNCE_DIS 1 | Debounce disable 0: enabled 1: disabled | GPIO0 0 | GPIO1 0 | GPIO2 0 | GPIO3 0 | GPIO4 0 | GPIO 5 0 | GPIO6 0 | GPIO7 0 |
| 0x2A | DEBOUNCE_DIS 2 | Debounce disable 0: enabled 1: disabled | GPIO15 0 | GPIO14 0 | GPIO13 0 | GPIO12 0 | GPIO11 0 | GPIO 10 0 | GPIO9 0 | GPIO8 0 |
| 0x2B | DEBOUNCE_DIS 3 | Debounce disable 0: enabled 1: disabled | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | GPIO17 0 | GPIO16 0 |
| 0x2C | GPIO_PULL1 | GPIO pulldown 0: pulldown enabled 1: pulldown disabled | GPIO0 0 | GPIO1 0 | GPIO2 0 | GPIO3 0 | GPIO4 0 | GPIO 5 0 | GPIO6 0 | GPIO7 0 |
| 0x2D | GPIO_PULL2 | GPIO pulldown 0: pulldown enabled 1: pulldown disabled | GPIO15 0 | GPIO14 0 | GPIO13 0 | GPIO12 0 | GPIO11 0 | GPIO 10 0 | GPIO9 0 | GPIO8 0 |
| 0x2E | GPIO_PULL3 | GPIO pulldown 0: pulldown enabled 1: pulldown disabled | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | N/A 0 | GPIO17 0 | GPIO16 0 |
| 0x2F | Reserved | | | | | | | | | |

Interrupt Status Register, INT_STAT (Address 0x02)

GPI_INT (BIT1) reflects the status of the $\overline{\text{INT}}$ pin. If GPI_INT is 1, $\overline{\text{INT}}$ is asserted. Write 0x02 to INT_STAT register to clear interrupt.

GPIO Interrupt Status Registers, GPIO_INT_STAT1–3 (Address 0x11–0x13)

These registers are used to check GPIO interrupt status and are cleared on read.

GPIO Data Status Registers, GPIO_DAT_STAT1–3 (Address 0x14–0x16)

These registers show GPIO state when read for inputs and outputs.

GPIO Data Out Registers, GPIO_DAT_OUT1–3 (Address 0x17–0x19)

These registers contain GPIO data to be written to GPIO out driver; inputs are not affected. This is needed so that the value can be written prior to being set as an output.

GPIO Interrupt Enable Registers, GPIO_INT_EN1–3 (Address 0x1A–0x1C)

These registers enable interrupts for GP inputs only.

GPIO Data Direction Registers, GPIO_DIR1–3 (Address 0x23–0x25)

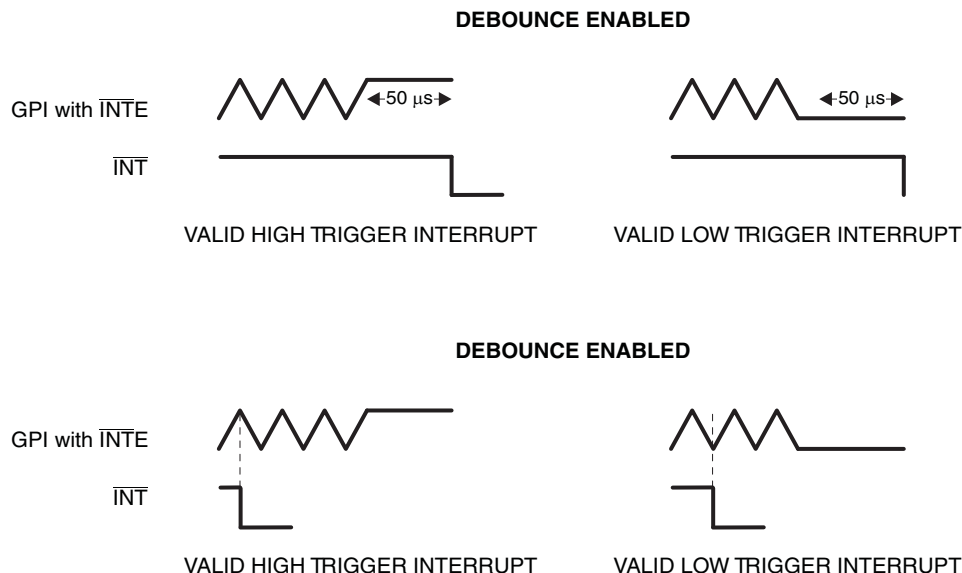
A bit value of '0' in any of the unreserved bits sets the corresponding pin as an input. A '1' in any of these bits sets the pin as an output.

GPIO Edge/Level Detect Registers, GPIO_INT_LVL1–3 (Address 0x26–0x28)

A bit value of '0' indicates that interrupt will be triggered on a high-to-low transition for the inputs in GPIO mode. A bit value of '1' indicates that interrupt will be triggered on a low-to-high value for the inputs in GPIO mode.

Debounce Disable Registers, DEBOUNCE_DIS1–3 (Address 0x29–0x2B)

This is for pins configured as inputs. A bit value of '0' in any of the unreserved bits enables the debounce while a bit value of '1' disables the debounce.



The reset line always has a 50- μ s debounce time.

The 50 μ s debounce time for inputs is the time required for the input to be stable to be noticed.

GPIO Pull Disable Register, GPIO_PULL1–3 (Address 0x2C–0x2E)

This register enables or disables pulldown registers from inputs.

Bus Transactions

Data is exchanged between the master and TCA6418E through write and read commands.

Writes

Data is transmitted to the TCA6418E by sending the device address and setting the least significant bit (LSB) to a logic 0. The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.

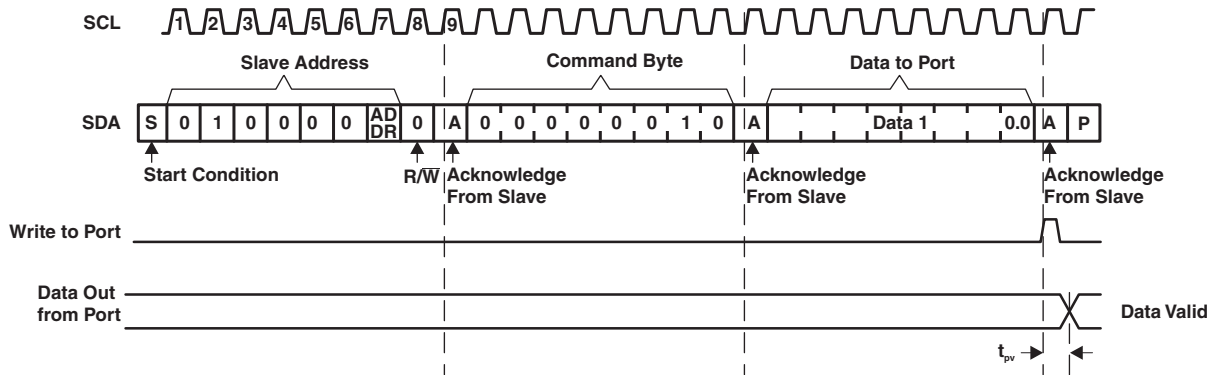


Figure 8. Write to Output Port Register

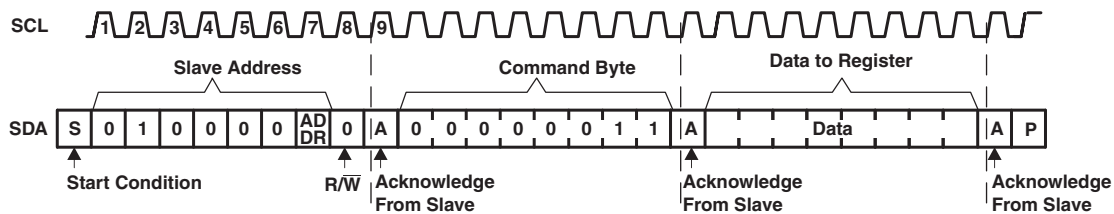


Figure 9. Write to Configuration or Polarity Inversion Register

Reads

The bus master first must send the TCA6418E address with the LSB set to a logic 0. The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the TCA6418E (see Figure 10 and Figure 11). Data is clocked into the register on the rising edge of the ACK clock pulse.

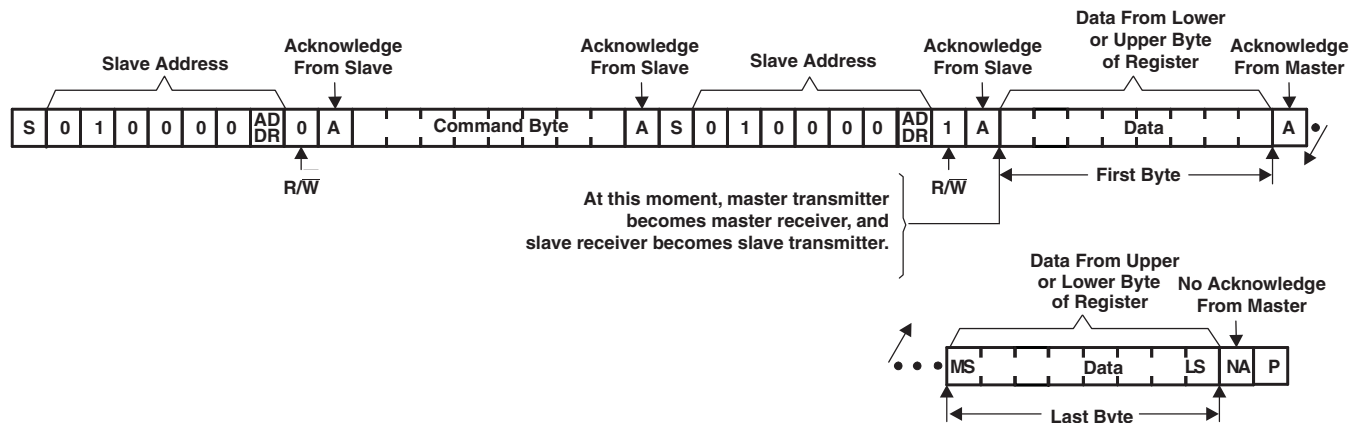


Figure 10. Read From Register

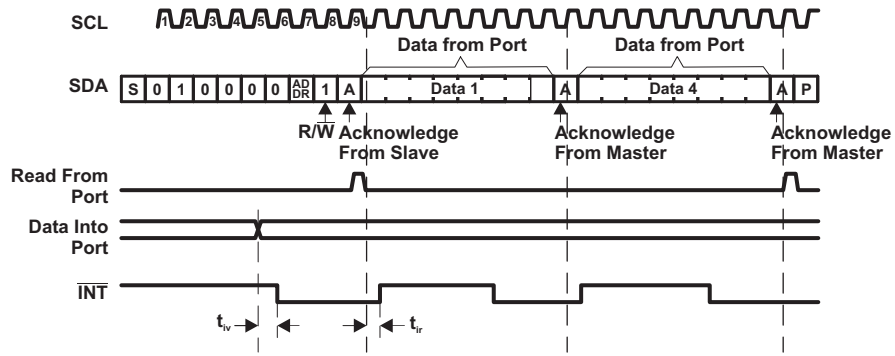
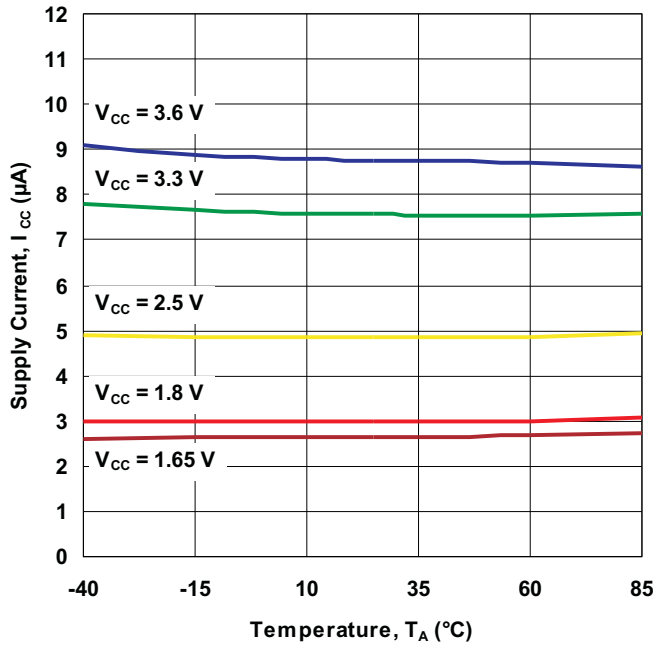


Figure 11. Read From Input Port Register

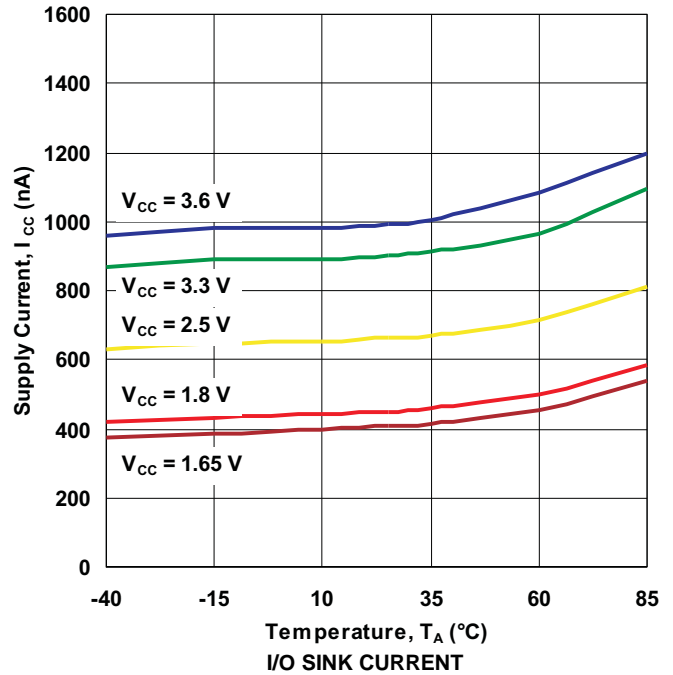
TYPICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

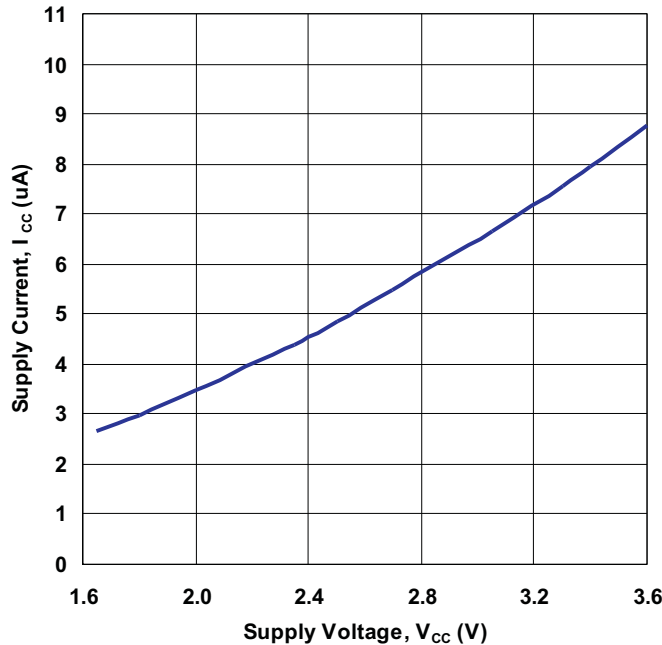
SUPPLY CURRENT
vs
TEMPERATURE



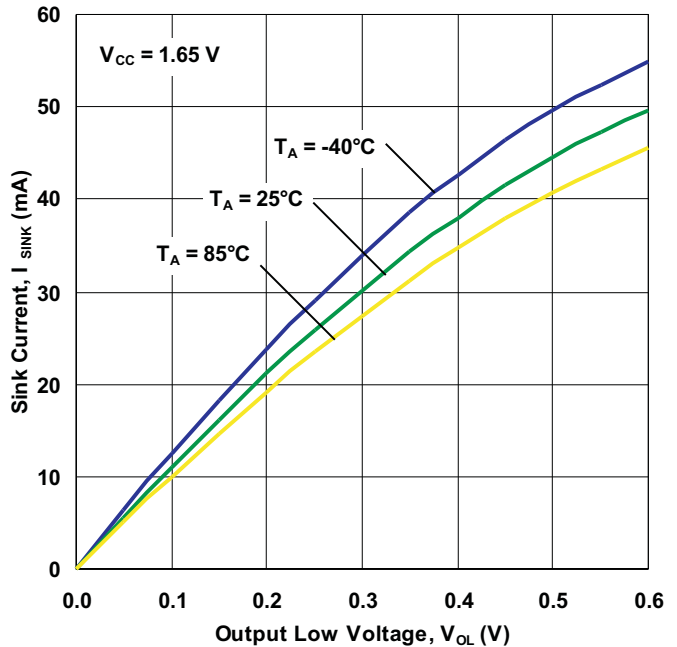
STANDBY SUPPLY CURRENT
vs
TEMPERATURE



SUPPLY CURRENT
vs
SUPPLY VOLTAGE

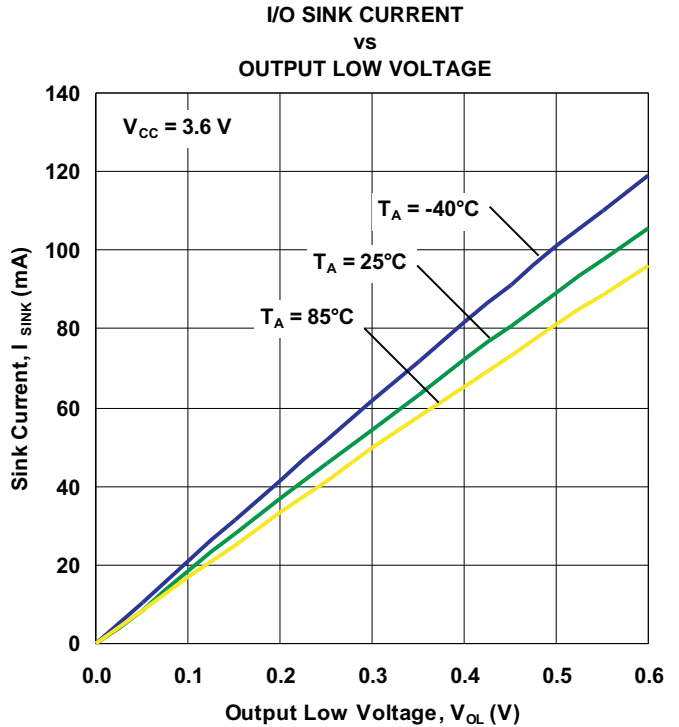
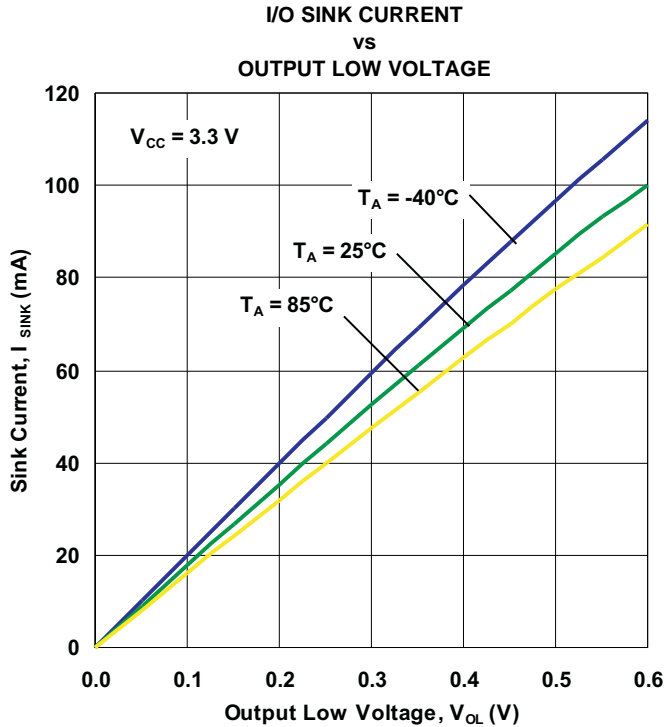
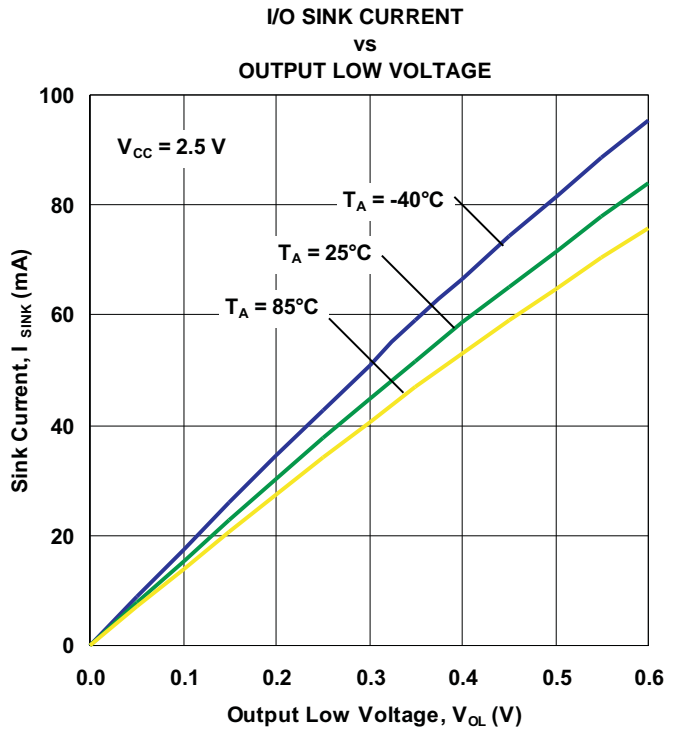
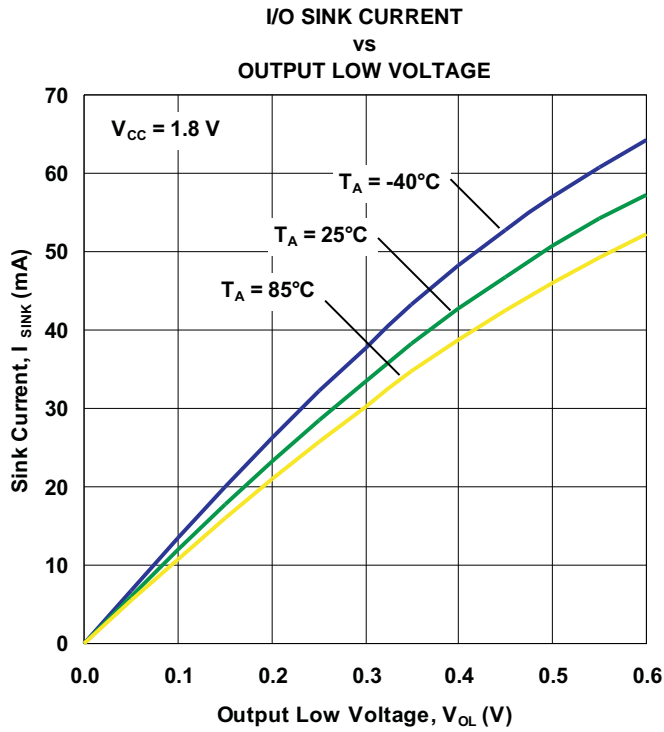


OUTPUT LOW VOLTAGE



TYPICAL CHARACTERISTICS (continued)

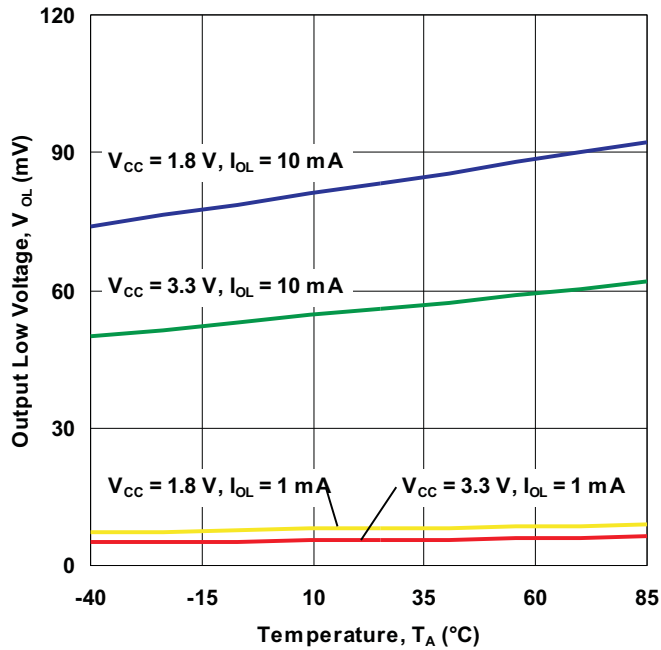
$T_A = 25^\circ\text{C}$ (unless otherwise noted)



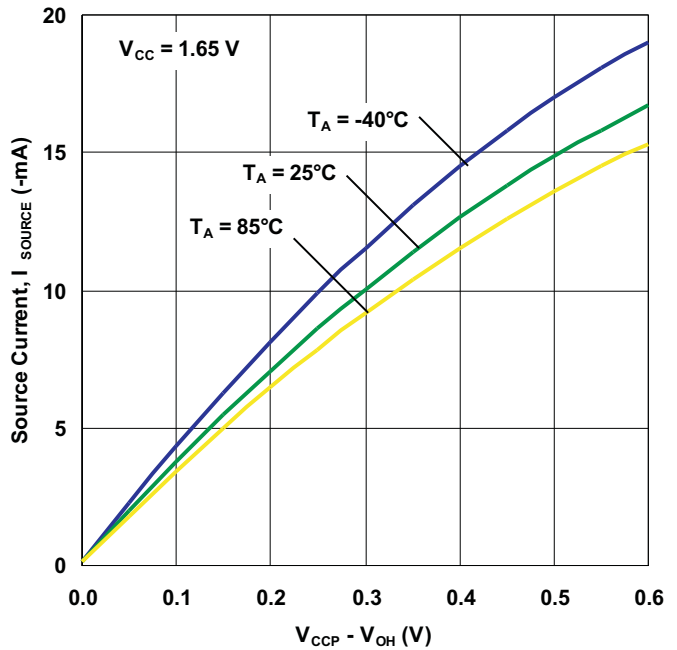
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C (unless otherwise noted)

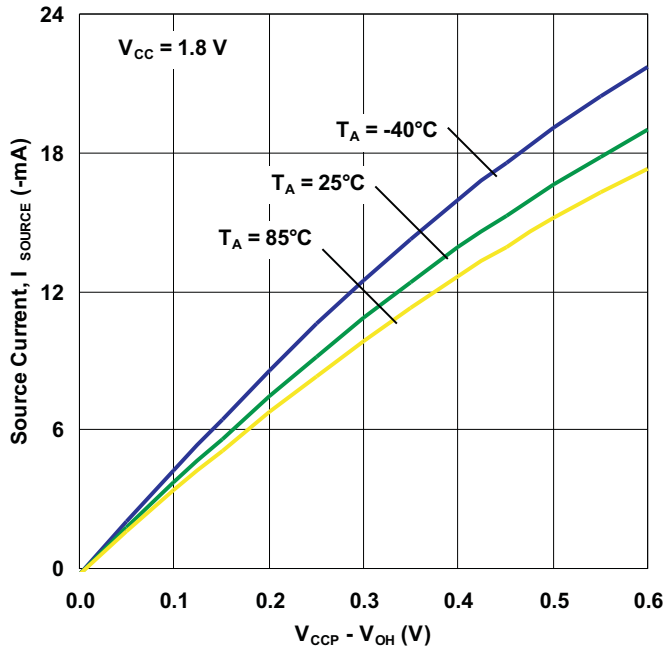
I/O LOW VOLTAGE
vs
TEMPERATURE



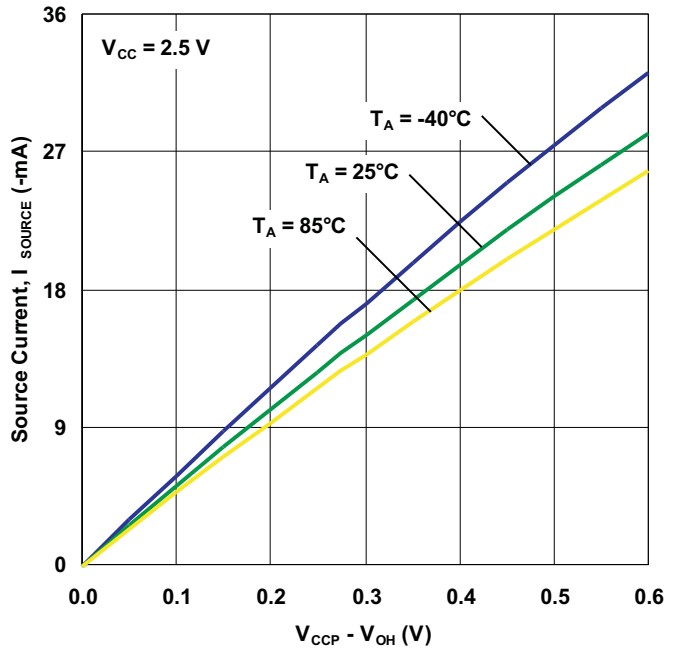
I/O SOURCE CURRENT
vs
OUTPUT HIGH VOLTAGE



I/O SOURCE CURRENT
vs
OUTPUT HIGH VOLTAGE



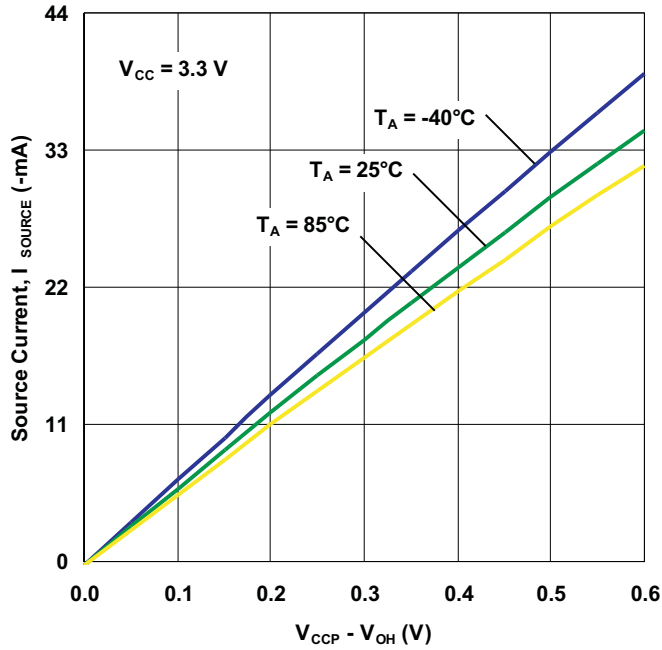
I/O SOURCE CURRENT
vs
OUTPUT HIGH VOLTAGE



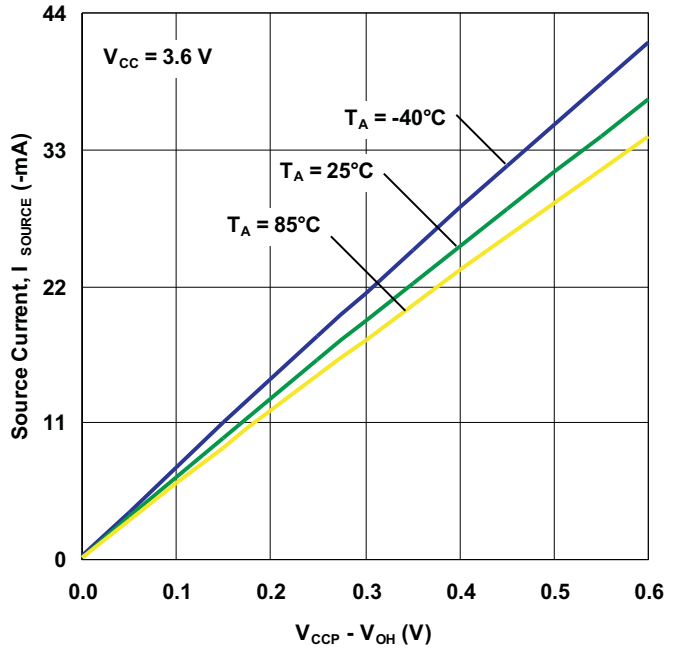
TYPICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

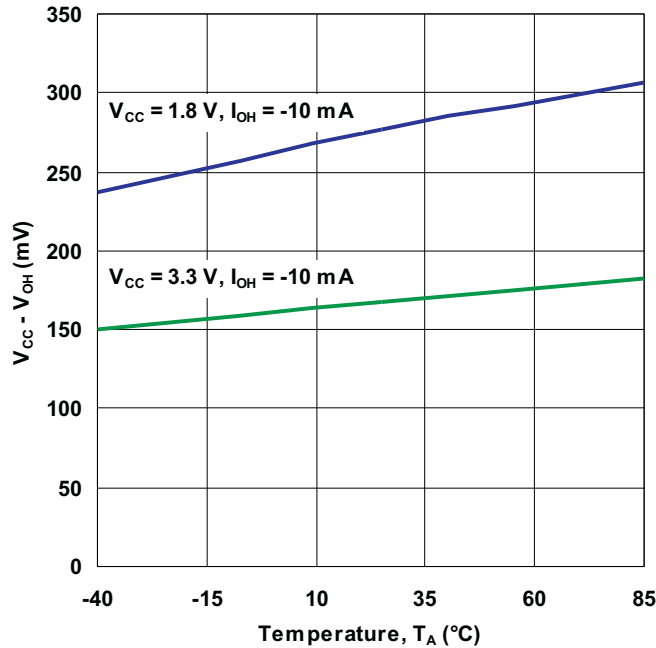
**I/O SOURCE CURRENT
vs
OUTPUT HIGH VOLTAGE**



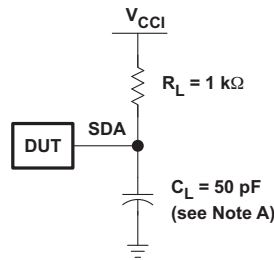
**I/O SOURCE CURRENT
vs
OUTPUT HIGH VOLTAGE**



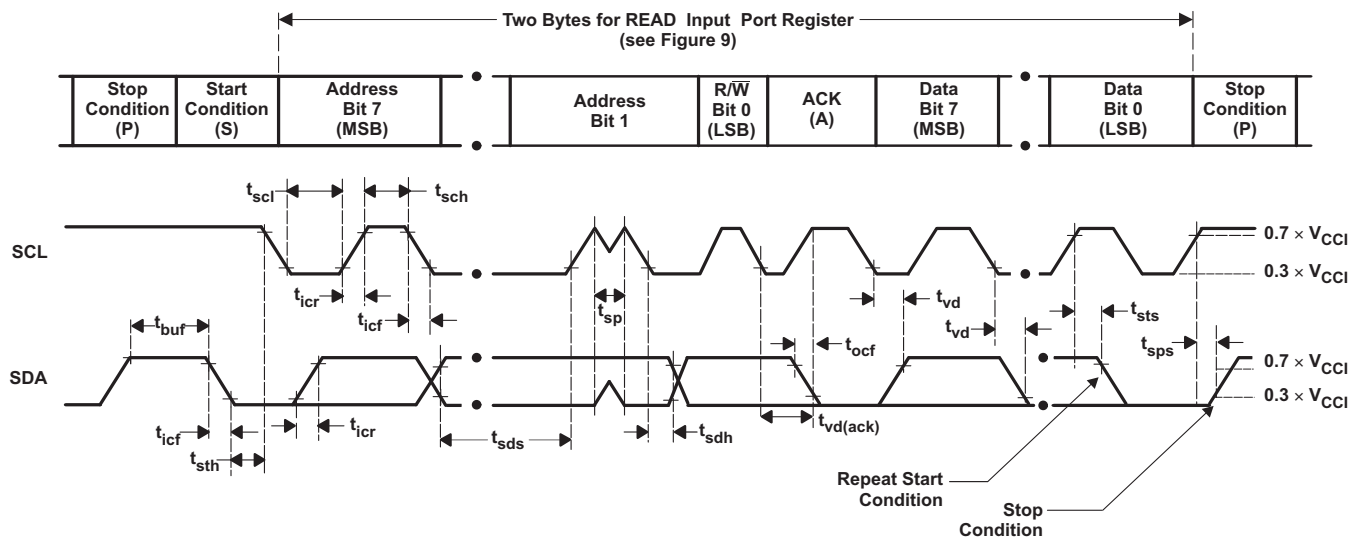
**I/O HIGH VOLTAGE
vs
TEMPERATURE**



PARAMETER MEASUREMENT INFORMATION



SDA LOAD CONFIGURATION



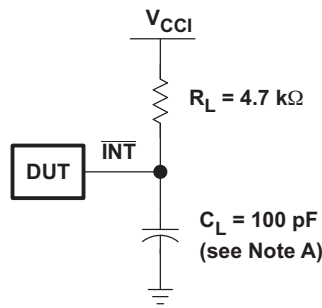
VOLTAGE WAVEFORMS

| BYTE | DESCRIPTION |
|------|--------------------------|
| 1 | I ² C address |
| 2 | Input register port data |

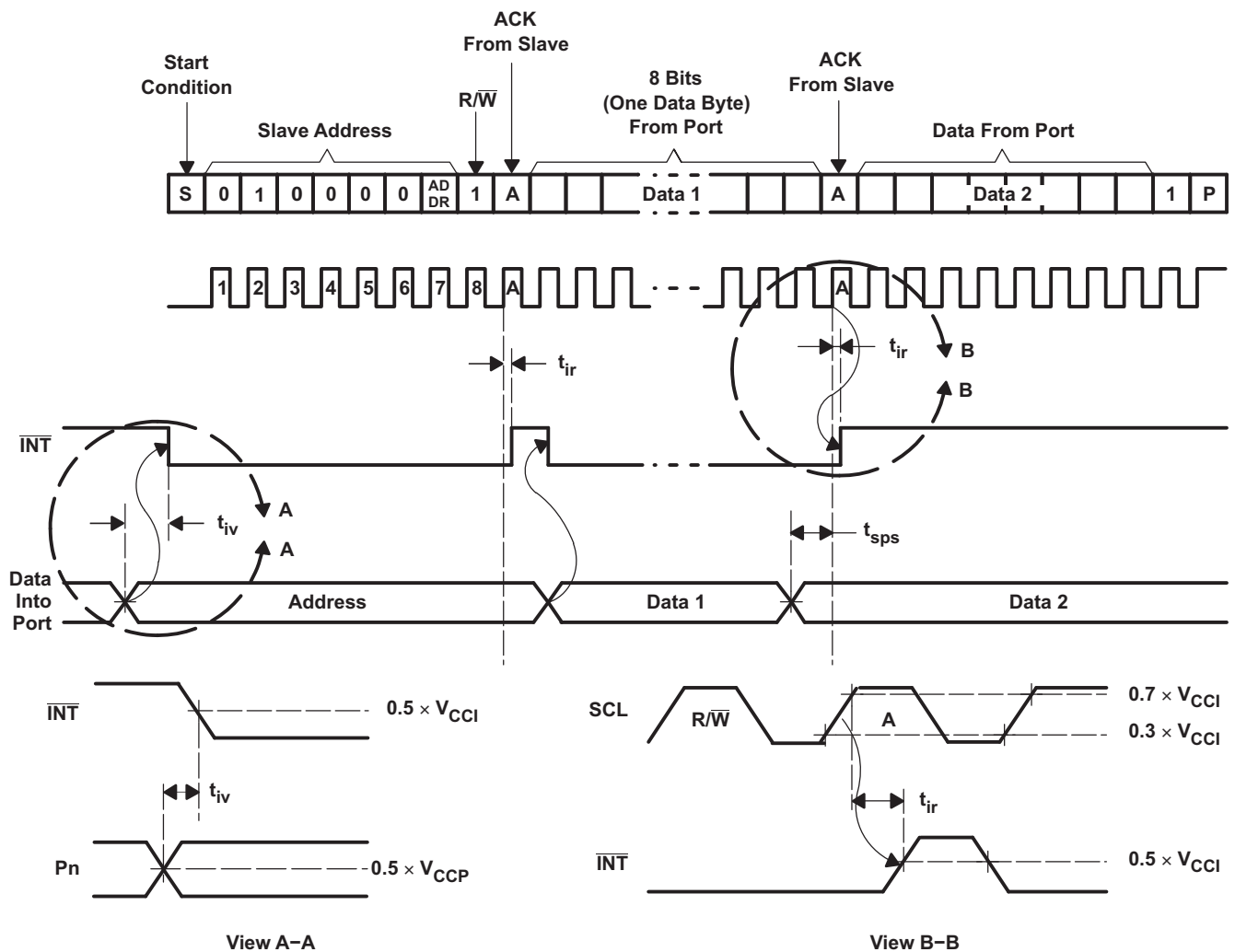
- A. C_L includes probe and jig capacitance. t_{ocf} is measured with C_L of 10 pF or 400 pF.
- B. All inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r/t_f \leq 30$ ns.
- C. All parameters and waveforms are not applicable to all devices.

Figure 12. I²C Interface Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



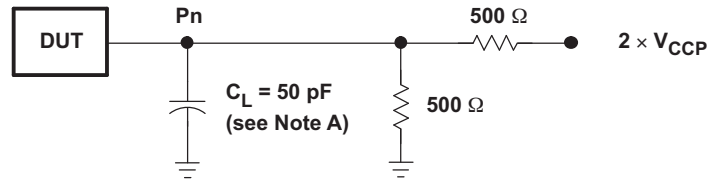
INTERRUPT LOAD CONFIGURATION



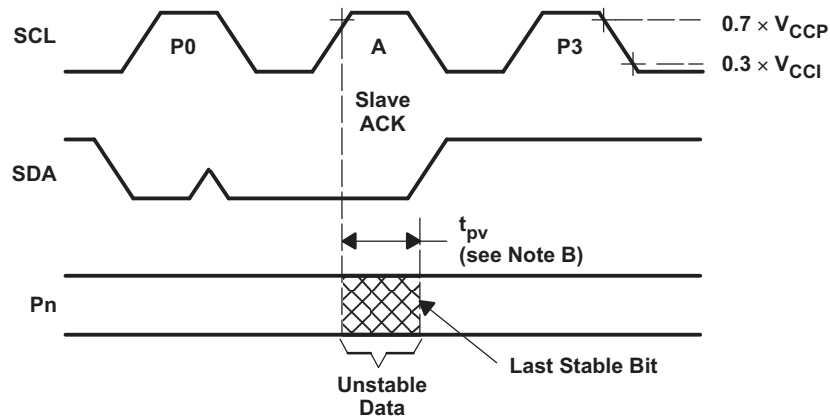
- A. C_L includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r/t_f \leq 30$ ns.
- C. All parameters and waveforms are not applicable to all devices.

Figure 13. Interrupt Load Circuit and Voltage Waveforms

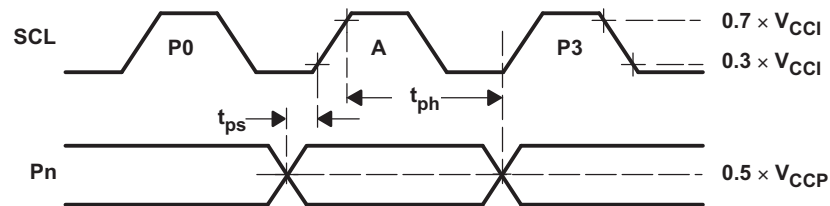
PARAMETER MEASUREMENT INFORMATION (continued)



P-PORT LOAD CONFIGURATION



WRITE MODE ($R/\bar{W} = 0$)

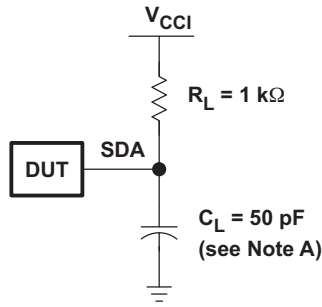


READ MODE ($R/\bar{W} = 1$)

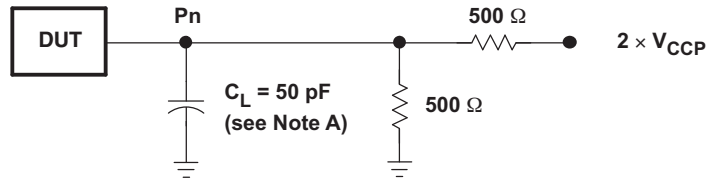
- A. C_L includes probe and jig capacitance.
- B. t_{pv} is measured from $0.7 \times V_{CC}$ on SCL to 50% I/O (Pn) output.
- C. All inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r/t_f \leq 30$ ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 14. P Port Load Circuit and Timing Waveforms

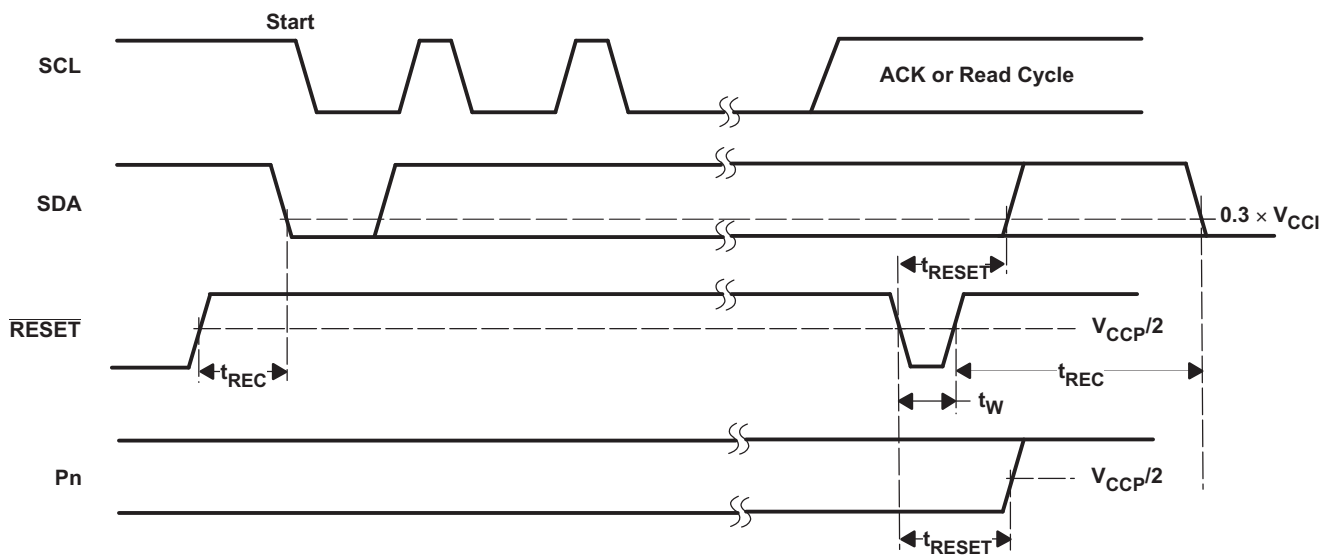
PARAMETER MEASUREMENT INFORMATION (continued)



SDA LOAD CONFIGURATION



P-PORT LOAD CONFIGURATION



- A. C_L includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r/t_f \leq 30\text{ ns}$.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. I/Os are configured as inputs.
- E. All parameters and waveforms are not applicable to all devices.

Figure 15. Reset Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|----------------|
| TCA6418EYFPR | ACTIVE | DSBGA | YFP | 25 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (AZ2, AZN) | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

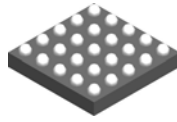
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TCA6418EYFPR | DSBGA | YFP | 25 | 3000 | 178.0 | 9.2 | 2.09 | 2.09 | 0.62 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TCA6418EYFPR | DSBGA | YFP | 25 | 3000 | 220.0 | 220.0 | 35.0 |

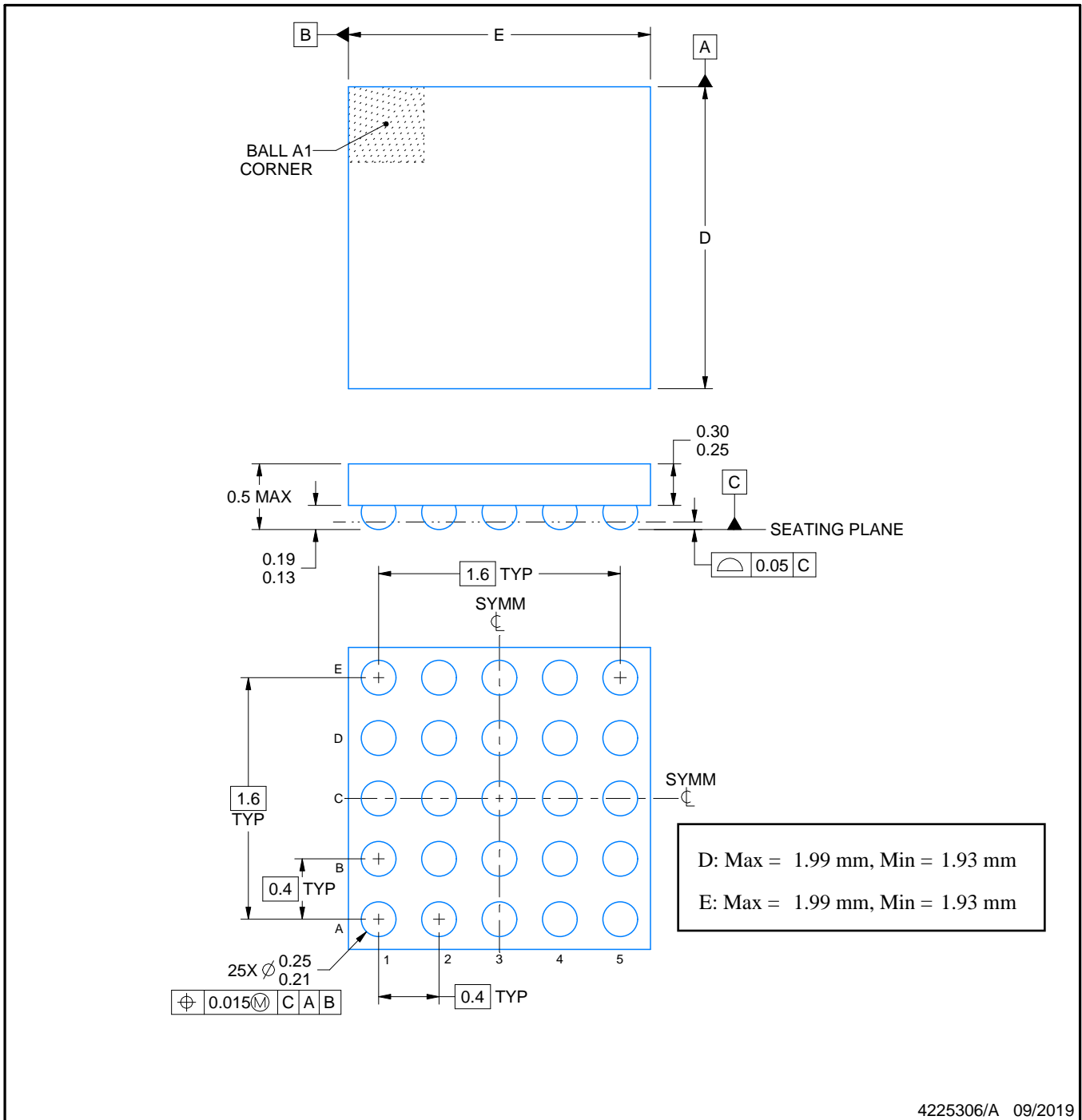
YFP0025



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

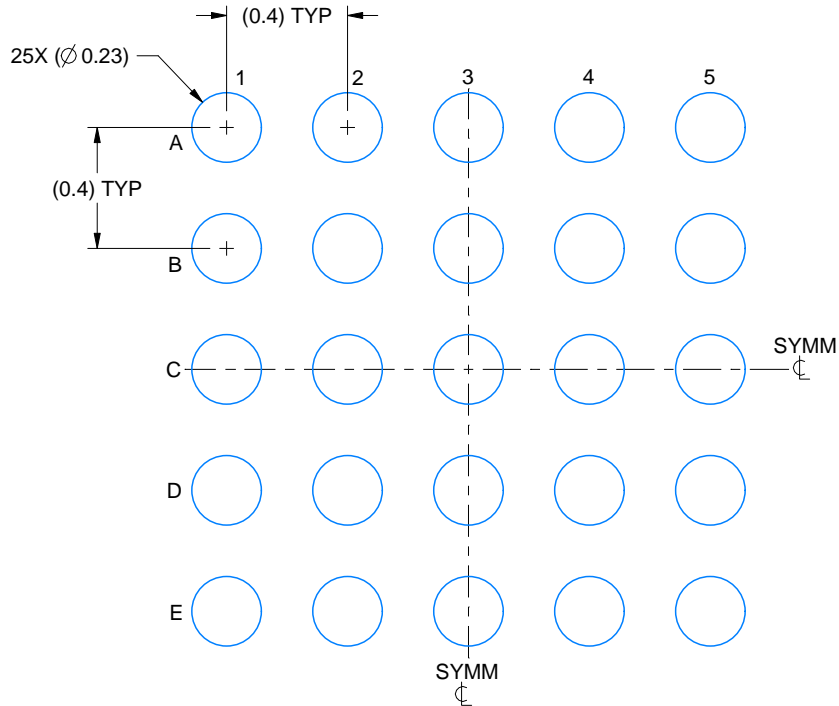
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

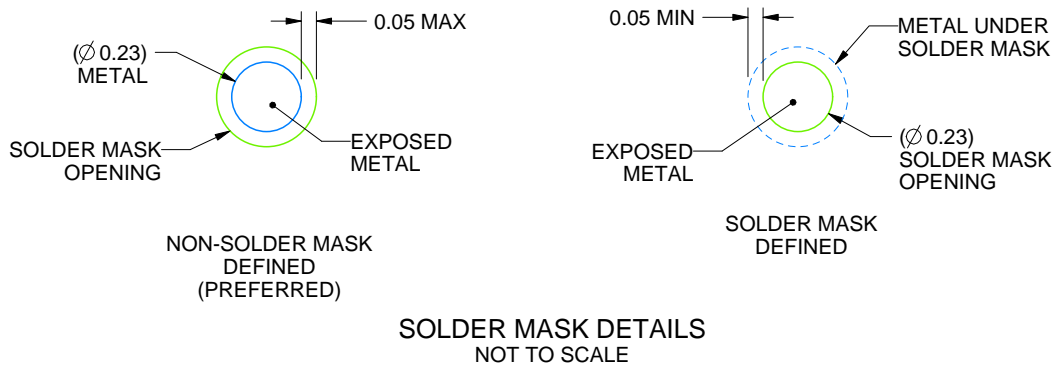
YFP0025

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

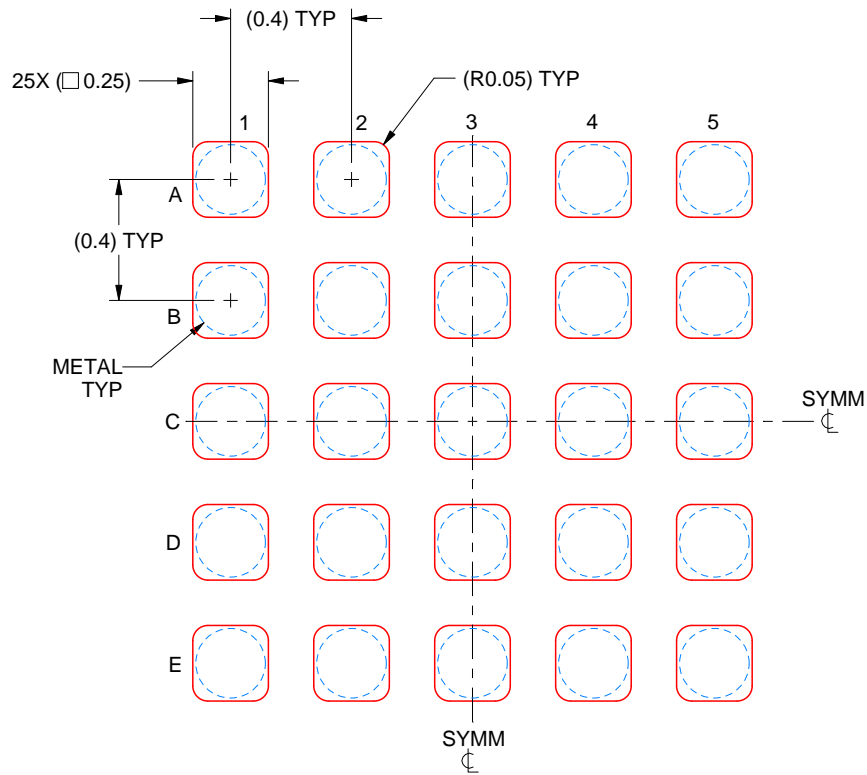
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0025

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

4225306/A 09/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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