4-Channel Video Amplifier with 1-SD and 3-HD Sixth-Order Filters and 6-dB Gain

Check for Samples: THS7373

FEATURES

- **One SDTV Video Amplifier for CVBS Video**
- **Three HDTV Video Amplifiers for Y'/P'$_B$/P'$_R$, 720p/1080i/1080p30, or G'B'R' (R'G'B')**
- **Sixth-Order Low-Pass Filters:**
  - **CVBS Channel: –3 dB at 9.5-MHz**
  - **HD Channels: –3 dB at 36-MHz with 350-MHz Bypass for 1080p60 Support**
- **Versatile Input Biasing:**
  - **DC-Coupled with 300-mV Output Shift**
  - **AC-Coupled with Sync-Tip Clamp**
  - **Allows AC-Coupling with Biasing**
- **Built-in 6-dB Gain (2 V/V)**
- **+3-V to +5-V Single-Supply Operation**
- **Rail-to-Rail Output:**
  - **Output Swings Within 100 mV from the Rails: Allows AC or DC Output Coupling**
  - **Supports Driving Two Video Lines/Channel**
- **Low Total Quiescent Current: 16.2 mA at 3.3 V**
- **Disabled Supply Current Function: 0.1 µA**
- **Low Differential Gain/Phase: 0.15%/0.25°**
- **RoHS-Compliant Package: TSSOP-14**

APPLICATIONS

- **Set Top Box Output Video Buffering**
- **PVR/DVDR/ BluRay™ Output Buffering**
- **Low-Power Video Buffering**

DESCRIPTION

Fabricated using the revolutionary, complementary Silicon-Germanium (SiGe) BiCom3X process, the THS7373 is a low-power, single-supply, 3-V to 5-V, four-channel integrated video buffer. It incorporates one standard-definition (CVBS) and three high-definition (HD) filter channels. All filters feature sixth-order Butterworth characteristics that are useful as digital-to-analog converter (DAC) reconstruction filters or as analog-to-digital converter (ADC) anti-aliasing filters. The HD filters can be bypassed to support 1080p60 video or up to quad extended graphics array (QXGA) RGB video.

As part of the THS7373 flexibility, the input can be configured for ac- or dc-coupled inputs. The 300-mV output level shift allows for a full sync dynamic range at the output with 0-V input. The ac-coupled modes include a transparent sync-tip clamp option for composite video (CVBS), Y', and G'B'R' signals. AC-coupled biasing for C'/P'$_B$/P'$_R$ channels can easily be achieved by adding an external resistor to V_{S+}.

The THS7373 rail-to-rail output stage with 6-dB gain allows for both ac and dc line driving. The ability to drive two lines, or 75-Ω loads, allows for maximum flexibility as a video line driver. The 16.2-mA total quiescent current at 3.3 V and 0.1 µA (disabled mode) makes it an excellent choice for power-sensitive video applications.

The THS7373 is available in a small TSSOP-14 package that is lead-free and green (RoHS-compliant).

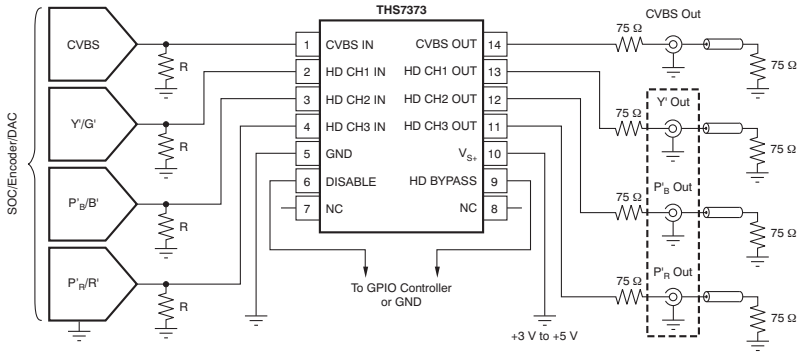

Figure 1. Single-Supply, DC-Input/DC-Output Coupled Video Line Driver

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1) (2)

PRODUCT	PACKAGE-LEAD	TRANSPORT MEDIA, QUANTITY	ECO STATUS(2)
THS7373IPW	TSSOP-14	Rails, 90	Pb-Free, Green
THS7373IPWR		Tape and Reel, 2000	

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) These packages conform to Lead (Pb)-free and green manufacturing specifications. Additional details including specific material content can be accessed at www.ti.com/leadfree.
GREEN: TI defines Green to mean Lead (Pb)-Free and in addition, uses less package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1% of total product weight. N/A: Not yet available Lead (Pb)-Free; for estimated conversion dates, go to www.ti.com/leadfree. Pb-FREE: TI defines Lead (Pb)-Free to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		THS7373	UNIT
Supply voltage, V_{S+} to GND		5.5	V
Input voltage, V_I		–0.4 to V_{S+}	V
Output current, I_O		±90	mA
Continuous power dissipation		See the Dissipation Ratings Table	
Maximum junction temperature, any condition(2), T_J		+150	°C
Maximum junction temperature, continuous operation, long-term reliability(3), T_J		+125	°C
Storage temperature range, T_{STG}		–60 to +150	°C
ESD rating:	Human body model (HBM)	2500	V
	Charge device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.

(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	AT $T_A \le +25°C$ POWER RATING	AT $T_A = +85°C$ POWER RATING
TSSOP-14 (PW)	38	115(1)	870 mW	348 mW

(1) These data were taken with the JEDEC High-K test printed circuit board (PCB). For the JEDEC low-K test PCB, the θ_{JA} is 130°C/W.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{S+}	3		5.5	V
Ambient temperature, T_A	–40	+25	+85	°C

ELECTRICAL CHARACTERISTICS: V_{S+} = +3.3 V

At T_A = +25°C, R_L = 150 Ω to GND, Filter mode, and dc-coupled input/output, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7373 MIN	THS7373 TYP	THS7373 MAX	UNITS	TEST LEVEL(1)
AC PERFORMANCE (CVBS CHANNEL)						
Passband bandwidth	–1 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	7	8.2	10.2	MHz	B
Small- and large-signal bandwidth	–3 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	7.8	9.5	11.4	MHz	B
Attenuation	With respect to 500 kHz(2), f = 6.75 MHz	–0.9	0.2	1.1	dB	B
	With respect to 500 kHz(2), f = 27 MHz	42	54		dB	B
Group delay	f = 100 kHz		70		ns	C
Group delay variation	f = 5.1 MHz with respect to 100 kHz		9		ns	C
Differential gain	NTSC/PAL		0.15/0.25		%	C
Differential phase	NTSC/PAL		0.25/0.35		Degrees	C
Total harmonic distortion	f = 1 MHz, V_O = 1.4 V_{PP}		–70		dB	C
Signal-to-noise ratio	100 kHz to 6 MHz, non-weighted		70		dB	C
	100 kHz to 6 MHz, unified weighting		78		dB	C
Gain	T_A = +25°C	5.7	6	6.3	dB	A
	T_A = –40°C to +85°C	5.65		6.35	dB	B
Output impedance	f = 6.75 MHz		0.8		Ω	C
	Disabled		20 || 3		kΩ || pF	C
Return loss	f = 6.75 MHz		45		dB	C
Crosstalk	f = 1 MHz, CVBS channel to HD channels		–85		dB	C
AC PERFORMANCE (HD CHANNELS)						
Passband bandwidth	–1 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	27.8	33	38.8	MHz	B
Small- and large-signal bandwidth	–3 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	30.3	36	42.5	MHz	B
Bypass mode bandwidth	–3 dB; V_O = 0.2 V_{PP}	170	350		MHz	B
Slew rate	Bypass mode; V_O = 2 V_{PP}	400	450		V/µs	B
Attenuation	With respect to 500 kHz(2), f = 27 MHz	–1	–0.1	1	dB	B
	With respect to 500 kHz(2), f = 74 MHz	34	40		dB	B
Group delay	f = 100 kHz		20		ns	C
Group delay variation	f = 27 MHz with respect to 100 kHz		6		ns	C
Channel-to-channel delay			0.3		ns	C
Differential gain	NTSC/PAL		0.1/0.1		%	C
Differential phase	NTSC/PAL		0.1/0.15		Degrees	C
Total harmonic distortion	f = 10 MHz, V_O = 1.4 V_{PP}		–52		dB	C
Signal-to-noise ratio	100 kHz to 30 MHz, non-weighted		62.5		dB	C
	unified weighting		72		dB	C
Gain	All channels, T_A = +25°C	5.7	6	6.3	dB	A
	All channels, T_A = –40°C to +85°C	5.65		6.35	dB	B

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation only. **(C)** Typical value only for information.

(2) 3.3-V supply filter specifications are ensured by 100% testing at 5-V supply along with design and characterization.

ELECTRICAL CHARACTERISTICS: V_{S+} = +3.3 V (continued)

At T_A = +25°C, R_L = 150 Ω to GND, Filter mode, and dc-coupled input/output, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7373 MIN	THS7373 TYP	THS7373 MAX	UNITS	TEST LEVEL(1)
AC PERFORMANCE (HD CHANNELS) (continued)						
Output impedance	f = 30 MHz, Filter mode		1.4		Ω	C
	f = 30 MHz, Bypass mode		1		Ω	C
	Disabled		1.8 || 3		kΩ || pF	C
Return loss	f = 30 MHz, Filter mode		41		dB	C
Crosstalk	f = 1 MHz, HD to CVBS channel		–78		dB	C
	f = 1 MHz, CVBS to HD channels		–85		dB	C
	f = 1 MHz, HD to HD channels		–78		dB	C
DC PERFORMANCE						
Biased output voltage	V_{IN} = 0 V, CVBS channel	200	300	400	mV	A
	V_{IN} = 0 V, HD channels	200	300	400	mV	A
Input voltage range	DC input, limited by output		–0.1/1.46		V	C
Sync-tip clamp charge current	V_{IN} = –0.1 V, CVBS channel	140	200		µA	A
	V_{IN} = –0.1 V, HD channels	280	400		µA	A
Input impedance			800 || 2		kΩ || pF	C
OUTPUT CHARACTERISTICS						
High output voltage swing	R_L = 150 Ω to +1.65 V		3.15		V	C
	R_L = 150 Ω to GND	2.85	3.1		V	A
	R_L = 75 Ω to +1.65 V		3.1		V	C
	R_L = 75 Ω to GND		3		V	C
Low output voltage swing	R_L = 150 Ω to +1.65 V (V_{IN} = –0.2 V)		0.04		V	C
	R_L = 150 Ω to GND (V_{IN} = –0.2 V)		0.03	0.1	V	A
	R_L = 75 Ω to +1.65 V (V_{IN} = –0.2 V)		0.1		V	C
	R_L = 75 Ω to GND (V_{IN} = –0.2 V)		0.05		V	C
Output current (sourcing)	R_L = 10 Ω to +1.65 V		80		mA	C
Output current (sinking)	R_L = 10 Ω to +1.65 V		70		mA	C
POWER SUPPLY						
Operating voltage		2.6	3.3	5.5	V	B
Total quiescent current, no load	V_{IN} = 0 V, all channels on	13.4	16.2	21	mA	A
	V_{IN} = 0 V, all channels off, $V_{DISABLE}$ = 3 V		0.1	10	µA	A
Power-supply rejection ratio (PSRR)	At dc		52		dB	C
LOGIC CHARACTERISTICS(3)						
V_{IH}	Disabled or Bypass mode	2	1.8		V	A
V_{IL}	Enabled or Filter mode		0.7	0.65	V	A
I_{IH}	Applied voltage = 3.3 V		0.2		µA	C
I_{IL}	Applied voltage = 0 V		0.2		µA	C
Disable time			150		ns	C
Enable time			150		ns	C
Bypass/filter switch time			15		ns	C

(3) The logic input pins should not be left floating. They must be connected to logic low (or GND) or logic high (or V_{S+}).

ELECTRICAL CHARACTERISTICS: V_{S+} = +5 V

At T_A = +25°C, R_L = 150 Ω to GND, Filter mode, and dc-coupled input/output, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7373 MIN	THS7373 TYP	THS7373 MAX	UNITS	TEST LEVEL(1)
AC PERFORMANCE (CVBS CHANNEL)						
Passband bandwidth	–1 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	7	8.2	10.2	MHz	B
Small- and large-signal bandwidth	–3 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	7.8	9.5	11.4	MHz	B
Attenuation	With respect to 500 kHz, f = 6.75 MHz	–0.9	0.2	1.1	dB	A
	With respect to 500 kHz, f = 27 MHz	42	54		dB	A
Group delay	f = 100 kHz		70		ns	C
Group delay variation	f = 5.1 MHz with respect to 100 kHz		9		ns	C
Differential gain	NTSC/PAL		0.15/0.25		%	C
Differential phase	NTSC/PAL		0.25/0.4		Degrees	C
Total harmonic distortion	f = 1 MHz, V_O = 1.4 V_{PP}		–73		dB	C
Signal-to-noise ratio	100 kHz to 6 MHz, non-weighted		70		dB	C
	100 kHz to 6 MHz, unified weighting		78		dB	C
Gain	T_A = +25°C	5.7	6	6.3	dB	A
	T_A = –40°C to +85°C	5.65		6.35	dB	B
Output impedance	f = 6.75 MHz		0.8		Ω	C
	Disabled		20 || 3		kΩ || pF	C
Return loss	f = 6.75 MHz		45		dB	C
Crosstalk	f = 1 MHz, CVBS channel to HD channels		–86		dB	C
AC PERFORMANCE (HD CHANNELS)						
Passband bandwidth	–1 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	27.8	33	38.8	MHz	B
Small- and large-signal bandwidth	–3 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	30.3	36	42.5	MHz	B
Bypass mode bandwidth	–3 dB; V_O = 0.2 V_{PP}	170	375		MHz	B
Slew rate	Bypass mode; V_O = 2 V_{PP}	400	450		V/µs	B
Attenuation	With respect to 500 kHz, f = 27 MHz	–1	–0.1	1	dB	A
	With respect to 500 kHz, f = 74 MHz	34	40		dB	A
Group delay	f = 100 kHz		20		ns	C
Group delay variation	f = 27MHz with respect to 100 kHz		6		ns	C
Channel-to-channel delay			0.3		ns	C
Differential gain	NTSC/PAL		0.1/0.1		%	C
Differential phase	NTSC/PAL		0.15/0.2		Degrees	C
Total harmonic distortion	f = 10 MHz, V_O = 1.4 V_{PP}		–55		dB	C
Signal-to-noise ratio	100 kHz to 30 MHz, non-weighted		62.5		dB	C
	unified weighting		72		dB	C
Gain	All channels, T_A = +25°C	5.7	6	6.3	dB	A
	All channels, T_A = –40°C to +85°C	5.65		6.35	dB	B
Output impedance	f = 30 MHz, Filter mode		1.4		Ω	C
	f = 30 MHz, Bypass mode		1		Ω	C
	Disabled		1.8 || 3		kΩ || pF	C

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation only. **(C)** Typical value only for information.

ELECTRICAL CHARACTERISTICS: V_{S+} = +5 V (continued)

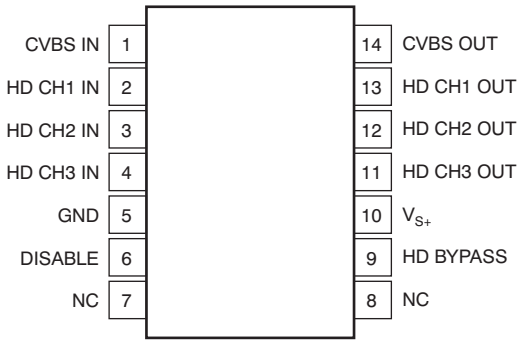
At T_A = +25°C, R_L = 150 Ω to GND, Filter mode, and dc-coupled input/output, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7373 MIN	THS7373 TYP	THS7373 MAX	UNITS	TEST LEVEL(1)
AC PERFORMANCE (HD CHANNELS) (continued)						
Return loss	f = 30 MHz, Filter mode		41		dB	C
Crosstalk	f = 1 MHz, HD to CVBS channel		–78		dB	C
	f = 1 MHz, CVBS to HD channels		–86		dB	C
	f = 1 MHz, HD to HD channels		–78		dB	C
DC PERFORMANCE						
Biased output voltage	V_{IN} = 0 V, CVBS channel	200	300	400	mV	A
	V_{IN} = 0 V, HD channels	200	300	400	mV	A
Input voltage range	DC input, limited by output		–0.1/2.3		V	C
Sync-tip clamp charge current	V_{IN} = –0.1 V, CVBS channel	140	200		µA	A
	V_{IN} = –0.1 V, HD channels	280	400		µA	A
Input impedance			800 || 2		kΩ || pF	C
OUTPUT CHARACTERISTICS						
High output voltage swing	R_L = 150 Ω to +2.5 V		4.85		V	C
	R_L = 150 Ω to GND	4.5	4.75		V	A
	R_L = 75 Ω to +2.5V		4.7		V	C
	R_L = 75 Ω to GND		4.5		V	C
Low output voltage swing	R_L = 150 Ω to +2.5 V (V_{IN} = –0.2 V)		0.05		V	C
	R_L = 150 Ω to GND (V_{IN} = –0.2 V)		0.03	0.1	V	A
	R_L = 75 Ω to +2.5 V (V_{IN} = –0.2 V)		0.1		V	C
	R_L = 75 Ω to GND (V_{IN} = –0.2 V)		0.05		V	C
Output current (sourcing)	R_L = 10 Ω to +2.5 V		90		mA	C
Output current (sinking)	R_L = 10 Ω to +2.5 V		85		mA	C
POWER SUPPLY						
Operating voltage		2.6	5	5.5	V	B
Total quiescent current, no load	V_{IN} = 0 V, all channels on	14	16.9	22	mA	A
	V_{IN} = 0 V, all channels off, $V_{DISABLE}$ = 3 V		1	10	µA	A
Power-supply rejection ratio (PSRR)	At dc		52		dB	C
LOGIC CHARACTERISTICS(2)						
V_{IH}	Disabled or Bypass engaged	2.2	2.1		V	A
V_{IL}	Enabled or Bypass disengaged		0.8	0.75	V	A
I_{IH}	Applied voltage = 3.3 V		0.2		µA	C
I_{IL}	Applied voltage = 0 V		0.2		µA	C
Disable time			100		ns	C
Enable time			100		ns	C
Bypass/filter switch time			10		ns	C

(2) The logic input pins should not be left floating. They must be connected to logic low (or GND) or logic high (or V_{S+}).

PIN CONFIGURATION

PW PACKAGE
TSSOP-14
(TOP VIEW)

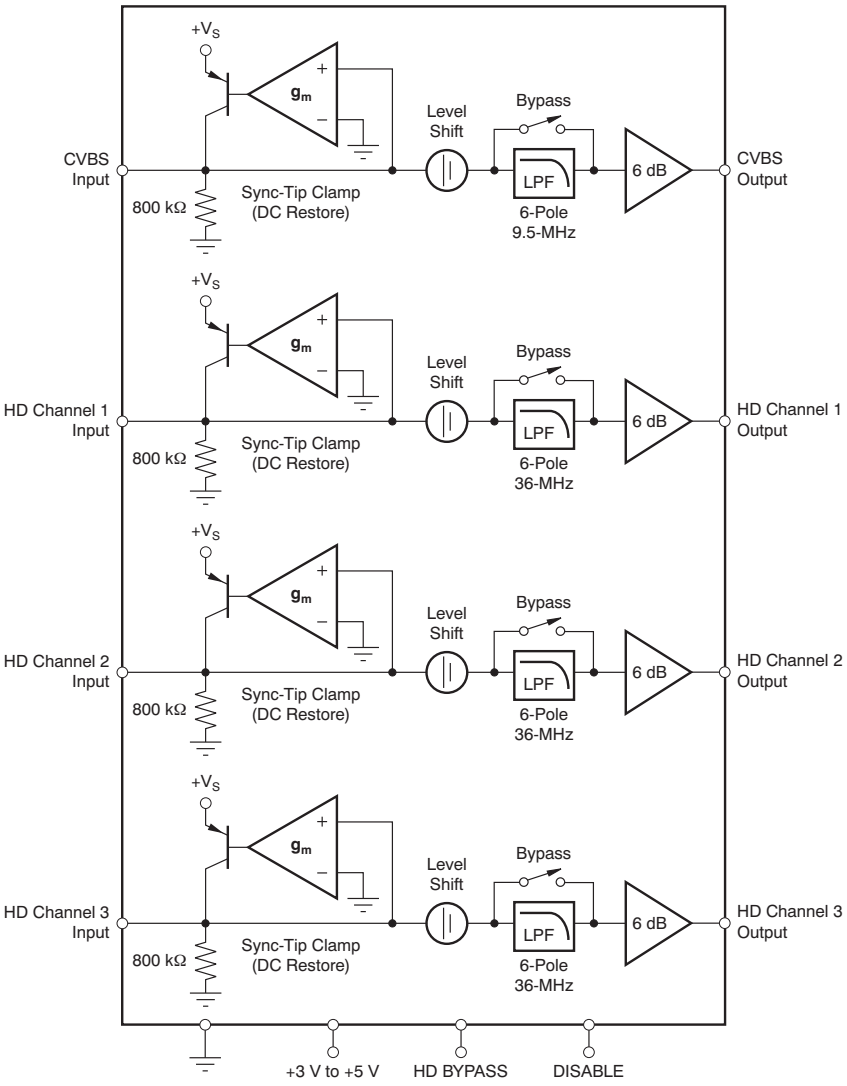


NOTE: NC = No connection.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CVBS IN	1	I	CVBS filter video input
HD CH.1 IN	2	I	HD channels 1 video input
HD CH.2 IN	3	I	HD channels 2 video input
HD CH.3 IN	4	I	HD channels 3 video input
GND	5	I	Ground pin for all internal circuitry
DISABLE	6	I	Disable pin. Logic high disables the part; logic low enables the part. This pin must not be left floating. It must be connected to a defined logic state (or GND or VS+).
NC	7, 8	—	No internal connection
HD BYPASS	9	I	Internal HD filter bypass. Logic high bypasses the internal HD low-pass filter; logic low uses the HD internal filters. This pin must not be left floating. It must be connected to a defined logic state (or GND or VS+).
V_{S+}	10	I	Positive power-supply pin; connect to +3 V to +5 V
HD CH.3 OUT	11	O	HD channels 3 video output
HD CH.2 OUT	12	O	HD channels 2 video output
HD CH.1 OUT	13	O	HD channels 1 video output
CVBS OUT	14	O	CVBS filter video output

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Table 1. Table of Graphs: +3.3 V and +5 V

TITLE	FIGURE
Maximum Output Voltage vs Temperature	Figure 2
Minimum Output Voltage vs Temperature	Figure 3
CVBS Channel Output Impedance vs Frequency	Figure 4
CVBS Channel S22 Output Reflection Ratio vs Frequency	Figure 5
HD Channels Output Impedance vs Frequency	Figure 6
HD Channels S22 Output Reflection Ratio vs Frequency	Figure 7
CVBS Channel Disabled Output Impedance vs Frequency	Figure 8
HD Channels Disabled Output Impedance vs Frequency	Figure 9
Input Resistance vs Temperature	Figure 10
Total Quiescent Current vs Temperature	Figure 11
Total Quiescent Current vs Supply Voltage	Figure 12

Table 2. Table of Graphs: 3.3 V, Standard-Definition (CVBS) Channels

TITLE	FIGURE
CVBS Channel Small-Signal Gain vs Frequency	Figure 13, Figure 14, Figure 17
CVBS Channel Large-Signal Gain vs Frequency	Figure 15, Figure 16
CVBS Channel Phase vs Frequency	Figure 18
CVBS Channel Group Delay vs Frequency	Figure 19
CVBS Channel Second-Order Harmonic Distortion vs Frequency	Figure 23
CVBS Channel Third-Order Harmonic Distortion vs Frequency	Figure 24
Crosstalk vs Frequency	Figure 27, Figure 28
CVBS Channel Slew Rate vs Output Voltage	Figure 29
Disable Mode Response vs Time	Figure 30
CVBS Channel Differential Gain	Figure 21
CVBS Channel Differential Phase	Figure 22
CVBS Channel Small-Signal Pulse Response vs Time	Figure 25
CVBS Channel Large-Signal Pulse Response vs Time	Figure 26
CVBS Channel PSRR vs Frequency	Figure 20
Output Offset Voltage vs Temperature	Figure 31

Table 3. Table of Graphs: 3.3 V, High-Definition (HD) Channels

TITLE	FIGURE
HD Channels Small-Signal Gain vs Frequency	Figure 32, Figure 33, Figure 36, Figure 37
HD Channels Large-Signal Gain vs Frequency	Figure 34, Figure 35
HD Channels Phase vs Frequency	Figure 38
HD Channels Group Delay vs Frequency	Figure 39
HD Channels Second-Order Harmonic Distortion vs Frequency	Figure 41, Figure 43
HD Channels Third-Order Harmonic Distortion vs Frequency	Figure 42, Figure 44
HD Channels Slew Rate vs Output Voltage	Figure 49
Bypass Mode Response vs Time	Figure 50
Disable Mode Response vs Time	Figure 51, Figure 52
HD Channels Small-Signal Pulse Response vs Time	Figure 45, Figure 47
HD Channels Large-Signal Pulse Response vs Time	Figure 46, Figure 48
HD Channels PSRR vs Frequency	Figure 40

Table 4. Table of Graphs: 5 V, Standard-Definition (CVBS) Channels

TITLE	FIGURE
CVBS Channel Small-Signal Gain vs Frequency	Figure 53, Figure 54, Figure 57
CVBS Channel Large-Signal Gain vs Frequency	Figure 55, Figure 56
CVBS Channel Phase vs Frequency	Figure 58
CVBS Channel Group Delay vs Frequency	Figure 59
CVBS Channel Second-Order Harmonic Distortion vs Frequency	Figure 63
CVBS Channel Third-Order Harmonic Distortion vs Frequency	Figure 64
Crosstalk vs Frequency	Figure 67, Figure 68
CVBS Channel Slew Rate vs Output Voltage	Figure 69
Disable Mode Response vs Time	Figure 70
CVBS Channel Small-Signal Pusle Response vs Time	Figure 65
CVBS Channel Large-Signal Pulse Response vs Time	Figure 66
CVBS Channel PSRR vs Frequency	Figure 60
CVBS Channel Differential Gain	Figure 61
CVBS Channel Differential Phase	Figure 62
CVBS Channel Attenuation at 6.75 MHz vs Temperature	Figure 71
CVBS Channel Attenuation at 27 MHz vs Temperature	Figure 72
Output Offset Voltage vs Temperature	Figure 73

Table 5. Table of Graphs: 5 V, High-Definition (HD) Channels

TITLE	FIGURE
HD Channels Small-Signal Gain vs Frequency	Figure 74, Figure 75, Figure 78, Figure 79
HD Channels Large-Signal Gain vs Frequency	Figure 76, Figure 77
HD Channels Phase vs Frequency	Figure 80
HD Channels Group Delay vs Frequency	Figure 81
HD Channels Second-Order Harmonic Distortion vs Frequency	Figure 83, Figure 85
HD Channels Third-Order Harmonic Distortion vs Frequency	Figure 84, Figure 86
HD Channels Slew Rate vs Output Voltage	Figure 91
Bypass Mode Response vs Time	Figure 92
Disable Mode Response vs Time	Figure 93, Figure 94
HD Channels PSRR vs Frequency	Figure 82
HD Channels Small-Signal Pulse Response vs Time	Figure 87, Figure 89
HD Channels Large-Signal Pulse Response vs Time	Figure 88, Figure 90
HD Channels Attenuation at 27 MHz vs Temperature	Figure 95
HD Channels Attenuation at 74 MHz vs Temperature	Figure 96

TYPICAL CHARACTERISTICS: +3.3 V and +5 V

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

MAXIMUM OUTPUT VOLTAGE vs TEMPERATURE

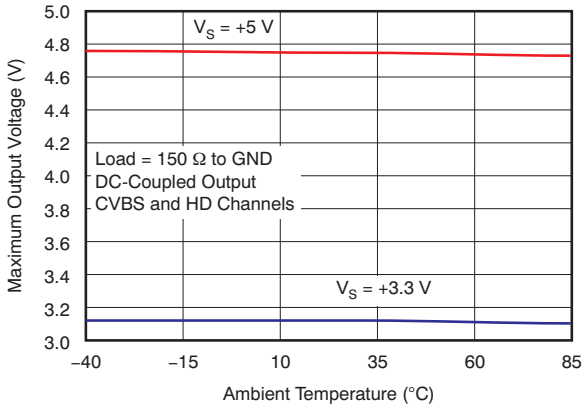


Figure 2.

MINIMUM OUTPUT VOLTAGE vs TEMPERATURE

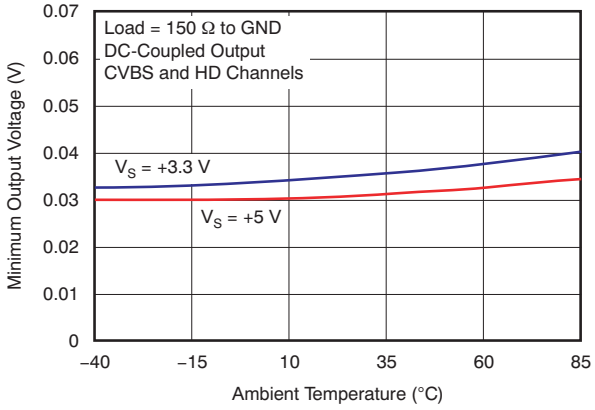


Figure 3.

CVBS CHANNEL OUTPUT IMPEDANCE vs FREQUENCY

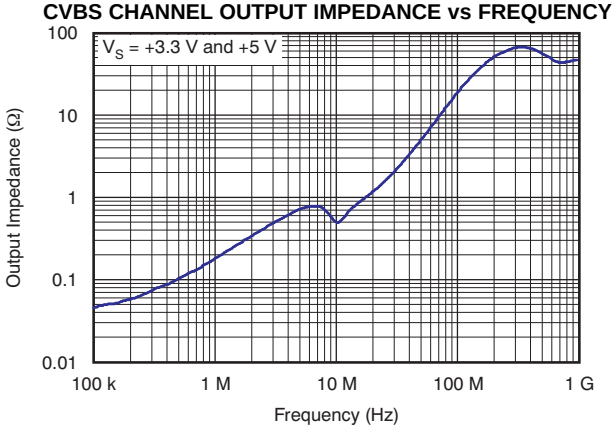


Figure 4.

CVBS CHANNEL S22 OUTPUT REFLECTION RATIO vs FREQUENCY

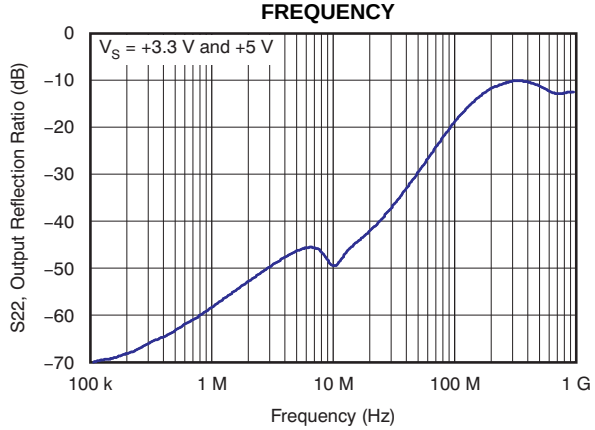


Figure 5.

HD CHANNELS OUTPUT IMPEDANCE vs FREQUENCY

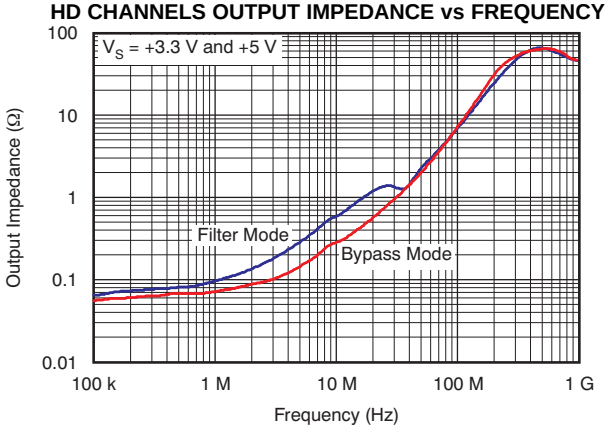


Figure 6.

HD CHANNELS S22 OUTPUT REFLECTION RATIO vs FREQUENCY

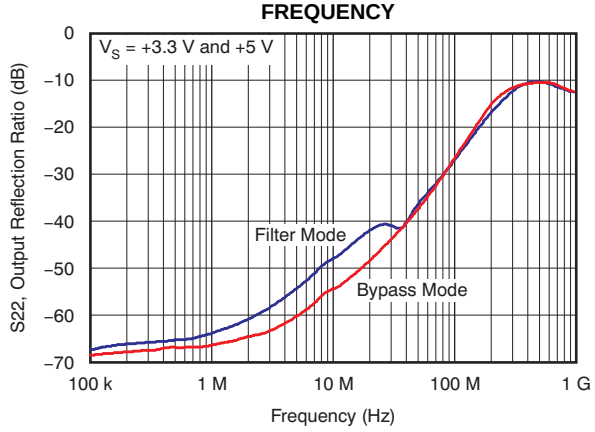


Figure 7.

TYPICAL CHARACTERISTICS: +3.3 V and +5 V (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

CVBS CHANNEL DISABLED OUTPUT IMPEDANCE vs FREQUENCY

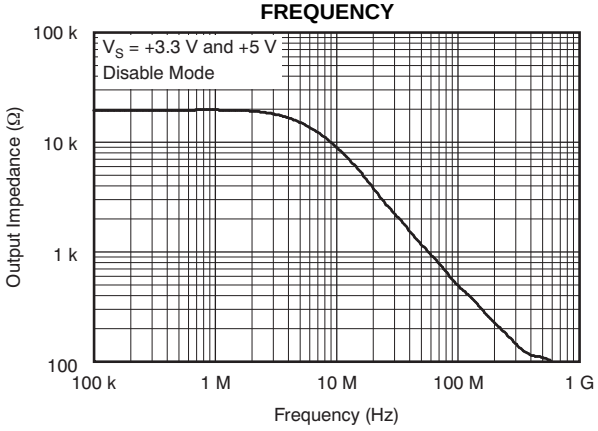


Figure 8.

HD CHANNELS DISABLED OUTPUT IMPEDANCE vs FREQUENCY

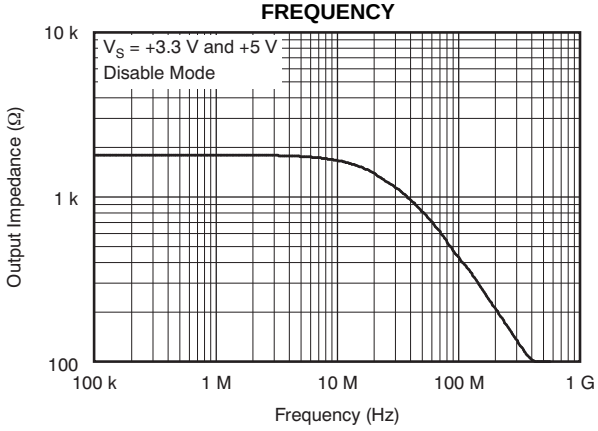


Figure 9.

INPUT RESISTANCE vs TEMPERATURE

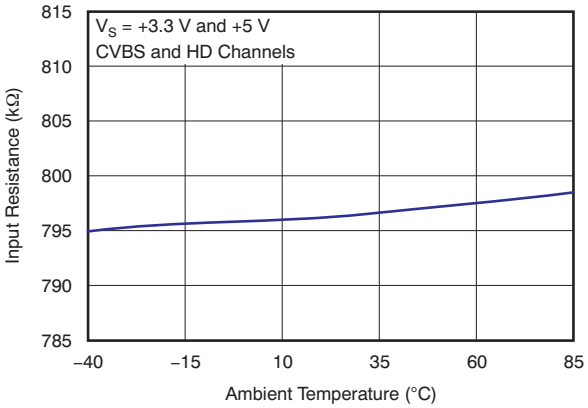


Figure 10.

TOTAL QUIESCENT CURRENT vs TEMPERATURE

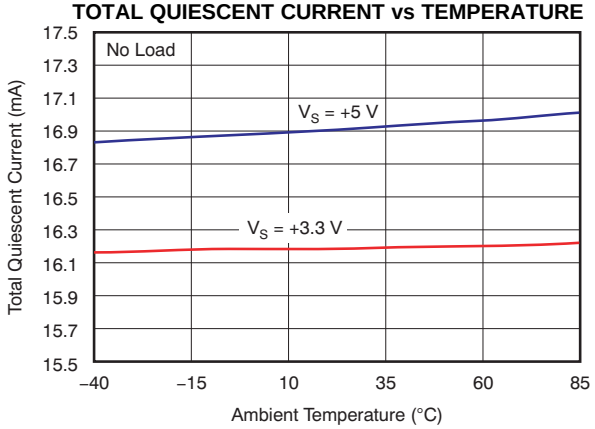


Figure 11.

TOTAL QUIESCENT CURRENT vs SUPPLY VOLTAGE

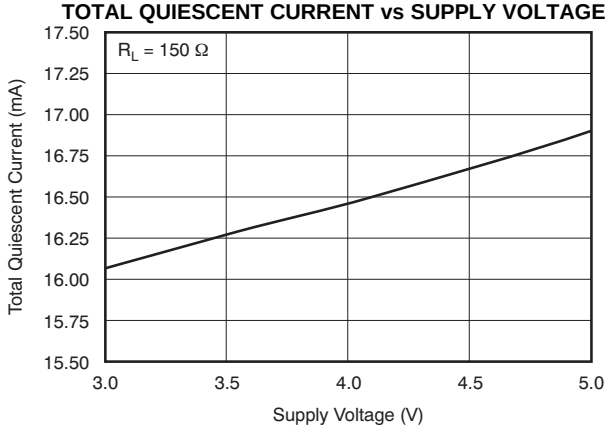


Figure 12.

TYPICAL CHARACTERISTICS: 3.3 V, Standard-Definition (CVBS) Channels

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

CVBS CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

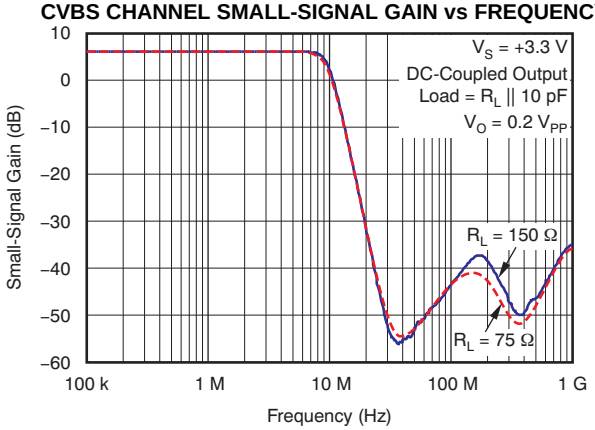


Figure 13.

CVBS CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

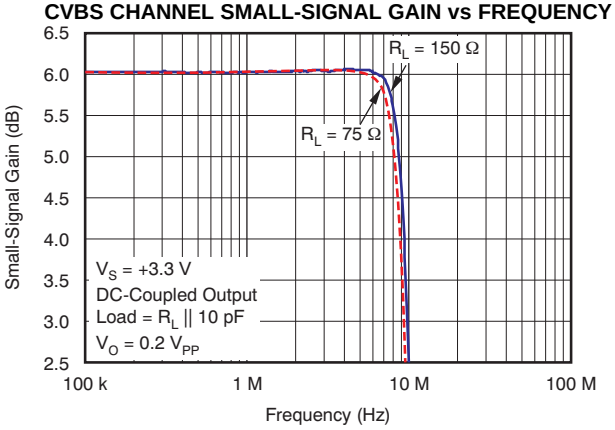


Figure 14.

CVBS CHANNEL LARGE-SIGNAL GAIN vs FREQUENCY

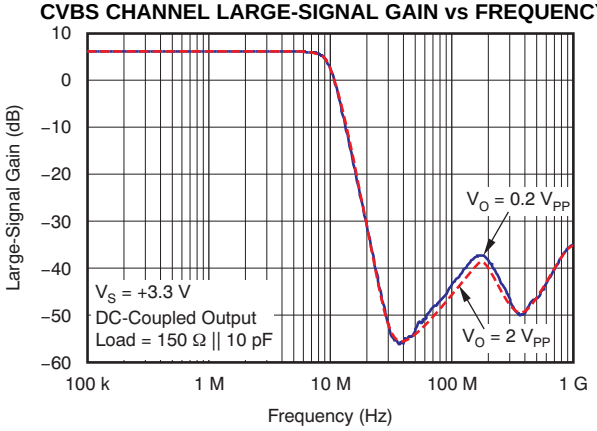


Figure 15.

CVBS CHANNEL LARGE-SIGNAL GAIN vs FREQUENCY

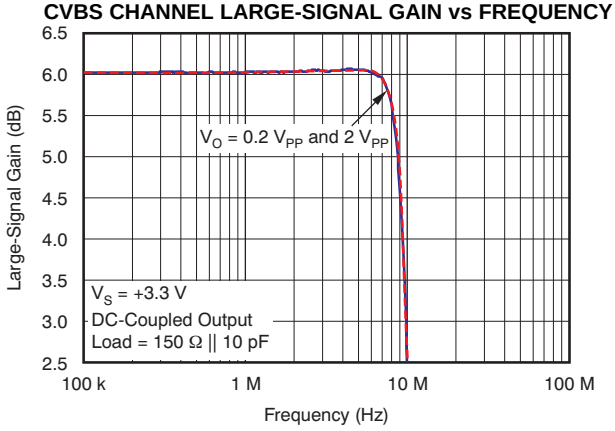


Figure 16.

CVBS CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

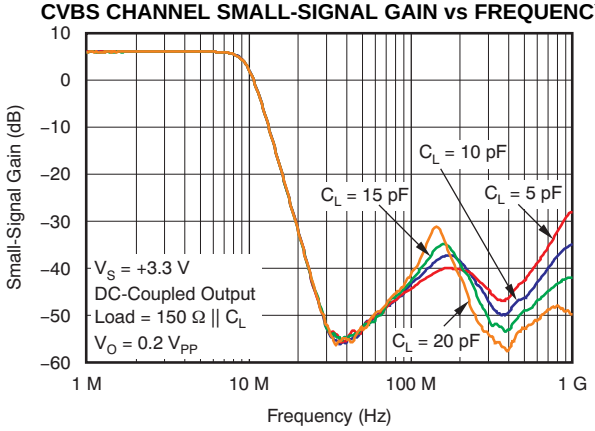


Figure 17.

CVBS CHANNEL PHASE vs FREQUENCY

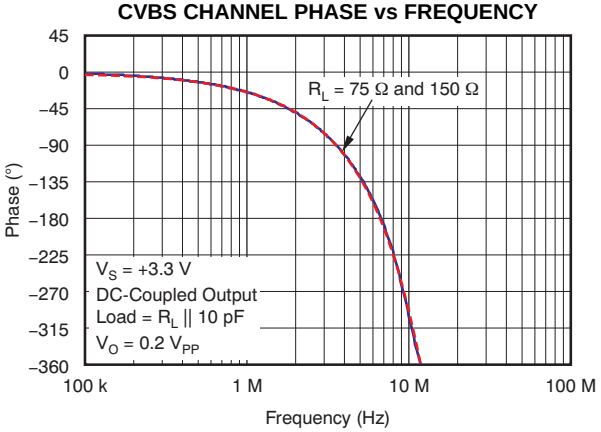


Figure 18.

TYPICAL CHARACTERISTICS: 3.3 V, Standard-Definition (CVBS) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

CVBS CHANNEL GROUP DELAY vs FREQUENCY

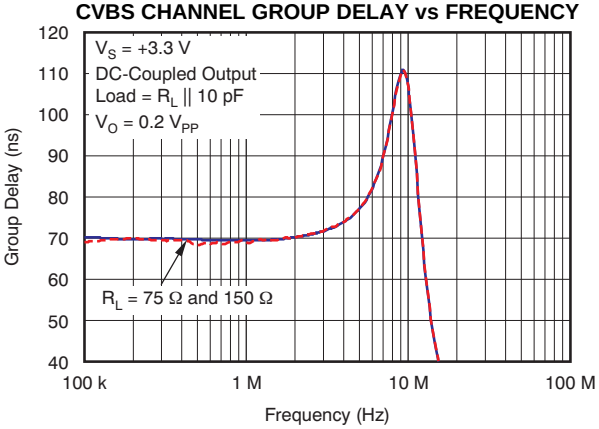


Figure 19.

CVBS CHANNEL PSRR vs FREQUENCY

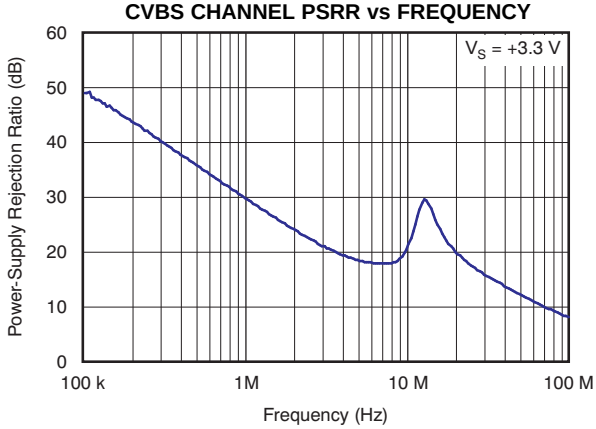


Figure 20.

CVBS CHANNEL DIFFERENTIAL GAIN

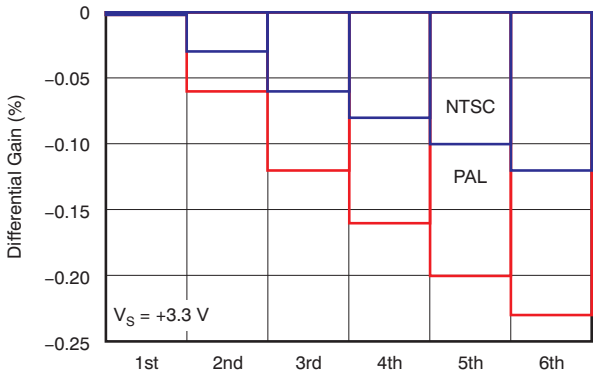


Figure 21.

CVBS CHANNEL DIFFERENTIAL PHASE

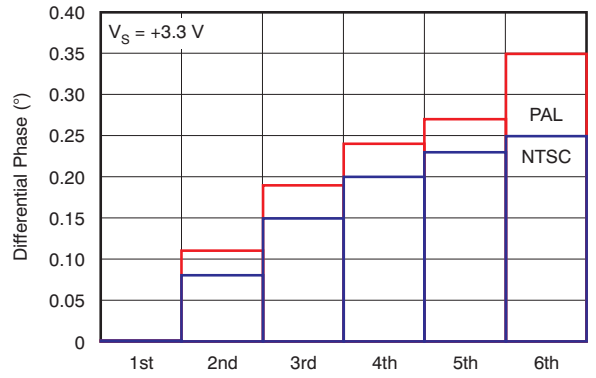


Figure 22.

CVBS CHANNEL SECOND-ORDER HARMONIC DISTORTION vs FREQUENCY

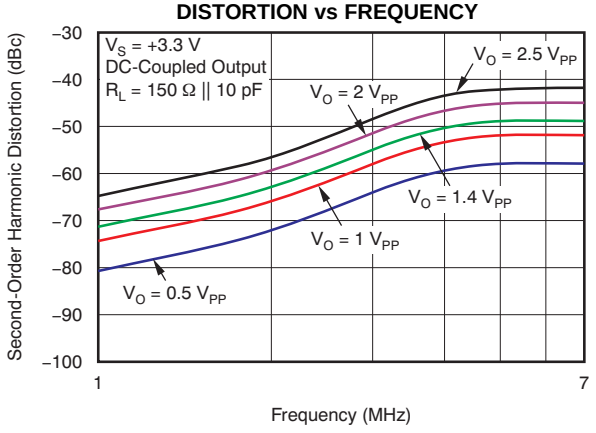


Figure 23.

CVBS CHANNEL THIRD-ORDER HARMONIC DISTORTION vs FREQUENCY

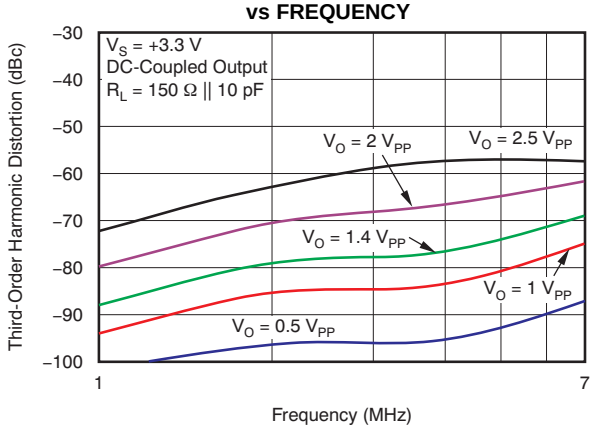


Figure 24.

TYPICAL CHARACTERISTICS: 3.3 V, Standard-Definition (CVBS) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

CVBS CHANNEL SMALL-SIGNAL PULSE RESPONSE vs TIME

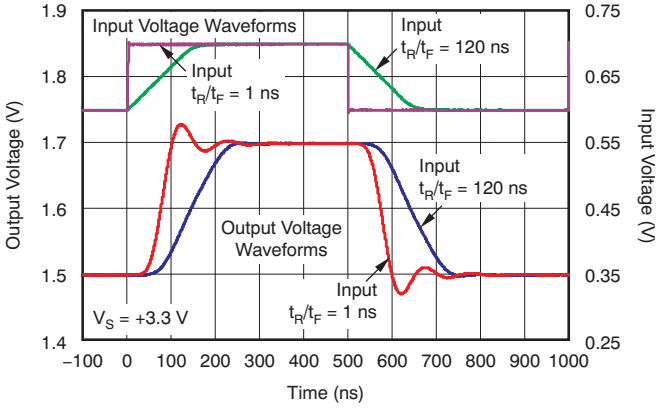


Figure 25.

CVBS CHANNEL LARGE-SIGNAL PULSE RESPONSE vs TIME

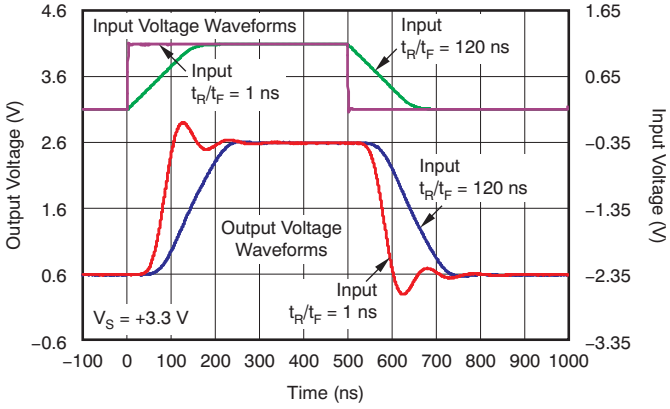


Figure 26.

CROSSTALK vs FREQUENCY

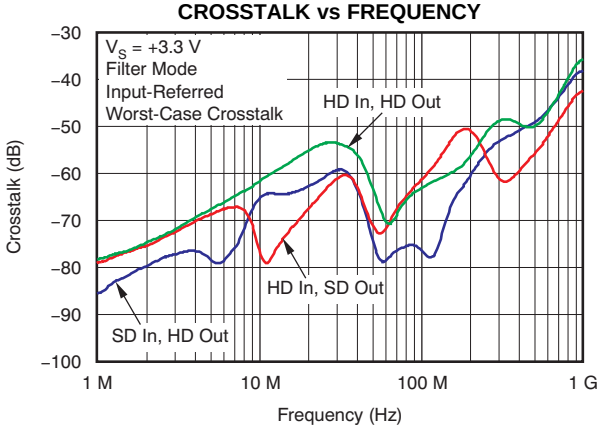


Figure 27.

CROSSTALK vs FREQUENCY

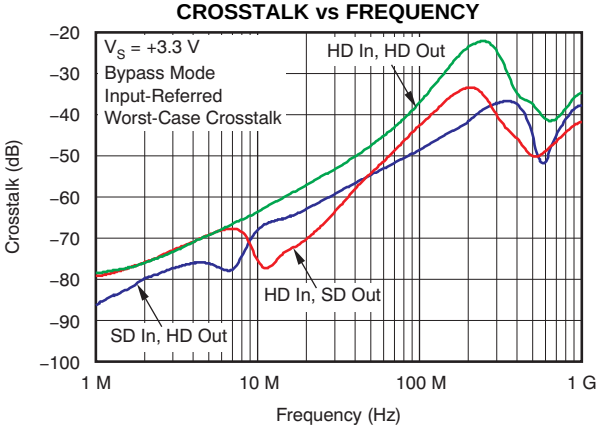


Figure 28.

CVBS CHANNEL SLEW RATE vs OUTPUT VOLTAGE

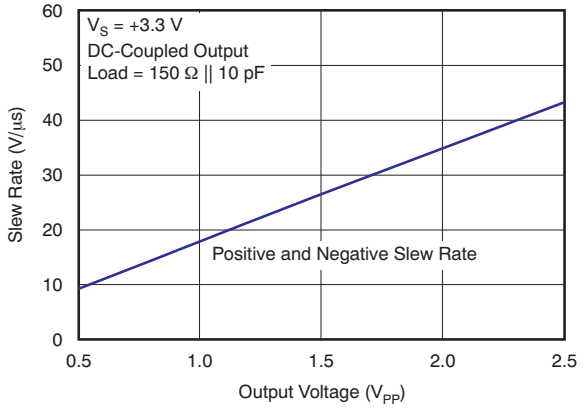


Figure 29.

CVBS CHANNEL DISABLE MODE RESPONSE vs TIME

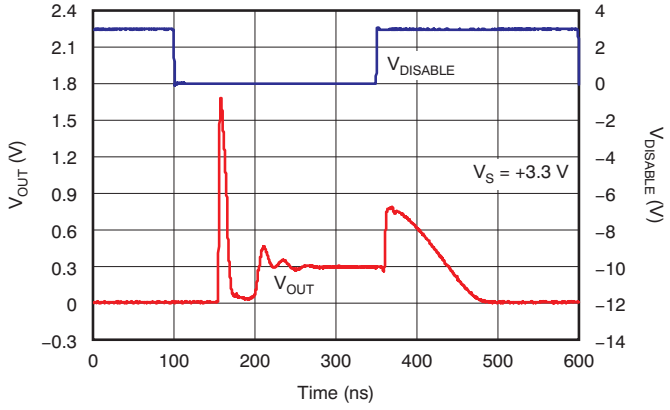


Figure 30.

TYPICAL CHARACTERISTICS: 3.3 V, Standard-Definition (CVBS) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

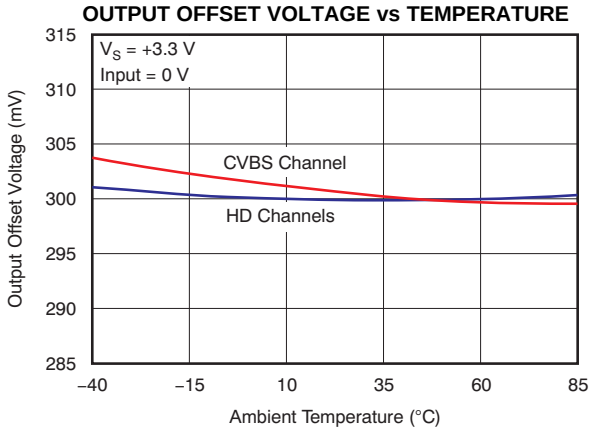


Figure 31.

TYPICAL CHARACTERISTICS: 3.3 V, High-Definition (HD) Channels

With load = 150 Ω || 5 pF, dc-coupled input and output, unless otherwise noted.

HD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY

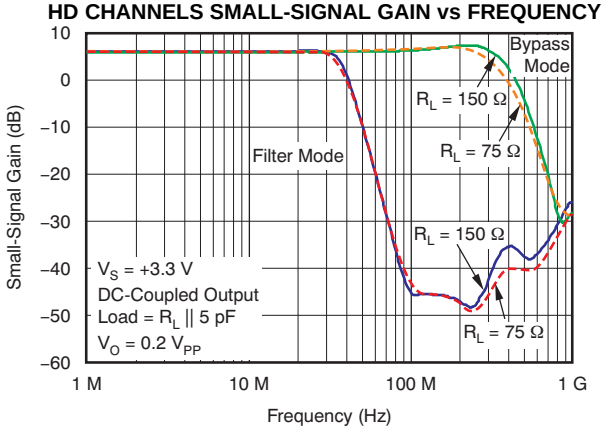


Figure 32.

HD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY

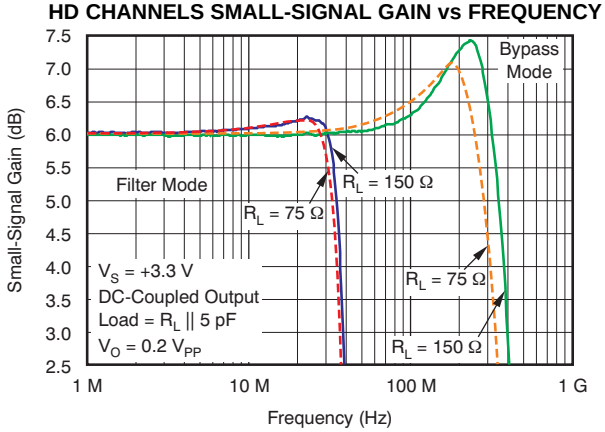


Figure 33.

HD CHANNELS LARGE-SIGNAL GAIN vs FREQUENCY

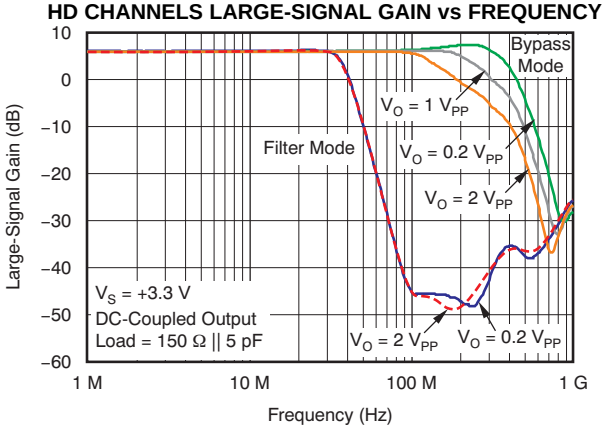


Figure 34.

HD CHANNELS LARGE-SIGNAL GAIN vs FREQUENCY

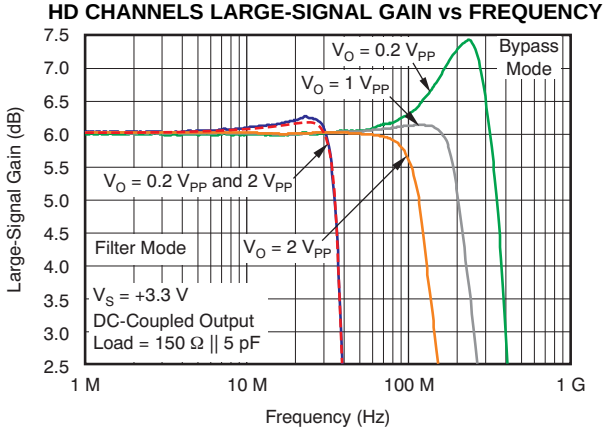


Figure 35.

HD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY

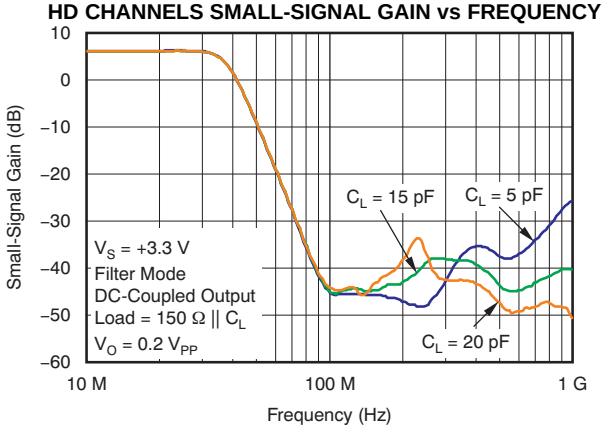


Figure 36.

HD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY

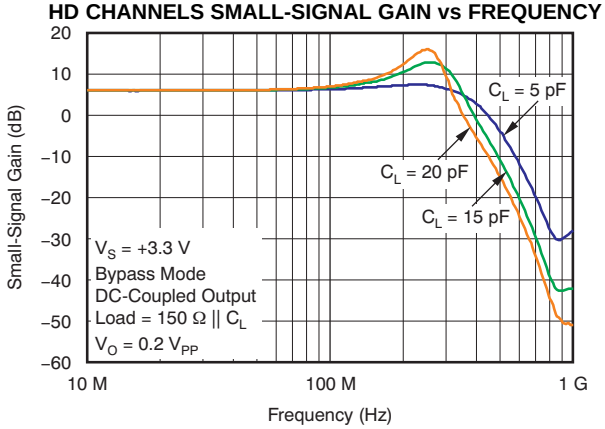


Figure 37.

TYPICAL CHARACTERISTICS: 3.3 V, High-Definition (HD) Channels (continued)

With load = 150 Ω || 5 pF, dc-coupled input and output, unless otherwise noted.

HD CHANNELS PHASE vs FREQUENCY

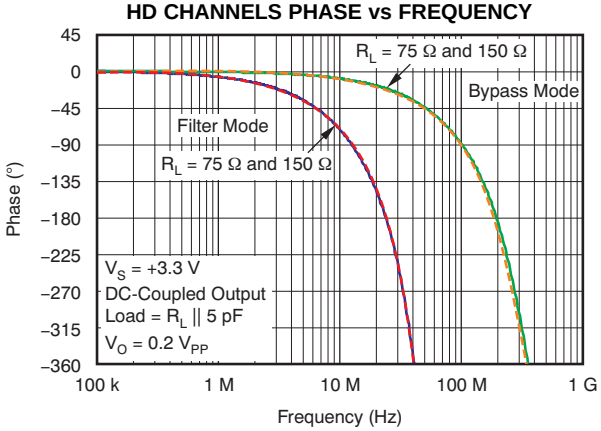


Figure 38.

HD CHANNELS GROUP DELAY vs FREQUENCY

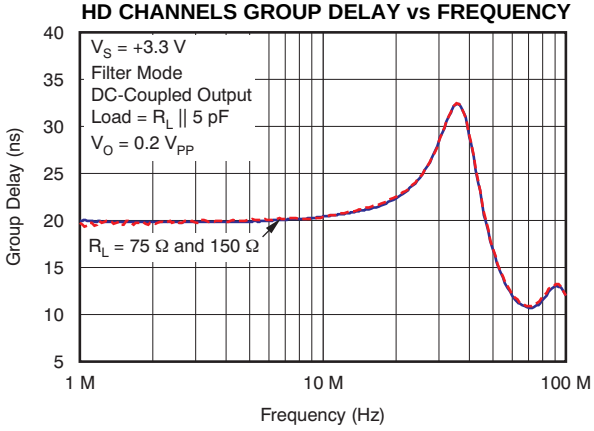


Figure 39.

HD CHANNELS PSRR vs FREQUENCY

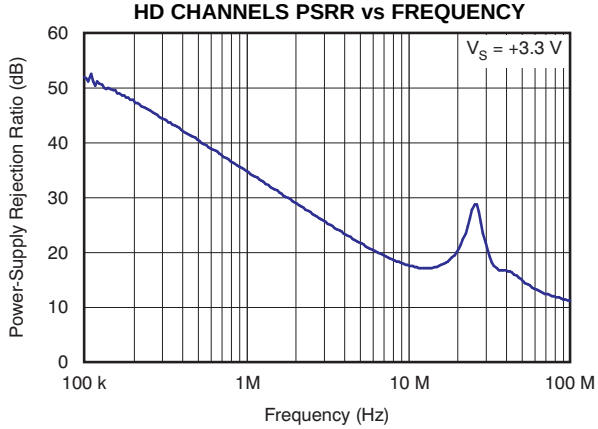


Figure 40.

HD CHANNELS SECOND-ORDER HARMONIC DISTORTION vs FREQUENCY

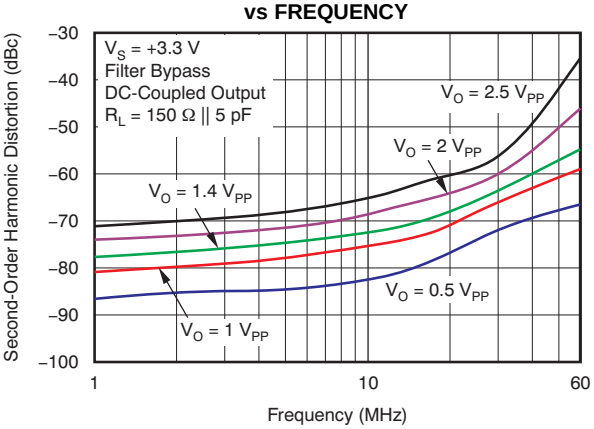


Figure 41.

HD CHANNELS THIRD-ORDER HARMONIC DISTORTION vs FREQUENCY

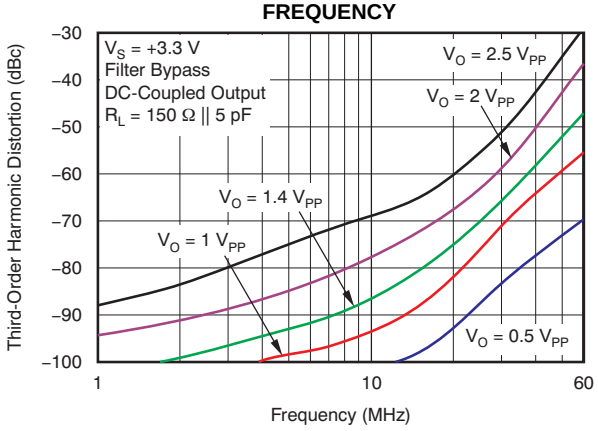


Figure 42.

HD CHANNELS SECOND-ORDER HARMONIC DISTORTION vs FREQUENCY

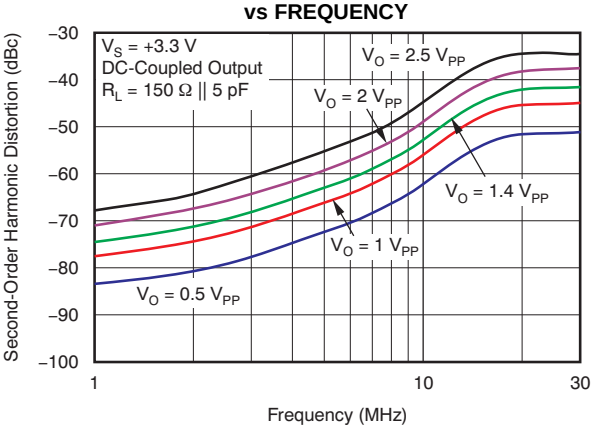


Figure 43.

TYPICAL CHARACTERISTICS: 3.3 V, High-Definition (HD) Channels (continued)

With load = 150 Ω || 5 pF, dc-coupled input and output, unless otherwise noted.

HD CHANNELS THIRD-ORDER HARMONIC DISTORTION vs FREQUENCY

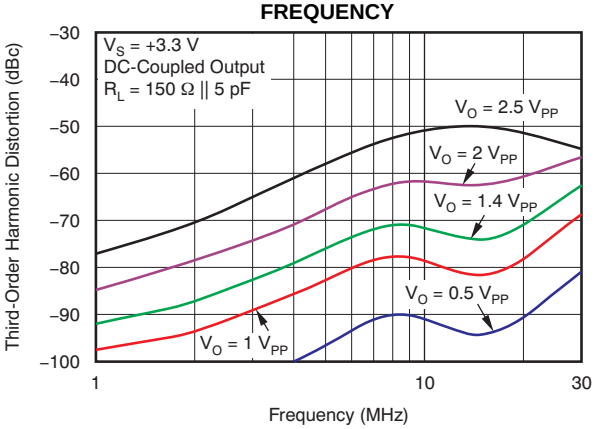


Figure 44.

HD CHANNELS SMALL-SIGNAL PULSE RESPONSE vs TIME

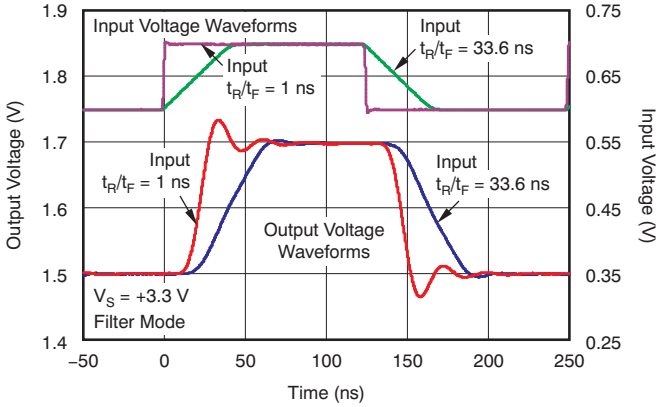


Figure 45.

HD CHANNELS LARGE-SIGNAL PULSE RESPONSE vs TIME

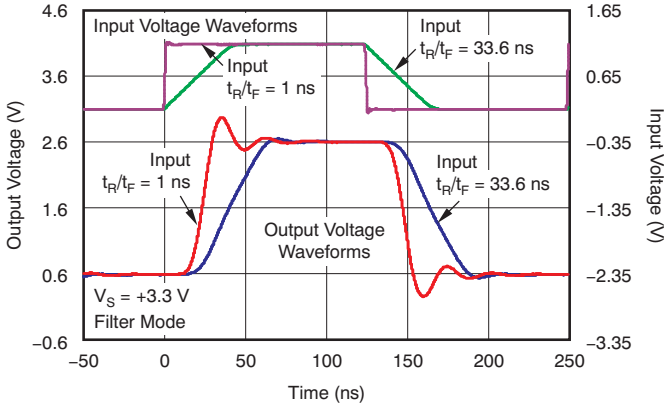


Figure 46.

HD CHANNELS SMALL-SIGNAL PULSE RESPONSE vs TIME

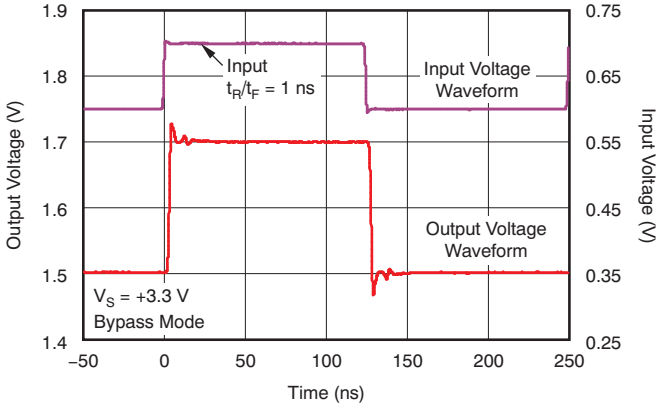


Figure 47.

HD CHANNELS LARGE-SIGNAL PULSE RESPONSE vs TIME

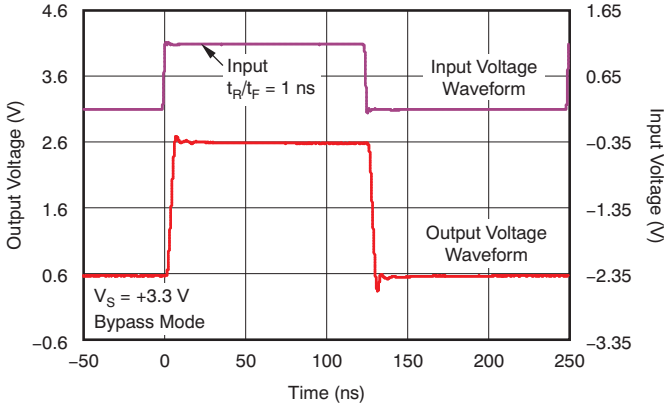


Figure 48.

HD CHANNELS SLEW RATE vs OUTPUT VOLTAGE

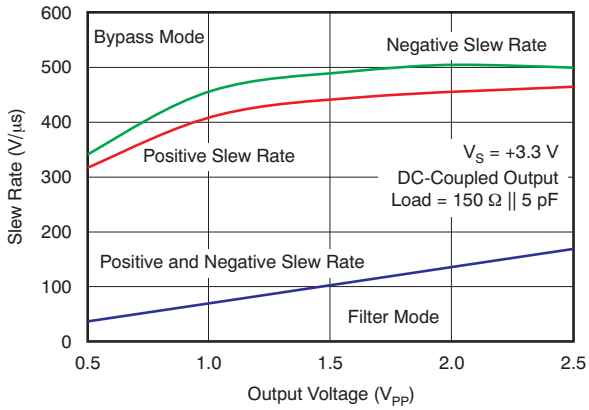


Figure 49.

TYPICAL CHARACTERISTICS: 3.3 V, High-Definition (HD) Channels (continued)

With load = 150 Ω || 5 pF, dc-coupled input and output, unless otherwise noted.

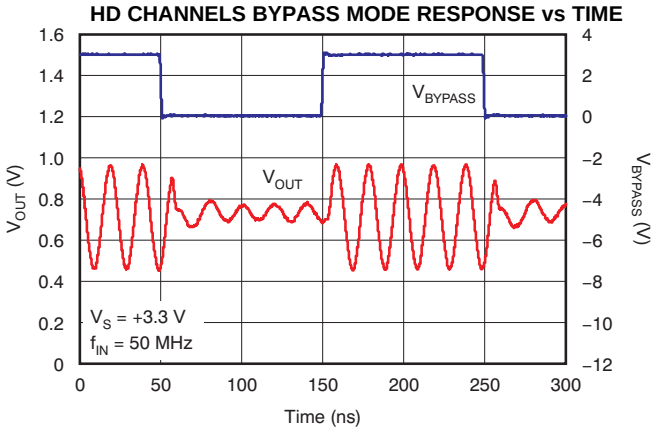


Figure 50.

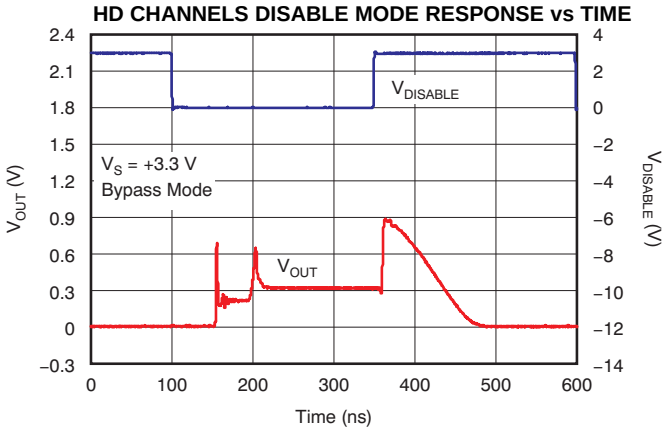


Figure 51.

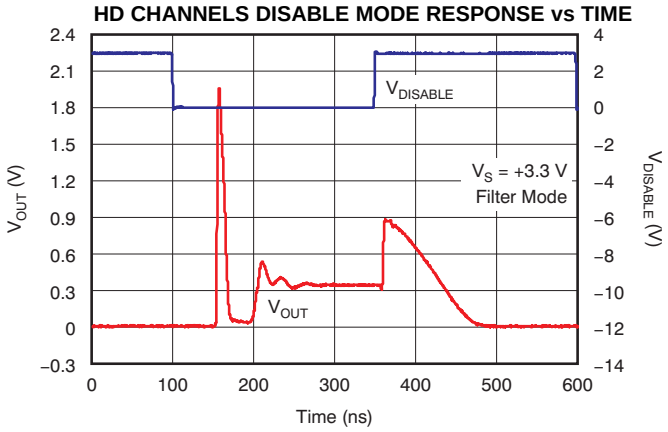


Figure 52.

TYPICAL CHARACTERISTICS: 5 V, Standard-Definition (CVBS) Channels

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

CVBS CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

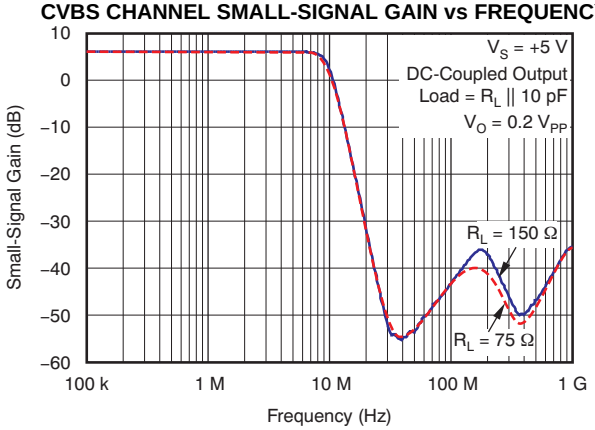


Figure 53.

CVBS CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

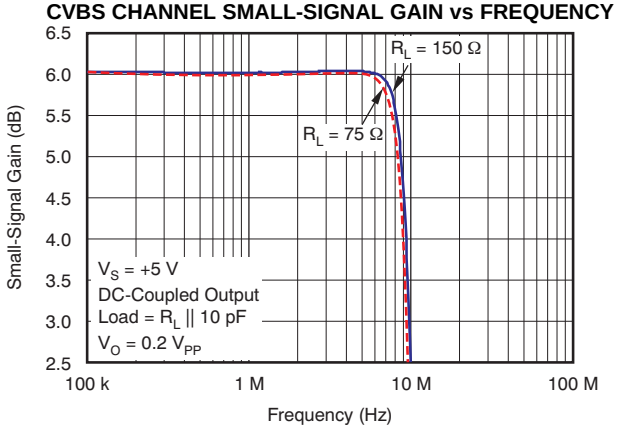


Figure 54.

CVBS CHANNEL LARGE-SIGNAL GAIN vs FREQUENCY

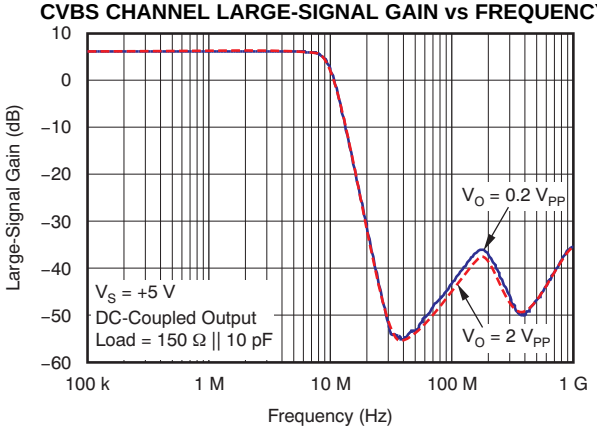


Figure 55.

CVBS CHANNEL LARGE-SIGNAL GAIN vs FREQUENCY

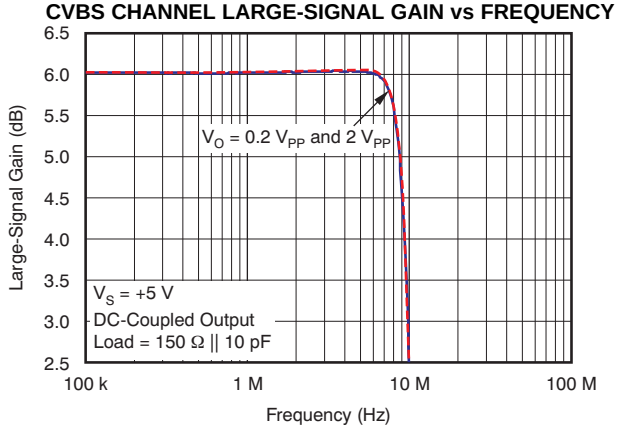


Figure 56.

CVBS CHANNEL SMALL-SIGNAL GAIN vs FREQUENCY

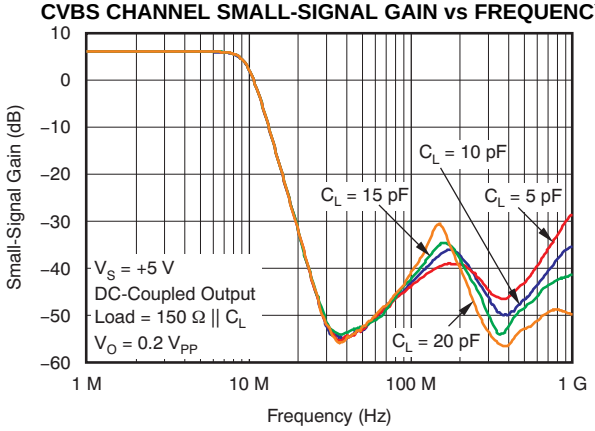


Figure 57.

CVBS CHANNEL PHASE vs FREQUENCY

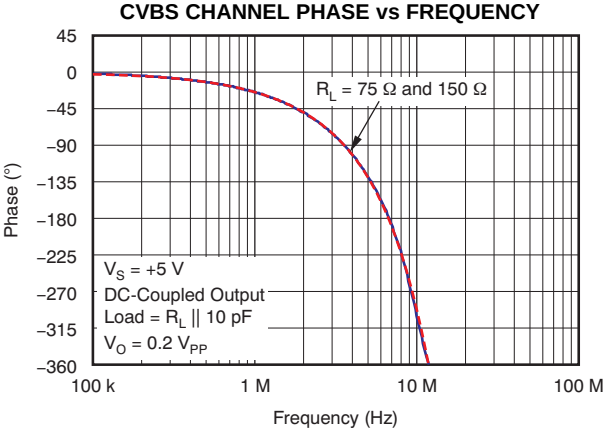


Figure 58.

TYPICAL CHARACTERISTICS: 5 V, Standard-Definition (CVBS) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

CVBS CHANNEL GROUP DELAY vs FREQUENCY

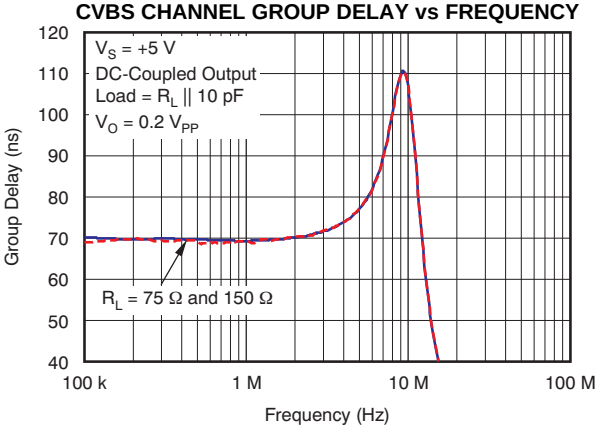


Figure 59.

CVBS CHANNEL PSRR vs FREQUENCY

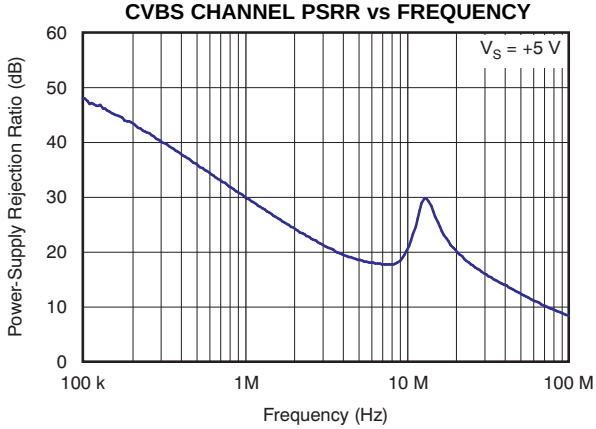


Figure 60.

CVBS CHANNEL DIFFERENTIAL GAIN

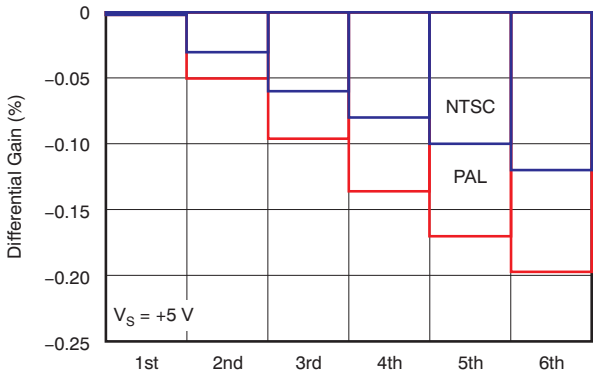


Figure 61.

CVBS CHANNEL DIFFERENTIAL PHASE

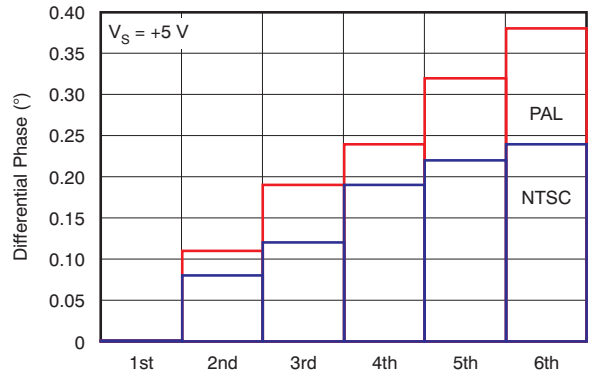


Figure 62.

CVBS CHANNEL SECOND-ORDER HARMONIC DISTORTION vs FREQUENCY

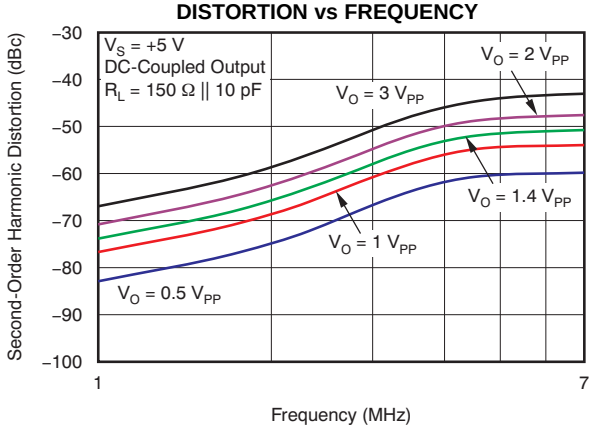


Figure 63.

CVBS CHANNEL THIRD-ORDER HARMONIC DISTORTION vs FREQUENCY

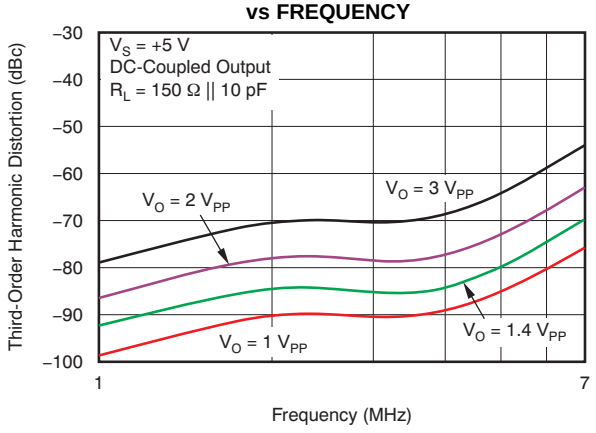


Figure 64.

TYPICAL CHARACTERISTICS: 5 V, Standard-Definition (CVBS) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

CVBS CHANNEL SMALL-SIGNAL PUSLE RESPONSE vs TIME

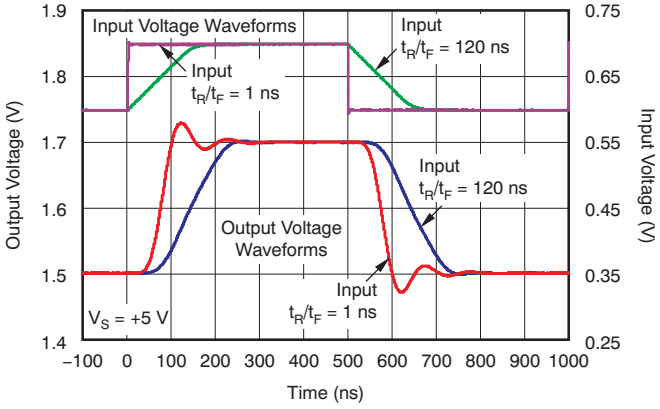


Figure 65.

CVBS CHANNEL LARGE-SIGNAL PUSLE RESPONSE vs TIME

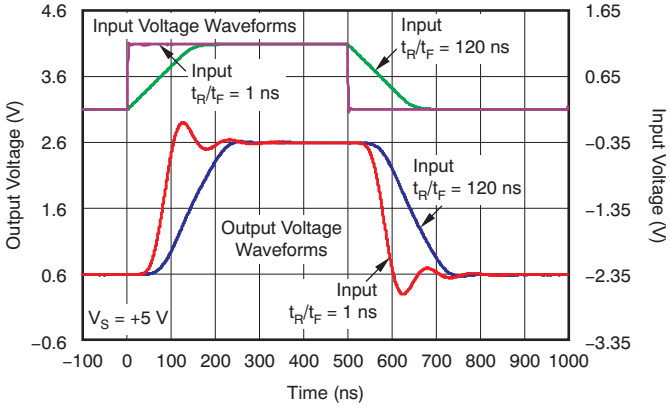


Figure 66.

CROSSTALK vs FREQUENCY

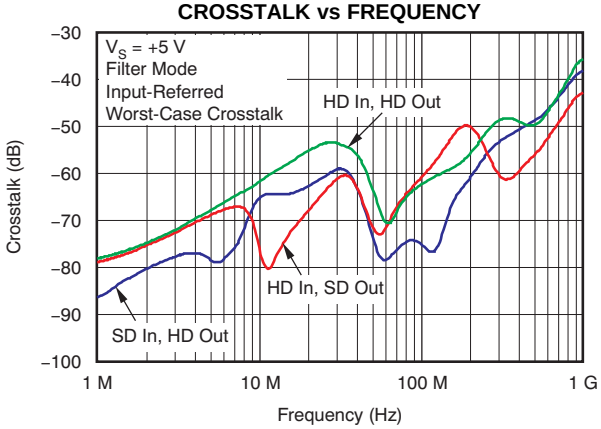


Figure 67.

CROSSTALK vs FREQUENCY

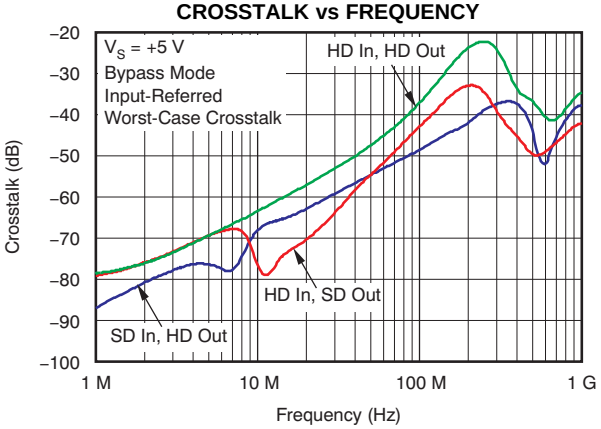


Figure 68.

CVBS CHANNEL SLEW RATE vs OUTPUT VOLTAGE

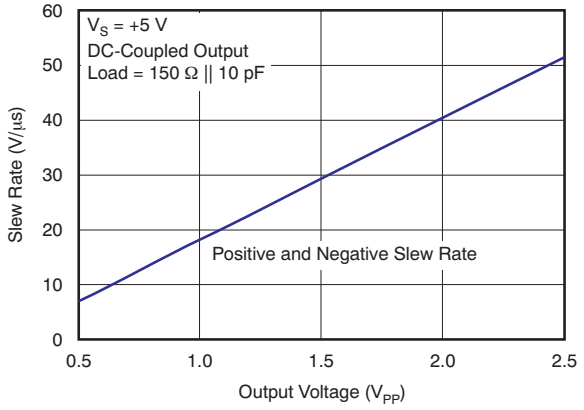


Figure 69.

CVBS CHANNEL DISABLE MODE RESPONSE vs TIME

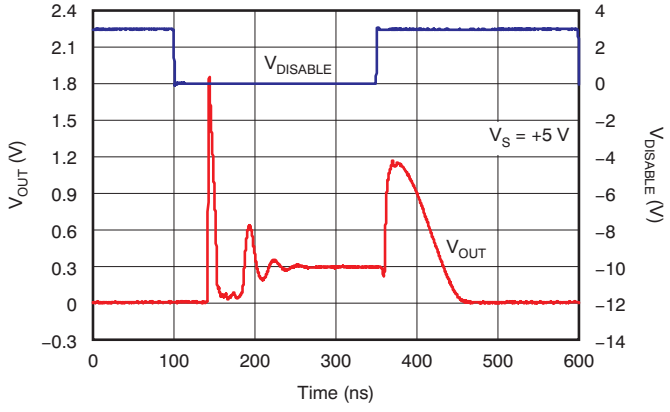


Figure 70.

TYPICAL CHARACTERISTICS: 5 V, Standard-Definition (CVBS) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

CVBS CHANNEL ATTENUATION AT 6.75 MHz vs TEMPERATURE

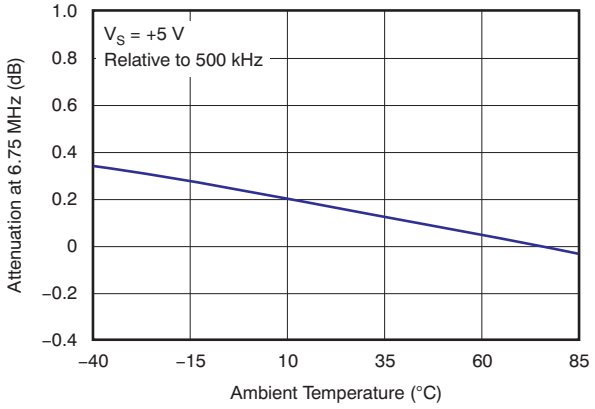


Figure 71.

CVBS CHANNEL ATTENUATION AT 27 MHz vs TEMPERATURE

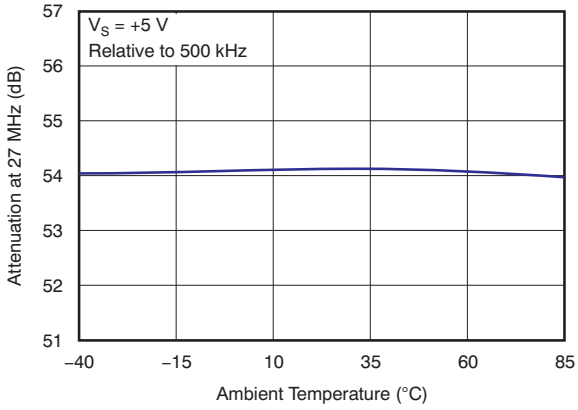


Figure 72.

OUTPUT OFFSET VOLTAGE vs TEMPERATURE

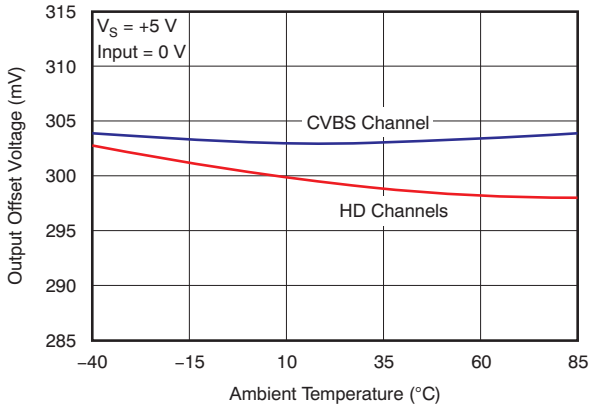


Figure 73.

TYPICAL CHARACTERISTICS: 5 V, High-Definition (HD) Channels

With load = 150 Ω || 5 pF, dc-coupled input and output, unless otherwise noted.

HD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY

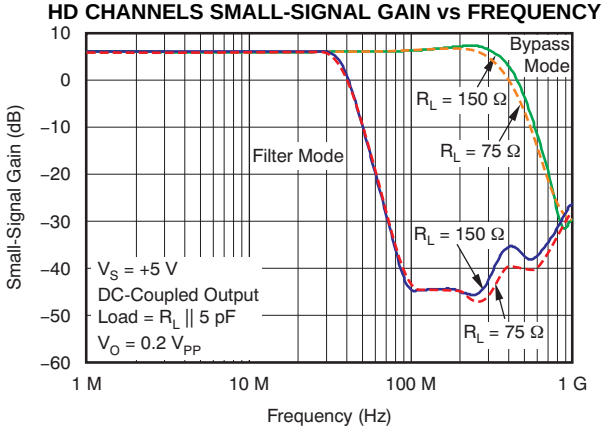


Figure 74.

HD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY

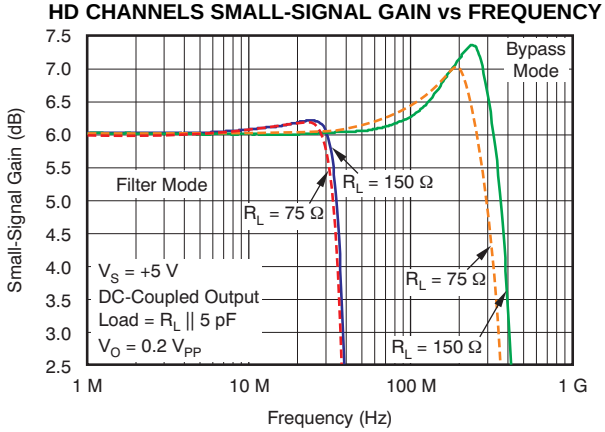


Figure 75.

HD CHANNELS LARGE-SIGNAL GAIN vs FREQUENCY

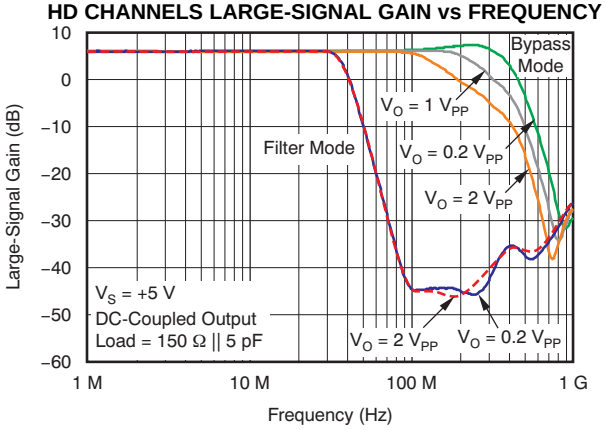


Figure 76.

HD CHANNELS LARGE-SIGNAL GAIN vs FREQUENCY

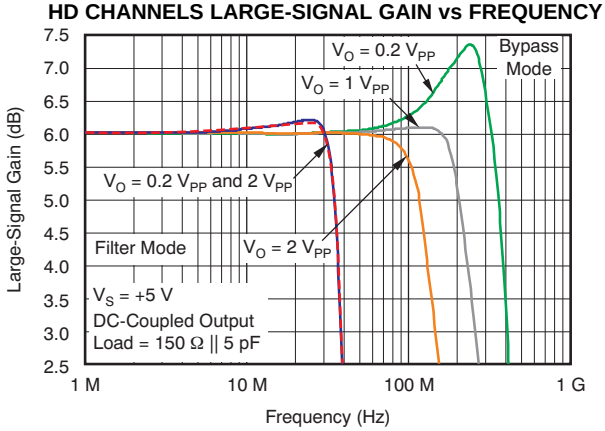


Figure 77.

HD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY

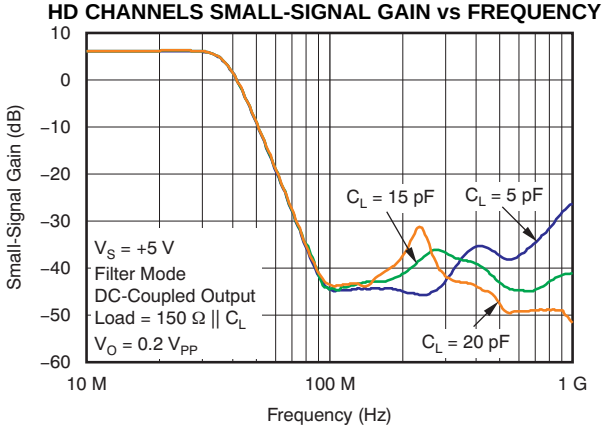


Figure 78.

HD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY

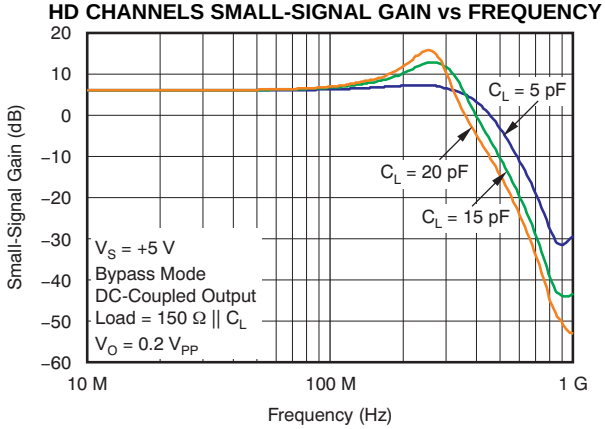


Figure 79.

TYPICAL CHARACTERISTICS: 5 V, High-Definition (HD) Channels (continued)

With load = 150 Ω || 5 pF, dc-coupled input and output, unless otherwise noted.

HD CHANNELS PHASE vs FREQUENCY

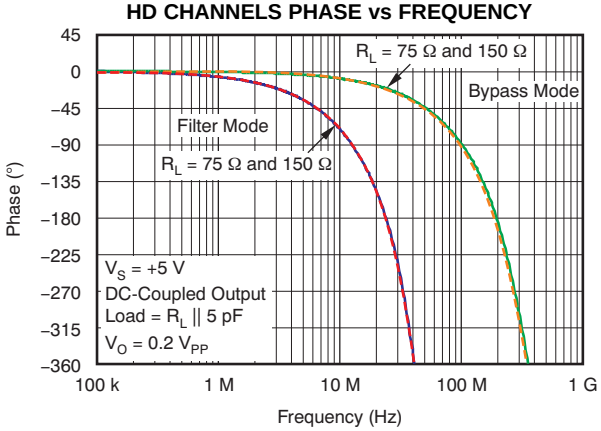


Figure 80.

HD CHANNELS GROUP DELAY vs FREQUENCY

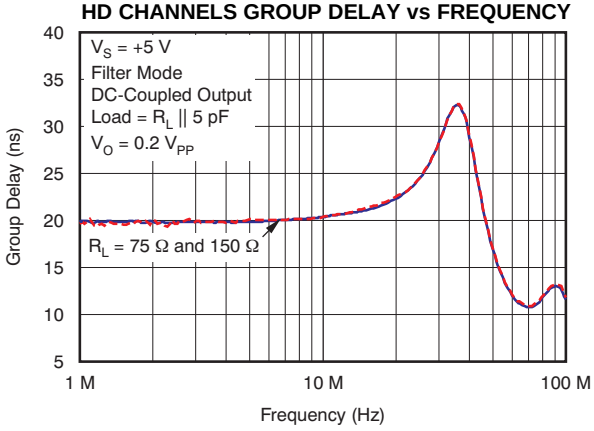


Figure 81.

HD CHANNELS PSRR vs FREQUENCY

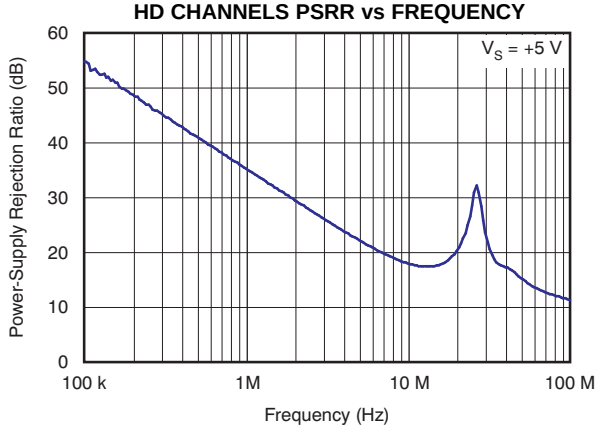


Figure 82.

HD CHANNELS SECOND-ORDER HARMONIC DISTORTION vs FREQUENCY

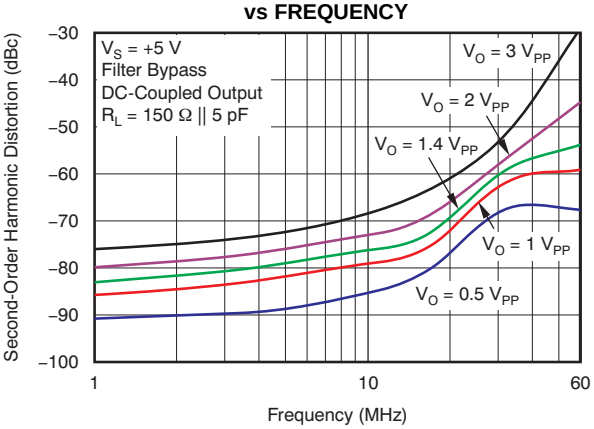


Figure 83.

HD CHANNELS THIRD-ORDER HARMONIC DISTORTION vs FREQUENCY

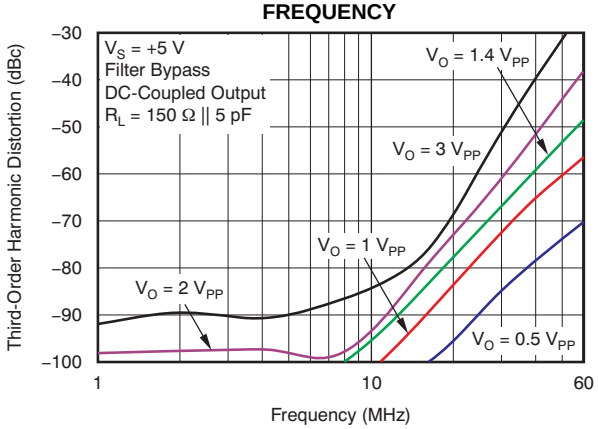


Figure 84.

HD CHANNELS SECOND-ORDER HARMONIC DISTORTION vs FREQUENCY

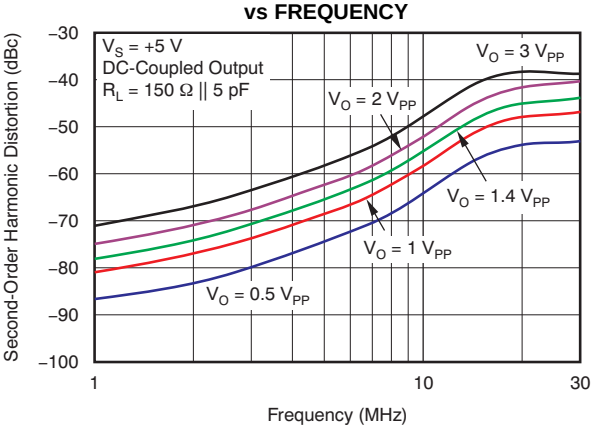


Figure 85.

TYPICAL CHARACTERISTICS: 5 V, High-Definition (HD) Channels (continued)

With load = 150 Ω || 5 pF, dc-coupled input and output, unless otherwise noted.

HD CHANNELS THIRD-ORDER HARMONIC DISTORTION vs FREQUENCY

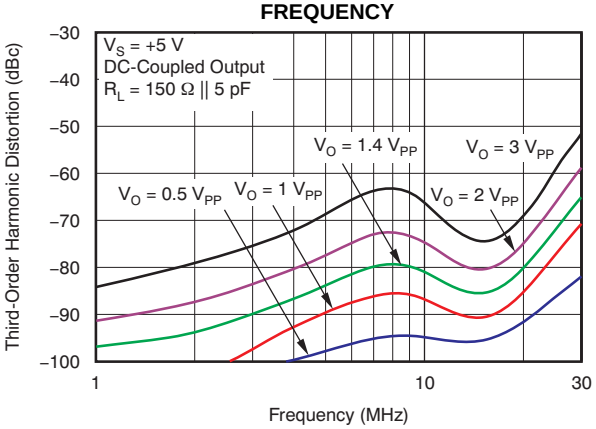


Figure 86.

HD CHANNELS SMALL-SIGNAL PULSE RESPONSE vs TIME

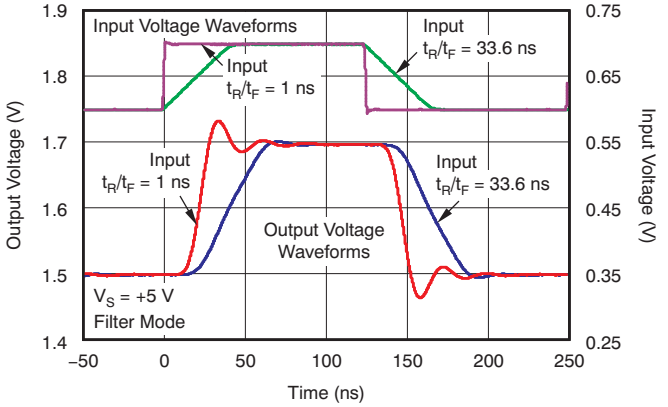


Figure 87.

HD CHANNELS LARGE-SIGNAL PULSE RESPONSE vs TIME

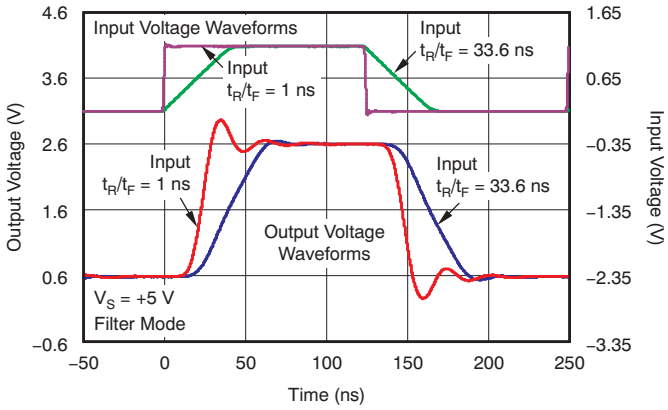


Figure 88.

HD CHANNELS SMALL-SIGNAL PULSE RESPONSE vs TIME

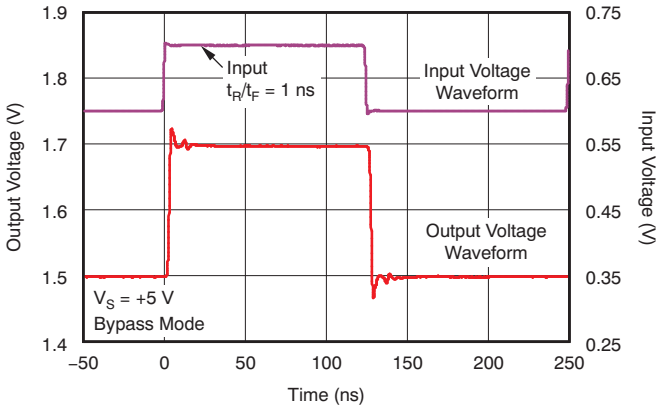


Figure 89.

HD CHANNELS LARGE-SIGNAL PULSE RESPONSE vs TIME

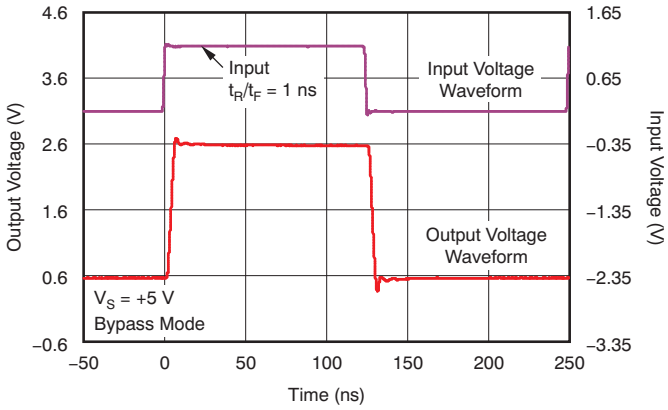


Figure 90.

HD CHANNELS SLEW RATE vs OUTPUT VOLTAGE

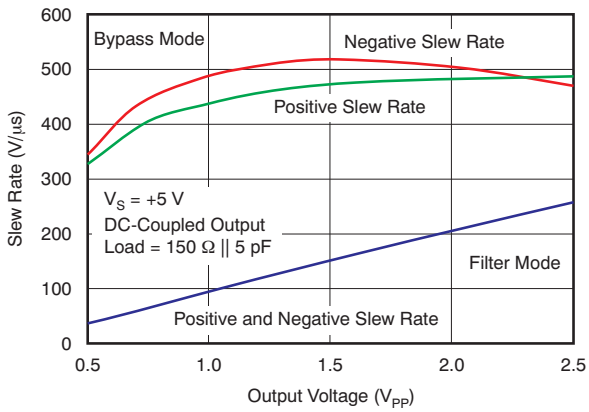


Figure 91.

TYPICAL CHARACTERISTICS: 5 V, High-Definition (HD) Channels (continued)

With load = 150 Ω || 5 pF, dc-coupled input and output, unless otherwise noted.

HD CHANNELS BYPASS MODE RESPONSE vs TIME

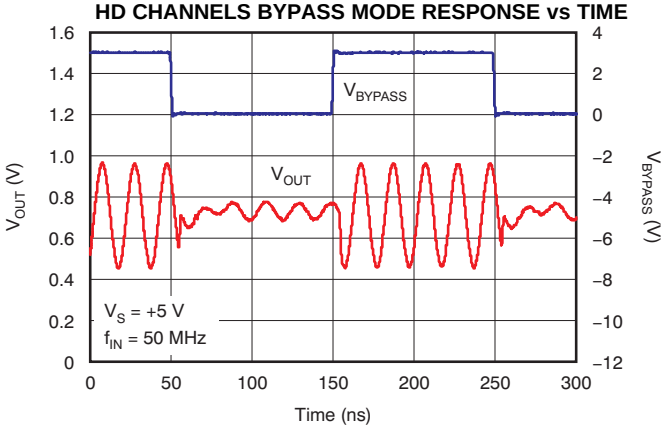


Figure 92.

HD CHANNELS DISABLE MODE RESPONSE vs TIME

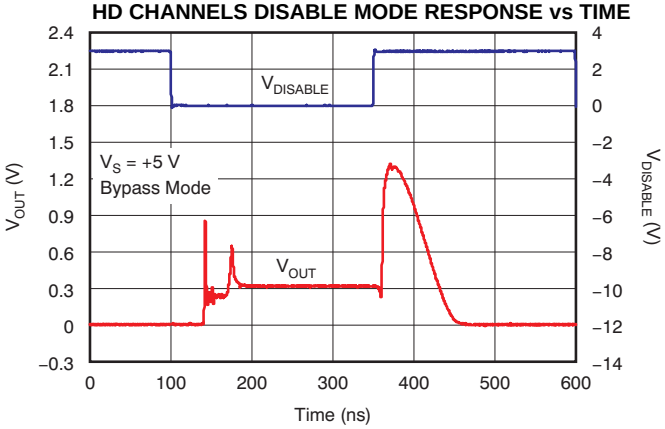


Figure 93.

HD CHANNEL DISABLE MODE RESPONSE vs TIME

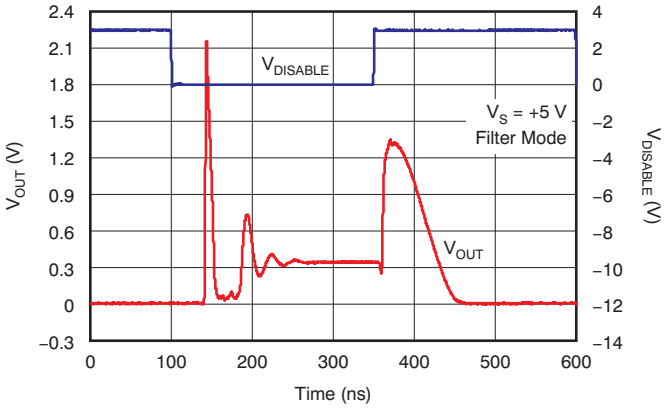


Figure 94.

HD CHANNELS ATTENUATION AT 27 MHz vs TEMPERATURE

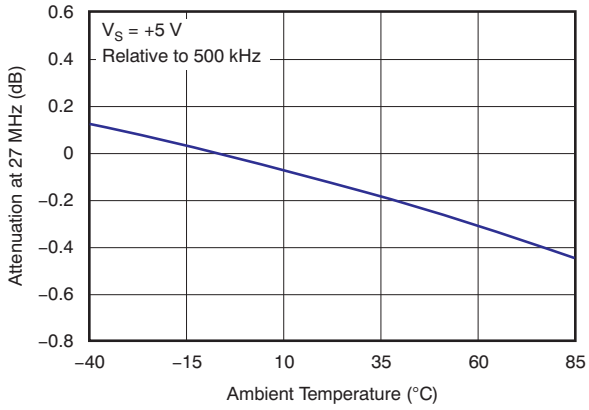


Figure 95.

HD CHANNELS ATTENUATION AT 74 MHz vs TEMPERATURE

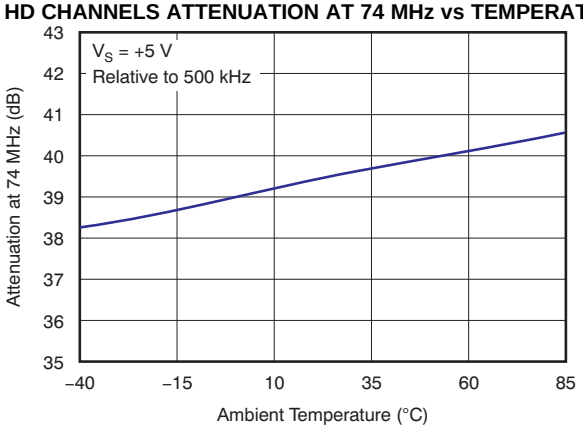


Figure 96.

APPLICATION INFORMATION

The THS7373 is targeted for systems that require a single standard-definition (CVBS) video output for CVBS video support along with three high-definition (HD) video outputs. Although it can be used for numerous other applications, the needs and requirements of the video signal are the most important design parameters of the THS7373. Built on the revolutionary, complementary Silicon Germanium (SiGe) BiCom3X process, the THS7373 incorporates many features not typically found in integrated video parts while consuming very low power. The THS7373 includes the following features:

- Single-supply 3-V to 5-V operation with low total quiescent current of 16.2 mA at 3.3 V and 16.9 mA at 5 V
- Disable mode allows for shutting down the THS7373 to save system power in power-sensitive applications
- Input configuration accepting dc + level shift, ac sync-tip clamp, or ac-bias:
  - Reduces quiescent current to as low as 0.1 µA
- Flexible input configurations allows for dc + level shift, ac sync-tip clamp, or ac-biasing:
  - AC-biasing is configured by use of an external pull-up resistor to the positive power supply
- Sixth-order, low-pass filter for DAC reconstruction or ADC image rejection:
  - 9.5 MHz for NTSC, PAL, or SECAM composite video baseband signal (CVBS)
  - 36 MHz for 720p, 1080i, or up to 1080p30 Y'/P'$_B$/P'$_R$ or G'B'R' signals
- HD bypass mode bypasses the HD low-pass filters for all three channels:
  - HD channels can support 1080p60 or QXGA video with 350-MHz and 450-V/µs performance
- Internal fixed gain of 2 V/V (+6 dB)
- Supports driving two video lines per channel with dc-coupling or traditional ac-coupling
- Flow-through configuration using a TSSOP-14 package that complies with the latest lead-free (RoHS-compatible) and green manufacturing requirements

OPERATING VOLTAGE

The THS7373 is designed to operate from 3 V to 5 V over the –40°C to +85°C temperature range. The impact on performance over the entire temperature range is negligible as a result of the implementation of thin film resistors and high-quality, low-temperature coefficient capacitors. The design of the THS7373 allows operation down to 2.6 V, but it is recommended to use at least a 3-V supply to ensure that no issues arise with headroom or clipping with 100% color-saturated CVBS signals.

A 0.1-µF capacitor should be placed as close as possible to the power-supply pins to avoid potential ringing or oscillations. Additionally, a large capacitor (such as 22 µF to 100 µF) should be placed on the power-supply line to minimize interference with 50-/60-Hz line frequencies.

INPUT VOLTAGE

The THS7373 input range allows for an input signal range from –0.4 V to approximately (V_{S+} – 1.5 V). However, because of the internal fixed gain of 2 V/V (+6 dB) and the internal output level shift of 300 mV, the output is generally the limiting factor for the allowable linear input range. For example, with a 5-V supply, the linear input range is from –0.4 V to 3.5 V. However, because of the gain and level shift, the linear output range limits the allowable linear input range to approximately –0.1 V to 2.3 V.

INPUT OVERVOLTAGE PROTECTION

The THS7373 is built using a very high-speed, complementary, bipolar, and CMOS process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All input and output device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 97.

These diodes provide moderate protection to input overdrive voltages above and below the supplies as well. The protection diodes can typically support 30 mA of continuous current when overdriven.

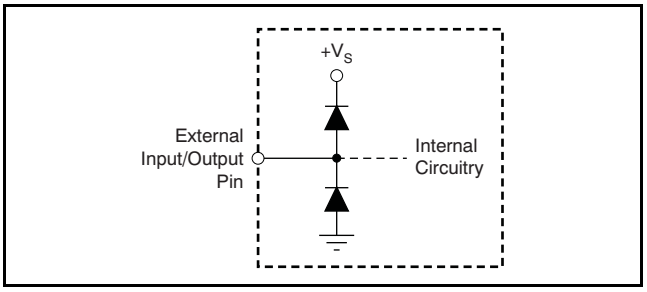


Figure 97. Internal ESD Protection

TYPICAL CONFIGURATION AND VIDEO TERMINOLOGY

A typical application circuit using the THS7373 as a video buffer is shown in Figure 98. It shows a DAC or encoder driving the input channels of the THS7373. One channel is a CVBS connection using the standard definition (CVBS) video filters. This signal can be an NTSC, PAL, or SECAM video signal. The other three channels are the component video Y'/P'$_B$/P'$_R$ (sometimes labeled Y'U'V' or incorrectly labeled Y'/C'$_B$/C'$_R$) video signals. These signals are typically 720p, 1080i, or up to 1080p30 signals. If the video DAC samples at greater than 74.25 MHz, then 480i/576i or 480p/576p signals are also supported while effectively minimizing DAC images. Because the HD filters can be bypassed, other formats such as 1080p60 (also known as Full-HD or True-HD) or computer R'G'B' resolutions up to QXGA can also be supported with the THS7373.

Note that the *Y'* term is used for the luma channels throughout this document rather than the more common luminance (*Y*) term. This usage accounts for the definition of luminance as stipulated by the International Commission on Illumination (CIE). Video departs from true luminance because a nonlinear term, *gamma*, is added to the true RGB signals to form R'G'B' signals. These R'G'B' signals are then used to mathematically create luma (Y'). Thus, luminance (Y) is not maintained, providing a difference in terminology.

This rationale is also used for the chroma (*C'*) term. Chroma is derived from the nonlinear R'G'B' terms and, thus, it is nonlinear. Chominance (*C*) is derived from linear RGB, giving the difference between chroma (C') and chrominance (C). The color difference signals (P'$_B$/P'$_R$/U'/V') are also referenced in this manner to denote the nonlinear (gamma corrected) signals.

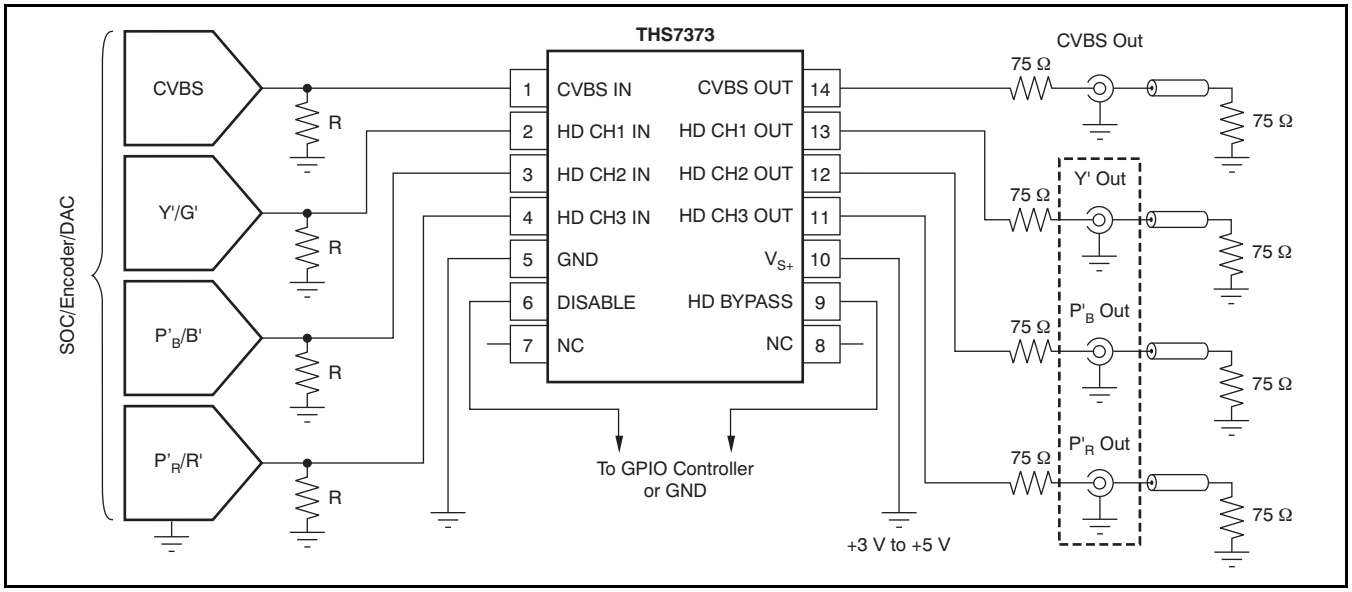


Figure 98. Typical Four-Channel System Inputs from DC-Coupled Encoder/DAC with DC-Coupled Line Driving

R'G'B' (commonly mislabeled *RGB*) is also called G'B'R' (again commonly mislabeled as *GBR*) in professional video systems. The Society of Motion Picture and Television Engineers (SMPTE) component standard stipulates that the luma information is placed on the first channel, the blue color difference is placed on the second channel, and the red color difference signal is placed on the third channel. This practice is consistent with the $Y'/P'_B/P'_R$ nomenclature. Because the luma channel (Y') carries the sync information and the green channel (G') also carries the sync information, it makes logical sense that G' be placed first in the system. Because the blue color difference channel (P'_B) is next and the red color difference channel (P'_R) is last, then it also makes logical sense to place the B' signal on the second channel and the R' signal on the third channel, respectfully. Thus, hardware compatibility is better achieved when using G'B'R' rather than R'G'B'. Note that for many G'B'R' systems, sync is embedded on all three channels, but this configuration may not always be the case in all systems.

INPUT MODE OF OPERATION: DC

The inputs to the THS7373 allow for both ac- and dc-coupled inputs. Many DACs or video encoders can be dc-connected to the THS7373. One of the drawbacks to dc-coupling is when 0 V is applied to the input. Although the input of the THS7373 allows for a 0-V input signal without issue, the output swing of a traditional amplifier cannot yield a 0-V signal, resulting in possible clipping. This limitation is true for any single-supply amplifier because of the characteristics of the output transistors. Neither CMOS nor bipolar transistors can achieve 0 V while sinking current. This transistor characteristic is also the same reason why the highest output voltage is always less than the power-supply voltage when sourcing current.

This output clipping can reduce the sync amplitudes (both horizontal and vertical sync) on the video signal. A problem occurs if the video signal receiver uses an automatic gain control (AGC) loop to account for losses in the transmission line. Some video AGC circuits derive gain from the horizontal sync amplitude. If clipping occurs on the sync amplitude, then the AGC circuit can increase the gain too much—resulting in too much luma and/or chroma amplitude gain correction. This correction may result in a picture with an overly bright display with too much color saturation.

Other AGC circuits use the chroma burst amplitude for amplitude control; reduction in the sync signals does not alter the proper gain setting. However, it is good engineering design practice to ensure that saturation/clipping does not take place. Transistors always take a finite amount of time to come out of saturation. This saturation could possibly result in timing delays or other aberrations in the signals.

To eliminate saturation or clipping problems, the THS7373 has a 150-mV input level shift feature. This feature takes the input voltage and adds an internal +150-mV shift to the signal. Because the THS7373 also has a gain of 6 dB (2 V/V), the resulting output with a 0-V applied input signal is approximately 300 mV. The THS7373 rail-to-rail output stage can create this output level while connected to a typical video load. This configuration ensures that no saturation or clipping of the sync signals occur. This shift is constant, regardless of the input signal. For example, if a 1-V input is applied, the output is 2.3 V.

Because the internal gain is fixed at +6 dB, the gain dictates what the allowable linear input voltage range can be without clipping concerns. For example, if the power supply is set to 3 V, the maximum output is approximately 2.9 V while driving a significant amount of current. Thus, to avoid clipping, the allowable input is ([2.9 V – 0.3 V]/2) = 1.3 V. This range is valid for up to the maximum recommended 5-V power supply that allows approximately a ([4.9 V – 0.3 V]/2) = 2.3 V input range while avoiding clipping on the output.

The input impedance of the THS7373 in this mode of operation is dictated by the internal, 800-kΩ pull-down resistor, as shown in Figure 99. Note that the internal voltage shift does not appear at the input pin; it only shows at the output pin.

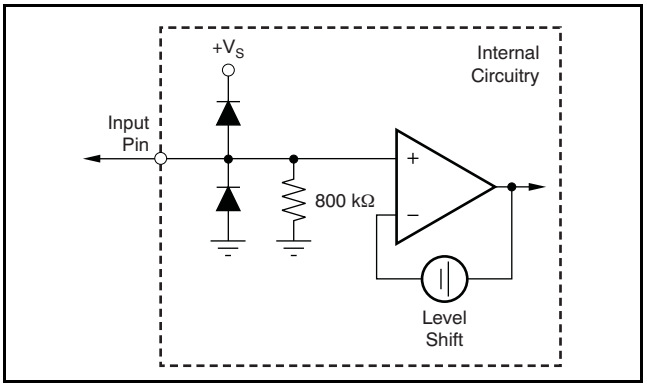


Figure 99. Equivalent DC Input Mode Circuit

INPUT MODE OF OPERATION: AC SYNC TIP CLAMP (STC)

Some video DACs or encoders are not referenced to ground but rather to the positive power supply. The resulting video signals are generally at too great a voltage for a dc-coupled video buffer to function properly. In other systems, the inputs may be connecting to an unknown source with unknown dc reference levels. To account for this scenario, the THS7373 incorporates a sync-tip clamp circuit. This function requires a capacitor (nominally 0.1 µF) to be in series with the input pin. Although the term *sync-tip-clamp* is used throughout this document, it should be noted that the THS7373 would probably be better termed as a *dc restoration circuit* based on how this function is performed. This circuit is an active clamp circuit and not a passive diode clamp function.

The input to the THS7373 has an internal control loop that sets the lowest input applied voltage to clamp at ground (0 V). By setting the reference at 0 V, the THS7373 allows a dc-coupled input to also function. Therefore, the sync-tip-clamp (STC) is considered transparent because it does not operate unless the input signal goes below ground. The signal then goes through the same 150-mV level shifter, resulting in an output voltage low level of 300 mV. If the input signal tries to go below 0 V, the internal control loop of the STC sources up to 6 mA of current to increase the input voltage level on the THS7373 input side of the coupling capacitor. As soon as the voltage goes above the 0-V level, the loop stops sourcing current and becomes very high impedance.

One of the concerns about the sync-tip-clamp level is how the clamp reacts to a sync edge that has overshoot—common in VCR signals or reflections found in poor printed circuit board (PCB) layouts. Ideally, the STC should not react to the overshoot voltage of the input signal. Otherwise, this response could result in clipping on the rest of the video signal because it may raise the bias voltage too much.

To help minimize this input signal overshoot problem, the control loop in the THS7373 has an internal low-pass filter, as shown in Figure 100. This filter reduces the response time of the STC circuit. This delay is a function of how far the voltage is below ground, but in general it is approximately an 800-ns delay for the 9.5-MHz filter and approximately a 250-ns delay for the 36-MHz filters. The effect of this filter is to slow down the response of the control loop so as not to clamp on the input overshoot voltage but rather the flat portion of the sync signal.

As a result of this delay, sync may have an apparent voltage shift. The amount of shift depends on the amount of droop in the signal as dictated by the input capacitor and the STC current flow. Because sync is used primarily for timing purposes with syncing occurring on the edge of the sync signal, this shift is transparent in most systems.

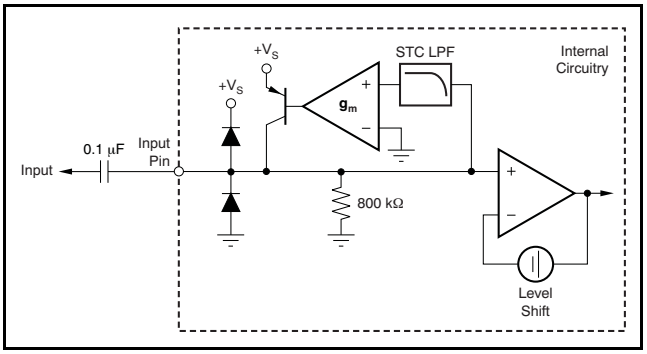


Figure 100. Equivalent AC Sync-Tip-Clamp Input Circuit

While this feature may not fully eliminate overshoot issues on the input signal, in cases of extreme overshoot and/or ringing, the STC system should help minimize improper clamping levels. As an additional method to help minimize this issue, an external capacitor (for example, 10 pF to 47 pF) to ground in parallel with the external termination resistors can help filter overshoot problems.

It should be noted that this STC system is dynamic and does not rely upon timing in any way. It only depends on the voltage that appears at the input pin at any given point in time. The STC filtering helps minimize level shift problems associated with switching noises or very short spikes on the signal line. This architecture helps ensure a very robust STC system.

When the ac STC operation is used, there must also be some finite amount of discharge bias current. As previously described, if the input signal goes below the 0-V clamp level, the internal loop of the THS7373 sources current to increase the voltage appearing at the input pin. As the difference between the signal level and the 0-V reference level increases, the amount of source current increases proportionally—supplying up to 6 mA of current. Thus, the time to re-establish the proper STC voltage can be very fast. If the difference is very small, then the source current is also very small to account for minor voltage droop.

However, what happens if the input signal goes above the 0-V input level? The problem is the video signal is always above this level and must not be altered in any way. Thus, if the sync level of the input signal is above this 0-V level, then the internal discharge (sink) current reduces the ac-coupled bias signal to the proper 0-V level.

This discharge current must not be large enough to alter the video signal appreciably or picture quality issues may arise. This effect is often seen by looking at the tilt (droop) of a constant luma signal being applied and the resulting output level. The associated change in luma level from the beginning and end of the video line is the amount of line tilt (droop).

If the discharge current is very small, the amount of tilt is very low, which is a generally a good thing. However, the amount of time for the system to capture the sync signal could be too long. This effect is also termed *hum rejection*. Hum arises from the ac line voltage frequency of 50 Hz or 60 Hz. The value of the discharge current and the ac-coupling capacitor combine to dictate the hum rejection and the amount of line tilt.

To allow for both dc- and ac-coupling in the same part, the THS7373 incorporates an 800-kΩ resistor to ground. Although a true constant current sink is generally preferred over a resistor, there can be issues when the voltage is near ground. This configuration can cause the current sink transistor to saturate and cause potential problems with the signal. The 800-kΩ resistor is large enough to not impact a dc-coupled DAC termination. For discharging an ac-coupled source, Ohm's Law is used. If the video signal is 1 V, then there is 1 V/800 kΩ = 1.25 µA of discharge current. If more hum rejection is desired or if a loss of sync occurs, then simply decrease the 0.1-µF input coupling capacitor. A decrease from 0.1 µF to 0.047 µF increases the hum rejection by a factor of 2.1. Alternatively, an external pull-down resistor to ground may be added that decreases the overall resistance and ultimately increases the discharge current.

To ensure proper stability of the ac STC control loop, the source impedance must be less than 1 kΩ with the input capacitor in place. Otherwise, there is a possibility of the control loop ringing, which may appear on the output of the THS7373. Because most DACs or encoders use resistors to establish the voltage, which are typically less than 300 Ω, meeting the less than 1 kΩ requirement is easily done. However, if the source impedance looking from the THS7373 input perspective is very high, then simply adding a 1-kΩ resistor to GND ensures proper operation of the THS7373.

The ac STC function is not recommended for ac-coupled component video $P'_B/P'_R/U'/V'$ signals. These signals either have no embedded sync or they have a mid-level sync. Using STC on these signals can cause clipping, saturation, or an apparent voltage shift in some video signals, such as 100% yellow for a few pixels in a video frame. For these signals and ac-input coupling, using the ac-bias mode is recommended.

INPUT MODE OF OPERATION: AC BIAS

Sync-tip clamps work very well for signals that have horizontal and/or vertical syncs associated with them; however, some video signals do not have a sync embedded within the signal. If ac-coupling of these signals is desired, then a dc bias is required to properly set the dc operating point within the THS7373. This function is easily accomplished with the THS7373 by simply adding an external pull-up resistor to the positive power supply, as shown in Figure 101.

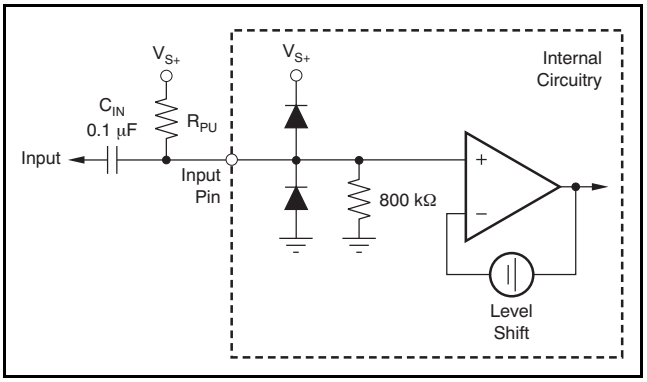


Figure 101. AC-Bias Input Mode Circuit Configuration

The dc voltage appearing at the input pin is equal to Equation 1:

$$V_{DC} = V_S \left(\frac{800\ k\Omega}{800\ k\Omega + R_{PU}} \right) \quad (1)$$

The THS7373 allowable input range is approximately 0 V to (V_{S+} – 1.5 V), allowing for a very wide input voltage range. As such, the input dc bias point is very flexible, with the output dc bias point being the primary factor. For example, if the output dc bias point is desired to be 1.6 V on a 3.3-V supply, then the input dc bias point should be (1.6 V – 300 mV)/2 = 0.65 V. Thus, the pull-up resistor calculates to approximately 3.3 MΩ, resulting in 0.644 V. If the output dc-bias point is desired to be 1.6 V with a 5-V power supply, then the pull-up resistor calculates to approximately 5.36 MΩ.

Keep in mind that the internal 800-kΩ resistor has approximately a ±20% variance. As such, the calculations should take this variance into account. For the 0.644-V example above, using an ideal 3.3-MΩ resistor, the input dc bias voltage is approximately 0.644 V ± 0.1 V.

The value of the output bias voltage is very flexible and is left to each individual design. It is important to ensure that the signal does not clip or saturate the video signal. Thus, it is recommended to ensure the output bias voltage is between 0.9 V and (V_{S+} – 1 V). For 100% color saturated CVBS or signals with Macrovision®, the CVBS signal can reach up to 1.23 V_{PP} at the input, or 2.46 V_{PP} at the output of the THS7373. In contrast, other signals are typically 1 V_{PP} or 0.7 V_{PP} at the input which translate to an output voltage of 2 V_{PP} or 1.4 V_{PP}. The output bias voltage must account for a worst-case situation, depending on the signals involved.

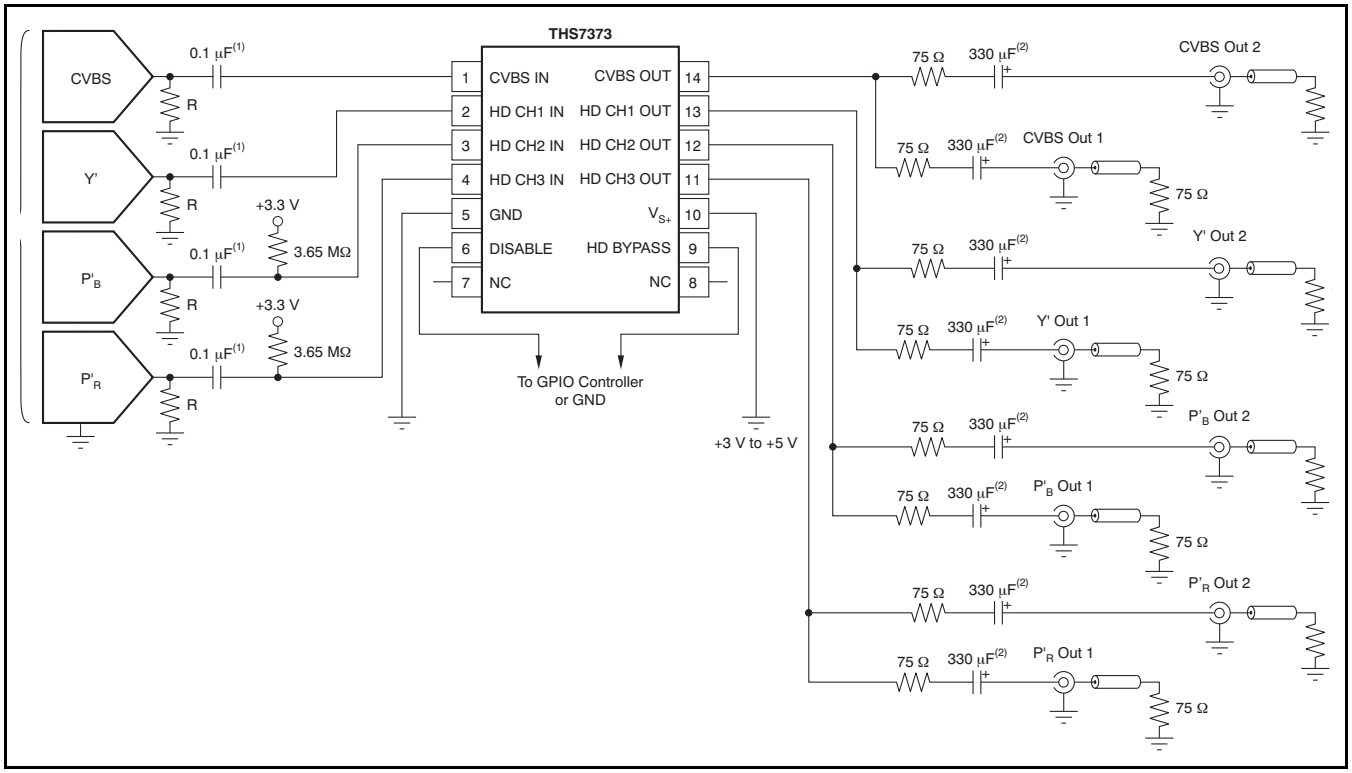
One other issue that must be taken into account is the dc-bias point is a function of the power supply. As such, there is an impact on system power-supply rejection ratio (PSRR). To help reduce this impact, the input capacitor combines with the pull-up resistance to function as a low-pass filter. Additionally, the time to charge the capacitor to the final dc bias point is a function of the pull-up resistor and the input capacitor. Lastly, the input capacitor forms a high-pass filter with the parallel impedance of the pull-up resistor and the 800-kΩ resistor. In general, it is good to have this high-pass filter at approximately 3 Hz to minimize any potential droop on a P'_B or P'_R signal. A 0.1-µF input capacitor with a 3.3-MΩ pull-up resistor equates to approximately a 2.5-Hz high-pass corner frequency.

AC biasing is recommended for use with component video P'_B, P'_R, U', or V' signals because these signals either have no embedded sync or the sync is a mid-level sync rather than a bottom-level sync. This method can also be used with sync signals if desired. The benefit of using the STC function is that it maintains a constant *back-porch* voltage as opposed to a back-porch voltage that fluctuates depending on the video content. Because the input corner frequency is a very low 2.5 Hz, the input corner frequency is also a very low 2.5 Hz, which is respectable (relative to a STC configuration).

OUTPUT MODE OF OPERATION: DC-COUPLED

The THS7373 incorporates a rail-to-rail output stage that can be used to drive the line directly without the need for large ac-coupling capacitors. This design offers the best line tilt and field tilt (droop) performance because no ac-coupling occurs. Keep in mind that if the input is ac-coupled, then the resulting tilt as a result of the input ac-coupling continues to be seen on the output, regardless of the output coupling.

The 80-mA output current drive capability of the THS7373 is designed to drive two video lines simultaneously per channel—essentially, a 75-Ω load—while keeping the output dynamic range as wide as possible. Figure 102 shows the THS7373 driving two video lines while keeping the output dc-coupled.



(1) This example shows an ac-coupled input. DC-coupling is also allowed as long as the DAC output voltage is within the allowable linear input and output voltage range of the THS7373. To achieve dc-coupling, remove the 0.1-µF input capacitors and the 3.65-MΩ pull-up resistors.

(2) This example shows ac-coupled outputs. DC-coupled outputs are also allowed by simply removing the series capacitors on each output.

Figure 102. Typical CVBS + Component Video System with AC-Coupled Inputs and Two Outputs Per Channel

One concern of dc-coupling arises, however, if the line is terminated to ground. If the ac-bias input configuration is used, the THS7373 output has a dc bias. With two lines terminated to ground, this configuration creates a dc current path that results in a slightly decreased high output voltage swing and an increase in power dissipation of the THS7373. While the THS7373 was designed to operate with a junction temperature of up to +125°C, care must be taken to ensure that the junction temperature does not exceed this level or else long-term reliability could suffer.

If the ac bias places 1.6 V on the output with two dc-coupled lines connected, then the output current flow without a signal is (1.6 V/75 Ω) = 21.3 mA per channel. With a 3.3-V supply, the power dissipation adds approximately [(3.3 V – 1.6 V) × 21.3 mA] = 36.2 mW per channel. With a 5-V power supply, this increases to 72.4 mW per channel. The overall low power dissipation of the THS7373 design minimizes potential thermal issues even when using the TSSOP package at high ambient temperatures. However, power and thermal analysis should always be examined in any system to ensure no issues arise. Be sure to use RMS power rather than instantaneous power when conducting thermal analysis.

Note that the THS7373 can drive the line with dc-coupling regardless of the input mode of operation. The only requirement is to make sure the video line has proper termination in series with the output (typically 75 Ω). This requirement helps isolate capacitive loading effects from the THS7373 output. Failure to properly isolate capacitive loads may result in ringing or oscillations. The stray capacitance appearing directly at the THS7373 output pins should be kept below 20 pF for the 9.5-MHz filter channels and below 15 pF for the 36-MHz filter channels. One way to help ensure this condition is satisfied is to make sure the 75-Ω source resistor is placed next to each THS7373 output pin. If a large ac-coupling capacitor is used, the capacitor should be placed after this resistor.

There are many reasons dc-coupling is desirable, including reduced system cost, PCB area, no line tilt, and no field tilt. A common question is whether or not there are any drawbacks to using dc-coupling. There are some potential issues that must be examined, such as the dc current bias as discussed above. Another potential risk is whether this configuration meets industry standards. EIA-770 stipulates that the back-porch shall be 0 V ± 1 V as measured at the receiver. With a double-terminated load system, this requirement implies a 0 V ± 2 V back-porch level at the video amplifier output. The THS7373 can easily meet this requirement without issue. However, in Japan, the EIAJ CP-1203 specification stipulates a 0 V ± 0.1 V level with no video signal. This requirement can be met with the THS7373 in shutdown mode, but while active it cannot meet this specification without output ac-coupling. AC-coupling the output essentially ensures that the video signal works with any system and any specification. For many modern systems, however, dc-coupling can satisfy most needs.

OUTPUT MODE OF OPERATION: AC-COUPLED

A very common method of coupling the video signal to the line is with a large capacitor. This capacitor is generally between 220 µF and 1000 µF, although 470 µF is very typical. The value of this capacitor must be large enough to minimize the line tilt (droop) and/or field tilt associated with ac-coupling as described previously in this document. AC-coupling is performed for several reasons, but the most common is to ensure full interoperability with the receiving video system. This approach ensures that regardless of the reference dc voltage used on the transmitting side, the receiving side re-establishes the dc reference voltage to its own requirements.

In the same way as the dc output mode of operation discussed previously, each line should have a 75-Ω source termination resistor in series with the ac-coupling capacitor. This resistor should be placed next to the THS7373 output to minimize stray capacitive effects. If two lines are to be driven, it is best to have each line use its own capacitor and resistor rather than sharing these components. This configuration helps ensure line-to-line dc isolation and eliminates the potential problems as described previously. Using a single, 1000-µF capacitor for two lines is permissible, but there is a chance for interference between the two receivers along with the capacitor potentially placing a capacitive load on the THS7373 output.

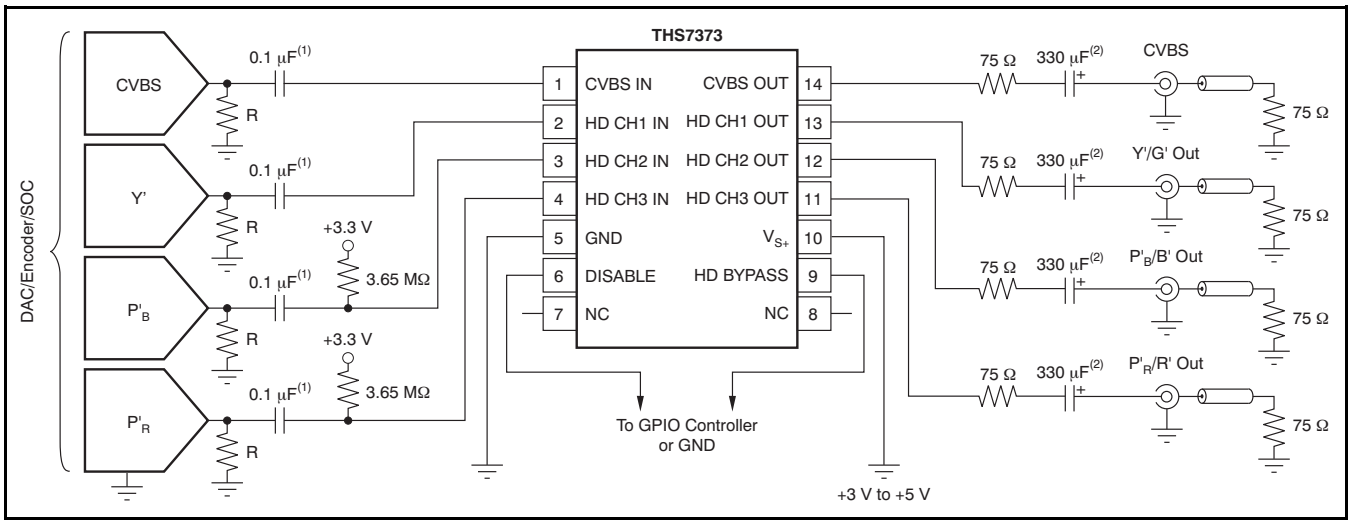
Lastly, because of the edge rates and frequencies of operation, it is recommended (but not required) to place a 0.1-µF to 0.01-µF capacitor in parallel with the large 220-µF to 1000-µF capacitor. These large value capacitors are most commonly aluminum electrolytic. It is well-known that these capacitors have significantly large equivalent series resistance (ESR), and the impedance at high frequencies is rather large as a result of the associated inductances involved with the leads and construction. The small 0.1-µF to 0.01-µF capacitors help pass these high-frequency signals (greater than 1 MHz) with much lower impedance than the large capacitors. Figure 103 shows a typical configuration where the input is dc-coupled and the output is also ac-coupled.

LOW-PASS FILTER

Each channel of the THS7373 incorporates a sixth-order, low-pass filter. These video reconstruction filters minimize DAC images from being passed onto the video receiver. Depending on the receiver design, failure to eliminate these DAC images can cause picture quality problems because of aliasing of the ADC. Another benefit of the filter is to smooth out aberrations in the signal that DACs typically have associated with the digital stepping of the signal. This benefit helps with picture quality and ensures that the signal meets video bandwidth requirements.

Each filter has an associated Butterworth characteristic. The benefit of the Butterworth response is that the frequency response is flat with a relatively steep initial attenuation at the corner frequency. The problem with this characteristic is that the group delay rises near the corner frequency. Group delay is defined as the change in phase (radians/second) divided by a change in frequency. An increase in group delay corresponds to a time domain pulse response that has overshoot and some possible ringing associated with the overshoot. The greater the variation in group delay, the greater the pulse response overshoot will be.

The use of other type of filters, such as elliptic or chebyshev, are not recommended for video applications because of the very large group delay variations near the corner frequency resulting in significant overshoot and ringing. While these filters may help meet the video standard specifications with respect to amplitude attenuation, the group delay is well beyond the standard specifications. Considering this delay with the fact that video can go from a white pixel to a black pixel over and over again, it is easy to see that ringing can occur. Ringing typically causes a display to have ghosting or fuzziness appear on the edges of a sharp transition. On the other hand, a Bessel filter has ideal group delay response, but the rate of attenuation is typically too low for acceptable image rejection. Thus, the Butterworth filter is a respectable compromise for both attenuation and group delay.



(1) This example shows an ac-coupled input. DC-coupling is also allowed as long as the DAC output voltage is within the allowable linear input and output voltage range of the THS7373. To achieve dc-coupling, remove the 0.1-µF input capacitors and the 3.65-MΩ pull-up resistors.

(2) This example shows ac-coupled outputs. DC-coupled outputs are also allowed by simply removing the series capacitors on each output.

Figure 103. Typical AC Input System Driving AC-Coupled Video Lines

The THS7373 CVBS CVBS filter has a nominal corner (–3 dB) frequency at 9.5-MHz and a –1-dB passband typically at 8.2 MHz. This 9.5-MHz filter is ideal for CVBS NTSC, PAL, and SECAM composite video (CVBS) signals. The 9.5-MHz, –3-dB corner frequency was designed to achieve 54 dB of attenuation at 27 MHz—a common sampling frequency between the DAC/ADC second and third Nyquist zones found in many video systems. This consideration is important because any signal that appears around this frequency can also appear in the baseband as a result of aliasing effects of an ADC found in a receiver.

The THS7373 HD filters have a nominal corner (–3-dB) frequency at 36MHz and a –1-dB passband typically at 33 MHz. This 36-MHz filter is ideal for HD 720p, 1080i, up to 1080p30 Y'/P'_B/P'_R, broadcast G'B'R' signals, and computer R'G'B' video signals. The 36-MHz, –3-dB corner frequency was designed to achieve 40 dB of attenuation at 74.25 MHz—a common sampling frequency between the DAC/ADC second and third Nyquist zones found in many video systems.

Keep in mind that images do not stop at the DAC sampling frequency, f_S (for example, 27 MHz for traditional CVBS DACs); they continue around the sampling frequencies of 2x f_S, 3x f_S, 4x f_S, and so on (that is, 54-MHz, 81-MHz, 108-MHz, etc.). Because of these multiple images, an ADC can fold down into the baseband signal, meaning that the low-pass filter must also eliminate these higher-order images. The THS7373 filters are Butterworth filters and, as such, do not *bounce* at higher frequencies, thus maintaining good attenuation performance.

The filter frequencies were chosen to account for process variations in the THS7373. To ensure the required video frequencies are effectively passed, the filter corner frequency must be high enough to allow component variations. The other consideration is that the attenuation must be large enough to ensure the anti-aliasing/reconstruction filtering is sufficient to meet the system demands. Thus, the selection of the filter frequencies was not arbitrarily selected and is a good compromise that should meet the demands of most systems.

HD FILTER BYPASS MODE

The THS7373 has an HD filter bypass mode that bypasses the HD channels internal filters, thus the THS7373 effectively becomes a fixed gain 2-V/V operational amplifier. Bypassing the HD filters results in an amplifier supporting a 350-MHz bandwidth and 450-V/µs slew rate. This bypass supports 1080p60 signals along with computer R'G'B' signals up to QXGA or UWXGA resolution. This mode still uses the dc + shift functionality along with the transparent sync-tip-clamp function. Essentially, the only difference in this mode is that the HD filters are bypassed.

BENEFITS OVER PASSIVE FILTERING

Two key benefits of using an integrated filter system, such as the THS7373, over a passive system are PCB area and filter variations. The small TSSOP-14 package for four video channels is much smaller over a passive RLC network, especially a six-pole passive network. Additionally, consider that inductors have at best ±10% tolerances (normally, ±15% to ±20% is common) and capacitors typically have ±10% tolerances. Using a Monte Carlo analysis shows that the filter corner frequency (–3 dB), flatness (–1 dB), Q factor (or peaking), and channel-to-channel delay have wide variations. These variances can lead to potential performance and quality issues in mass-production environments. The THS7373 solves most of these problems with the corner frequency being essentially the only variable.

Another concern about passive filters is the use of inductors. Inductors are magnetic components, and are therefore susceptible to electromagnetic coupling/interference (EMC/EMI). Some common coupling can occur because of other video channels nearby using inductors for filtering, or it can come from nearby switched-mode power supplies. Some other forms of coupling could be from outside sources with strong EMI radiation and can cause failure in EMC testing such as required for CE compliance.

One concern about an active filter in an integrated circuit is the variation of the filter characteristics when the ambient temperature and the subsequent die temperature change. To minimize temperature effects, the THS7373 uses low-temperature coefficient resistors and high-quality, low-temperature coefficient capacitors found in the BiCom3X process. These filters have been specified by design to account for process variations and temperature variations to maintain proper filter characteristics. This approach maintains a low channel-to-channel time delay that is required for proper video signal performance.

Another benefit of the THS7373 over a passive RLC filter is the input and output impedance. The input impedance presented to the DAC varies significantly, from 35 Ω to over 1.5 kΩ with a passive network, and may cause voltage variations over frequency. The THS7373 input impedance is 800 kΩ, and only the 2-pF input capacitance plus the PCB trace capacitance impact the input impedance. As such, the voltage variation appearing at the DAC output is better controlled with a fixed termination resistor and the high input impedance buffer of the THS7373.

On the output side of the filter, a passive filter again has a large impedance variation over frequency. EIA770 specifications require the return loss to be at least 25 dB over the video frequency range of usage. For a video system, this requirement implies that the source impedance (which includes the source, series resistor, and the filter) must be better than 75 Ω, +9/–8 Ω. The THS7373 is an operational amplifier that approximates an ideal voltage source, which is desirable because the output impedance is very low and can source and sink current. To properly match the transmission line characteristic impedance of a video line, a 75-Ω series resistor is placed on the output. To minimize reflections and to maintain a good return loss meeting EIA specifications, this output impedance must maintain a 75-Ω impedance. A passive filter impedance variation cannot ensure this level of performance. On the other hand, the THS7373 has approximately 0.8 Ω of output impedance at 6.75 MHz for the 9.5-MHz filter and approximately 1.4 Ω of output impedance at 30 MHz for the 36-MHz filters. Thus, the system is matched significantly better with a THS7373 compared to a passive filter.

One final benefit of the THS7373 over a passive filter is power dissipation. A DAC driving a video line must be able to drive a 37.5-Ω load: the receiver 75-Ω resistor and the 75-Ω impedance matching resistor next to the DAC to maintain the source impedance requirement. This requirement forces the DAC to drive at least 1.25 V_P (100% saturation CVBS)/37.5 Ω = 33.3 mA. A DAC is a current-steering element, and this amount of current flows internally to the DAC even if the output is 0 V. Thus, power dissipation in the DAC may be very high, especially when six channels are being driven. Using the THS7373 with a high input impedance and the capability to drive up to two video lines per channel can reduce DAC power dissipation significantly. This outcome is possible because the resistance that the DAC drives can be substantially increased. It is common to set this resistance in a DAC by a current-setting resistor on the DAC itself. Thus, the resistance can be 300 Ω or more, substantially reducing the current drive demands from the DAC and saving significant amounts of power. For example, a 3.3-V, four-channel DAC dissipates 440 mW alone for the steering current capability (four channels × 33.3 mA × 3.3 V) if it must drive a 37.5-Ω load. With a 300-Ω load, the DAC power dissipation as a result of current steering current would only be 55 mW (four channels × 4.16 mA × 3.3 V).

EVALUATION MODULE

To evaluate the THS7373, an evaluation module (EVM) is available. The THS7373EVM allows for testing the THS7373 in many different configurations. Inputs and outputs include BNC connectors commonly found in video systems, along with 75-Ω input termination resistors, 75-Ω series source termination resistors, and 75-Ω characteristic impedance traces. Several unpopulated component pads are found on the EVM to allow for different input and output configurations as dictated by the user. This EVM is designed to be used with a single supply from 2.6 V up to 5 V.

The EVM default input configuration sets all channels for dc input coupling. The input signal must be within 0 V to approximately 1.4 V for proper operation. Failure to be within this range saturates and/or clips the output signal. If the input range is beyond this, if the signal voltage is unknown, or if coming from a current sink DAC, then ac input configuration is desired. This option is easily accomplished with the EVM by simply replacing the Z_1 through Z_4 0-Ω resistors with 0.1-µF capacitors.

For an ac-coupled input and sync-tip clamp (STC) functionality commonly used for CVBS, s-video Y', component Y' signals, and R'G'B' signals, no other changes are needed. However, if a bias voltage is needed after the input capacitor which is commonly needed for s-video C', component P'_B and P'_R signals, then a pull-up resistor should be added to the signal on the EVM. This configuration is easily achieved by simply adding a resistor to any of the following resistor pads: RX1, RX3, RX5, or RX7. A common value to use is 3.3 MΩ. Note that even signals with embedded sync can also use bias mode if desired.

The EVM default output configuration sets all channels for ac output coupling. The 470-µF and 0.1-µF capacitors work well for most ac-coupled systems. However, if dc-coupled output is desired, then replacing the 0.1-µF capacitors (C12, C14, C16, and/or C17) with 0-Ω resistors works well. Removing the 470-µF capacitors is optional, but removing them from the EVM eliminates a few picofarads of stray capacitance on each signal path which may be desirable.

The THS7373 incorporates an easy method to configure the bypass mode and the disable mode. The use of JP1 controls the disable feature and JP4 controls the HD channels filter/bypass mode. While there is a space on the EVM for JP2 and JP3, these are not used for the THS7373.

Connection of JP1 to GND applies 0 V to the disable pin and the THS7373 operates normally. Moving JP1 to $+V_S$ causes all channels of the THS7373 to be in disable mode.

Connection of JP4 to GND places the THS7373 HD channels in filter mode while moving JP4 to $+V_S$ places the THS7373 HD channels in bypass mode.

The THS7373EVM also includes a method to improve the ESD performance of all the analog inputs and outputs beyond the ratings shown in the Absolute Maximum Ratings table. By using very low cost BAV99 diodes, the EVM has the ability to pass IEC ±8kV surge testing. Another common protection diode commonly utilized is the BAT54S which also achieves the same surge suppression performance as the BAV99 diodes.

Figure 104 shows the THS7373EVM schematic. Figure 105 and Figure 106 illustrate the two layers of the EVM PCB, incorporating standard high-speed layout practices. Table 6 lists the bill of materials as the board comes supplied from Texas Instruments.

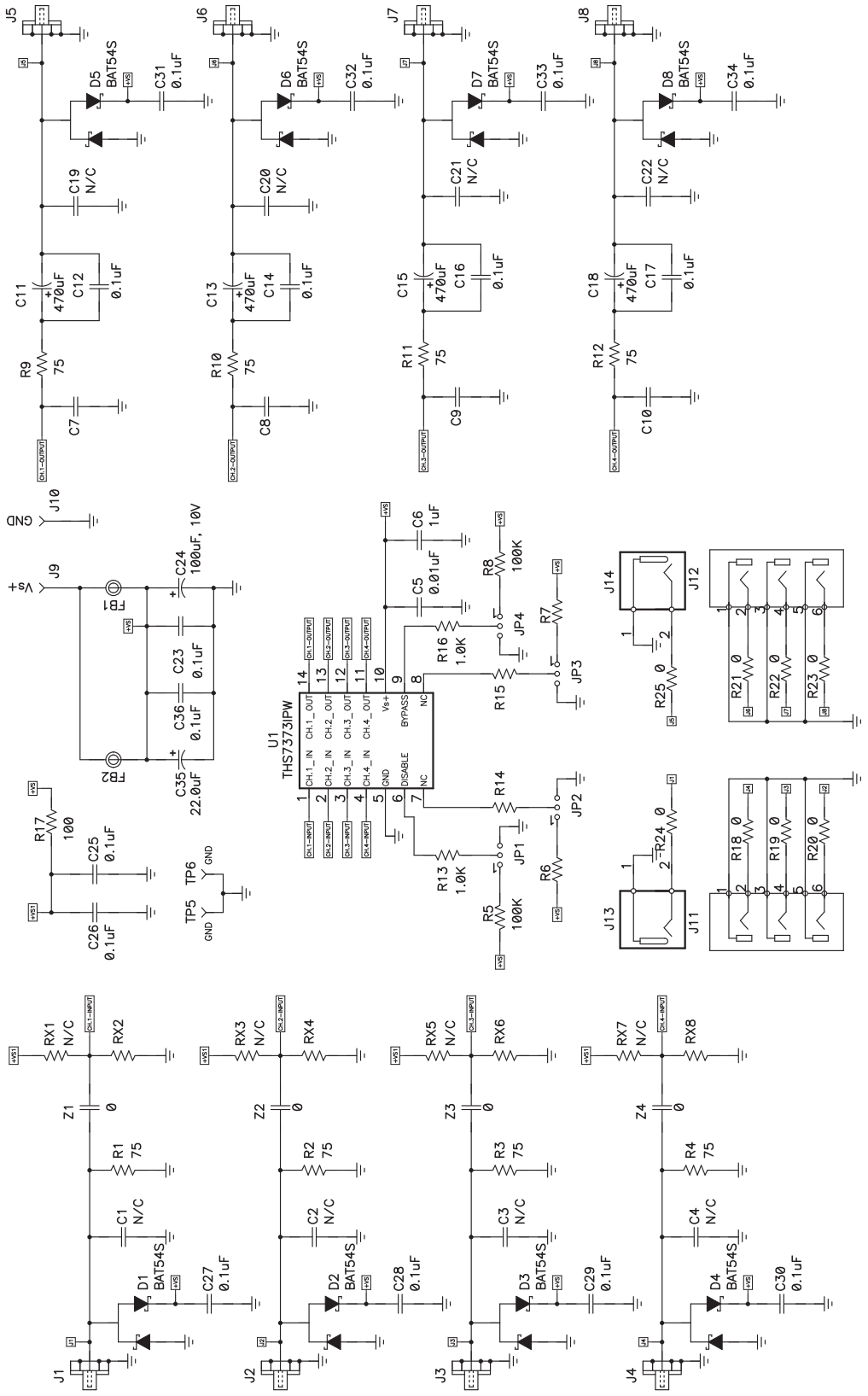


Figure 104. THS7373EVM Schematic

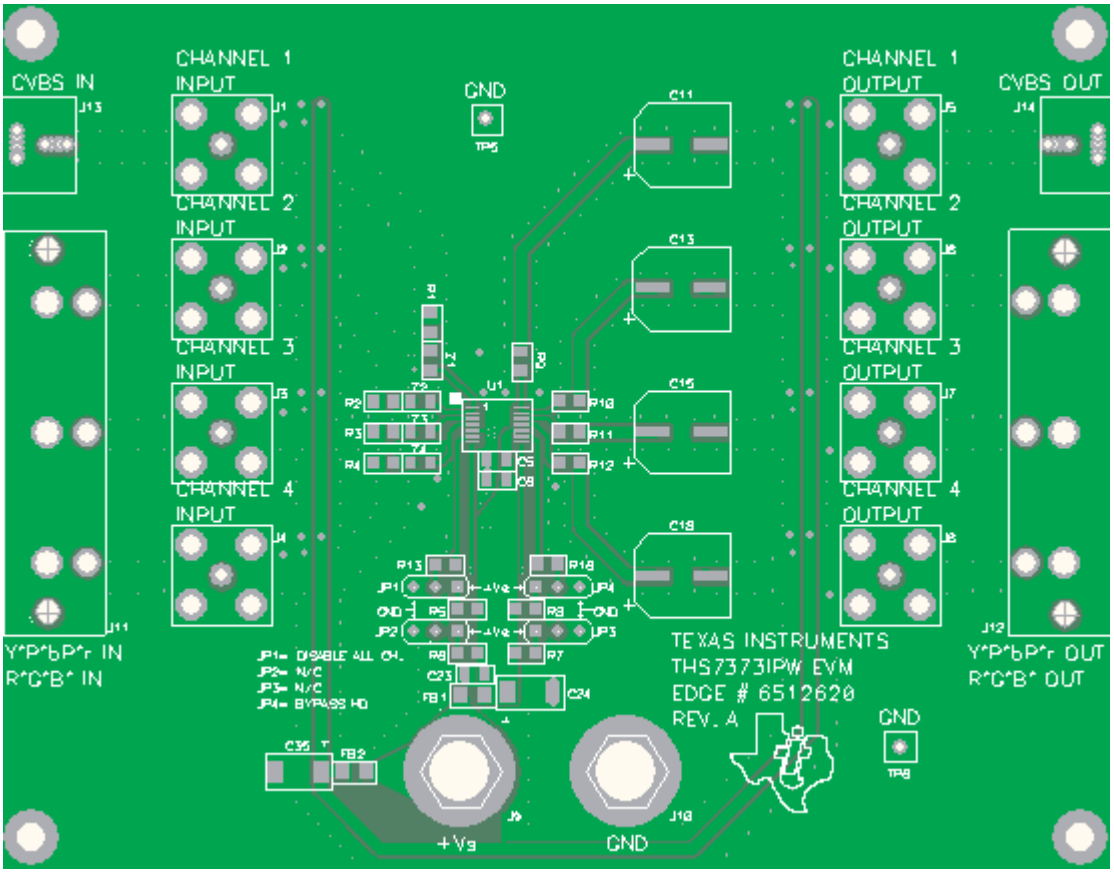


Figure 105. THS7373EVM PCB Top Layer

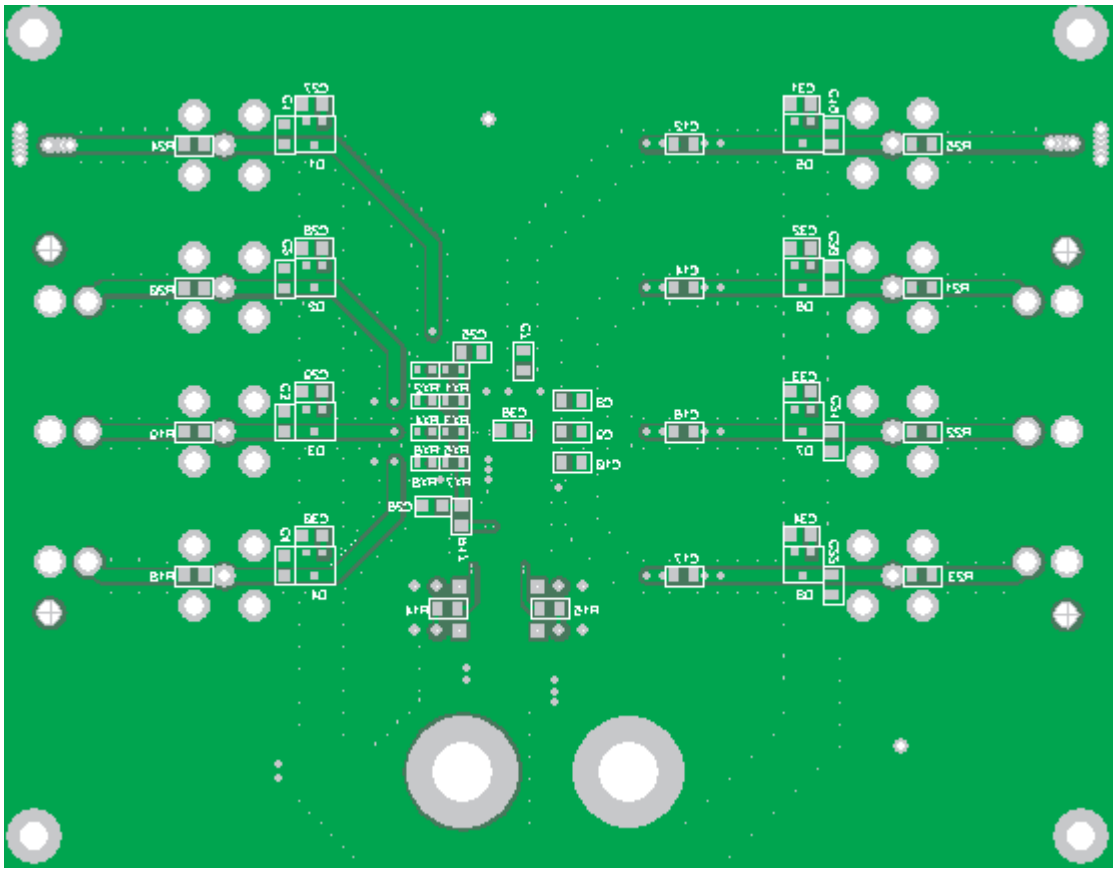


Figure 106. THS7373EVM PCB Bottom Layer

THS7373EVM Bill of Materials

Table 6. THS7373EVM

ITEM	REF DES	QTY	DESCRIPTION	SMD SIZE	MANUFACTURER PART NUMBER	DISTRIBUTOR PART NUMBER
1	FB1, FB2	2	Bead, ferrite, 2.5A, 330 Ω	0805	(TDK) MPZ2012S331A	(DIGI-KEY) 445-1569-1-ND
2	C24	1	Capacitor, 100 µF, tantalum, 10V, 10%, low ESR	C	(AVX) TPSC107K010R0100	(DIGI-KEY) 478-1765-1-ND
3	C35	1	Capacitor, 22 µF, tantalum, 16V, 10%, low ESR	C	(AVX) TPSC226K016R0375	(DIGI-KEY) 478-1767-1-ND
4	C1-C4, C7-C10, C19-C22	12	Open	0805		
5	C5	1	Capacitor, 0.01 µF, ceramic, 100V, X7R	0805	(AVX) 08051C103KAT2A	(DIGI-KEY) 478-1358-1-ND
6	C12, C14, C16, C17, C23, C25-C34, C36	16	Capacitor, 0.1 µF, ceramic, 50V, X7R	0805	(AVX) 08055C104KAT2A	(DIGI-KEY) 478-1395-1-ND
7	C6	1	Capacitor, 1 µF, ceramic, 16V, X7R	0805	(TDK) C2012X7R1C105K	(DIGI-KEY) 445-1358-1-ND
8	C11, C13, C15, C18	4	Capacitor, aluminum, 470 µF, 10V, 20%	F	(PANASONIC) EEE-FP1A471AP	(DIGI-KEY) PCE4526CT-ND
9	RX1-RX8	8	Open	0603		
10	R6, R7, R14, R15	4	Open	0805		
11	Z1-Z4, R18-R25	12	Resistor, 0 Ω	0805	(ROHM) MCR10EZHJ000	(DIGI-KEY) RHM0.0ACT-ND
12	R1-R4, R9-R12	8	Resistor, 75 Ω, 1/8W, 1%	0805	(ROHM) MCR10EZHF75.0	(DIGI-KEY) RHM75.0CCT-ND
13	R17	1	Resistor, 100 Ω, 1/8W, 1%	0805	(ROHM) MCR10EZHF1000	(DIGI-KEY) RHM100CCT-ND
14	R13, R16	2	Resistor, 1k Ω, 1/8W, 1%	0805	(ROHM) MCR10EZHF1001	(DIGI-KEY) RHM1.00KCCT-ND
15	R5, R8	2	Resistor, 100k Ω, 1/8W, 1%	0805	(ROHM) MCR10EZHF1003	(DIGI-KEY) RHM100KCCT-ND
16	D1-D8	8	Diode, ultrafast		(FAIRCHILD) BAV99	(DIGI-KEY) BAV99FSCT-ND
17	J9, J10	2	Jack, banana receptance, 0.25" diameter hole		(SPC) 813	(NEWARK) 39N867
18	J1-J8	8	Connector, BNC, jack, 75 Ω		(AMPHENOL) 31-5329-72RFX	(NEWARK) 93F7554
19	J13, J14	2	Connector, RCA jack, yellow		(CUI) RCJ-044	(DIGI-KEY) CP-1421-ND
20	J11, J12	2	Connector, RCA, jack, R/A		(CUI) RCJ-32265	(DIGI-KEY) CP-1446-ND
21	TP5, TP6	2	Test point, black		(KEYSTONE) 5001	(DIGI-KEY) 5001K-ND
22	JP2, JP3	2	Open	3 pos.		
23	JP1, JP4	2	Header, 0.1" CTRS, 0.025" square pins	3 pos.	(SULLINS) PBC36SAAN	(DIGI-KEY) S1011E-36-ND
24	JP1, JP4	2	Shunts		(SULLINS) SSC02SYAN	(DIGI-KEY) S9002-ND
25	U1	1	IC, THS7373	PW	(TI) THS7373IPW	
26	—	4	Standoff, 4-40 hex, 0.625" length		(KEYSTONE) 1808	(DIGI-KEY) 1808K-ND
27	—	4	Screw, Phillips, 4-40, 0.250"		(BF) PMS 440 0031 PH	(DIGI-KEY) H343-ND
28	—	1	Board, printed circuit		EDGE # 6512620 Rev.A	

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2009) to Revision A	Page
• Changed *Supply Voltage* parameter maximum specification in Recommended Operating Conditions table	2

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.6 V to 5.5 V single-supply and the output voltage range of 0 V to 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS7373IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7373	Samples
THS7373IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7373	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

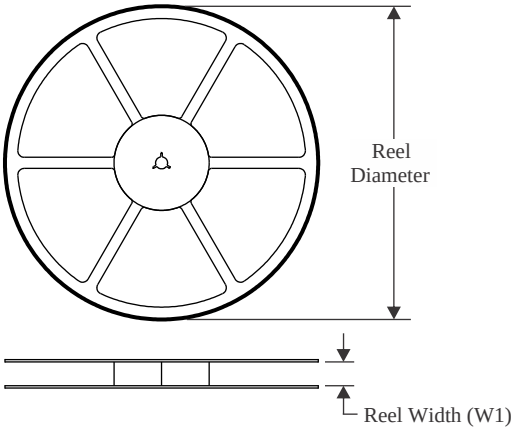
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

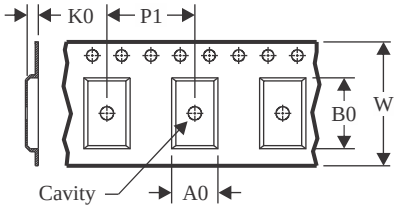
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

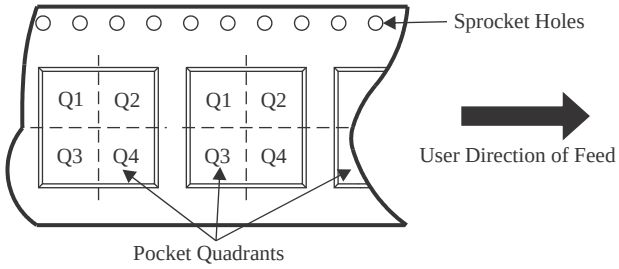


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

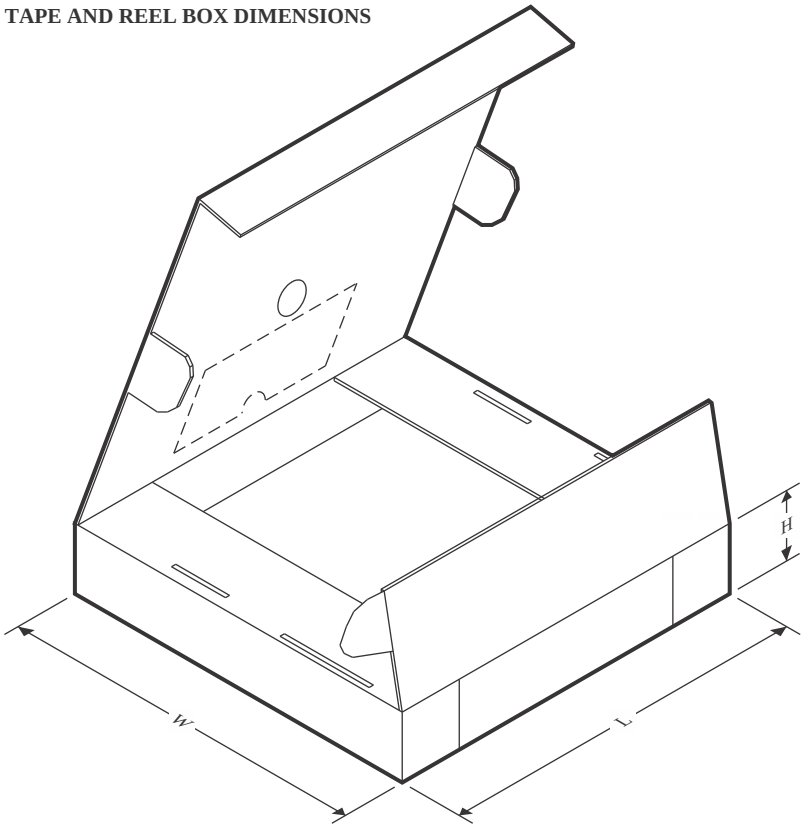
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7373IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

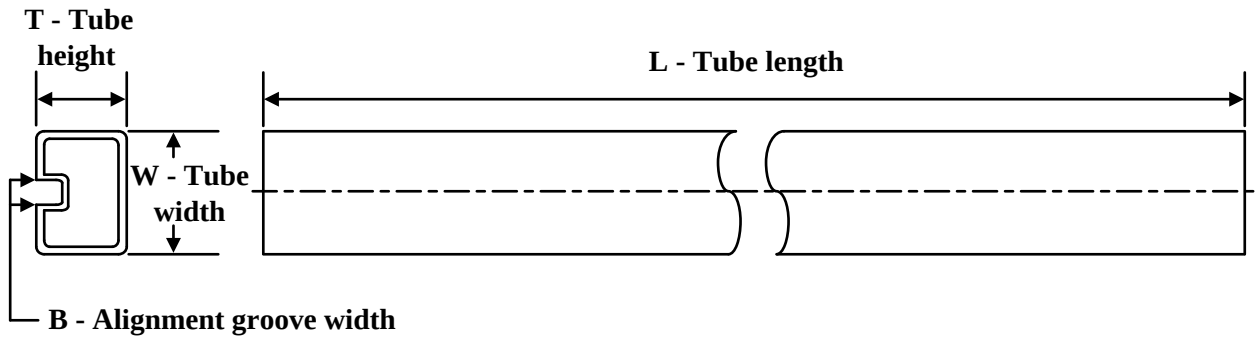
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS7373IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

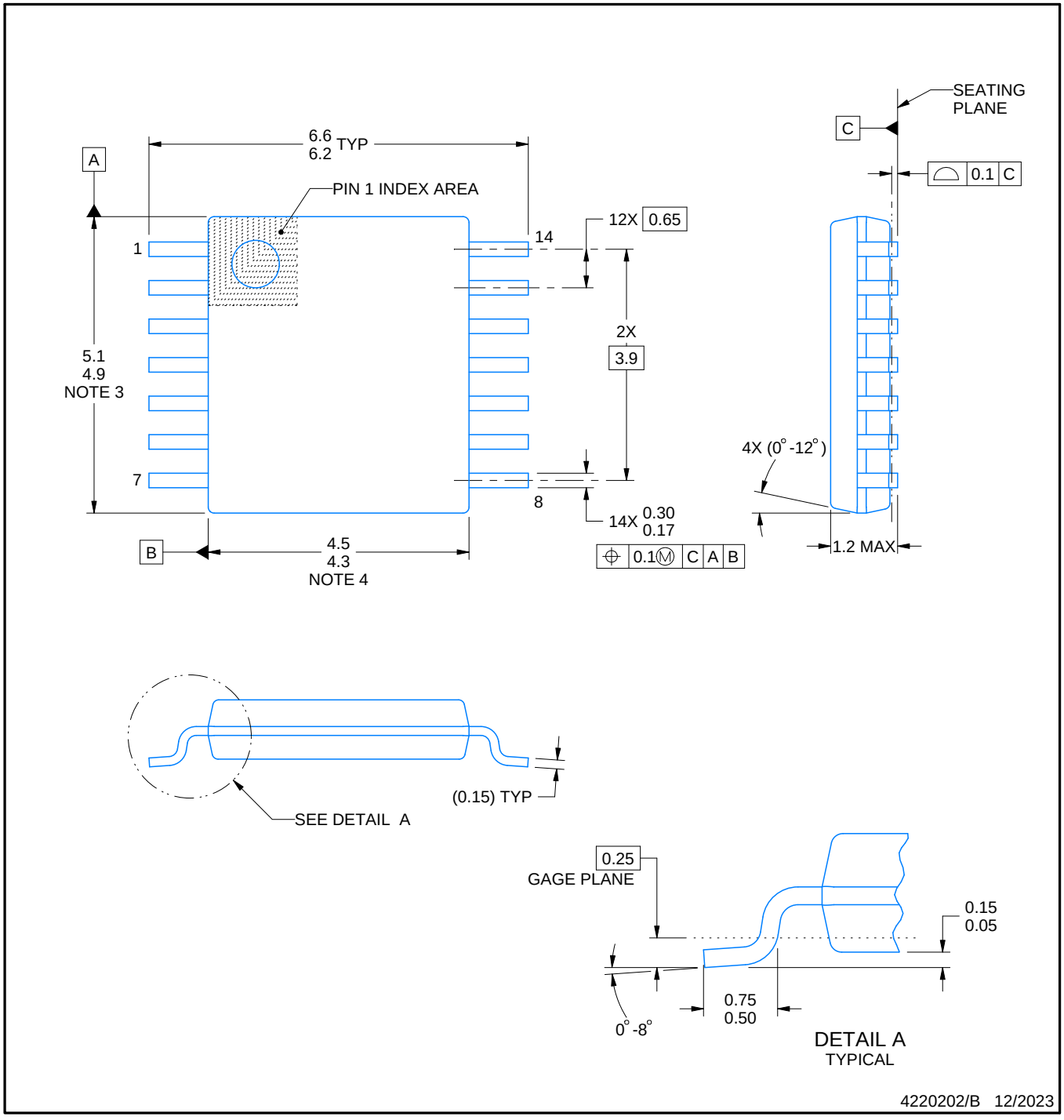
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS7373IPW	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0014A

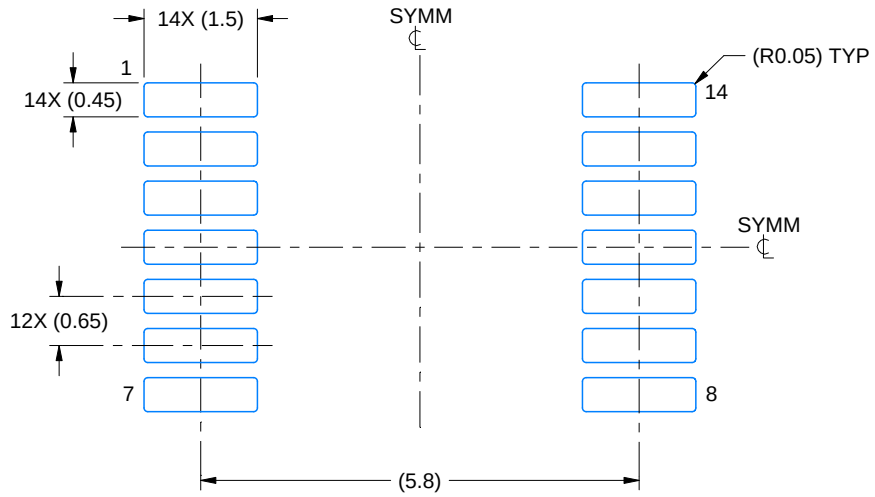
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

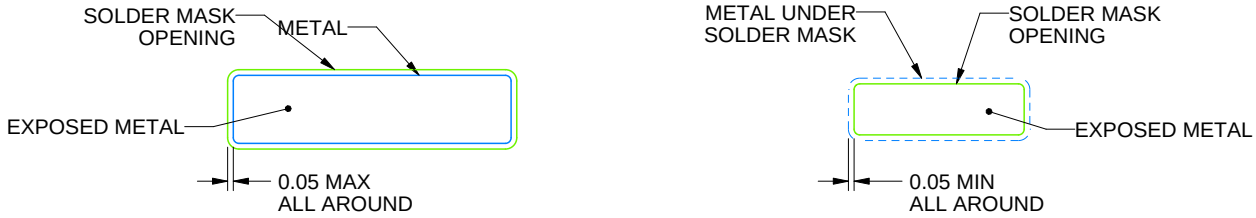


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

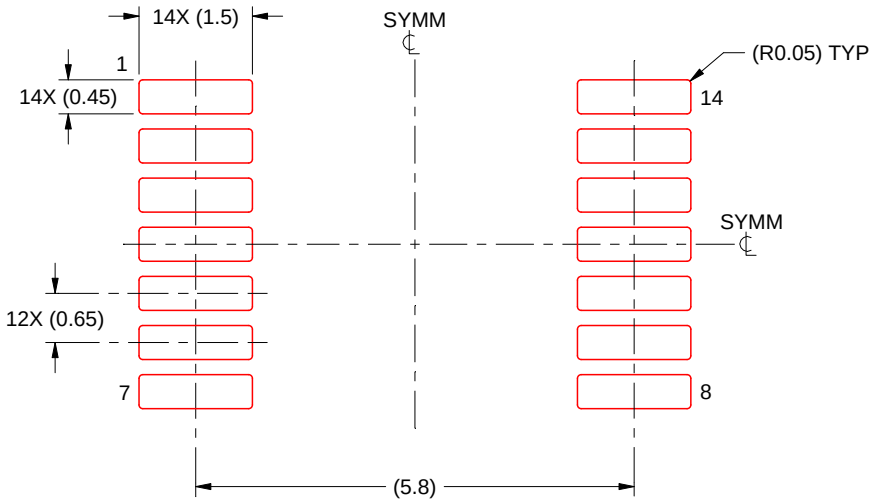


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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