

## RAIL-TO-RAIL OUTPUT, VERY LOW-NOISE OPERATIONAL AMPLIFIERS

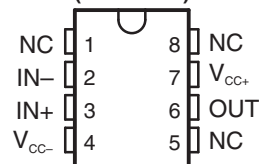
 Check for Samples: [TL971-Q1](#), [TL972-Q1](#), [TL974-Q1](#)

### FEATURES

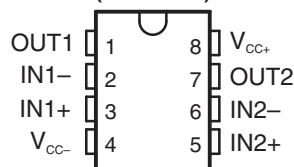
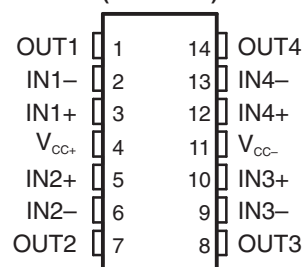
- Qualified for Automotive Applications
- Rail-to-Rail Output Voltage Swing:  
 $\pm 2.4\text{ V}$  at  $V_{CC} = \pm 2.5\text{ V}$
- Very Low Noise Level:  $4\text{ nV}/\sqrt{\text{Hz}}$
- Ultra-Low Distortion: 0.003%
- High Dynamic Features: 12 MHz, 5 V/ $\mu\text{s}$
- Operating Range: 2.7 V to 12 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B)
  - 200-V Machine Model (A115-A)
  - 1500-V Charged-Device Model (C101)

### APPLICATIONS

- Portable Equipment (CD Players, PDAs)
- Portable Communications (Cell Phones, Pagers)
- Instrumentation and Sensors
- Professional Audio Circuits

**TL971...D PACKAGE  
(TOP VIEW)**


NC – No internal connection

**TL972...D OR PW PACKAGE  
(TOP VIEW)**

**TL974...PW PACKAGE  
(TOP VIEW)**


### DESCRIPTION/ORDERING INFORMATION

The TL97x family of operational amplifiers operates at voltages as low as  $\pm 1.35\text{ V}$  and features output rail-to-rail signal swing. The TL97x boast characteristics that make them particularly well suited for portable and battery-supplied equipment. Very low noise and low distortion characteristics make them ideal for audio preamplification.

#### ORDERING INFORMATION<sup>(1)(2)</sup>

$T_A$	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TL971QDRQ1	TL971Q
	TL972QDRQ1	TL972Q
	TL972QPWRQ1	TL972Q
	TL974QPWRQ1	TL974Q

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

$V_{CC}$	Supply voltage range <sup>(2)</sup>			2.7 V to 15 V
$V_{ID}$	Differential input voltage <sup>(3)</sup>			±1 V
$V_{IN}$	Input voltage range <sup>(4)</sup>			$V_{CC-} - 0.3$ V to $V_{CC+} + 0.3$ V
$\theta_{JA}$	Package thermal impedance, junction to free air	D package <sup>(5)</sup>	8 pin	97°C/W
		PW package <sup>(5)</sup>	8 pin	149°C/W
			14 pin	113°C/W
$T_J$	Maximum junction temperature			150°C
$T_{lead}$	Maximum lead temperature	Soldering, 10 seconds		260°C
$T_{stg}$	Storage temperature range			-65°C to 150°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM)		2000 V
		Machine Model (MM)		200 V
		Charged-Device Model (CDM)		1500 V

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground terminal.
- (3) Differential voltages for the noninverting input terminal are with respect to the inverting input terminal.
- (4) The input and output voltages must never exceed  $V_{CC} + 0.3$  V.
- (5) Package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.7	12	V
$V_{ICM}$	Common-mode input voltage	$V_{CC-} + 1.15$	$V_{CC+} - 1.15$	V
$T_A$	Operating free-air temperature	-40	125	°C

## ELECTRICAL CHARACTERISTICS

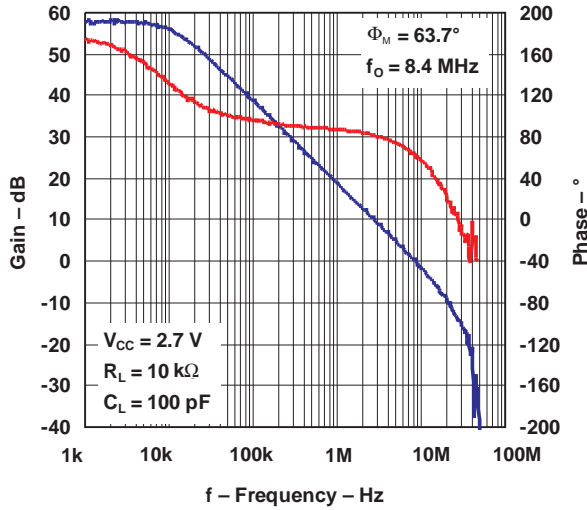
 $V_{CC+} = 2.5\text{ V}$ ,  $V_{CC-} = -2.5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$ <sup>(1)</sup>	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage		25°C		1	4	mV
			Full range			6	
$\alpha V_{IO}$	Input offset voltage drift	$V_{ICM} = 0\text{ V}$ , $V_O = 0\text{ V}$	25°C		5		$\mu\text{V}/^\circ\text{C}$
$I_{IO}$	Input offset current	$V_{ICM} = 0\text{ V}$ , $V_O = 0\text{ V}$	25°C		10	150	nA
$I_{IB}$	Input bias current	$V_{ICM} = 0\text{ V}$ , $V_O = 0\text{ V}$	25°C		200	750	nA
			Full range			1000	
$V_{ICM}$	Common-mode input voltage		25°C	-1.35		1.35	V
CMRR	Common-mode rejection ratio	$V_{ICM} = \pm 1.35\text{ V}$	25°C	60	85		dB
SVR	Supply-voltage rejection ratio	$V_{CC} = \pm 2\text{ V}$ to $\pm 3\text{ V}$	25°C	60	70		dB
$A_{VD}$	Large-signal voltage gain	$R_L = 2\text{ k}\Omega$	25°C	70	80		dB
$V_{OH}$	High-level output voltage	$R_L = 2\text{ k}\Omega$	25°C	2	2.4		V
$V_{OL}$	Low-level output voltage	$R_L = 2\text{ k}\Omega$	25°C		-2.4	-2	V
$I_{source}$	Output source current	$V_{OUT}$ shorted to -2.5 V	25°C	1.2	1.4		mA
			Full range		1		
$I_{sink}$	Output sink current	$V_{OUT}$ shorted to +2.5 V	25°C	50	80		mA
			Full range		25		
$I_{CC}$	Supply current (per amplifier)	Unity gain, No load	25°C		2	2.8	mA
			Full range			3.2	
GBWP	Gain bandwidth product	$f = 100\text{ kHz}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$	25°C	8.5	12		MHz
SR	Slew rate	$A_V = 1$ , $V_{IN} = \pm 1\text{ V}$	25°C	3.5	5		V/ $\mu\text{s}$
			Full range		3		
$\Phi_m$	Phase margin at unity gain	$R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$	25°C		60		°
Gm	Gain margin	$R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$	25°C		10		dB
$V_n$	Equivalent input noise voltage	$f = 100\text{ kHz}$	25°C		4		$\text{nV}/\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$f = 1\text{ kHz}$ , $A_V = -1$ , $R_L = 10\text{ k}\Omega$	25°C		0.003		%

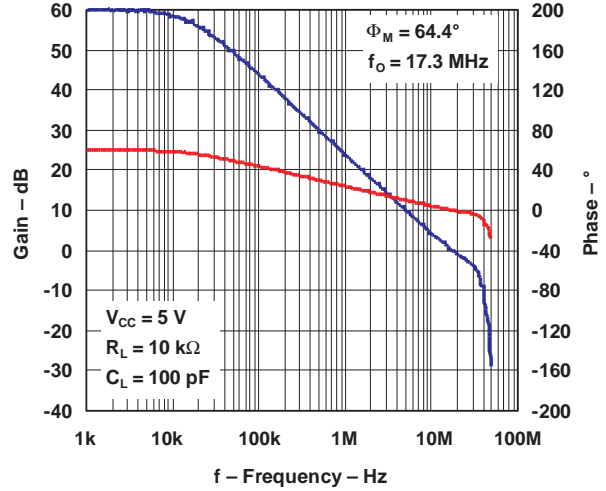
 (1) Full range  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$

TYPICAL CHARACTERISTICS

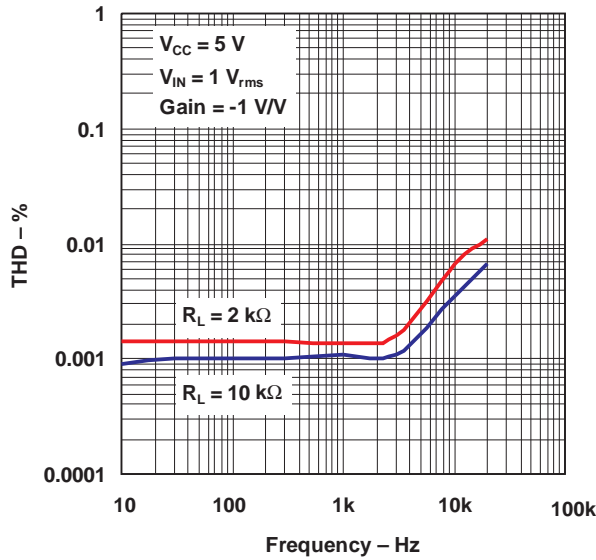
GAIN AND PHASE  
 vs  
 FREQUENCY



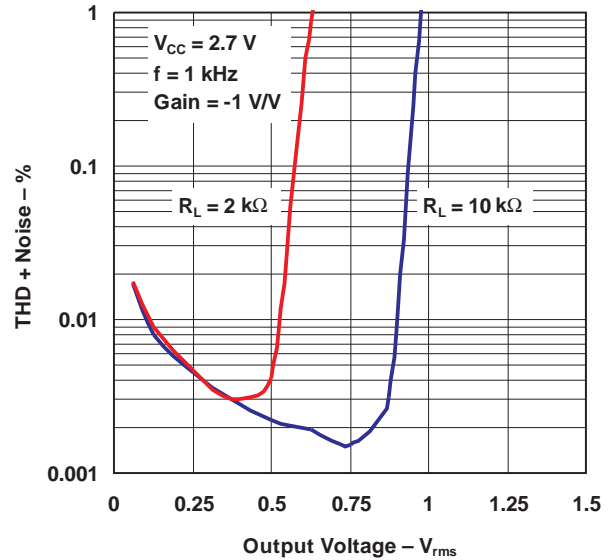
GAIN AND PHASE  
 vs  
 FREQUENCY



TOTAL HARMONIC DISTORTION  
 vs  
 FREQUENCY

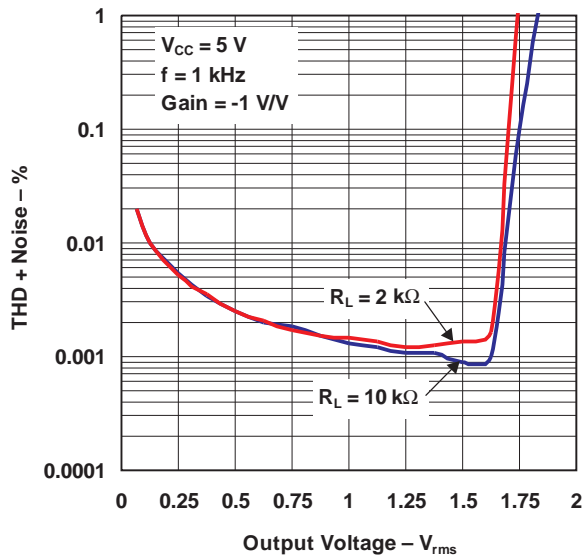


TOTAL HARMONIC DISTORTION + NOISE  
 vs  
 OUTPUT VOLTAGE

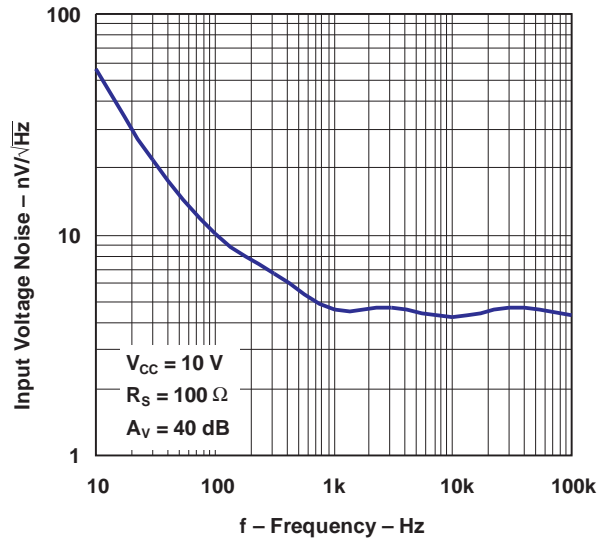


**TYPICAL CHARACTERISTICS (continued)**

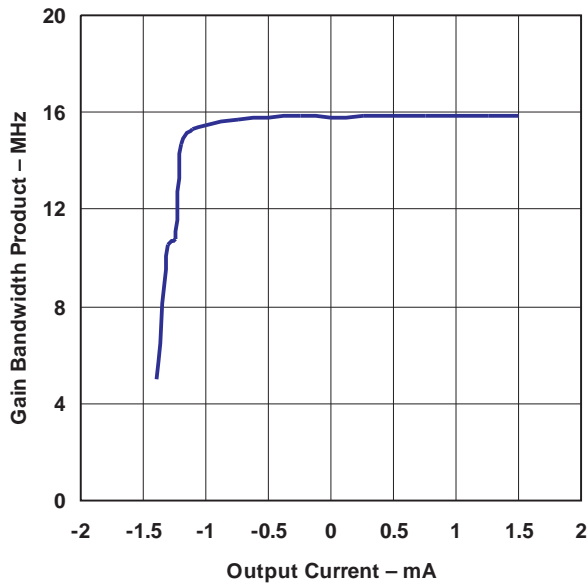
**TOTAL HARMONIC DISTORTION + NOISE**  
vs  
**OUTPUT VOLTAGE**



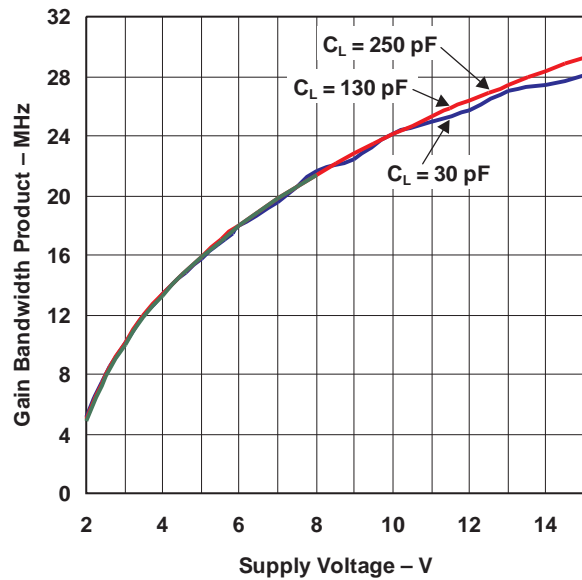
**INPUT VOLTAGE NOISE**  
vs  
**FREQUENCY**



**GAIN BANDWIDTH PRODUCT**  
vs  
**OUTPUT CURRENT**

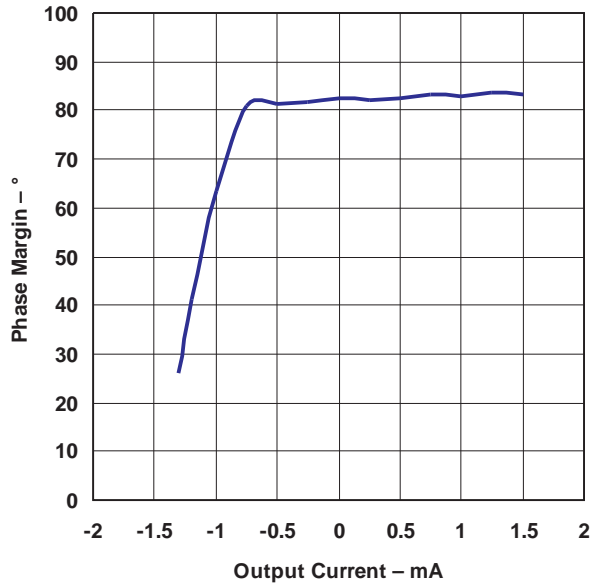


**GAIN BANDWIDTH PRODUCT**  
vs  
**SUPPLY VOLTAGE**

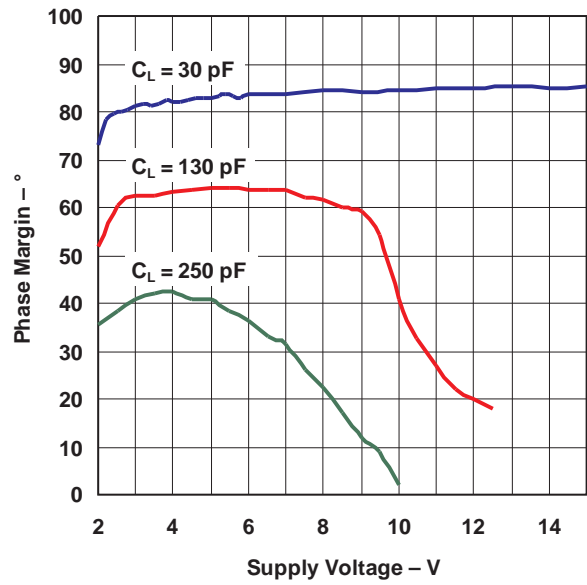


**TYPICAL CHARACTERISTICS (continued)**

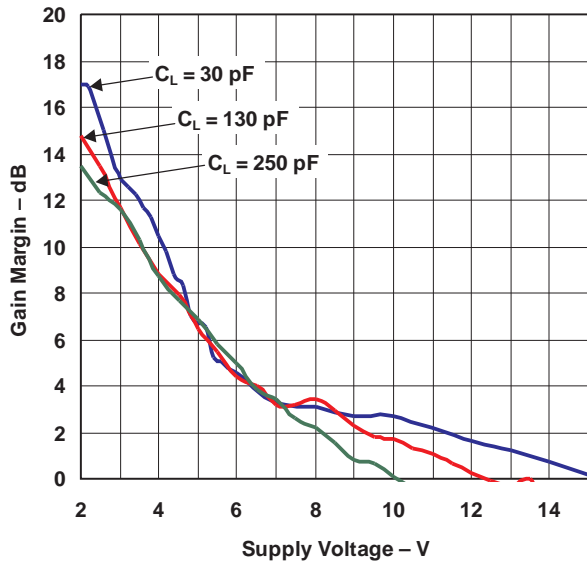
**PHASE MARGIN  
 vs  
 OUTPUT CURRENT**



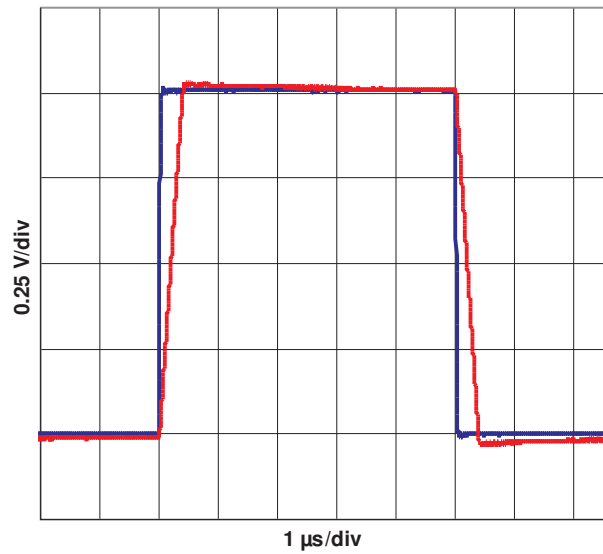
**PHASE MARGIN  
 vs  
 SUPPLY VOLTAGE**



**GAIN MARGIN  
 vs  
 SUPPLY VOLTAGE**

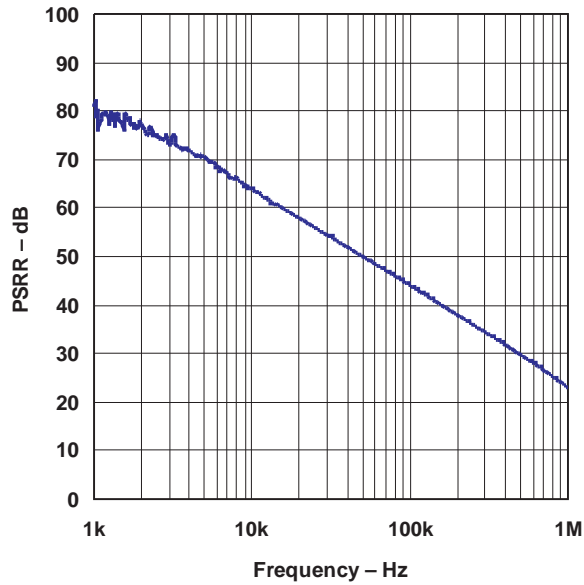


**INPUT RESPONSE**

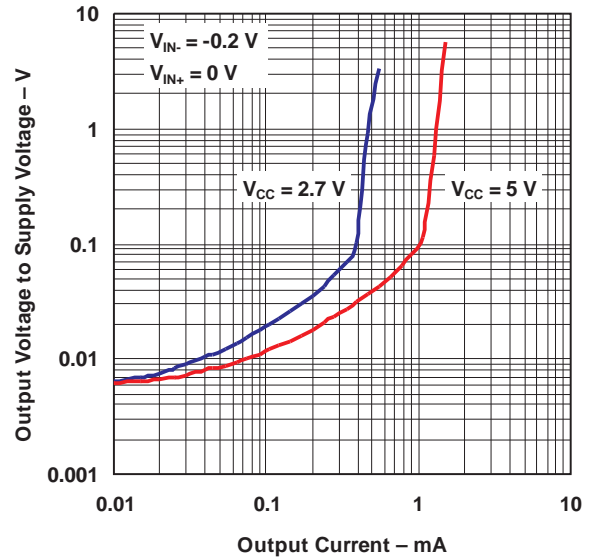


TYPICAL CHARACTERISTICS (continued)

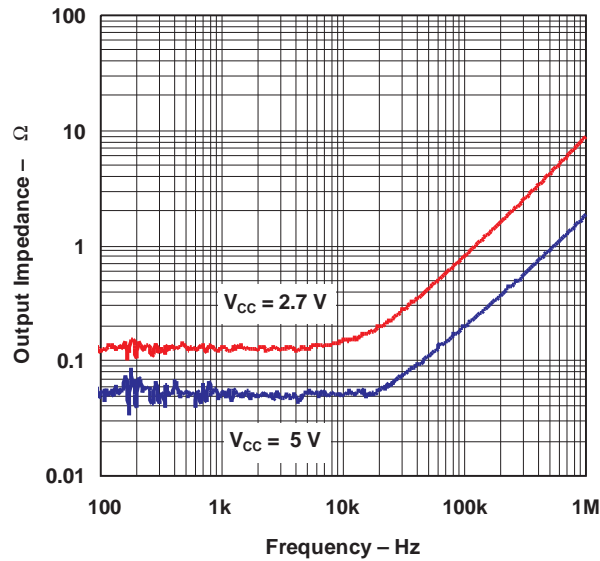
POWER-SUPPLY RIPPLE REJECTION  
vs  
FREQUENCY



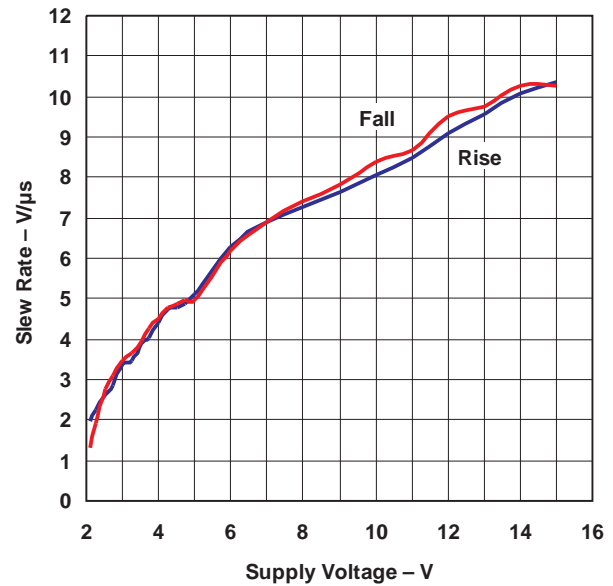
OUTPUT VOLTAGE  
vs  
OUTPUT CURRENT



OUTPUT IMPEDANCE  
vs  
FREQUENCY



SLEW RATE  
vs  
SUPPLY VOLTAGE



## REVISION HISTORY

Changes from Original (March 2009) to Revision A	Page
• Removed packaging column from the ordering information table. ....	1
• Changed $V_{OUT} = \pm 2.5\text{ V}$ to $V_{OUT}$ shorted to $-2.5\text{ V}$ for $I_{SOURCE}$ , and changed $V_{OUT} = \pm 2.5\text{ V}$ to $V_{OUT}$ shorted to $+2.5\text{ V}$ for $I_{SINK}$ . ....	3



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL971QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL971Q	<a href="#">Samples</a>
TL972QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL972Q	<a href="#">Samples</a>
TL972QPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL972Q	<a href="#">Samples</a>
TL974QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TL971-Q1, TL972-Q1, TL974-Q1 :**

- Catalog: [TL971](#), [TL972](#), [TL974](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL972QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL972QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL974QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL972QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TL972QPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
TL974QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0008A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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