

## 8-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER

### features

- **8-Bit Resolution**
- **Differential Linearity Error**
  - $\pm 0.3$  LSB Typ,  $\pm 1$  LSB Max (25°C)
  - $\pm 1$  LSB Max
- **Integral Linearity Error**
  - $\pm 0.6$  LSB,  $\pm 0.75$  LSB Max (25°C)
  - $\pm 1$  LSB Max
- **Maximum Conversion Rate of 40 Megasamples Per Second (MSPS) Max**
- **Internal Sample and Hold Function**
- **5-V Single Supply Operation**
- **Low Power Consumption . . . 85 mW Typ**
- **Analog Input Bandwidth . . .  $\geq 75$  MHz Typ**
- **Internal Reference Voltage Generators**

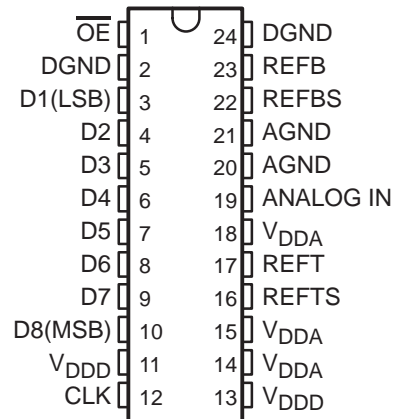
### applications

- **Quadrature Amplitude Modulation (QAM) and Quadrature Phase Shift Keying (QPSK) Demodulators**
- **Digital Television**
- **Charge-Coupled Device (CCD) Scanners**
- **Video Conferencing**
- **Digital Set-Top Box**
- **Digital Down Converters**
- **High-Speed Digital Signal Processor Front End**

### description

The TLC5540 is a high-speed, 8-bit analog-to-digital converter (ADC) that converts at sampling rates up to 40 megasamples per second (MSPS). Using a semiflash architecture and CMOS process, the TLC5540 is able to convert at high speeds while still maintaining low power consumption and cost. The analog input bandwidth of 75 MHz (typ) makes this device an excellent choice for undersampling applications. Internal resistors are provided to generate 2-V full-scale reference voltages from a 5-V supply, thereby reducing external components. The digital outputs can be placed in a high impedance mode. The TLC5540 requires only a single 5-V supply for operation.

PW OR NS PACKAGE  
(TOP VIEW)



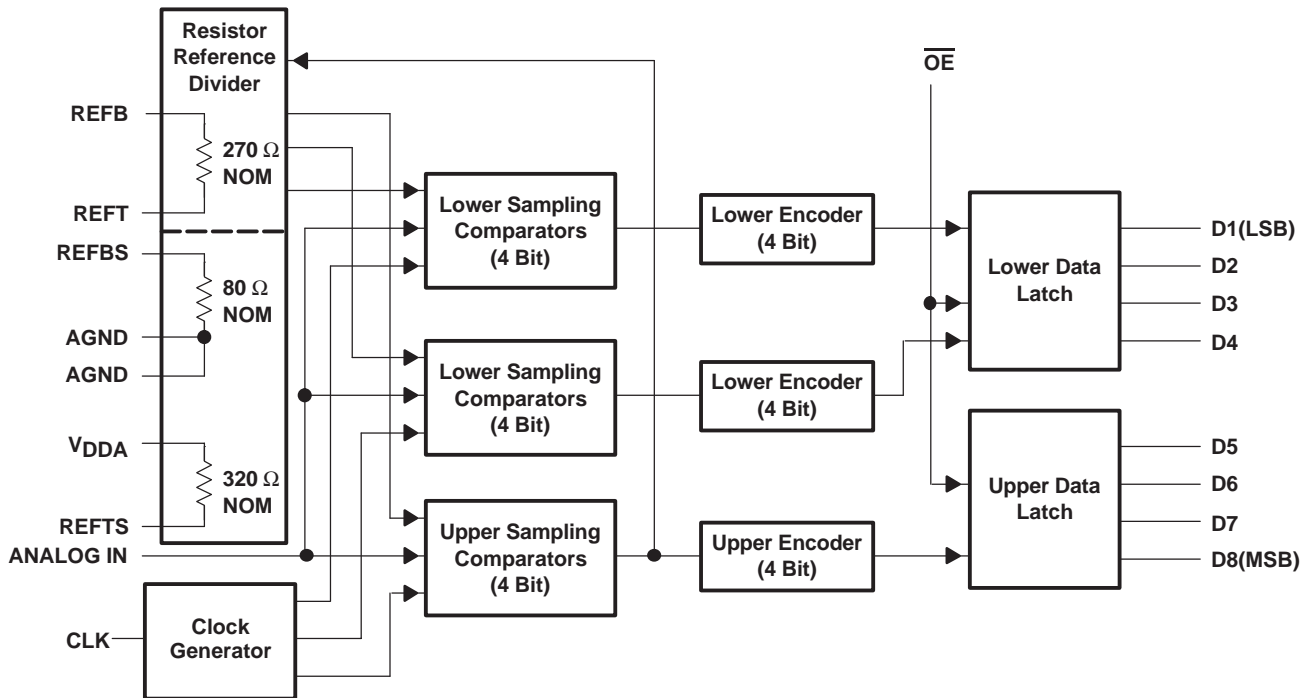
AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGE	
	TSSOP (PW)	SOP (NS)
–0°C to 70°C	TLC5540CPW	TLC5540CNSLE
–40°C to 85°C	TLC5540IPW	TLC5540INSLE

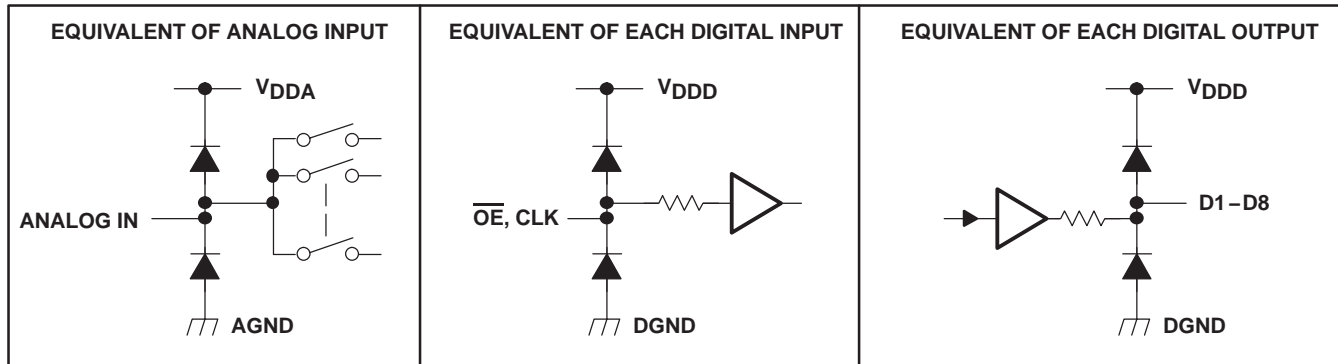


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functional block diagram



schematics of inputs and outputs



**Terminal Functions**

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	20, 21		Analog ground
ANALOG IN	19	I	Analog input
CLK	12	I	Clock input
DGND	2, 24		Digital ground
D1–D8	3–10	O	Digital data out. D1:LSB, D8:MSB
$\overline{OE}$	1	I	Output enable. When $\overline{OE} = L$ , data is enabled. When $\overline{OE} = H$ , D1–D8 is high impedance.
$V_{DDA}$	14, 15, 18		Analog $V_{DD}$
$V_{DDD}$	11, 13		Digital $V_{DD}$
REFB	23	I	ADC reference voltage in (bottom)
REFBS	22		Reference voltage (bottom). When using the internal voltage divider to generate a nominal 2-V reference, the REFBS terminal is shorted to the REFB terminal and the REFTS terminal is shorted to the REFT terminal (see Figure 13 and Figure 14).
REFT	17	I	Reference voltage in (top)
REFTS	16		Reference voltage (top). When using the internal voltage divider to generate a nominal 2-V reference, the REFTS terminal is shorted to the REFT terminal and the REFBS terminal is shorted to the REFB terminal (see Figure 13 and Figure 14).

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{DDA}$ , $V_{DDD}$	7 V
Reference voltage input range, $V_{I(REFT)}$ , $V_{I(REFB)}$ , $V_{I(REFBS)}$ , $V_{I(REFTS)}$	AGND to $V_{DDA}$
Analog input voltage range, $V_{I(ANLG)}$	AGND to $V_{DDA}$
Digital input voltage range, $V_{I(DGTL)}$	DGND to $V_{DDD}$
Digital output voltage range, $V_{O(DGTL)}$	DGND to $V_{DDD}$
Operating free-air temperature range, $T_A$ : TLC5540C	0°C to 70°C
TLC5540I	–40°C to 85°C
Storage temperature range, $T_{stg}$	–55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
Supply voltage	V <sub>DDA</sub> –AGND	4.75	5	5.25	V
	V <sub>DDD</sub> –AGND	4.75	5	5.25	
	AGND–DGND	–100	0	100	mV
Reference input voltage (top), V <sub>I(REFT)</sub>		V <sub>I(REFB)</sub> +1.8	V <sub>I(REFB)</sub> +2	V <sub>DDA</sub>	V
Reference input voltage (bottom), V <sub>I(REFB)</sub>		0	0.6	V <sub>I(REFT)</sub> –1.8	V
Analog input voltage range, V <sub>I(ANLG)</sub> (see Note 1)		V <sub>I(REFB)</sub>		V <sub>I(REFT)</sub>	V
Full scale voltage, V <sub>I(REFT)</sub> – V <sub>I(REFB)</sub>		1.8		5	V
High-level input voltage, V <sub>IH</sub>		4			V
Low-level input voltage, V <sub>IL</sub>				1	V
Pulse duration, clock high, t <sub>w(H)</sub>		12.5			ns
Pulse duration, clock low, t <sub>w(L)</sub>		12.5			ns
Operating free-air temperature, T <sub>A</sub>	TLC5540C	0		70	°C
	TLC5540I	–40		85	°C

(1)  $1.8\text{ V} \leq V_{I(\text{REFT})} - V_{I(\text{REFB})} < V_{\text{DD}}$

**electrical characteristics at  $V_{DD} = 5\text{ V}$ ,  $V_{I(REFT)} = 2.6\text{ V}$ ,  $V_{I(REFB)} = 0.6\text{ V}$ ,  $f_s = 40\text{ MSPS}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
E <sub>L</sub>	Linearity error, integral	f <sub>s</sub> = 40 MSPS, V <sub>I</sub> = 0.6 V to 2.6 V	T <sub>A</sub> = 25°C		±0.6	±1	LSB
			T <sub>A</sub> = MIN to MAX			±1	
E <sub>D</sub>	Linearity error, differential		T <sub>A</sub> = 25°C		±0.3	±0.75	
			T <sub>A</sub> = MIN to MAX			±1	
	Self bias (1), V <sub>RB</sub>	Short REFB to REFBS	See Figure 13	0.57	0.61	0.65	V
	Self bias (1), V <sub>RT</sub>	Short REFT to REFTS		2.47	2.63	2.80	
	Self bias (2), V <sub>RB</sub>	Short REFB to AGND	See Figure 14	AGND			
	Self bias (2), V <sub>RT</sub>	Short REFT to REFTS		2.18	2.29	2.4	
I <sub>ref</sub>	Reference-voltage current	V <sub>I(REFT)</sub> – V <sub>I(REFB)</sub> = 2 V		5.2	7.5	12	mA
R <sub>ref</sub>	Reference-voltage resistor	Between REFT and REFB terminals		165	270	350	Ω
C <sub>i</sub>	Analog input capacitance	V <sub>I(ANLG)</sub> = 1.5 V + 0.07 V <sub>rms</sub>			4		pF
E <sub>ZS</sub>	Zero-scale error	V <sub>I(REFT)</sub> – V <sub>I(REFB)</sub> = 2 V		-18	-43	-68	mV
E <sub>FS</sub>	Full-scale error			-25	0	25	
I <sub>IH</sub>	High-level input current	V <sub>DD</sub> = 5.25 V,	V <sub>IH</sub> = V <sub>DD</sub>			5	μA
I <sub>IL</sub>	Low-level input current	V <sub>DD</sub> = 5.25 V,	V <sub>IL</sub> = 0			5	
I <sub>OH</sub>	High-level output current	$\overline{\text{OE}}$ = GND,	V <sub>DD</sub> = 4.75 V, V <sub>OH</sub> = V <sub>DD</sub> – 0.5 V	-1.5			mA
I <sub>OL</sub>	Low-level output current	$\overline{\text{OE}}$ = GND,	V <sub>DD</sub> = 4.75 V, V <sub>OL</sub> = 0.4 V	2.5			
I <sub>OZH</sub> (I <sub>kg</sub> )	High-level high-impedance-state output leakage current	$\overline{\text{OE}}$ = V <sub>DD</sub> ,	V <sub>DD</sub> = 5.25, V <sub>OH</sub> = V <sub>DD</sub>			16	μA
I <sub>OZL</sub> (I <sub>kg</sub> )	Low-level high-impedance-state output leakage current	$\overline{\text{OE}}$ = V <sub>DD</sub> ,	V <sub>DD</sub> = 4.75, V <sub>OL</sub> = 0			16	
I <sub>DD</sub>	Supply current	f <sub>s</sub> = 40 MSPS, C <sub>L</sub> ≤ 25 pF, NTSC‡ ramp wave input, See Note 1			17	27	mA

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

‡ National Television System Committee

(1) Supply current specification does not include I<sub>ref</sub>.

operating characteristics at  $V_{DD} = 5\text{ V}$ ,  $V_{RT} = 2.6\text{ V}$ ,  $V_{RB} = 0.6\text{ V}$ ,  $f_s = 40\text{ MSPS}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

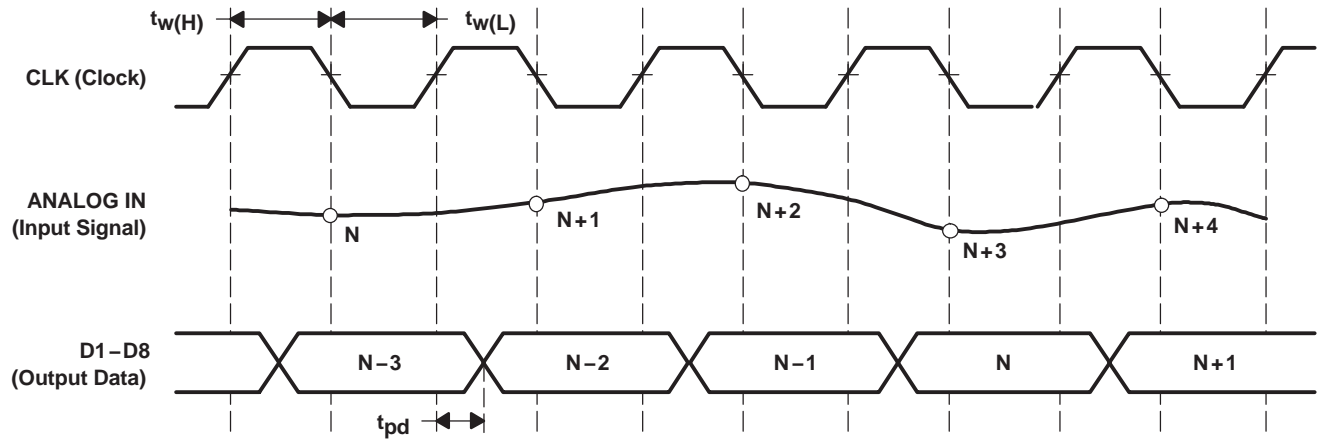
PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$f_s$	Maximum conversion rate	$T_A = \text{MIN to MAX}$	40			MSPS
$f_s$	Minimum conversion rate	$T_A = \text{MIN to MAX}$		5		MSPS
BW	Analog input full-power bandwidth	At $-3\text{ dB}$ , $V_{I(\text{ANLG})} = 2\text{ V}_{pp}$		75		MHz
$t_{pd}$	Delay time, digital output	$C_L \leq 10\text{ pF}$ (see Note 2)		9	15	ns
$t_{PHZ}$	Disable time, output high to Hi-Z	$C_L \leq 15\text{ pF}$ , $I_{OH} = -4.5\text{ mA}$			20	ns
$t_{PLZ}$	Disable time, output low to Hi-Z	$C_L \leq 15\text{ pF}$ , $I_{OL} = 5\text{ mA}$			20	ns
$t_{pZH}$	Enable time, Hi-Z to output high	$C_L \leq 15\text{ pF}$ , $I_{OH} = -4.5\text{ mA}$			15	ns
$t_{pZL}$	Enable time, Hi-Z to output low	$C_L \leq 15\text{ pF}$ , $I_{OL} = 5\text{ mA}$			15	ns
	Differential gain	NTSC 40 IRE‡ modulation wave,		1%		
	Differential phase	$f_s = 14.3\text{ MSPS}$		0.7		degrees
$t_{AJ}$	Aperture jitter time			30		ps
$t_{d(s)}$	Sampling delay time			4		ns
SNR	Signal-to-noise ratio	$f_s = 20\text{ MSPS}$	$f_1 = 1\text{ MHz}$		47	dB
			$f_1 = 3\text{ MHz}$	44	47	
			$f_1 = 6\text{ MHz}$		46	
			$f_1 = 10\text{ MHz}$		45	
		$f_s = 40\text{ MSPS}$	$f_1 = 3\text{ MHz}$		45.2	
			$f_1 = 6\text{ MHz}$	42	44	
ENOB	Effective number of bits	$f_s = 20\text{ MSPS}$	$f_1 = 1\text{ MHz}$		7.64	Bits
			$f_1 = 3\text{ MHz}$		7.61	
			$f_1 = 6\text{ MHz}$		7.47	
			$f_1 = 10\text{ MHz}$		7.16	
		$f_s = 40\text{ MSPS}$	$f_1 = 3\text{ MHz}$		7	
			$f_1 = 6\text{ MHz}$		6.8	
THD	Total harmonic distortion	$f_s = 20\text{ MSPS}$	$f_1 = 1\text{ MHz}$		43	dBc
			$f_1 = 3\text{ MHz}$	35	42	
			$f_1 = 6\text{ MHz}$		41	
			$f_1 = 10\text{ MHz}$		38	
		$f_s = 40\text{ MSPS}$	$f_1 = 3\text{ MHz}$		40	
			$f_1 = 6\text{ MHz}$		38	
Spurious-free dynamic range		$f_s = 20\text{ MSPS}$	$f_1 = 3\text{ MHz}$	41	46	dBc
		$f_s = 40\text{ MSPS}$	$f_1 = 3\text{ MHz}$		42	

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

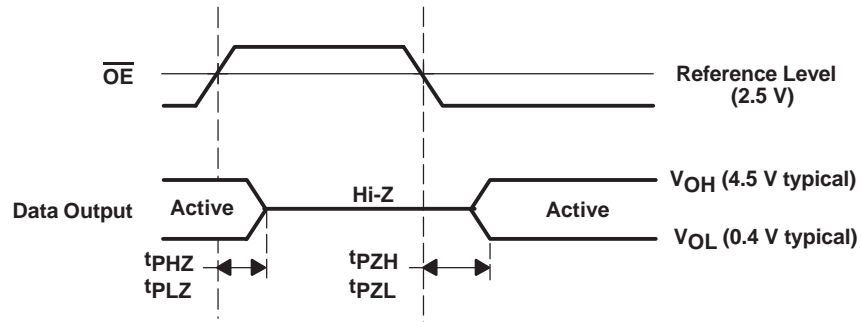
‡ Institute of Radio Engineers

(2)  $C_L$  includes probe and jig capacitance.

**PARAMETER MEASUREMENT INFORMATION**



**Figure 1. I/O Timing Diagram**



**Figure 2. I/O Timing Diagram**

TYPICAL CHARACTERISTICS

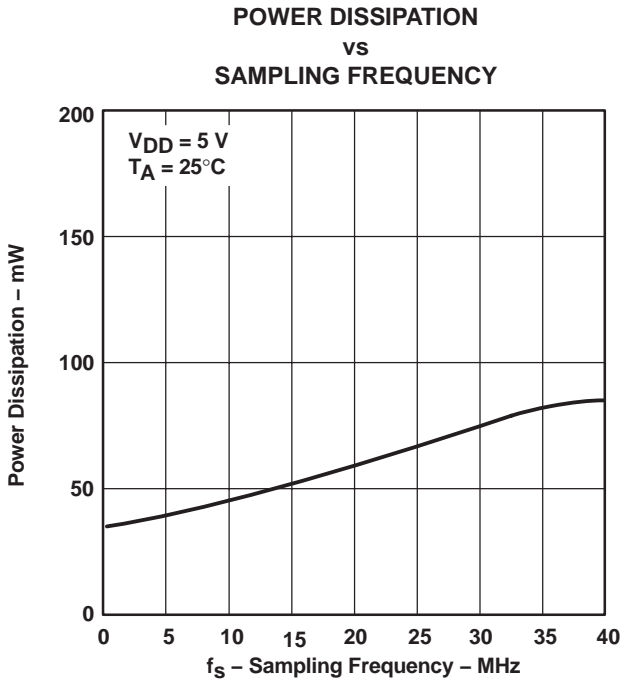


Figure 3

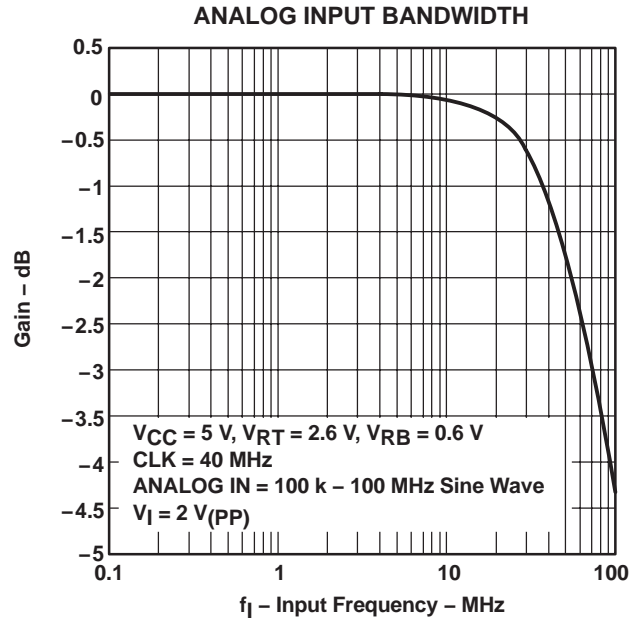


Figure 4

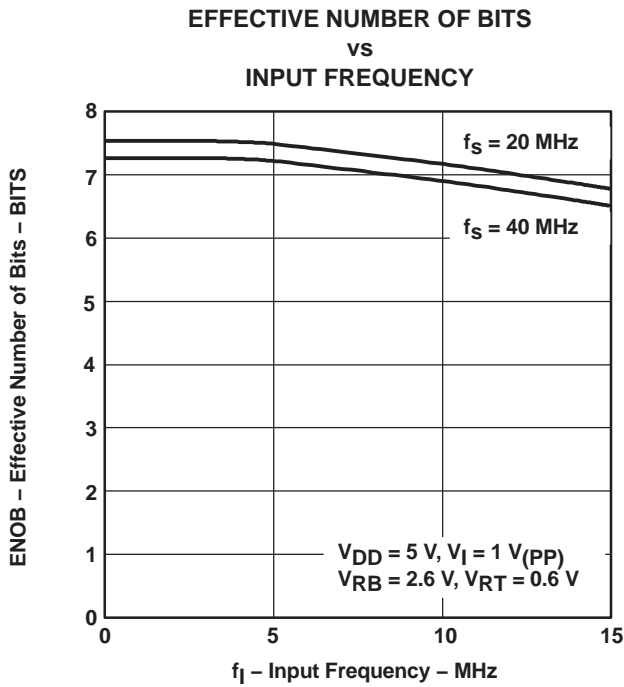


Figure 5

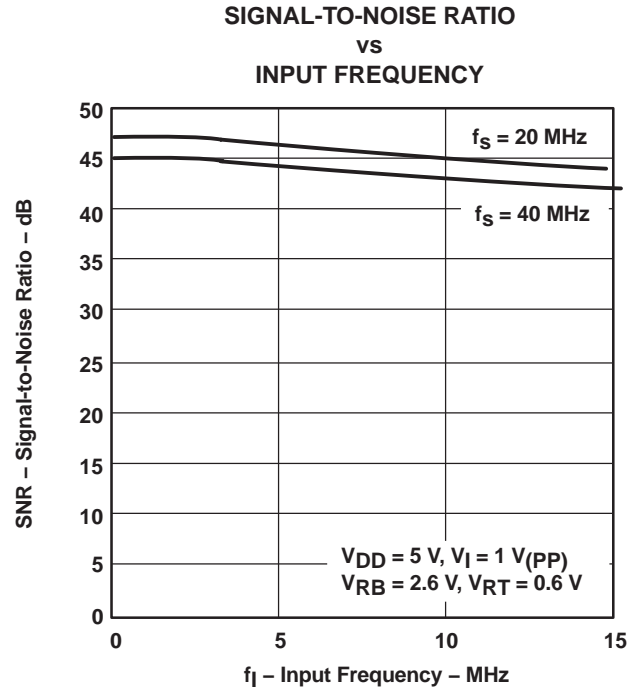


Figure 6



TYPICAL CHARACTERISTICS

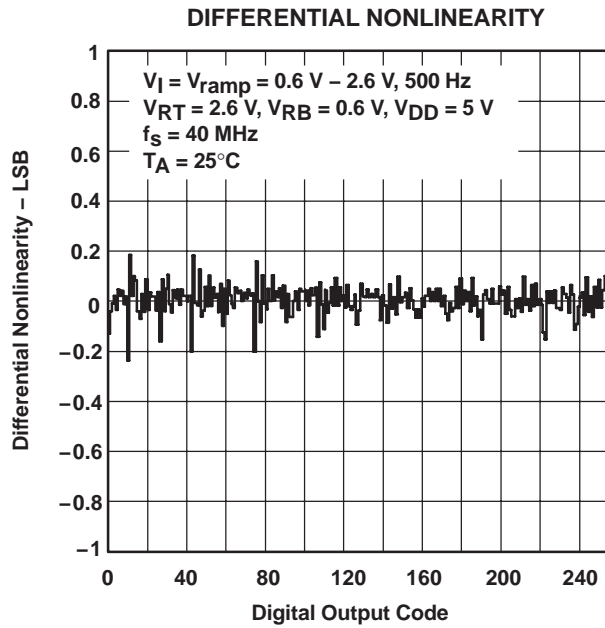


Figure 7

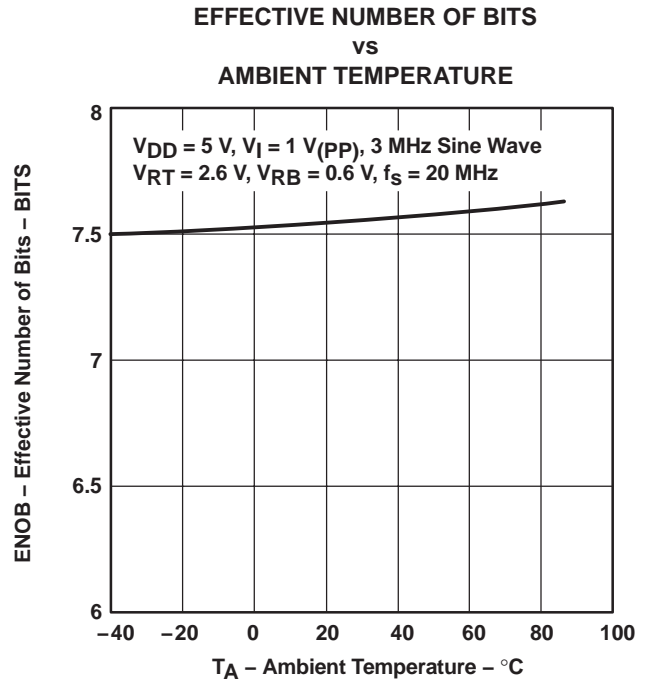


Figure 8

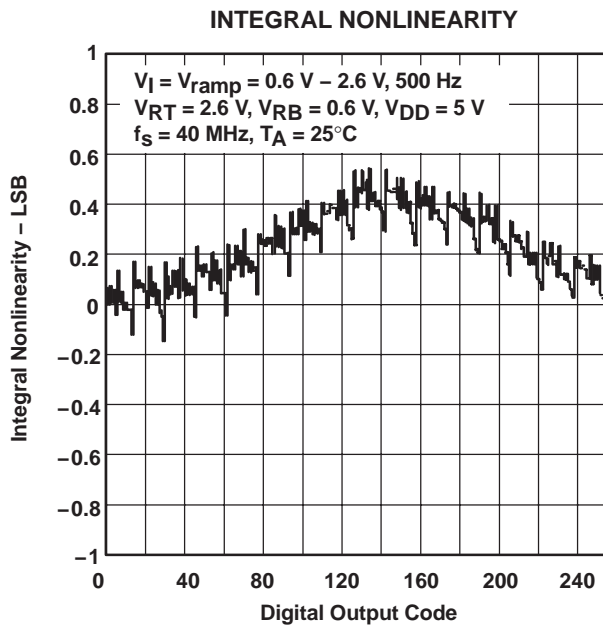


Figure 9

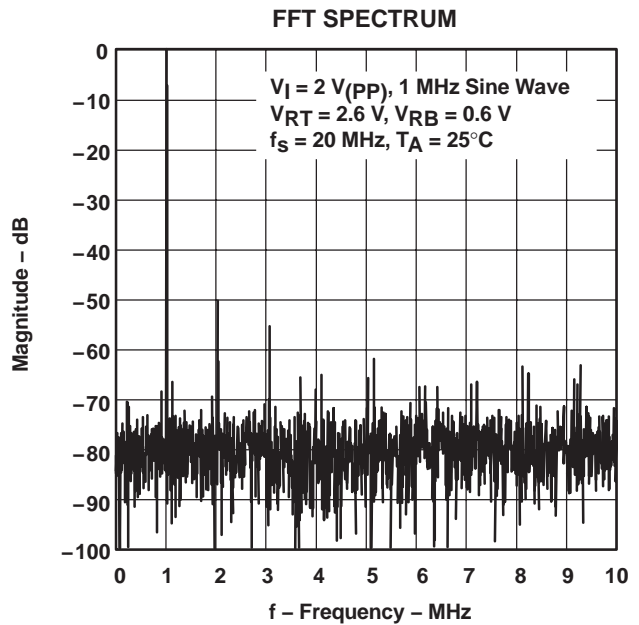


Figure 10

## APPLICATION INFORMATION

### grounding and power supply considerations

A signal ground is a low-impedance path for current to return to the source. Inside the TLC5540 A/D converter, the analog ground and digital ground are connected to each other through the substrate, which has a very small resistance ( $\sim 30\ \Omega$ ) to prevent internal latch-up. For this reason, it is strongly recommended that a printed circuit board (PCB) of at least 4 layers be used with the TLC5540 and the converter DGND and AGND pins be connected directly to the analog ground plane to avoid a ground loop. Figure 11 shows the recommended decoupling and grounding scheme for laying out a multilayer PC board with the TLC5540. This scheme ensures that the impedance connection between AGND and DGND is minimized so that their potential difference is negligible and noise source caused by digital switching current is eliminated.

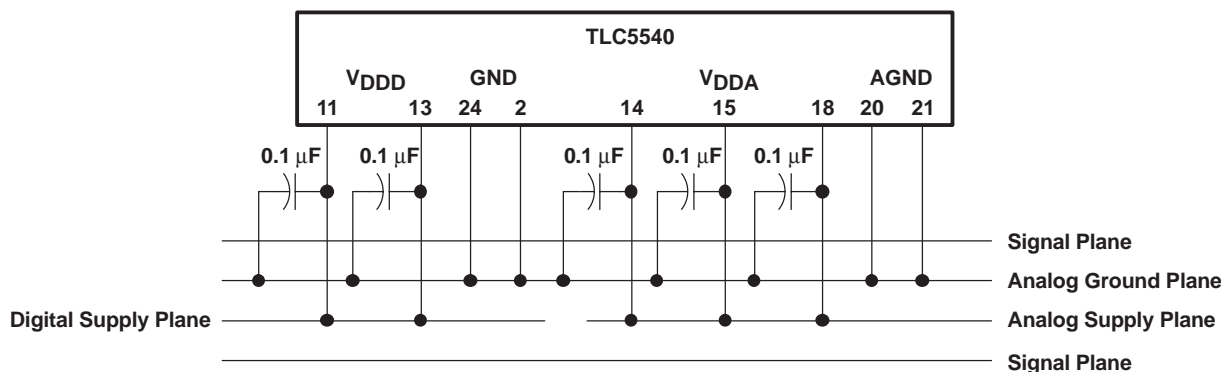


Figure 11.  $AV_{DD}$ ,  $DV_{DD}$ , AGND, and DGND Connections

### printed circuit board (PCB) layout considerations

When designing a circuit that includes high-speed digital and precision analog signals such as a high speed ADC, PCB layout is a key component to achieving the desired performance. The following recommendations should be considered during the prototyping and PCB design phase:

- Separate analog and digital circuitry physically to help eliminate capacitive coupling and crosstalk. When separate analog and digital ground planes are used, the digital ground and power planes should be several layers from the analog signals and power plane to avoid capacitive coupling.
- Full ground planes should be used. Do not use individual etches to return analog and digital currents or partial ground planes. For prototyping, breadboards should be constructed with copper clad boards to maximize ground plane.
- The conversion clock, CLK, should be terminated properly to reduce overshoot and ringing. Any jitter on the conversion clock degrades ADC performance. A high-speed CMOS buffer such as a 74ACT04 or 74AC04 positioned close to the CLK terminal can improve performance.
- Minimize all etch runs as much as possible by placing components very close together. It also proves beneficial to place the ADC in a corner of the PCB nearest to the I/O connector analog terminals.
- It is recommended to place the digital output data latch (if used) as close to the TLC5540 as possible to minimize capacitive loading. If D0 through D7 must drive large capacitive loads, internal ADC noise may be experienced.

## PRINCIPLES OF OPERATION

### functional description

The TLC5540 uses a modified semiflash architecture as shown in the functional block diagram. The four most significant bits (MSBs) of every output conversion result are produced by the upper comparator block CB1. The four least significant bits (LSBs) of each alternate output conversion result are produced by the lower comparator blocks CB-A and CB-B in turn (see Figure 12).

The reference voltage that is applied to the lower comparator resistor string is one sixteenth of the amplitude of the reference applied to the upper comparator resistor string. The sampling comparators of the lower comparator block require more time to sample the lower voltages of the reference and residual input voltage. By applying the residual input voltage to alternate lower comparator blocks, each comparator block has twice as much time to sample and convert as would be the case if only one lower comparator block were used.

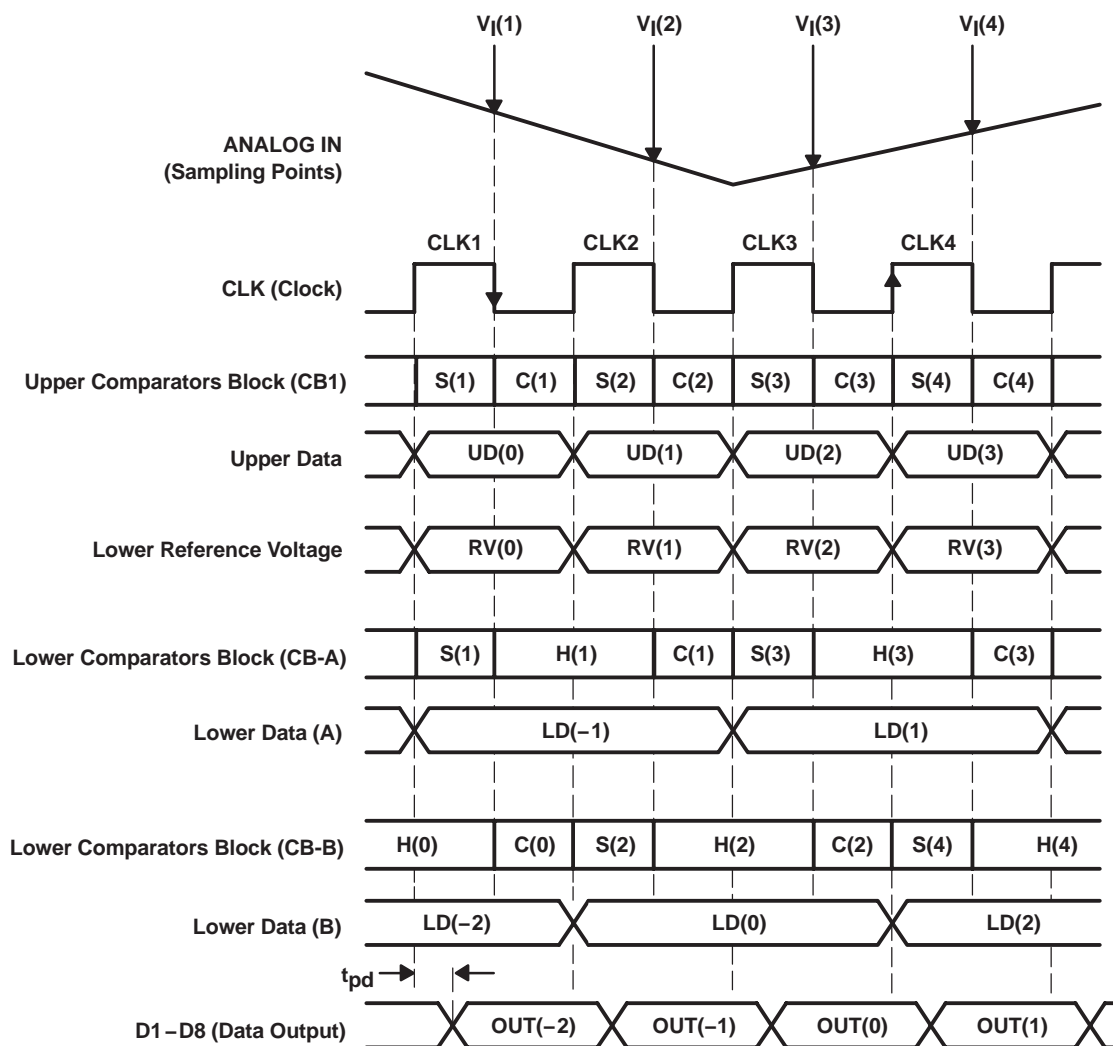


Figure 12. Internal Functional Timing Diagram

This conversion scheme, which reduces the required sampling comparators by 30 percent compared to standard semiflash architectures, achieves significantly higher sample rates than the conventional semiflash conversion method.

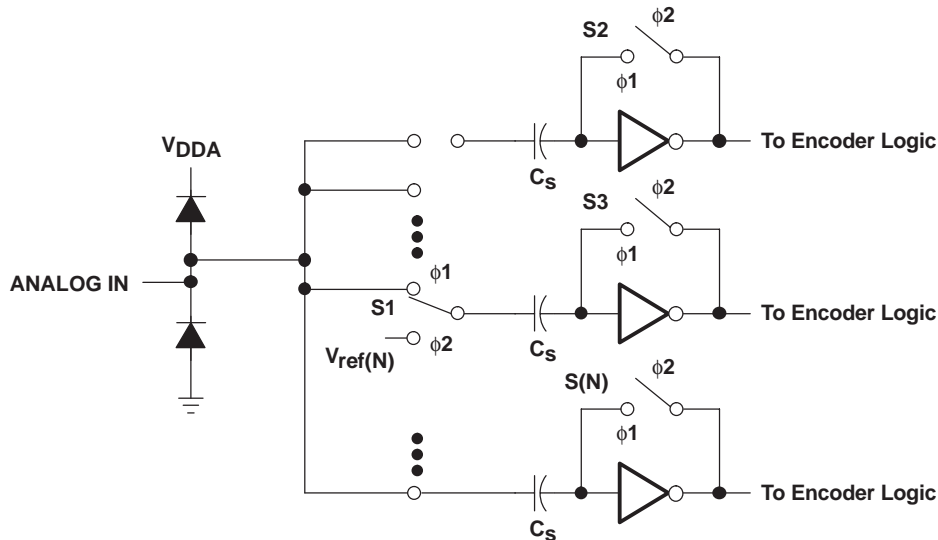
## PRINCIPLES OF OPERATION

### functional description (continued)

The MSB comparator block converts on the falling edge of each applied clock cycle. The LSB comparator blocks CB-A and CB-B convert on the falling edges of the first and second following clock cycles, respectively. The timing diagram of the conversion algorithm is shown in Figure 12.

### analog input operation

The analog input stage to the TLC5540 is a chopper-stabilized comparator and is equivalently shown below:



**Figure 13. External Connections for Using the Internal Reference Resistor Divider**

Figure 13 depicts the analog input for the TLC5540. The switches shown are controlled by two internal clocks,  $\phi 1$  and  $\phi 2$ . These are nonoverlapping clocks that are generated from the CLK input. During the sampling period,  $\phi 1$ , S1 is closed and the input signal is applied to one side of the sampling capacitor,  $C_s$ . Also during the sampling period, S2 through S(N) are closed. This sets the comparator input to approximately 2.5 V. The delta voltage is developed across  $C_s$ . During the comparison phase,  $\phi 2$ , S1 is switched to the appropriate reference voltage for the bit value N. S2 is opened and  $V_{ref(N)} - VC_s$  toggles the comparator output to the appropriate digital 1 or 0. The small resistance values for the switch, S1, and small value of the sampling capacitor combine to produce the wide analog input bandwidth of the TLC5540. The source impedance driving the analog input of the TLC5540 should be less than 100  $\Omega$  across the range of input frequency spectrum.

### reference inputs – REFBS, REFT, REFTS, REFTS

The range of analog inputs that can be converted are determined by REFBS and REFT, REFT being the maximum reference voltage and REFBS being the minimum reference voltage. The TLC5540 is tested with REFT = 2.6 V and REFBS = 0.6 V producing a 2-V full-scale range. The TLC5540 can operate with REFT – REFBS = 5 V, but the power dissipation in the reference resistor increases significantly (93 mW nominally). It is recommended that a 0.1  $\mu$ F capacitor be attached to REFBS and REFT whether using externally or internally generated voltages.

## PRINCIPLES OF OPERATION

### internal reference voltage conversion

Three internal resistors allow the device to generate an internal reference voltage. These resistors are brought out on terminals  $V_{DDA}$ , REFTS, REFT, REFB, REFBS, and AGND. Two different bias voltages are possible without the use of external resistors.

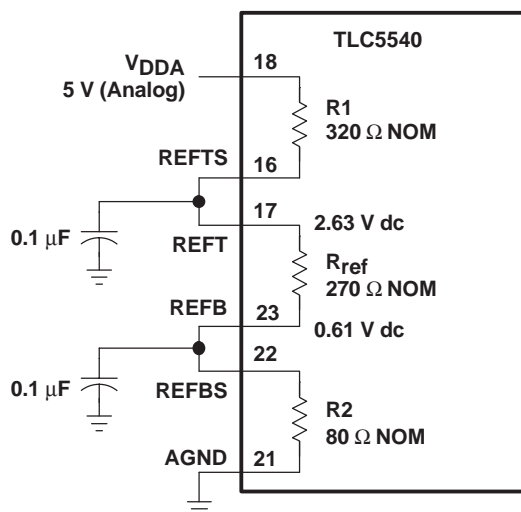
Internal resistors are provided to develop  $REFT = 2.6\text{ V}$  and  $REFB = 0.6\text{ V}$  (bias option one) with only two external connections. This is developed with a 3-resistor network connected to  $V_{DDA}$ . When using this feature, connect REFT to REFTS and connect REFB to REFBS. For applications where the variance associated with  $V_{DDA}$  is acceptable, this internal voltage reference saves space and cost (see Figure 14).

A second internal bias option (bias two option) is shown in Figure 15. Using this scheme  $REFB = AGND$  and  $REFT = 2.28\text{ V}$  nominal. These bias voltage options can be used to provide the values listed in the following table.

**Table 1. Bias Voltage Options**

BIAS OPTION	BIAS VOLTAGE		
	$V_{RB}$	$V_{RT}$	$V_{RT} - V_{RB}$
1	0.61	2.63	2.02
2	AGND	2.28	2.28

To use the internally-generated reference voltage, terminal connections should be made as shown in Figure 14 or Figure 15. The connections in Figure 14 provide the standard video 2-V reference.



**Figure 14. External Connections Using the Internal Bias One Option**

PRINCIPLES OF OPERATION

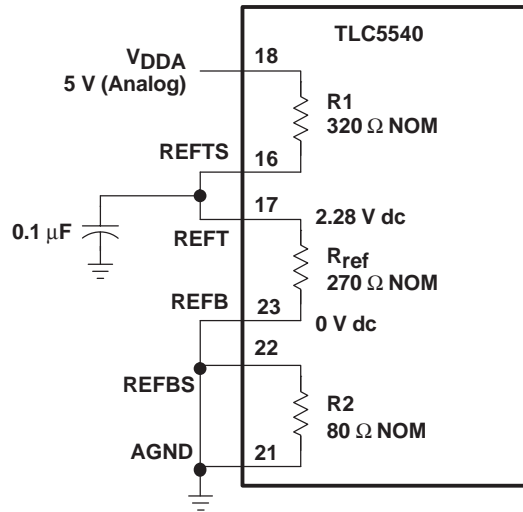


Figure 15. External Connections Using the Internal Bias Two Option

functional operation

Table 2 shows the TLC5540 functions.

Table 2. Functional Operation

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB							LSB
$V_{ref(T)}$	255	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	128	1	0	0	0	0	0	0	0
•	127	0	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
$V_{ref(B)}$	0	0	0	0	0	0	0	0	0

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5540CPW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	P5540	<a href="#">Samples</a>
TLC5540INSR	ACTIVE	SO	NS	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC5540I	<a href="#">Samples</a>
TLC5540IPW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	Y5540	<a href="#">Samples</a>
TLC5540IPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	Y5540	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5540INSR	SO	NS	24	2000	330.0	24.4	8.5	15.3	2.6	12.0	24.0	Q1
TLC5540IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5540INSR	SO	NS	24	2000	350.0	350.0	43.0
TLC5540IPWR	TSSOP	PW	24	2000	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLC5540CPW	PW	TSSOP	24	60	530	10.2	3600	3.5
TLC5540IPW	PW	TSSOP	24	60	530	10.2	3600	3.5

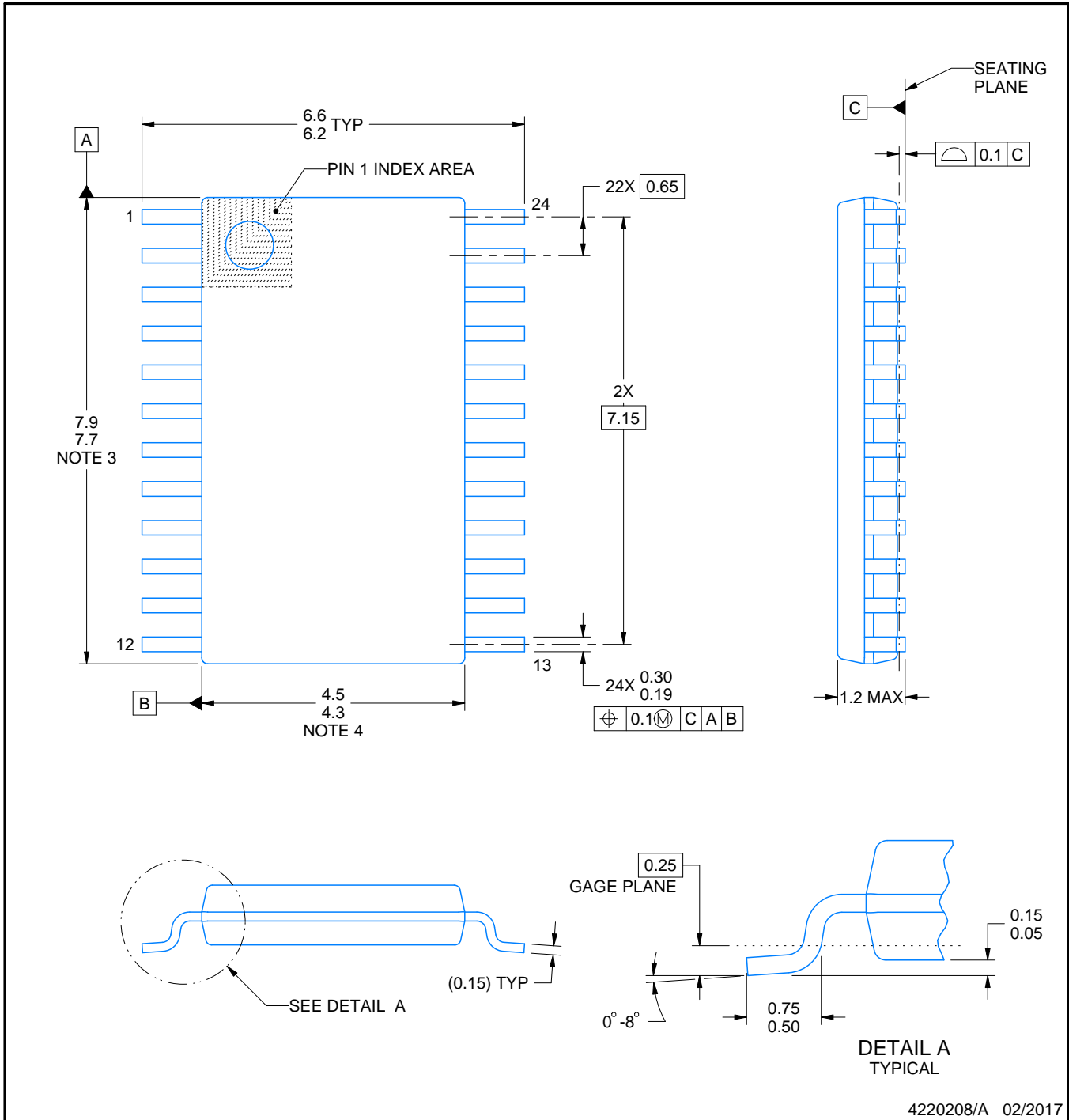
PW0024A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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