TLV8x3 3-Pin Voltage Supervisors with Active-Low, Open-Drain Reset

1 Features

- 3-Pin SOT23 Package
- Supply Current: 9 µA (Typical)
- Precision Supply Voltage Monitor: 2.5 V, 3 V, 3.3 V, 5 V
- Power-On Reset Generator with Fixed Delay Time of 200 ms
- Pin-for-Pin Compatible with MAX803
- Temperature Range: –40°C to +125°C
- Open-Drain, $\overline{RESET}$ Output

2 Applications

- Factory Automation
- Portable and Battery-Powered Equipment
- Set-Top Boxes
- Servers
- Appliances
- Electricity Meters
- Building Automation

3 Description

The TLV8x3 family of supervisory circuits provides circuit initialization and timing supervision, primarily for DSPs and processor-based systems.

The TLV803, TLV853, and TLV863 are functionally equivalent. The TLV853 and TLV863 provide an alternate pinout of the TLV803. The newer TLV803E device is a pin-to-pin alternative to all of these 3.

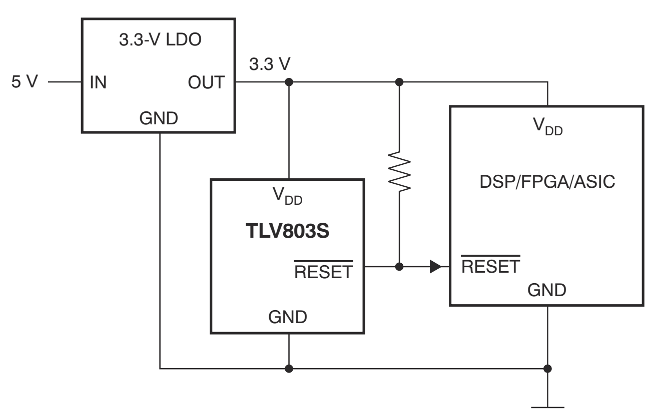
During power on, $\overline{RESET}$ asserts when the supply voltage (V_{DD}) exceeds 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps $\overline{RESET}$ active as long as V_{DD} remains below the threshold voltage V_{IT}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time ($t_{d(typ)}$ = 200 ms) starts after V_{DD} exceeds the threshold voltage, V_{IT}. When the supply voltage drops below the V_{IT} threshold voltage, the output is active (low) again. All the devices in this family have a fixed sense-threshold voltage (V_{IT}) set by an internal voltage divider.

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. These devices are available in a 3-pin SOT-23 package. The TLV803 devices are characterized for operation over a temperature range of –40°C to +125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV8x3	SOT-23 (3)	2.92 mm × 1.30 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Typical Application

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (November 2020) to Revision E (December 2020) **Page**

- Corrected missed VDD change from 7 to 6.5 in *Absolute Maximum Ratings* in note 2 ... 5

Changes from Revision C (September 2015) to Revision D (November 2020) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document ... 1
- Added new sentence regarding TLV803E to *Description* section ... 1
- Changed VDD from 7 to 6.5 in *Absolute Maximum Ratings* ... 5
- Changed V_{OL}@ 500µA from 0.2 to 0.3 in *Electrical Characteristics* ... 6
- Changed I_{OH} from 100 nA to 350 nA in *Electrical Characteristics* ... 6
- Changed t_w from 1 to 10 µs in *Switching Characteristics* ... 6
- Deleted figure Minimum Pulse Duration At V_{DD} vs Overdrive Voltage in Typical Characteristics ... 7
- Changed figure from Pulse Duration to V_{OL}, I_{OL} in the Typical Application Section ... 12

Changes from Revision B (August 2011) to Revision C (September 2015) **Page**

- Added TLV853 device to data sheet ... 1
- Changed device part numbers shown on page header to show single TLV803 device instead of lettered-device versions ... 1
- Added *Device Information* and *ESD Ratings* tables ... 1
- Added *Detailed Description*, *Application and Implementation*, *Power-Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Changed *Applications* section bullets ... 1
- Deleted pinouts from front page and moved to *Pin Configurations and Functions* section ... 1
- Changed "free-air temperature" to "junction temperature" in *Absolute Maximum Ratings* condition statement ... 5
- Deleted *Soldering temperature* from *Absolute Maximum Ratings* table ... 5
- Changed *Thermal Information* table; updated thermal resistance values for all parameters ... 5
- Changed "free-air temperature" to "junction temperature" in *Electrical Characteristics* condition statement ... 6

- Changed temperature noted in *Switching Characteristics* condition statement 6

Changes from Revision A (June 2011) to Revision B (August 2011)	Page

- Added new paragraph regarding TLV863 to *Description* section.. 1
- Added TLV863 pinout to front page.. 1
- Added TLV863 to Thermal Information..5
- Added TLV863M to Negative-Going Input Threshold Voltage parameter..6
- Added TLV863M to Hysteresis parameter..6
- Added TLV863 to Functional Block Diagram...8

5 Device Comparison

Table 5-1. Device Threshold Options

DEVICE	THRESHOLD VOLTAGE
TLV803Z	2.25 V
TLV803R	2.64 V
TLV803S	2.93 V
TLV803M	4.38 V
TLV853M	4.38 V
TLV863M	4.38 V

Table 5-2. Device Family Comparison

DEVICE	FUNCTION
TLV803	Open-Drain, $\overline{RESET}$ Output
TLV809	Push-Pull, $\overline{RESET}$ Output
TLV810	Push-Pull, RESET Output

6 Pin Configuration and Functions

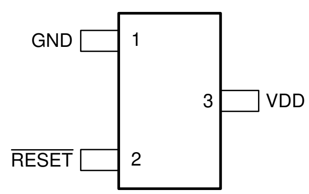


Figure 6-1. TLV803: DBZ Package 3-Pin SOT-23 Top View

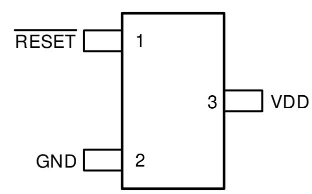


Figure 6-2. TLV853: DBZ Package 3-Pin SOT-23 Top View

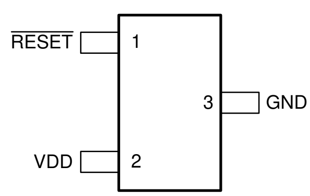


Figure 6-3. TLV863: DBZ Package 3-Pin SOT-23 Top View

Pin Functions

PIN				I/O	DESCRIPTION
NAME	TLV803	TLV853	TLV863		
GND	1	2	3	—	Ground pin.
$\overline{RESET}$	2	1	1	O	$\overline{RESET}$ is an open-drain output that is driven to a low impedance state when $\overline{RESET}$ is asserted. $\overline{RESET}$ remains low (asserted) for the delay time (t_d) after V_{DD} exceeds V_{IT-}. Use a 10-kΩ to 1-MΩ pullup resistor on this pin. The pullup voltage is not limited by V_{DD}.
VDD	3	3	2	I	Supply voltage pin. It is good analog design practice to place a 0.1-μF ceramic capacitor close to this pin.

7 Specifications

7.1 Absolute Maximum Ratings [(1)]

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage	VDD[(2)]	0	6.5	V
	All other pins[(2)]	–0.3	+6.5	
Current	Maximum low output current, I_{OL}		5	mA
	Maximum high output current, I_{OH}		–5	
	Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)		±20	
	Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)		±20	
Temperature	Operating junction temperature range, T_J	–40	125	°C
	Storage temperature range, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND. For reliable operation the device should not be operated at 6.5 V for more than t = 1000h continuously

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Thermal Information

THERMAL METRIC[(1)]		TLV8x3	UNITS
		DBZ (SOT-23)	
		3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	328.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	135.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	59.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.4 Recommended Operating Conditions

at specified temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	1.1	6	V
T_J	Operating junction temperature	–40	125	°C

7.5 Electrical Characteristics

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage		V_{DD} = 2 V to 6 V, I_{OL} = 500 µA			0.3	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA			0.4	
			V_{DD} = 6 V, I_{OL} = 4 mA			0.4	
	Power-up reset voltage[(1)]		I_{OL} = 50 µA, V_{OL} < 0.2 V	1.1			V
V_{IT-}	Negative-going input threshold voltage[(2)]	TLV803Z	T_J = – 40°C to +125°C	2.20	2.25	2.30	V
		TLV803R		2.58	2.64	2.70	
		TLV803S		2.87	2.93	2.99	
		TLV8x3M		4.28	4.38	4.48	
V_{hys}	Hysteresis	TLV803Z	T_J = 25°C, I_{OL} = 50 µA		30		mV
		TLV803R			35		
		TLV803S			40		
		TLV8x3M			60		
I_{DD}	Supply current		V_{DD} = 2 V, output unconnected		9	15	µA
			V_{DD} = 6 V, output unconnected		20	30	
I_{OH}	Output leakage current		V_{DD} = 6 V			350	nA

(1) The lowest supply voltage at which $\overline{\text{RESET}}$ becomes valid. $t_{r,VDD}$ ≤ 66.7 V/ms.
(2) To ensure best stability of the threshold voltage, place a bypass capacitor (0.1-µF ceramic) near the supply terminals.

7.6 Switching Characteristics

over operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse duration at V_{DD}	V_{DD} = 1.08 V_{IT-} to 0.92 V_{IT-}		10		µs
t_d	Delay time	V_{DD} ≥ V_{IT-} + 0.2 V; see Timing Diagram	120	200	280	ms

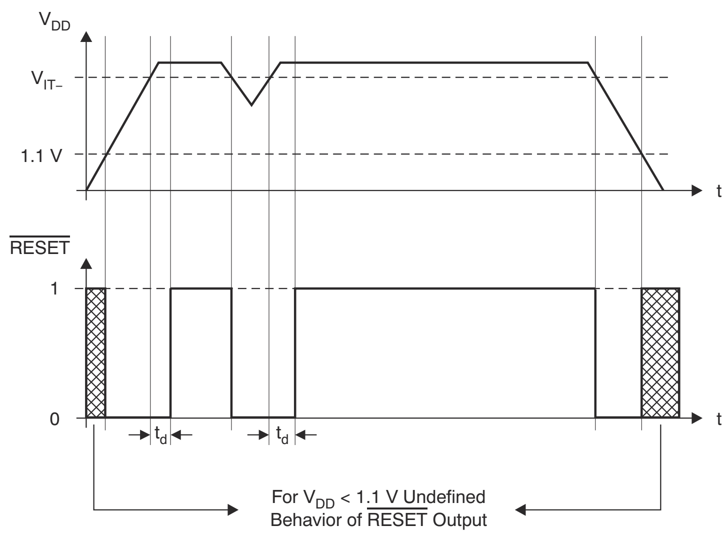


Figure 7-1. Timing Diagram

7.7 Typical Characteristics

at T_J = 25°C, V_{IT-} = 4.38 V, and V_{DD} = 5.0 V (unless otherwise noted)

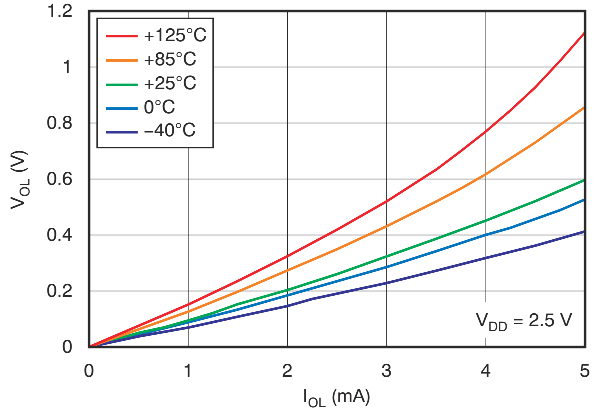


Figure 7-2. Low-Level Output Voltage vs Low-Level Output Current

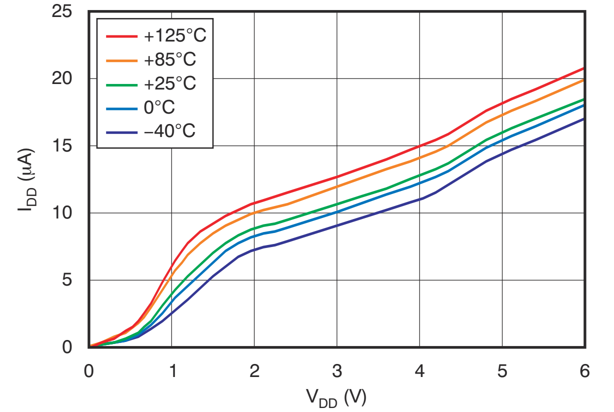


Figure 7-3. Supply Current vs Supply Voltage

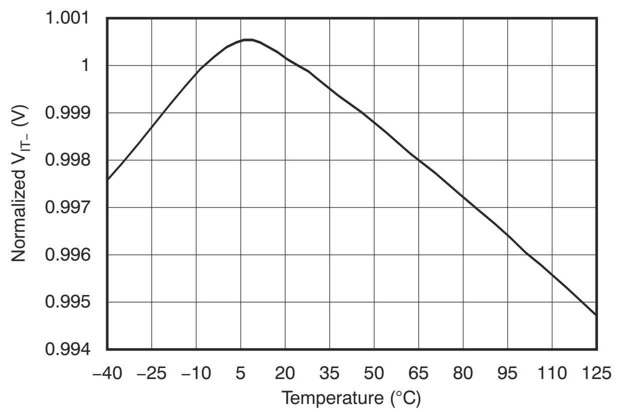


Figure 7-4. Normalized to 25°C Negative-Going Input Threshold Voltage vs Temperature

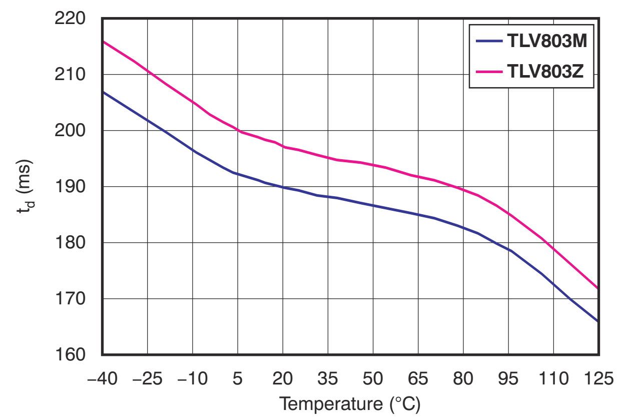


Figure 7-5. Delay Time vs Temperature

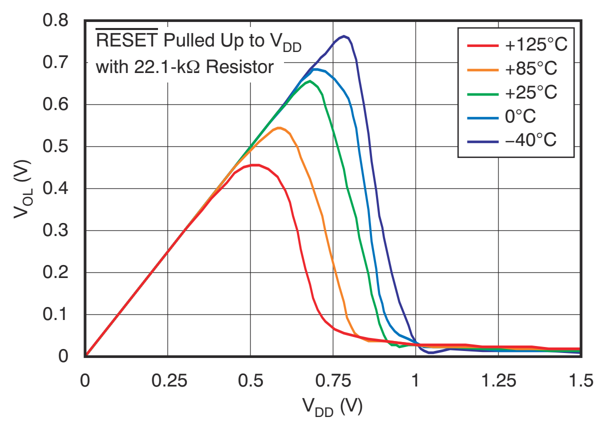


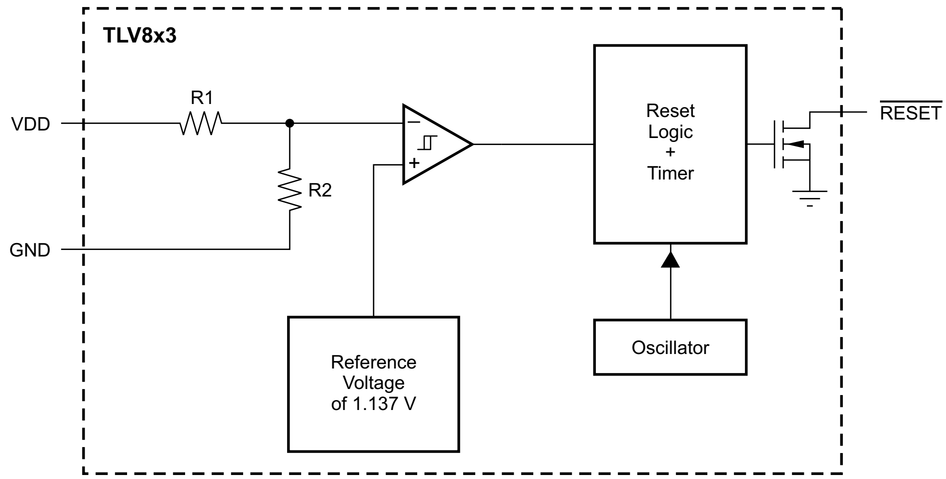
Figure 7-6. Power-Up Low-Level Output Voltage vs Supply Voltage

8 Detailed Description

8.1 Overview

The TLV803 family of supervisory circuits provides circuit initialization and timing supervision. The TLV853 and TLV863 are both functionally equivalent to the TLV803. These devices output a logic low whenever V_{DD} drops below the negative-going threshold voltage (V_{IT-}). The output, $\overline{\text{RESET}}$, remains low for approximately 200 ms after the V_{DD} voltage exceeds the positive-going threshold voltage ($V_{IT-} + V_{hys}$). These devices are designed to ignore fast transients on the V_{DD} pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 V_{DD} Transient Rejection

The TLV803 has built-in rejection of fast transients on the V_{DD} pin. The rejection of transients depends on both the duration and the amplitude of the transient. The amplitude of the transient is measured from the bottom of the transient to the negative threshold voltage of the TLV803, as shown in Figure 8-1.

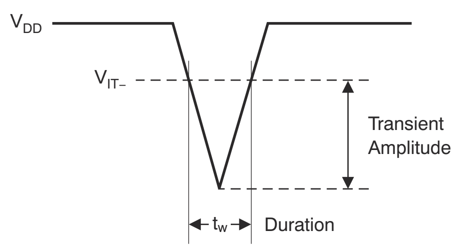


Figure 8-1. Voltage Transient Measurement

The TLV803 does not respond to transients that are fast duration/low amplitude or long duration/small amplitude. Transients meeting or longer than the t_w specified in the switching characteristics section triggers a reset.

8.3.2 Reset During Power Up and Power Down

The TLV803 output is valid when V_{DD} is greater than 1.1 V. When V_{DD} is less than 1.1 V, the output transistor turns off and becomes high impedance. The voltage on the $\overline{RESET}$ pin rises to the voltage level connected to the pull-up resistor. Figure 8-2 shows a typical waveform for power-up, assuming the $\overline{RESET}$ pin has a pull-up resistor connected to the V_{DD} pin.

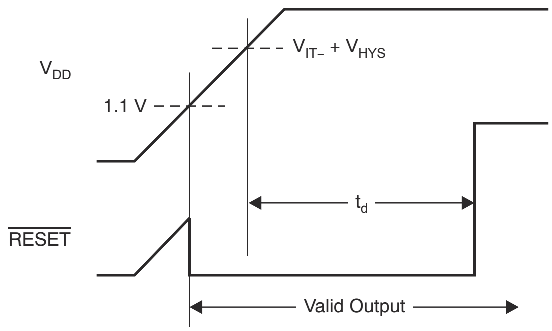


Figure 8-2. Power-Up Response

8.3.3 Bidirectional Reset Pins

Some microcontrollers have bidirectional reset pins that act as both inputs and outputs. In a situation where the TLV803 is pulling the $\overline{RESET}$ line low while the microcontroller is trying the force the $\overline{RESET}$ line high, a series resistor should be placed between the output of the TLV803 and the $\overline{RESET}$ pin of the microcontroller to protect against excessive current flow. Figure 8-3 shows the connection of the TLV803 to a microcontroller using a series resistor to drive a bidirectional $\overline{RESET}$ line.

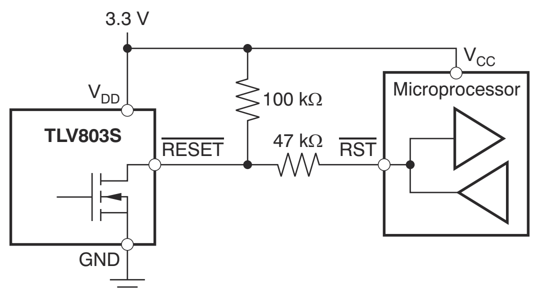


Figure 8-3. Connection To Bidirectional Reset Pin

8.4 Device Functional Modes

8.4.1 Normal Operation (VDD > Power-Up Reset Voltage)

When the voltage on VDD is greater than 1.1 V, the $\overline{RESET}$ signal asserts when V_{DD} is less than V_{IT-} and deasserts when V_{DD} is greater thanV_{IT-}.

8.4.2 Power On Reset (VDD < Power-Up Reset Voltage)

When the voltage on VDD is lower than the required voltage to internally pull the asserted output to GND (power-up reset voltage), both outputs are in a high-impedance state.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Monitoring Multiple Supplies

Because the TLV803 has an open-drain output, multiple TLV803 outputs can be directly tied together to form a logical OR-ing function for the $\overline{\text{RESET}}$ line. Only one pull-up resistor is required for this configuration. Figure 9-1 shows two TLV803s connected together to provide monitoring of a 3.3-V power rail and a 5.0-V power rail. A reset is generated if either power rail falls below the threshold voltage of its corresponding TLV803.

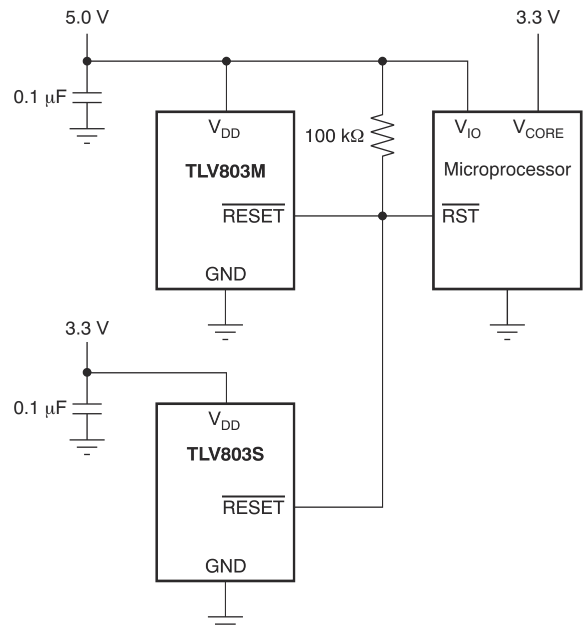


Figure 9-1. Multiple Voltage Rail Monitoring

9.1.2 Output Level Shifting

The $\overline{\text{RESET}}$ output of the TLV803 can be pulled to a maximum voltage of 6 V and can be pulled higher in voltage than V_{DD}. It is useful to provide level shifting of the output for cases where the monitored voltage is less than the useful logic levels of the load. Figure 9-2 shows the TLV803Z used to monitor a 2.5-V power rail, with a logic $\overline{\text{RESET}}$ input to a microprocessor that is connected to 5.0 V and has 5.0-V logic levels.

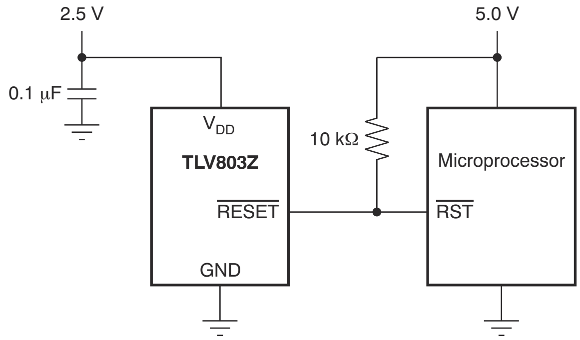


Figure 9-2. Output Voltage Level Shifting

9.2 Typical Application

Figure 9-3 shows TLV803S being used to monitor the supply rail for a DSP, FPGA, or ASIC.

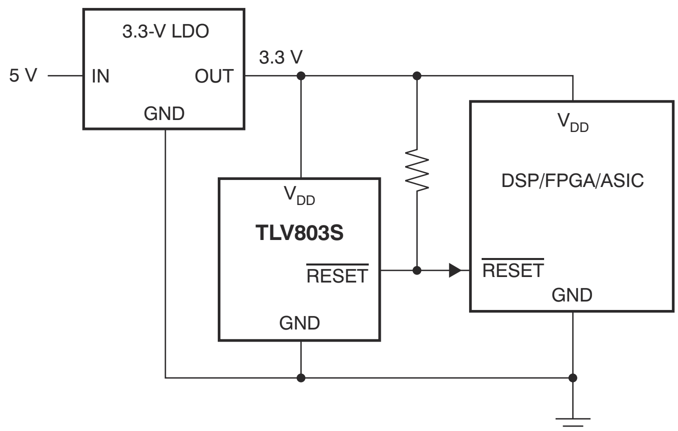


Figure 9-3. Typical Application

9.2.1 Design Requirements

This design calls for a 3.3-V rail to be monitored. The design resets if the supply rail falls below 2.93 V. The output must satisfy 3.3-V CMOS logic.

9.2.2 Detailed Design Procedure

Select the TLV803S to satisfy the voltage threshold requirement.

Place a pullup resistor on $\overline{\text{RESET}}$ to VDD in order to satisfy the output logic requirement.

9.2.3 Application Curves

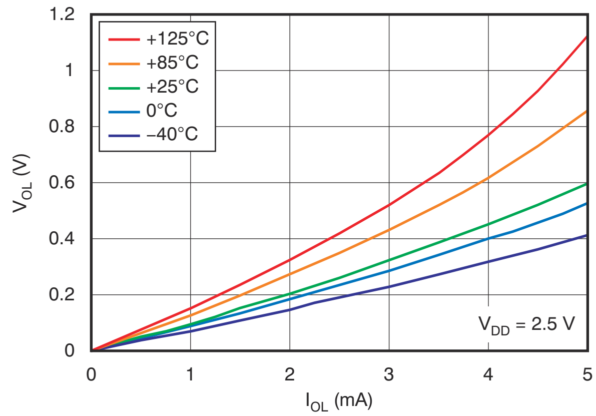


Figure 9-4. Low-Level Output Voltage vs Low-Level Output Current

10 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 1.1 V and 6 V.

11 Layout

11.1 Layout Guidelines

Place the C_{IN} decoupling capacitor close to the device.

11.2 Layout Example

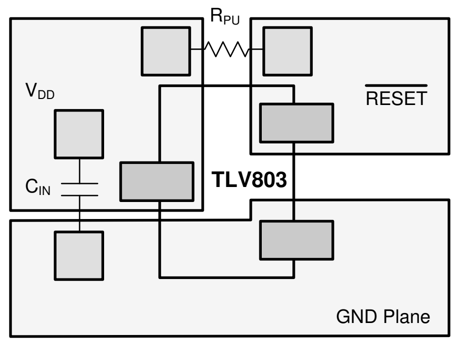


Figure 11-1. Layout Example (DBZ Package)

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV803. The TLV803SEVM-019 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

12.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. SPICE models for the TLV803, TLV853, and TLV863 are available through the respective device product folders under *Tools & Software*.

12.2 Documentation Support

12.2.1 Related Documentation

- TLV803SEVM-019 User's Guide. Literature number SLVU461.

12.3 Related Links

Table 12-1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV803	Click here	Click here	Click here	Click here	Click here
TLV853	Click here	Click here	Click here	Click here	Click here
TLV863	Click here	Click here	Click here	Click here	Click here

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV803MDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	VOUQ	Samples
TLV803MDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	VOUQ	Samples
TLV803RDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VOSQ	Samples
TLV803RDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	VOSQ	Samples
TLV803SDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VOTQ	Samples
TLV803SDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	VOTQ	Samples
TLV803ZDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VORQ	Samples
TLV803ZDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	VORQ	Samples
TLV853MDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	ZGM4	Samples
TLV853MDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	ZGM4	Samples
TLV863MDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	VTWM	Samples
TLV863MDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	VTWM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

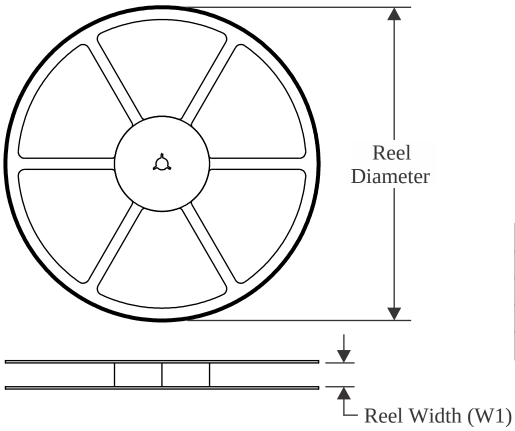
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

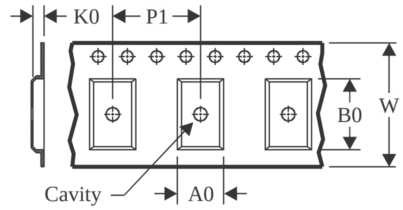
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

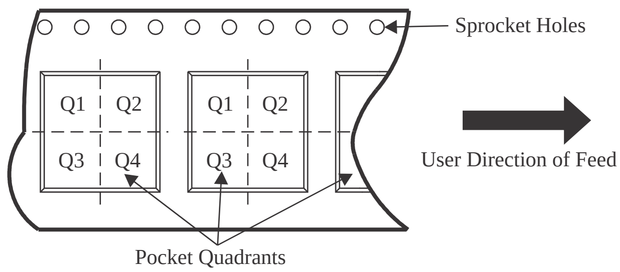


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

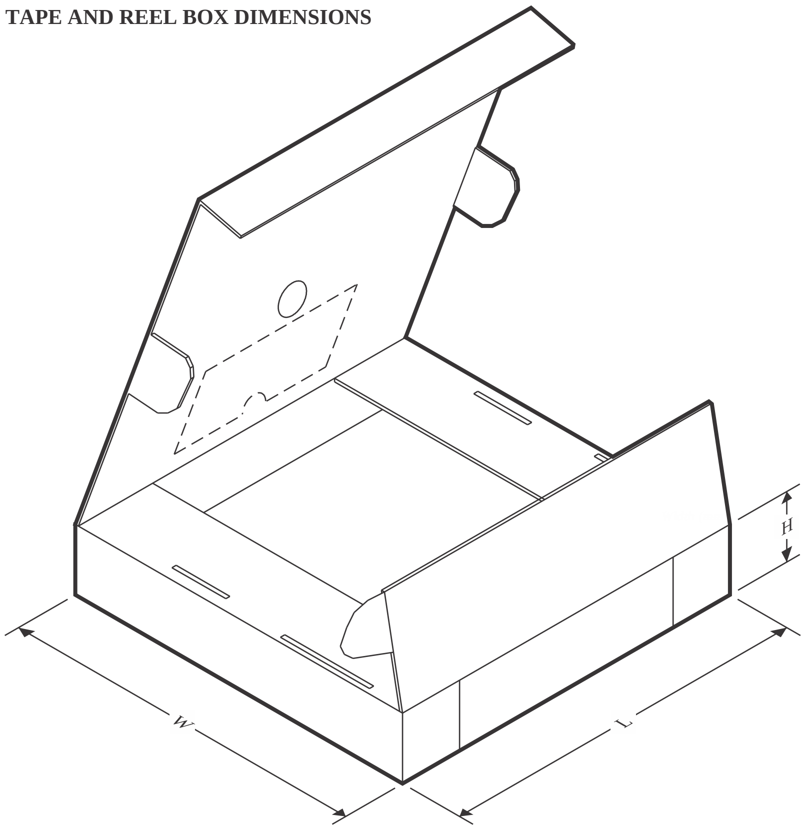
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

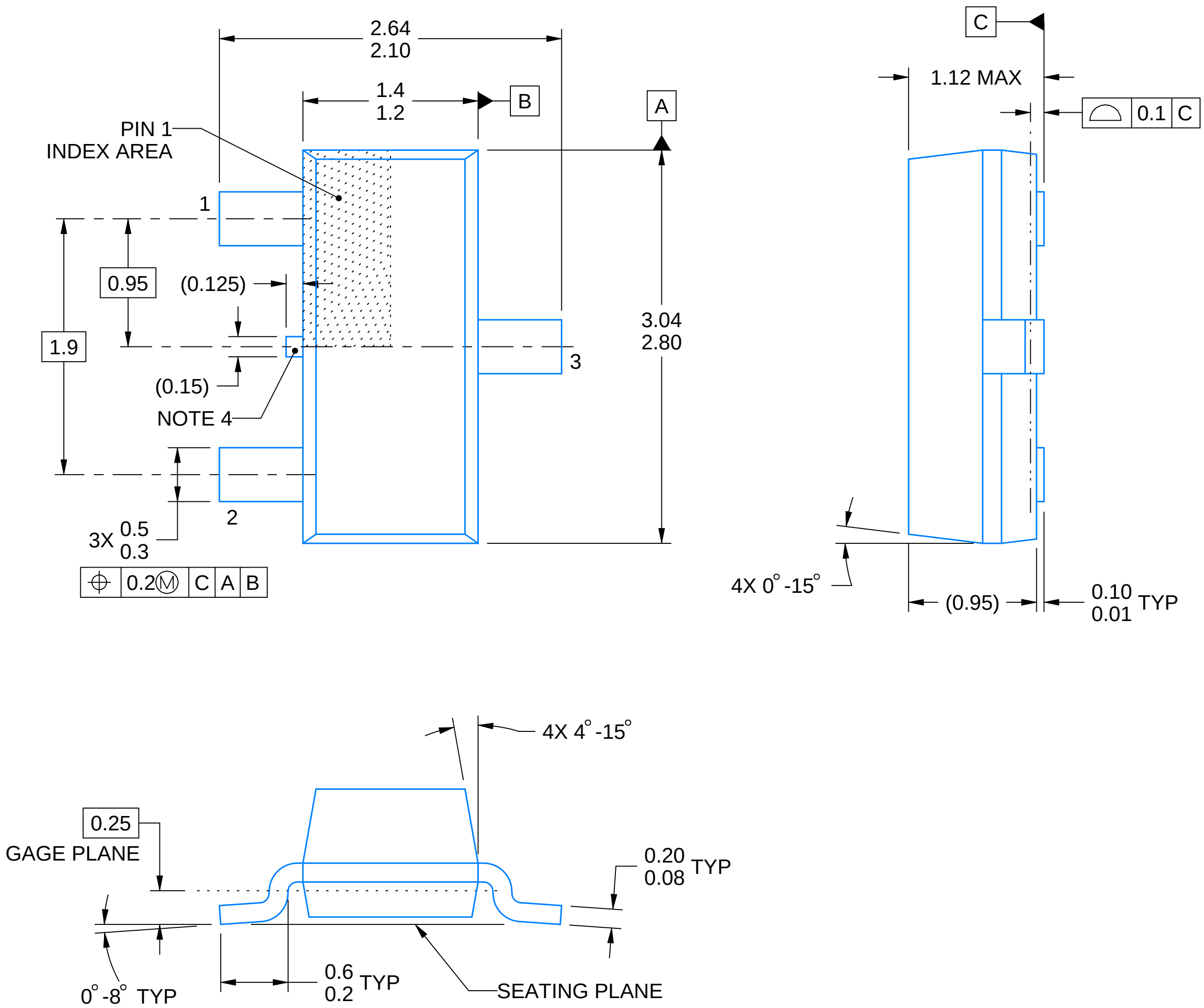
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV803MDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803MDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803RDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLV803RDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803SDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLV803SDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV803ZDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TLV803ZDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV853MDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV853MDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV863MDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV863MDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV803MDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV803MDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TLV803RDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV803RDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TLV803SDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV803SDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TLV803ZDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TLV803ZDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TLV853MDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV853MDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TLV863MDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV863MDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0



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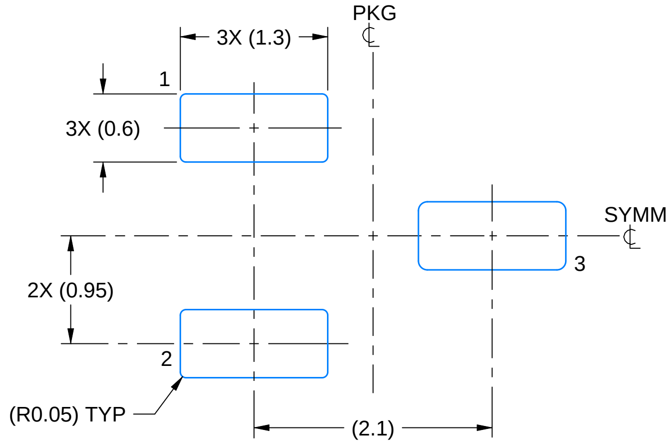
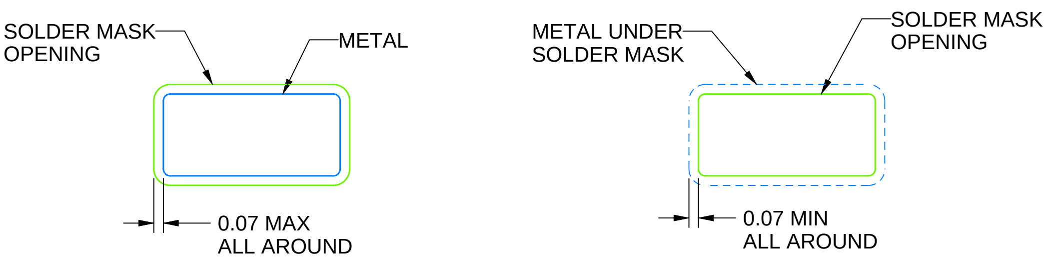
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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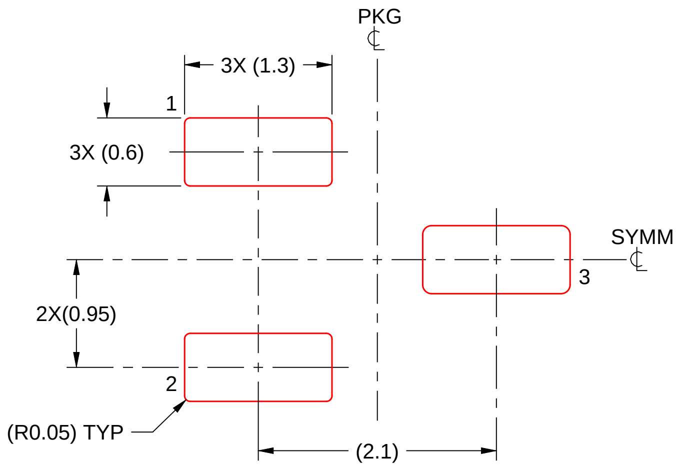
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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