TLV914x 18V, Rail-to-Rail Input and Output, 125kHz Low Power (7µA/Channel) Operational Amplifier

1 Features

- Wide supply voltage: 2.7V to 18V
- Low quiescent current: 7µA per amplifier
- Rail-to-rail input and output
- Low offset voltage: ±265µV (typical)
- Low offset voltage drift: ±0.2µV/°C (typical)
- High PSRR: 140dB (typical)
- Wide bandwidth: 125kHz GBW, unity-gain stable
- High output current drive: ±40mA
- Low 1/f flicker noise: 3.4µVp-p (f = 0.1Hz to 10Hz)
- High common-mode rejection: 108dB
- Internal RFI and EMI filtered input pins
- Operating temperature range: –40°C to 125°C

2 Applications

- Smoke & heat detector
- Field transmitter & sensor
  - Flow transmitter
  - Pressure transmitter
  - Temperature transmitter
  - Level transmitter
- Blood glucose monitor
- Oxygen concentrator
- IP network camera
- Motion detector

3 Description

The TLV914x family (TLV9141, TLV9142, and TLV9144) is a family of high voltage (18V) rail-to-rail input and output (RRIO) operational amplifiers. These devices offer excellent performance for low-power applications, because of the family's low quiescent current of 7µA/channel.

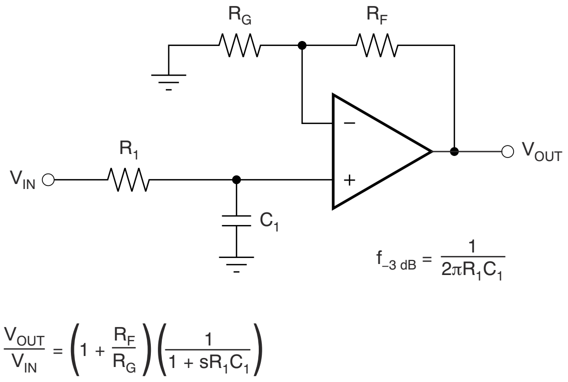
The TLV914x family offers excellent DC precision, including low offset voltage (±265µV, typical), low offset drift (±0.2µV/°C, typical), short-circuit current limit of 40mA, high PSRR of 140dB, and high CMRR of 108dB for high voltage operation within the main input pair. The devices are also rated to work at wide range of supply voltages from 2.7V to 18V. This makes the TLV914x a flexible, robust, and high-performance op amp for high-voltage industrial applications.

These devices also have a gain bandwidth product of 125kHz and low 1/f flicker noise of 3.4µV$_{\text{peak-to-peak}}$ (0.1Hz to 10Hz). The family was designed to be able to directly drive capacitive loads up to 350nF, while maintaining a phase margin of 30 degrees or higher. The TLV914x op amp family is available in several industry-standard packages and the devices are specified from –40°C to 125°C.

Package Information

PART NUMBER	CHANNEL COUNT	PACKAGE[1]	PACKAGE SIZE[2]
TLV9141	Single	DBV (SOT-23, 5)	2.9mm × 2.8mm
		D (SOIC, 8)	4.9mm × 6mm
TLV9142	Dual	PW (TSSOP, 8)	3mm × 6.4mm
		D (SOIC, 8)	4.9mm × 6mm
TLV9144	Quad	D (SOIC, 14)	8.65mm × 6mm
		PW (TSSOP, 14)	5mm × 6.4mm
		N (PDIP, 14)	19.3mm × 7.94mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Single-Pole, Low-Pass Filter

Table of Contents

4 Pin Configuration and Functions

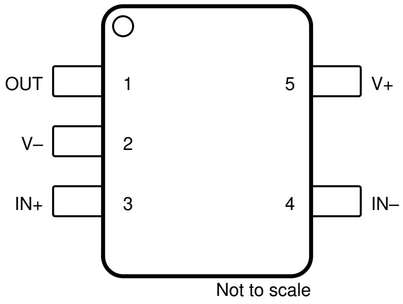
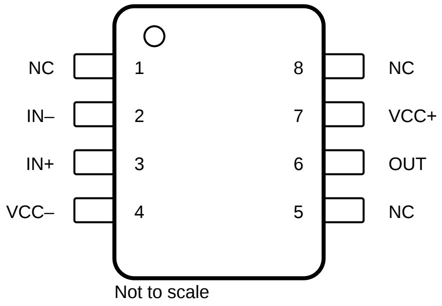


**Figure 4-1. TLV9141 DBV Package
5-Pin SOT-23
(Top View)**



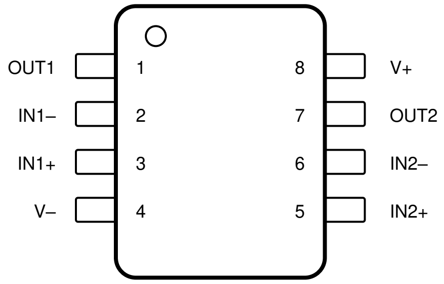
NC- no internal connection

**Figure 4-2. TLV9141 D Package
8-Pin SOIC
(Top View)**

Table 4-1. Pin Functions: TLV9141

PIN			TYPE[1]	DESCRIPTION
NAME	DBV	D		
IN–	4	2	I	Inverting input
IN+	3	3	I	Noninverting input
NC	—	1, 5, 8	—	Do not connect
OUT	1	6	O	Output
V–	2	4	—	Negative (lowest) power supply
V+	5	7	—	Positive (highest) power supply

(1) I = input, O = output



Not to scale

Figure 4-3. TLV9142 D, PW, and N Package, 8-Pin SOIC, TSSOP, and PDIP (Top View)

Table 4-2. Pin Functions: TLV9142

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2–	6	I	Inverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

(1) I = input, O = output

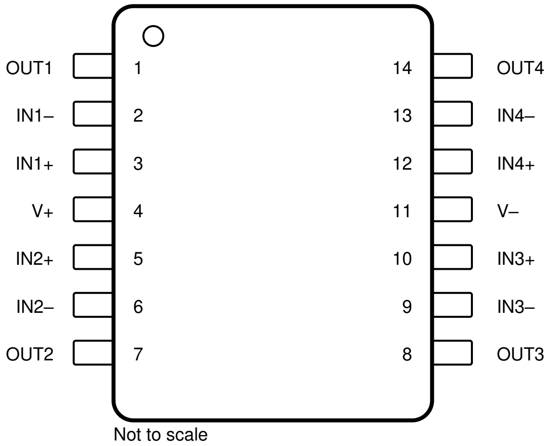


Figure 4-4. TLV9144 D and PW Package 14-Pin SOIC and TSSOP (Top View)

Table 4-3. Pin Functions: TLV9144

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2–	6	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3–	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4–	13	I	Inverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	20	V
Signal input pins	Common-mode voltage (3)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage (3)		V_S + 0.2	V
	Current (3)	–10	10	mA
Output short-circuit (2)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.

(2) Short-circuit to ground, one amplifier per package. This device has been designed to limit *electrical* damage due to excessive output current, but extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual *thermal* destruction.

(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	2.7	18	V
V_I	Input voltage range	(V–) – 0.2	(V+) + 0.2	V
T_A	Specified temperature	–40	125	°C

5.4 Thermal Information for Single Channel

THERMAL METRIC (1)		TLV9141		UNIT
		DBV (SOT-23)	D (SOIC)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	196.7	139.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	94.1	77.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.3	88.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	30.8	24.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.9	87.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Thermal Information for Dual Channel

THERMAL METRIC (1)		TLV9142		UNIT
		PW (TSSOP)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	162.2	129.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.1	68.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	101.4	78.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.2	17.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	99.8	77.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.6 Thermal Information for Quad Channel

THERMAL METRIC (1)		TLV9144			UNIT
		PW (TSSOP)	D (SOIC)	N (PDIP)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.2	90.4	72.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.7	50.6	50.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.0	48.5	46.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.6	11.6	28.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	69.3	48.0	45.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.7 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7V to 18V (±1.35V to ±9V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±0.265	±1	mV
			T_A = –40°C to 125°C			±1.5	mV
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±0.2		µV/°C
PSRR	Input offset voltage versus power supply	V_{CM} = V–, V_S = 5V to 18V	T_A = –40°C to 125°C		±0.112	±1	µV/V
					139	115	dB
		V_{CM} = V–, V_S = 2.7V to 18V(1)	T_A = –40°C to 125°C		±0.1	±1.8	µV/V
					140	114	dB
	Channel separation	f = 0Hz			5		µV/V
					106		dB
INPUT BIAS CURRENT							
I_B	Input bias current(1) (2)				±0.5	±10	pA
I_{OS}	Input offset current(1) (2)				±0.5	±10	pA
NOISE							
E_N	Input voltage noise	f = 0.1Hz to 10Hz			3.4		$µV_{PP}$
					0.5		$µV_{RMS}$
e_N	Input voltage noise density	f = 1kHz			50		nV/√Hz
i_N	Input current noise	f = 1kHz			0.5		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_S = 18V, (V–) – 0.1V < V_{CM} < (V+) – 2V (Main input pair)		99	108		dB
			T_A = –40°C to 125°C	99			
		V_S = 5V, (V–) – 0.1V < V_{CM} < (V+) – 2V (Main input pair)		86	94		
			T_A = –40°C to 125°C	85			
		V_S = 2.7V, (V–) – 0.1V < V_{CM} < (V+) – 2V (Main input pair)(1)		75	85		
			T_A = –40°C to 125°C	74			
		V_S = 2.7V to 18V, (V+) – 1V < V_{CM} < (V+) + 0.1V (Aux input pair)(1)			95		
			T_A = –40°C to 125°C	72			
		V_S = 18V, (V–) – 0.2V < V_{CM} < (V+) + 0.2V (Both input pairs)(1)		80	91		
			T_A = –40°C to 125°C	79			
		(V+) – 2V < V_{CM} < (V+) – 1V	T_A = –40°C to 125°C	See Input Offset Voltage vs Common-Mode Voltage			
INPUT CAPACITANCE							
Z_{ID}	Differential				500 || 3		GΩ || pF
Z_{ICM}	Common-mode				5 || 1		TΩ || pF

For V_S = (V+) – (V–) = 2.7V to 18V (±1.35V to ±9V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 18V, V_{CM} = V–, (V–) + 0.1V < V_O < (V+) – 0.1V		110	135		dB
			T_A = –40°C to 125°C		125		
		V_S = 5V, V_{CM} = V–, (V–) + 0.1V < V_O < (V+) – 0.1V		105	130		
			T_A = –40°C to 125°C		125		
		V_S = 2.7V, V_{CM} = V–, (V–) + 0.1V < V_O < (V+) – 0.1V(1)		100	120		
			T_A = –40°C to 125°C		115		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	R_L = 1MΩ			125		kHz
SR	Slew rate	V_S = 18V, G = +1, C_L = 20pF			0.1		V/µs
t_S	Settling time	To 0.01%, V_S = 18V, V_{STEP} = 10V , G = +1, C_L = 20pF			135		µs
		To 0.01%, V_S = 18V, V_{STEP} = 2V , G = +1, C_L = 20pF			68		
		To 0.1%, V_S = 18V, V_{STEP} = 10V , G = +1, C_L = 20pF			121		
		To 0.1%, V_S = 18V, V_{STEP} = 2V , G = +1, C_L = 20pF			51		
PM	Phase margin	G = +1, R_L = 100kΩ, C_L = 100pF			40		°
$t_{overload}$	Overload recovery time	V_{IN} × gain > V_S			35		µs
THD+N	Total harmonic distortion + noise (3)	V_S = 18V, V_O = $1V_{RMS}$, G = 1, f = 1kHz, R_L = 1MΩ			0.07		%
					73		dB
		V_S = 18V, V_O = $1V_{RMS}$, G = 1, f = 1kHz, R_L = 100kΩ			0.02		%
					63		dB
OUTPUT							
	Voltage output swing from rail	Positive and negative rail headroom	V_S = 18V, R_L = no load(1)		5	10	mV
			V_S = 18V, R_L = 10kΩ		50	60	
			V_S = 18V, R_L = 2kΩ		266	300	
			V_S = 2.7V, R_L = no load(1)		1	5	
			V_S = 2.7V, R_L = 10kΩ		12	20	
			V_S = 2.7V, R_L = 2kΩ		58	80	
I_{SC}	Short-circuit current				±40		mA
C_{LOAD}	Capacitive load drive				See Phase Margin vs Capacitive Load		pF
Z_O	Open-loop output impedance	I_O = 0A			See Open-Loop Output Impedance vs Frequency		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_{CM} = V–, I_O = 0A			7	9	µA
			T_A = –40°C to 125°C			9.5	

(1) Max value is specified by characterization only.
(2) Input differential voltages greater than 2.5V can cause increased I_B.
(3) Third-order filter; bandwidth = 80kHz at –3 dB.

5.8 Typical Characteristics

at T_A = 25°C, V_S = ±9V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)

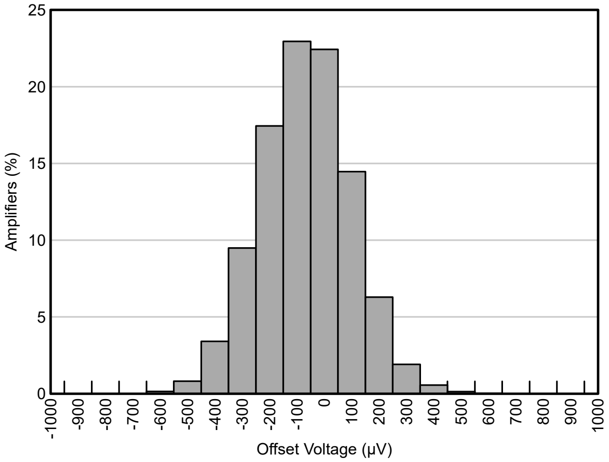


Figure 5-1. Offset Voltage Production Distribution

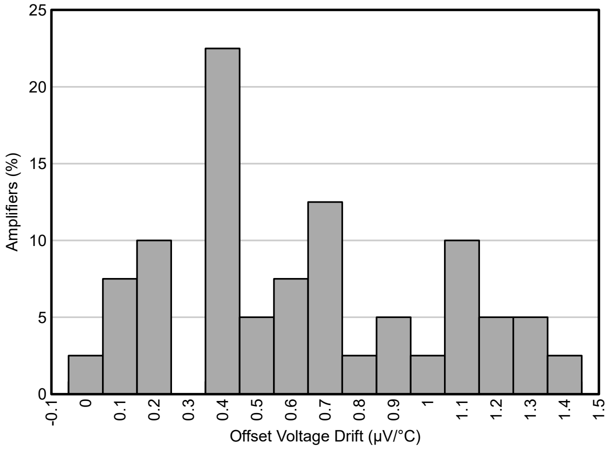
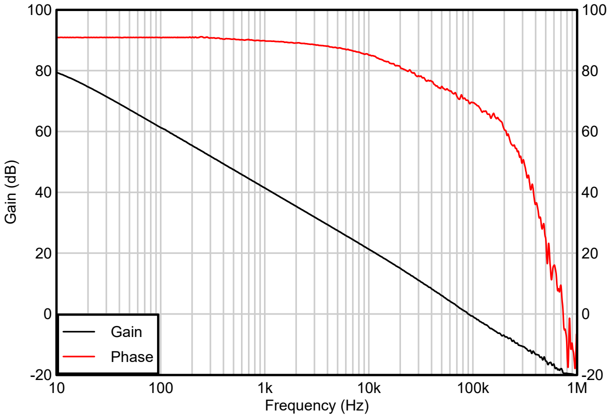
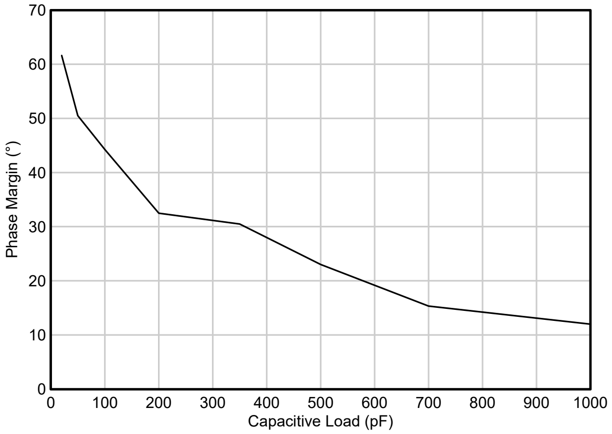


Figure 5-2. Offset Voltage Drift Distribution



R_L = 1MΩ, C_L = 20pF

Figure 5-3. Open-Loop Gain and Phase vs Frequency



R_L = 100kΩ

Figure 5-4. Phase Margin vs Capacitive Load

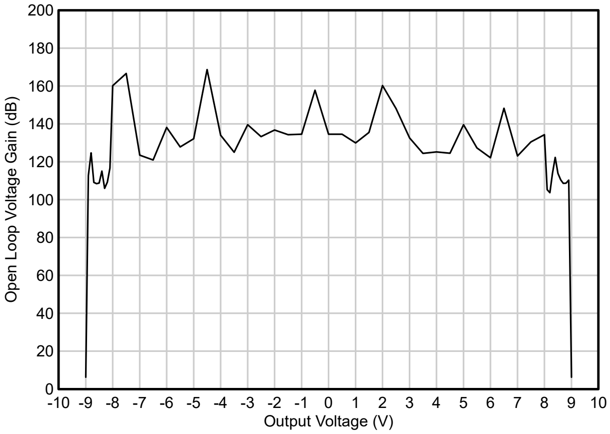
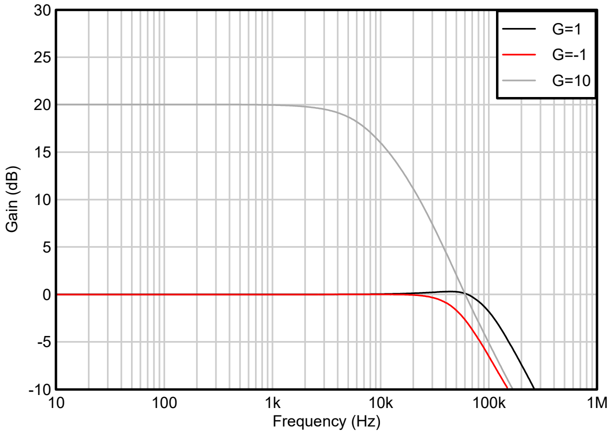


Figure 5-5. Open-Loop Gain vs Output Voltage



R_L = 1MΩ, C_L = 20pF

Figure 5-6. Closed-Loop Gain vs Frequency

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±9V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)

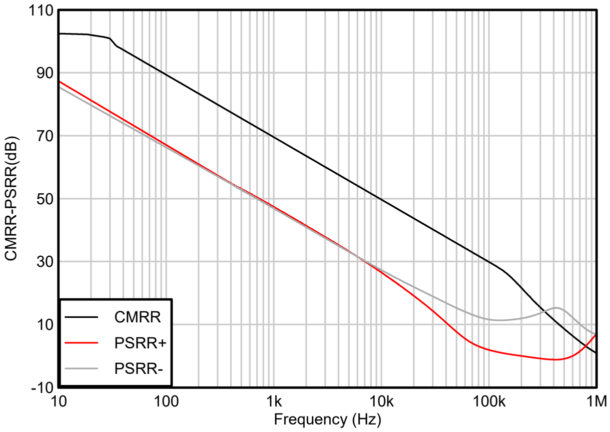


Figure 5-7. CMRR and PSRR vs Frequency

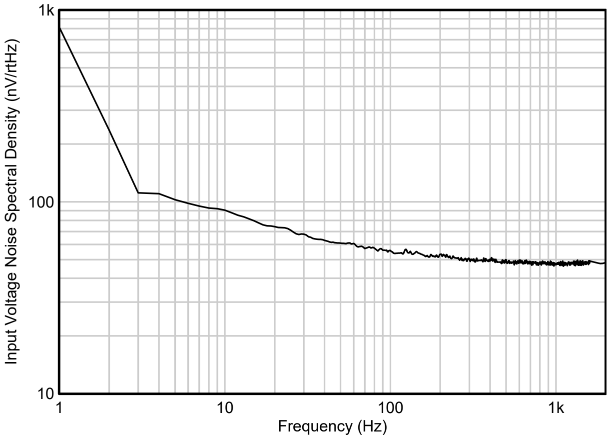
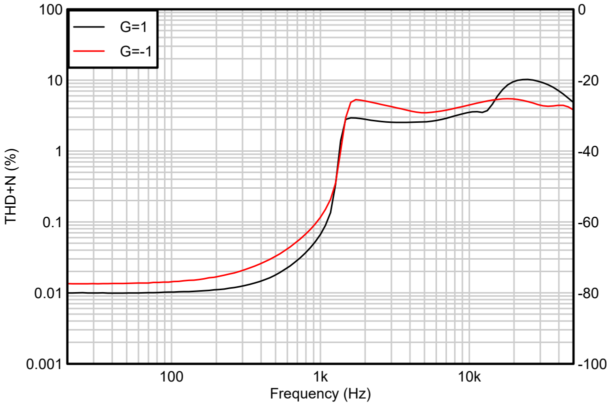
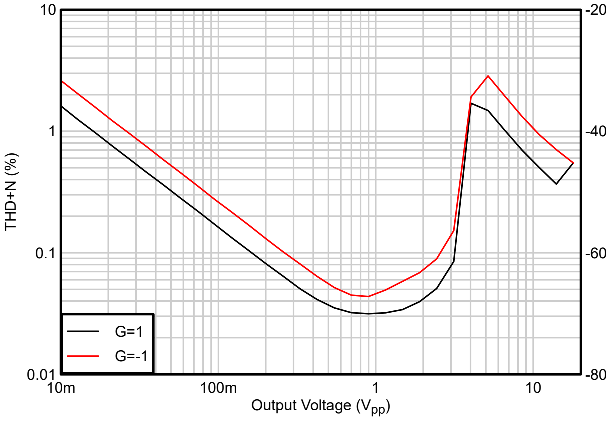


Figure 5-8. Input Voltage Noise Density vs Frequency



V_{OUT} = $1V_{RMS}$, R_L = 100kΩ

Figure 5-9. THD+N vs Frequency



f = 1kHz, R_L = 100kΩ

Figure 5-10. THD+N vs Output Voltage

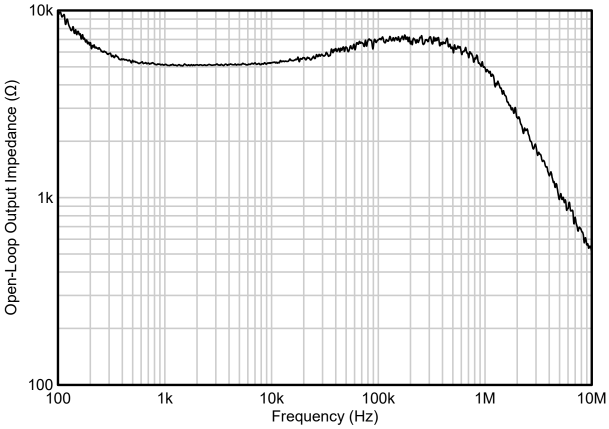


Figure 5-11. Open-Loop Output Impedance vs Frequency

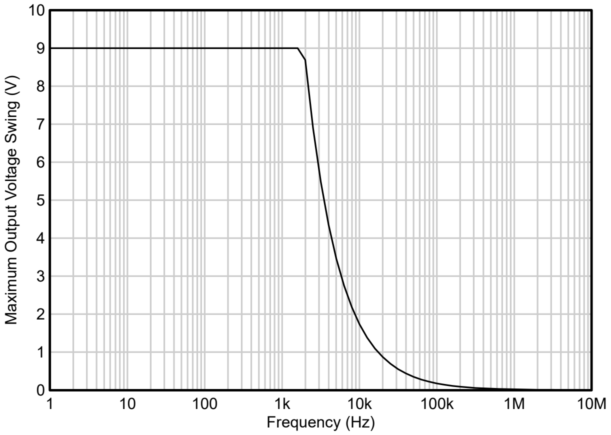


Figure 5-12. Maximum Output Voltage vs Frequency

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±9V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)

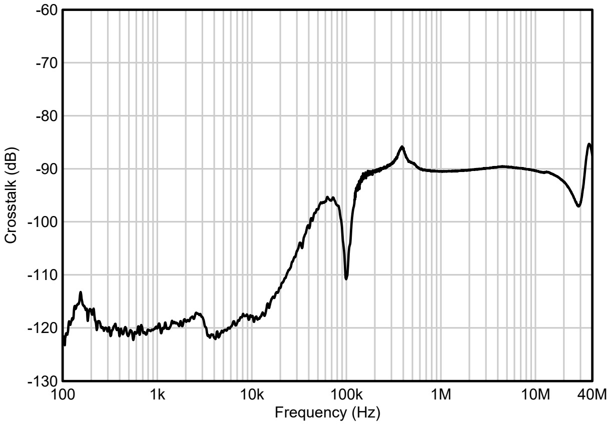


Figure 5-13. Crosstalk vs Frequency

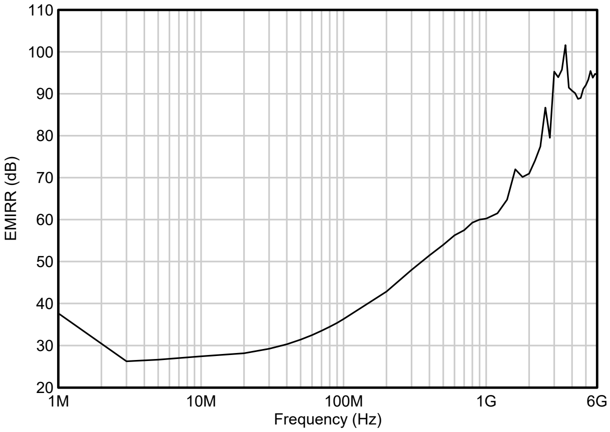
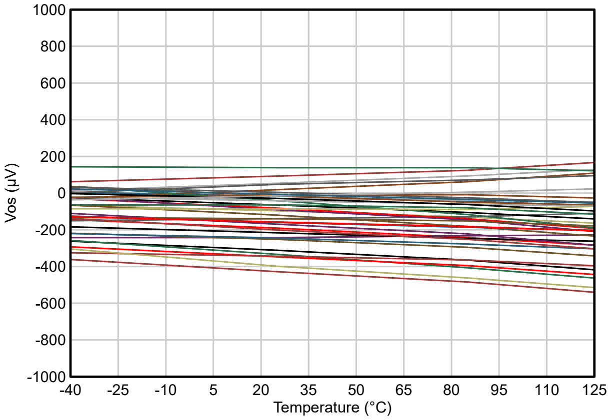
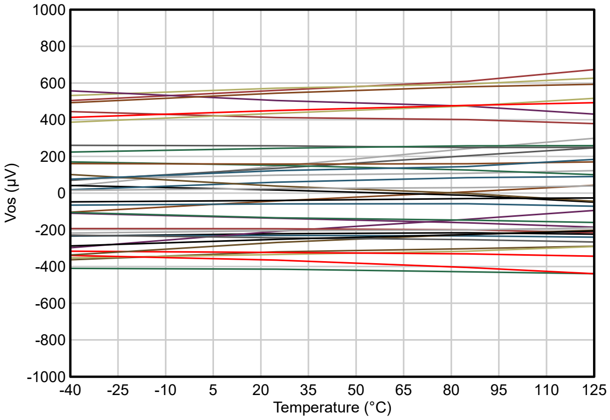


Figure 5-14. EMIRR vs Frequency



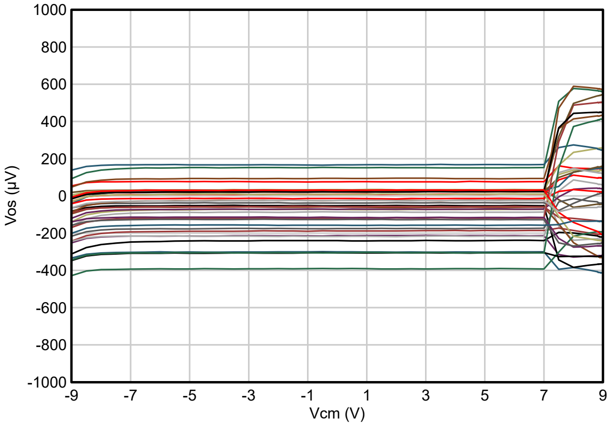
V_{CM} = V–

Figure 5-15. Input Offset Voltage vs Temperature



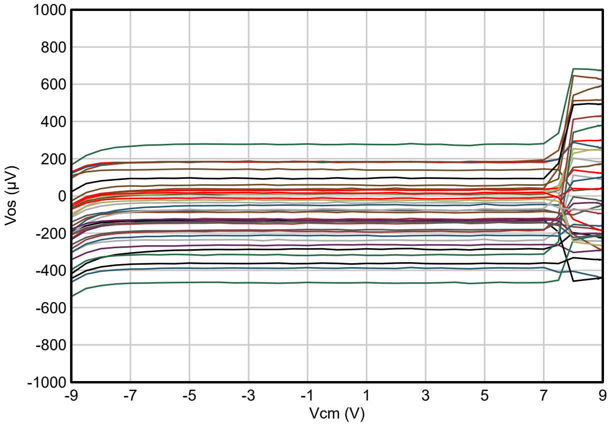
V_{CM} = V+

Figure 5-16. Input Offset Voltage vs Temperature



T = 25°C

Figure 5-17. Input Offset Voltage vs Common-Mode Voltage

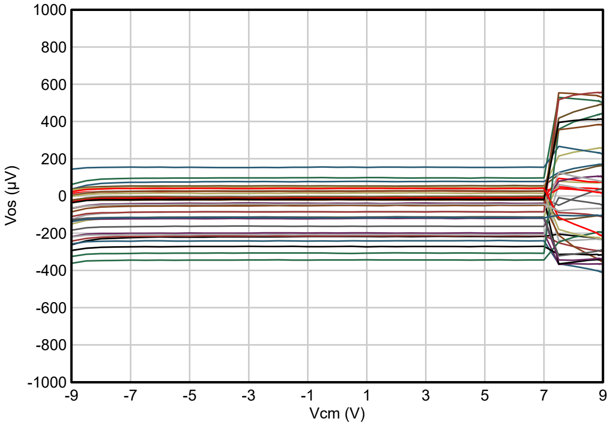


T = 125°C

Figure 5-18. Input Offset Voltage vs Common-Mode Voltage

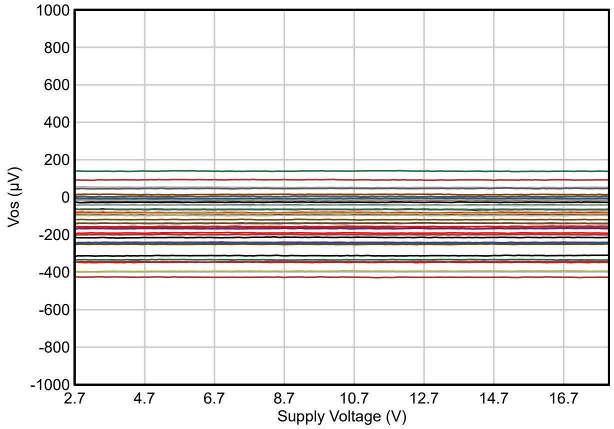
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±9V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



T = -40°C

Figure 5-19. Input Offset Voltage vs Common-Mode Voltage



V_S = 2.7V to 18V, V_{CM} = V–

Figure 5-20. Input Offset Voltage vs Supply Voltage

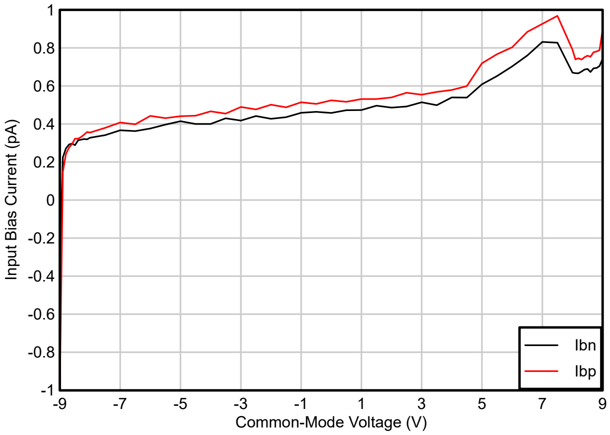


Figure 5-21. Input Bias Current vs Common-Mode Voltage

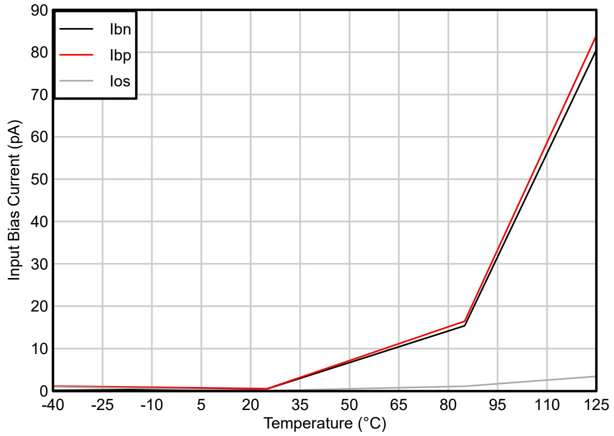
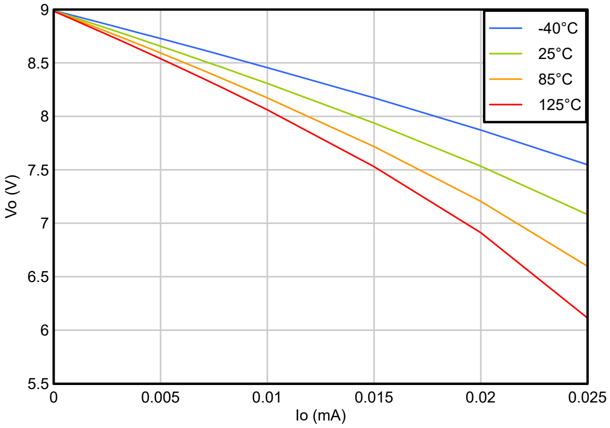
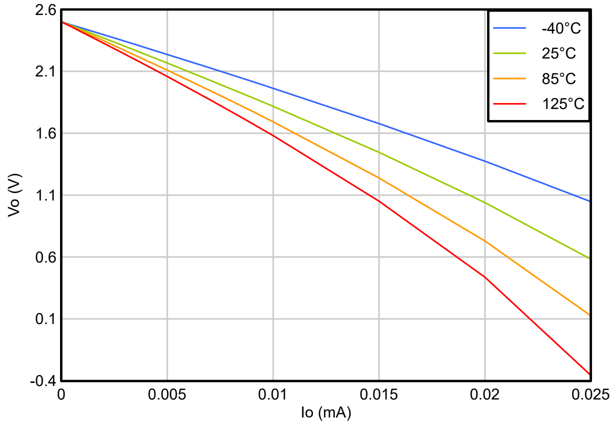


Figure 5-22. Input Bias Current vs Temperature



V_S = $\underline{+}$9V

Figure 5-23. Output Voltage Swing vs Output Current (Sourcing)

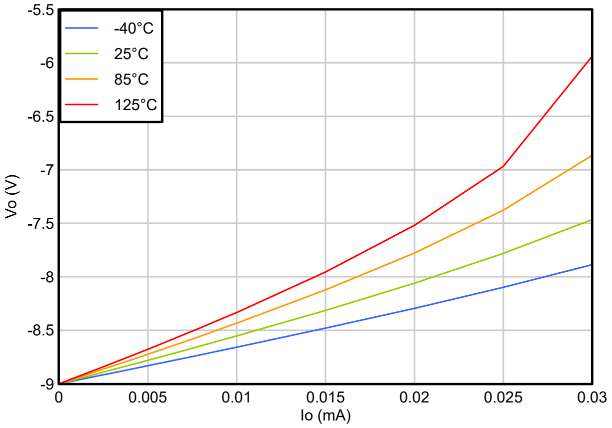


V_S = $\underline{+}$2.5V

Figure 5-24. Output Voltage Swing vs Output Current (Sourcing)

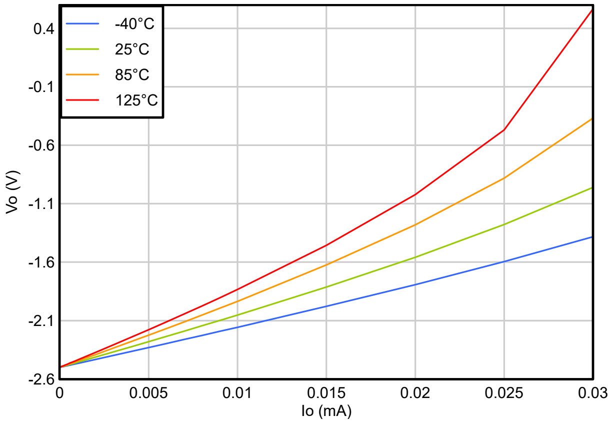
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±9V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



V_S = ±9V

Figure 5-25. Output Voltage Swing vs Output Current (Sinking)



V_S = ±2.5V

Figure 5-26. Output Voltage Swing vs Output Current (Sinking)

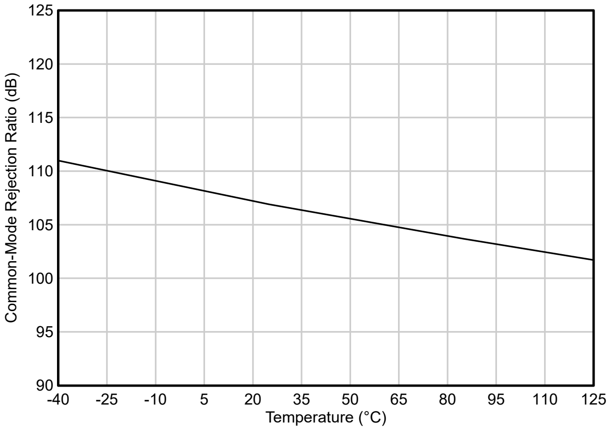


Figure 5-27. Common-Mode Rejection Ratio vs Temperature

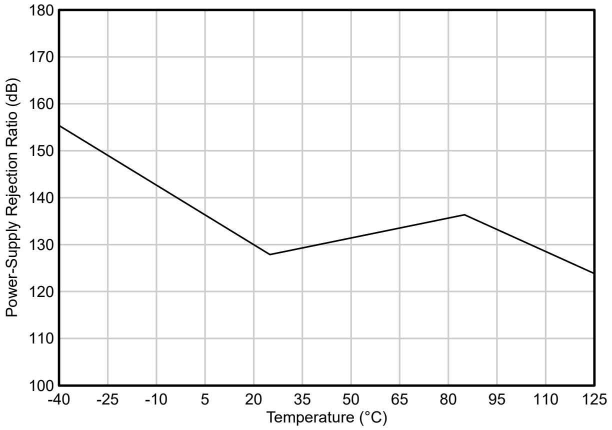


Figure 5-28. Power Supply Rejection Ratio vs Temperature

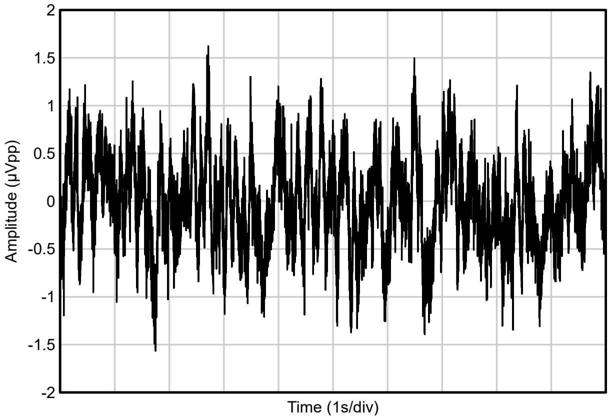
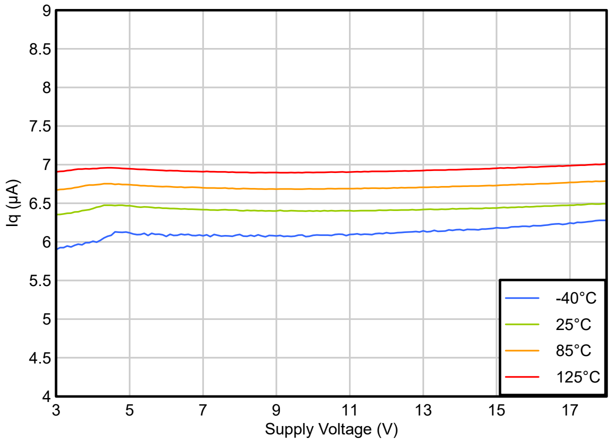


Figure 5-29. 0.1Hz to 10Hz Integrated Voltage Noise



V_{CM} = V–

Figure 5-30. Quiescent Current vs Supply Voltage

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±9V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)

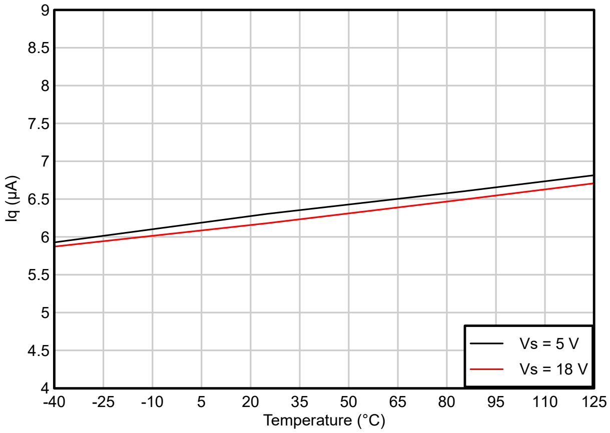


Figure 5-31. Quiescent Current vs Temperature

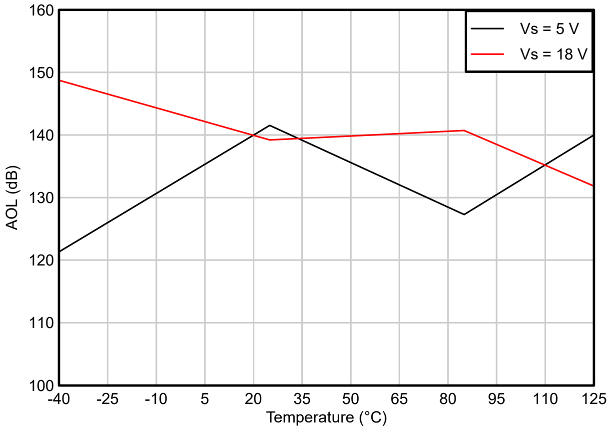
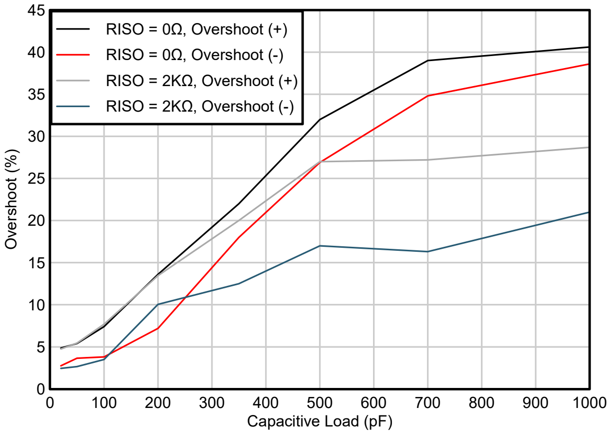
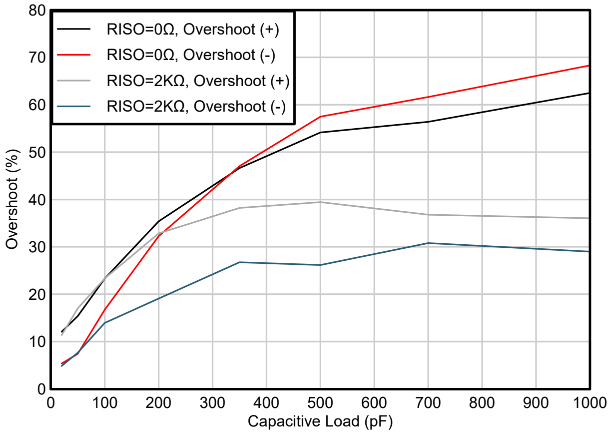


Figure 5-32. Open-Loop Gain vs Temperature



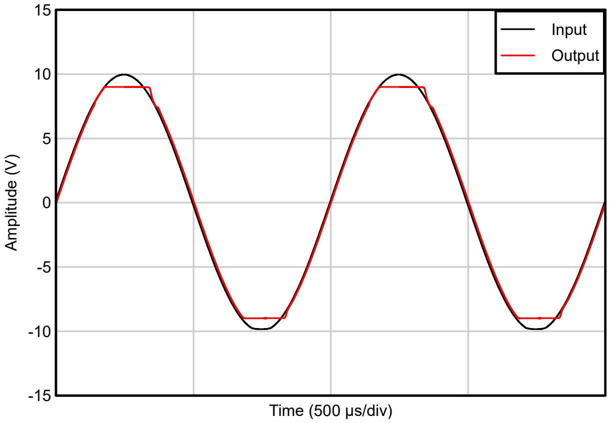
G = 1, V_{OUT} = 10mV$_{PP}$

Figure 5-33. Small-Signal Overshoot vs Capacitive Load



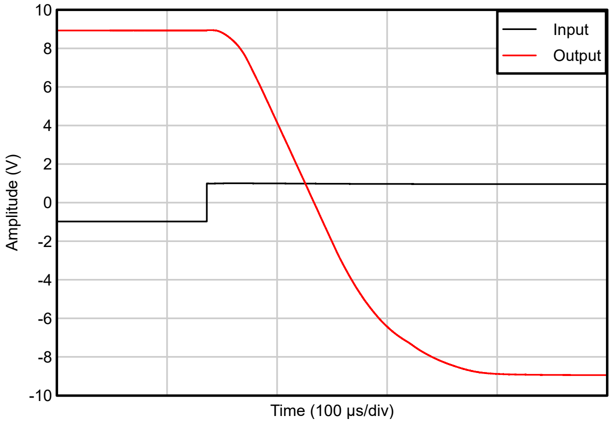
G = -1, V_{OUT} = 10mV$_{PP}$

Figure 5-34. Small-Signal Overshoot vs Capacitive Load



V_S = ±9V, V_{IN} = ±10V

Figure 5-35. No Phase Reversal

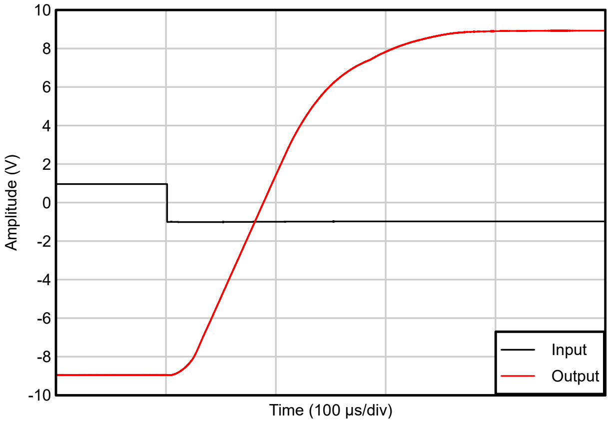


G = –10

Figure 5-36. Overload Recovery (Positive)

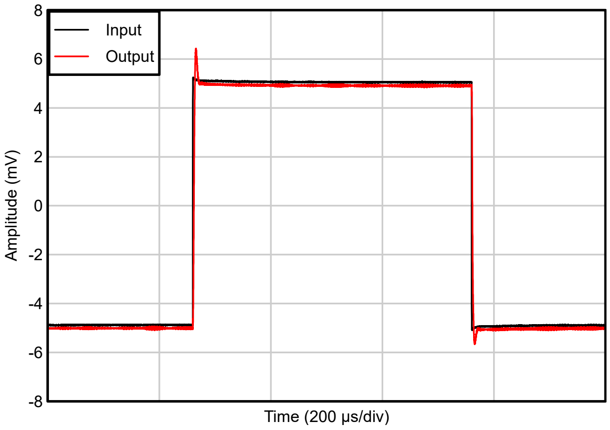
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±9V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



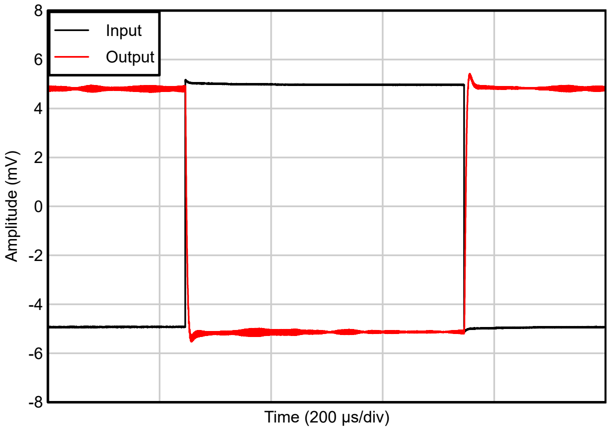
G = –10

Figure 5-37. Overload Recovery (Negative)



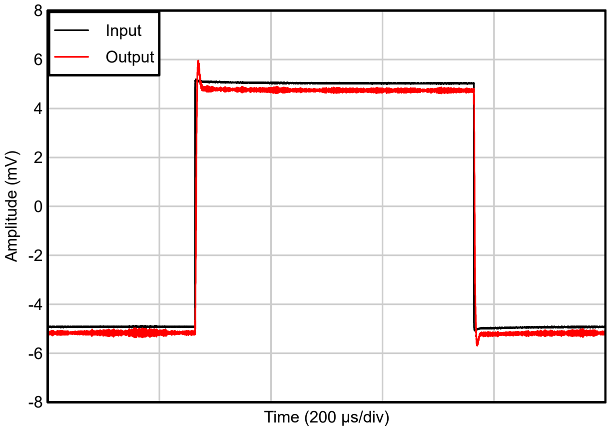
G = 1, V_S = 5V, V_{IN} = $10mV_{PP}$

Figure 5-38. Small-Signal Step Response



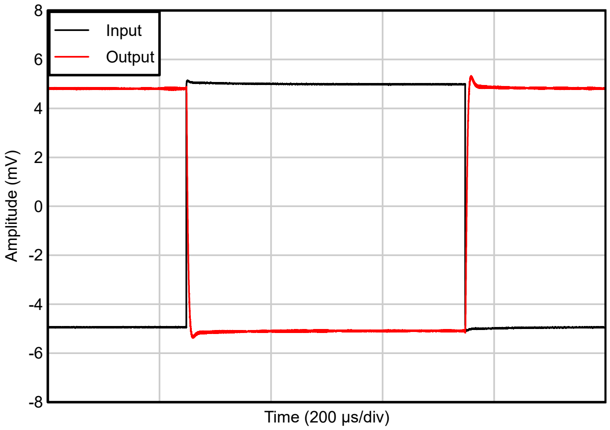
G = -1, V_S = 5V, V_{IN} = $10mV_{PP}$

Figure 5-39. Small-Signal Step Response



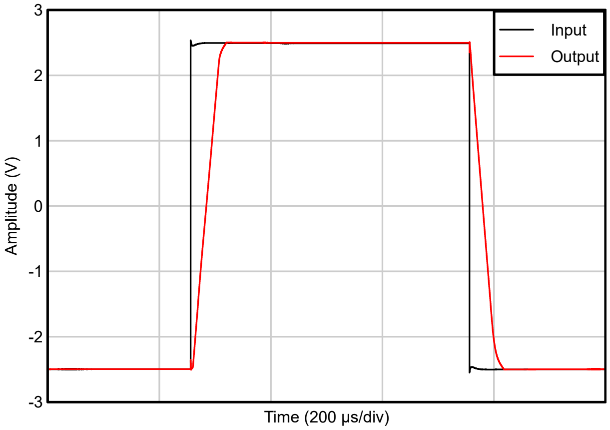
G = 1, V_S = 18V, V_{IN} = $10mV_{PP}$

Figure 5-40. Small-Signal Step Response



G = –1, V_S = 18V, V_{IN} = $10mV_{PP}$

Figure 5-41. Small-Signal Step Response

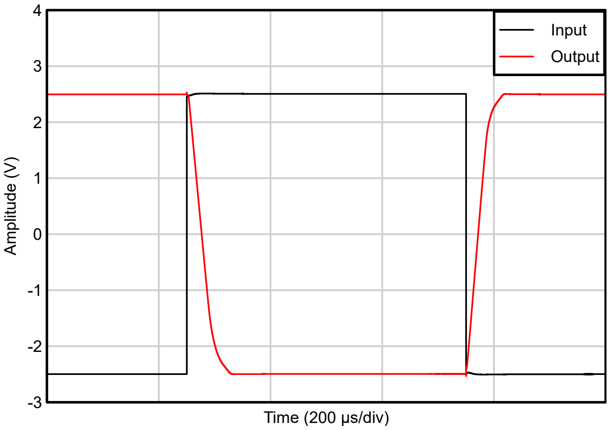


G = 1, V_{IN} = $5V_{PP}$

Figure 5-42. Large-Signal Step Response

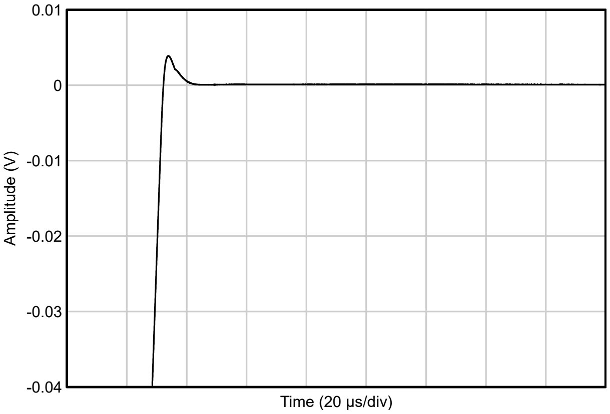
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±9V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



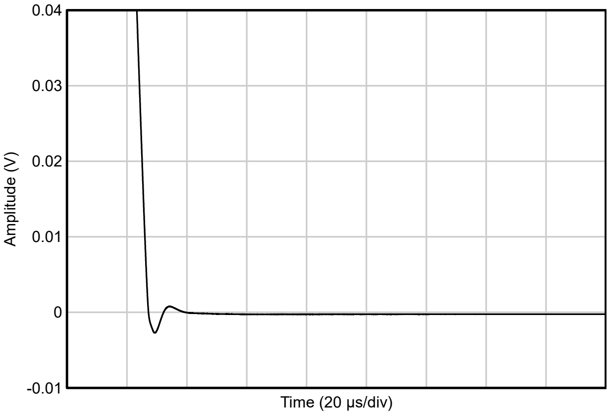
G = –1, V_{IN} = 5V_{PP}

Figure 5-43. Large-Signal Step Response



V_{IN} = 5V_{PP}

Figure 5-44. Settling Time (Positive)



V_{IN} = 5V_{PP}

Figure 5-45. Settling Time (Negative)

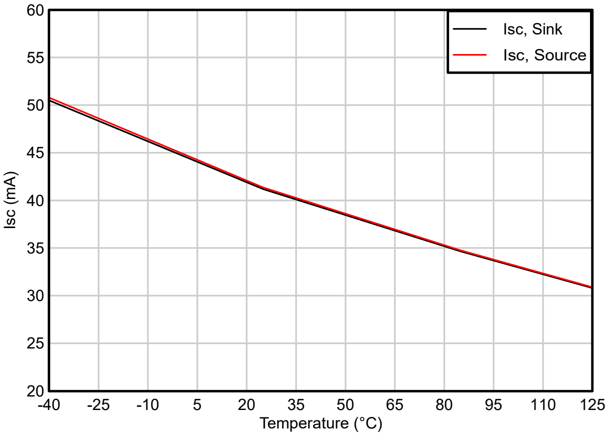


Figure 5-46. Short-Circuit Current vs Temperature

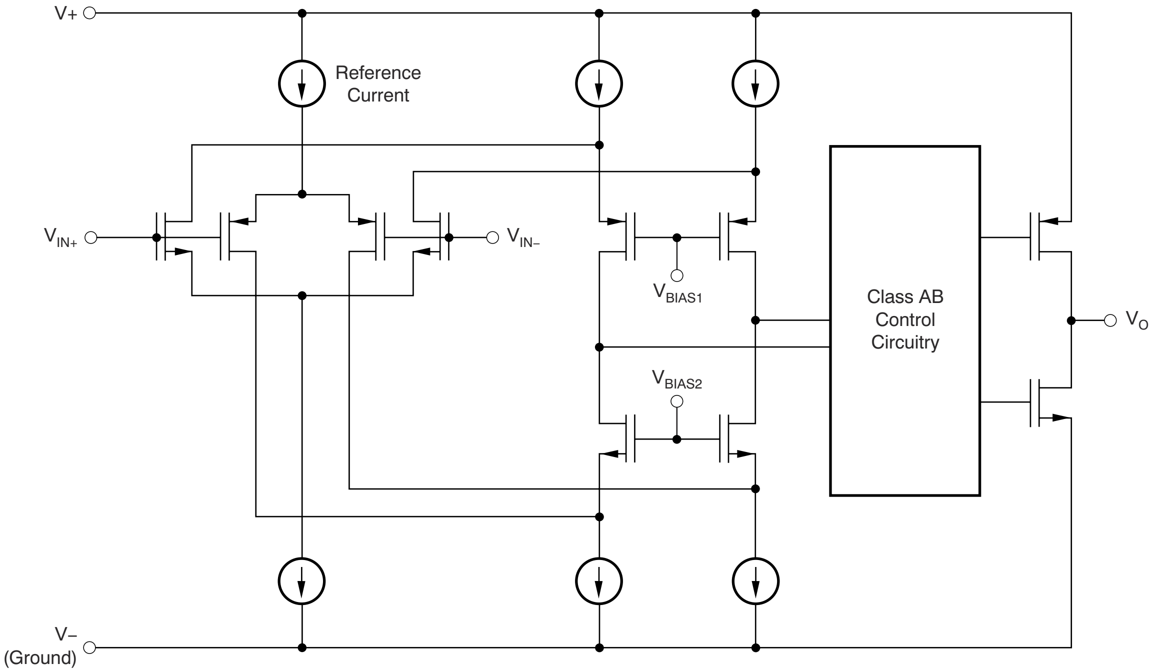
6 Detailed Description

6.1 Overview

The TLV914x family (TLV9141, TLV9142, and TLV9144) is a family of high voltage (18V) general purpose operational amplifiers.

The TLV914x is a low-power family that has a quiescent current of 7µA/channel. These devices also offer excellent DC precision, including rail-to-rail input/output, low offset (±265µV, typical), and low offset drift (±0.2µV/°C, typical). These devices also have a gain bandwidth product of 125kHz and low 1/f flicker noise of 3.4µV peak-to-peak (0.1Hz to 10Hz). These strong AC and DC parameters make the TLV914x an extremely flexible, robust, and high-performance operational amplifier for high-voltage industrial applications.

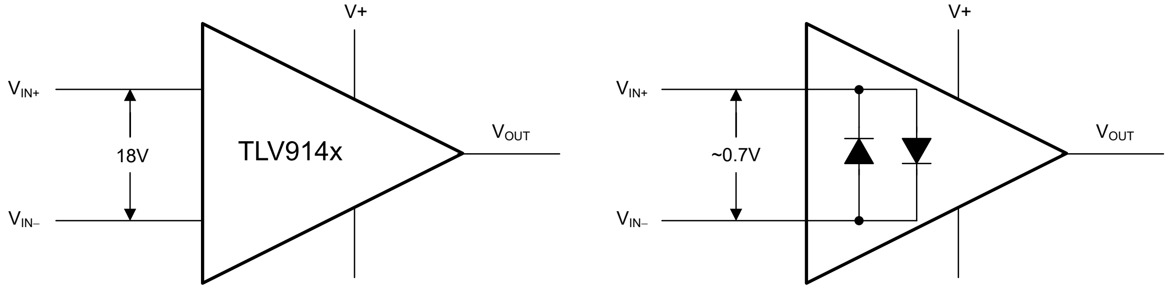
6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Input Protection Circuitry

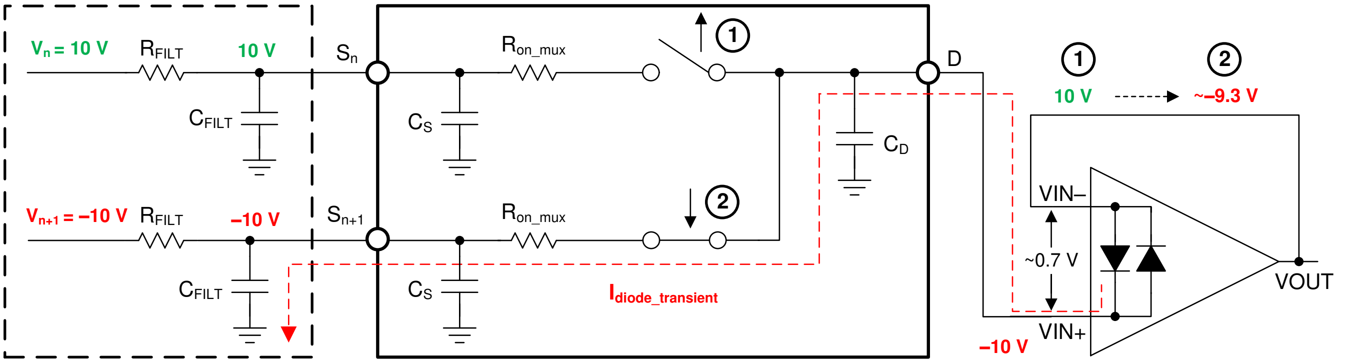
The TLV914x uses a special input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. Figure 6-1 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 6-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.



4Provides Full 18V Differential Input Range

Conventional Input Protection Limits Differential Input Range

Figure 6-1. TLV914x Input Protection Does Not Limit Differential Input Capability



Input Low-Pass Filter ***Simplified Mux Model*** ***Buffer Amplifier***

Figure 6-2. Back-to-Back Diodes Create Settling Issues

The TLV914x family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications using a patented input protection architecture that does not introduce additional signal distortion or delayed settling time, making the device an excellent choice op amp for multichannel, high-switched, input applications. The TLV914x tolerates a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 18V, allowing the device to be used in open-loop configurations. See the *MUX-Friendly Precision Operational Amplifiers* application brief for more information.

6.3.2 Common-Mode Voltage Range

The TLV914x is an 18V, true rail-to-rail input operational amplifier with an input common-mode range that extends to both supply rails. This wide range is achieved with paralleled complementary PMOS and NMOS differential input pairs, as shown in Figure 6-3. The NMOS pair is active for input voltages close to the positive rail, typically from (V+) – 1V to the positive supply. The PMOS pair is active for inputs from the negative supply to approximately (V+) – 2V. There is a small transition region, multichannel typically (V+) – 2V to (V+) – 1V, in which both input pairs are on. This transition region can vary modestly with process variation. Within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance can be degraded compared to operation outside this region.

Figure 5-17 shows this transition region for a typical device in terms of input voltage offset in more detail.

For more information on common-mode voltage range and complementary pair interaction, see the *Op amps with complementary-pair input stages: What are the design trade-offs?* Analog Design Journal.

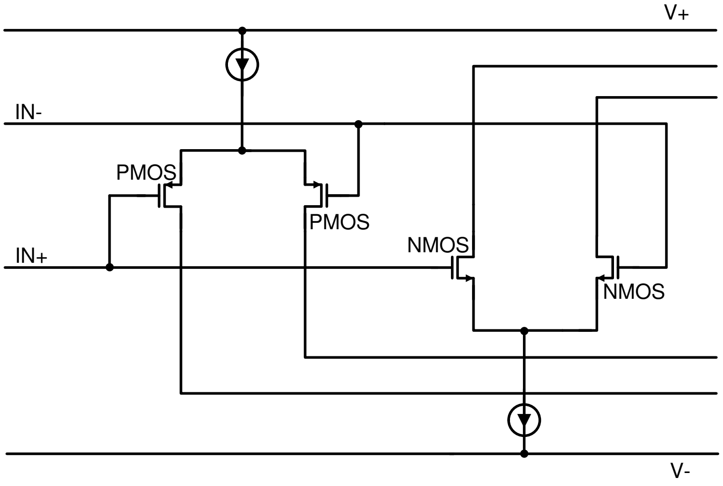


Figure 6-3. Rail-to-Rail Input Stage

6.3.3 EMI Rejection

The TLV914x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV914x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. Table 6-1 provides the EMIRR IN+ values for the TLV914x at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance and how EMIRR relates to op amps and is available for download from www.ti.com.

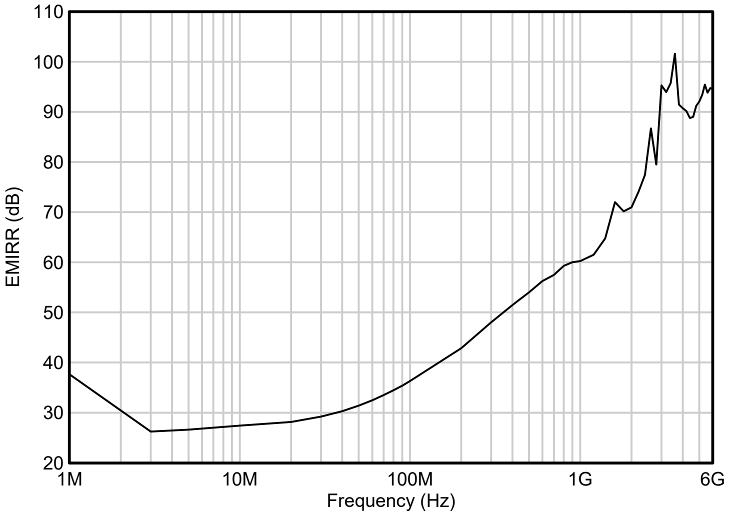


Figure 6-4. EMIRR Testing

Table 6-1. TLV914x EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	50.0dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	56.3dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	65.6dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	70.0dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	78.9dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	91.0dB

6.3.4 Phase Reversal Protection

The TLV914x family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The TLV914x is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in Figure 6-5. For more information on phase reversal, see *Op amps with complementary-pair input stages: What are the trade-offs?* Analog Design Journal.

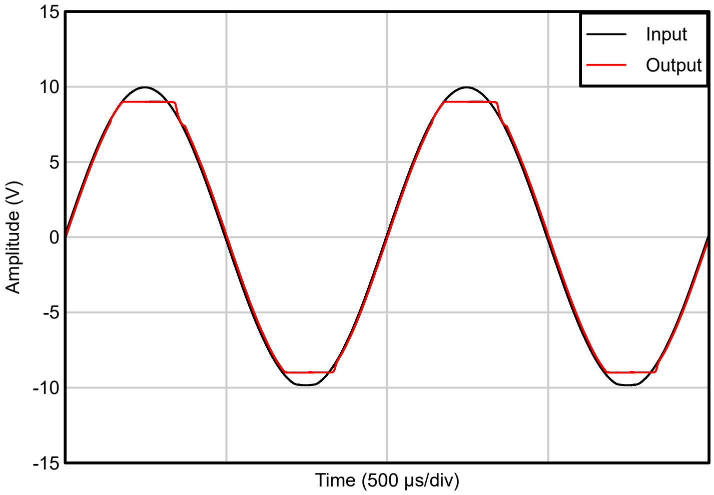


Figure 6-5. No Phase Reversal

6.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 6-6 shows an illustration of the ESD circuits contained in the TLV914x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

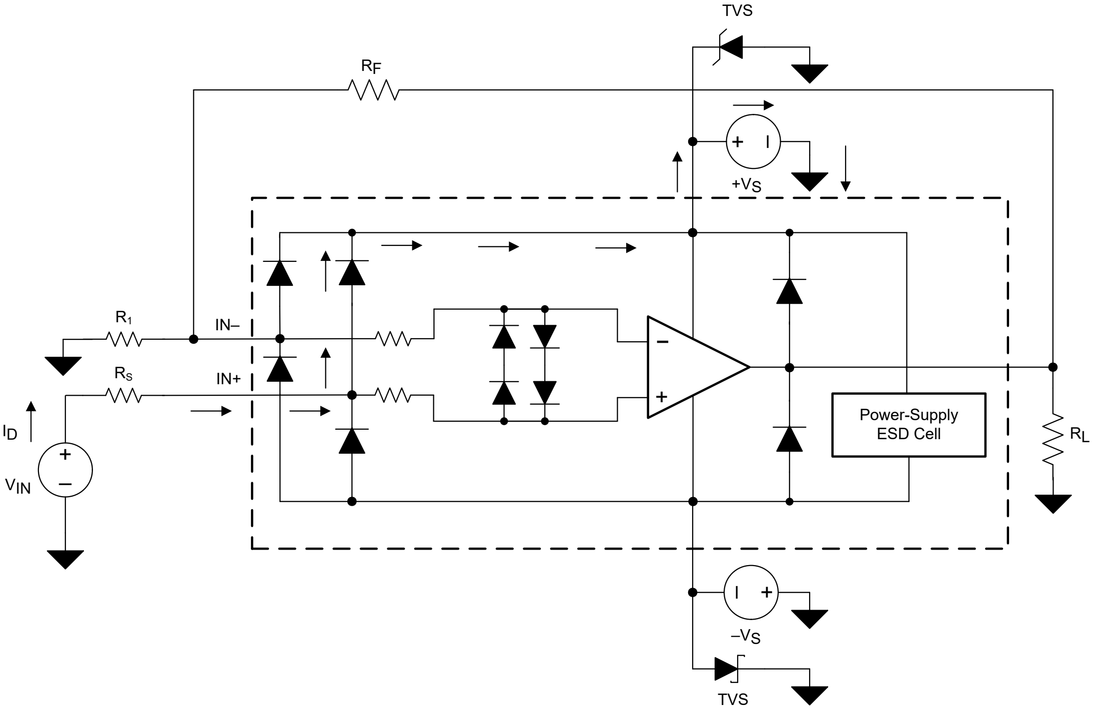


Figure 6-6. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device terminals, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the TLV914x but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (as shown in Figure 6-6), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given terminal. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 6-6 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0V. Again, this question depends on the supply characteristic while at 0V, or at a level below the input-signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply terminals; see Figure 6-6. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply terminal begins to rise above the safe-operating, supply-voltage level.

The TLV914x input terminals are protected from excessive differential voltage with back-to-back diodes; see Figure 6-6. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the TLV914x. Figure 6-6 shows an example configuration that implements a current-limiting feedback resistor.

6.3.6 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV914x is approximately 400ns.

6.3.7 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier can exhibit some amount of deviation from the expected value, like the input offset voltage of an amplifier. These deviations often follow *Gaussian* (*bell curve*), or *normal* distributions, and circuit designers can leverage this information to guardband a system, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.

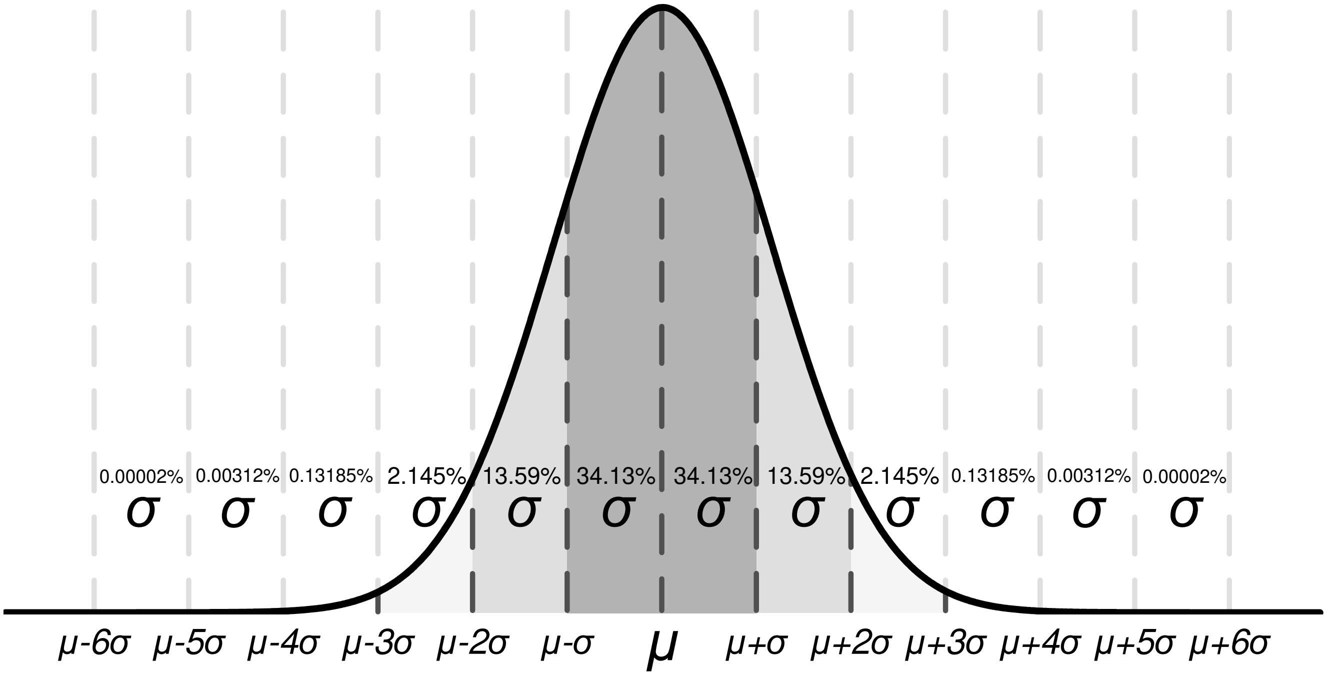


Figure 6-7. Gaussian Distribution

Figure 6-7 shows an example distribution, where *μ*, or *mu*, is the mean of the distribution, and where *σ*, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from *μ*–*σ* to *μ*+*σ*).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

Designers can use this chart to calculate approximate probability of a specification in a unit; for example, for TLV914x, the typical input voltage offset is 265μV. So 68.2% of all TLV914x devices are expected to have an offset from –265μV to +265μV. At 4*σ* (±800μV), 99.9937% of the distribution has an offset voltage less than ±1mV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are tested by TI, unless otherwise noted, and units outside these limits are removed from production material. For example, the TLV914x family has a maximum offset voltage of 1mV at 25°C, and even though this is extremely unlikely, units with larger offset than 1mV are removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for the designers application, and design worst-case conditions using this value. For example, the 6σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and can be an option as a wide guardband to design a system around. In this case, the TLV914x family does not have a maximum or minimum for offset voltage drift. Based on the typical value of 0.2µV/°C in the *Electrical Characteristics* table, the expected maximum value for the 6σ value of an offset voltage drift is approximately 1.2µV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

Note that process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot specify the maximum performance of a device. Only use this information to estimate the performance of a device.

6.4 Device Functional Modes

The TLV914x has a single functional mode and is operational when the power-supply voltage is greater than or equal to 2.7V (±1.35V). The maximum power supply voltage for the TLV914x is 18V (±9V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLV914x family offers excellent DC precision and AC performance. These devices operate up to 18V supply rails and offer true rail-to-rail input and output, low offset voltage and offset voltage drift, as well as 125kHz bandwidth and high output drive. These features make the TLV914x a robust, high-performance operational amplifier for high-voltage industrial applications.

7.2 Typical Applications

7.2.1 Low-Side Current Measurement

Figure 7-1 shows the TLV9141 configured in a low-side current sensing application. For a full analysis of the circuit shown in Figure 7-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0A to 1A Single-Supply Low-Side Current-Sensing Solution*.

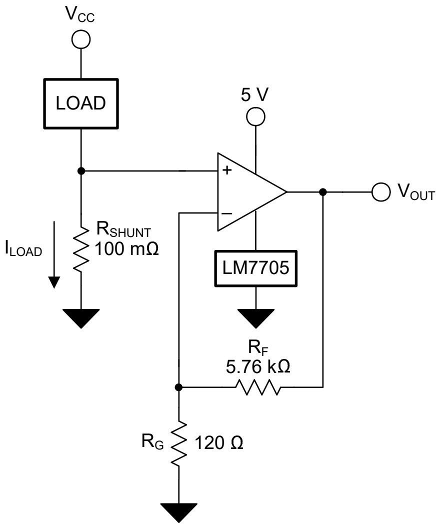


Figure 7-1. TLV914x in a Low-Side, Current-Sensing Application

7.2.1.1 Design Requirements

The design requirements for this design are as follows:

- Load current: 0A to 1A
- Max output voltage: 4.9V
- Maximum shunt voltage: 100mV

7.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 7-1 is given in Equation 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is defined using Equation 2:

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

Using Equation 2, R_{SHUNT} is calculated to be 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV9141 to produce an output voltage of 0V to 4.9V. The gain needed by the TLV9141 to produce the necessary output voltage is calculated using Equation 3:

$$\text{Gain} = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \quad (3)$$

Using Equation 3, the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G. Equation 4 is used to size the resistors, R_F and R_G, to set the gain of the TLV9141 to 49V/V.

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Choosing R_F as 5.76kΩ, R_G is calculated to be 120Ω. R_F and R_G were chosen as 5.76kΩ and 120Ω because those are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. However, excessively large resistors can generate thermal noise that exceeds the intrinsic noise of the op amp. Figure 7-2 shows the measured transfer function of the circuit shown in Figure 7-1.

7.2.1.3 Application Curve

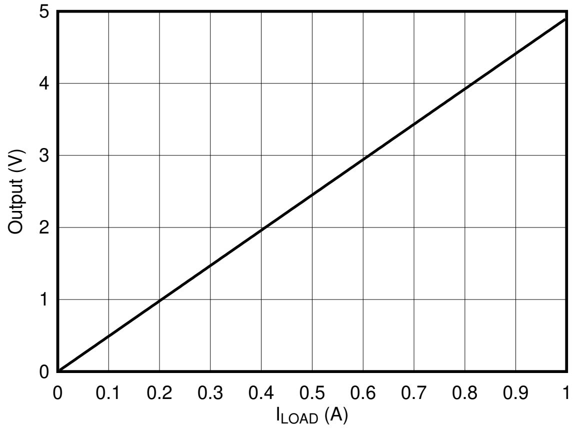


Figure 7-2. Low-Side, Current-Sense, Transfer Function

7.3 Power Supply Recommendations

The TLV914x is specified for operation from 2.7V to 18V (±1.35V to ±9V); many specifications apply from –40°C to 125°C or with specific supply voltages and test conditions.

CAUTION

Supply voltages larger than 20V can permanently damage the device; see *Absolute Maximum Ratings*.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to *Layout*.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and into the op amp. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 7-4, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

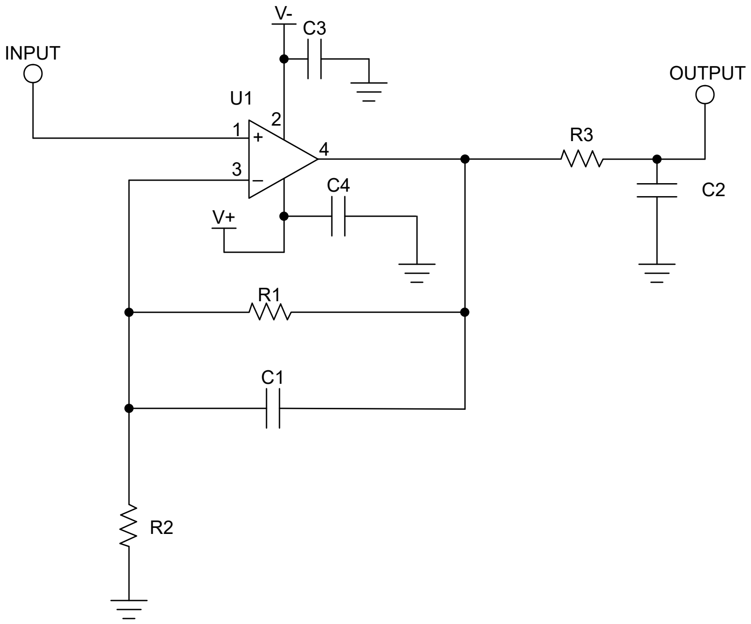


Figure 7-3. Schematic for Noninverting Configuration Layout Example

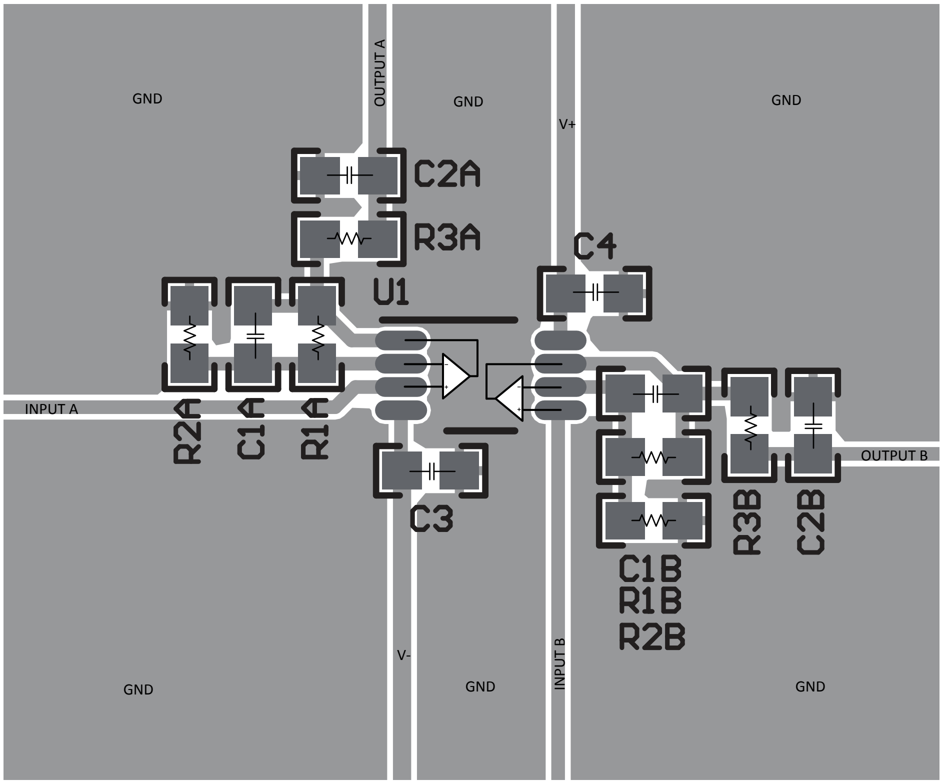


Figure 7-4. Example Layout for TLV9142

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *MUX-Friendly, Precision Operational Amplifiers* application brief
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application note
- Texas Instruments, *Op amps with complementary-pair input stages: What are the trade-offs?* Analog Design Journal
- Texas Instruments, *0A to 1A, Single-Supply, Low-Side, Current Sensing Solution* design guide

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TINA-TI™ and TI E2E™ are trademarks of Texas Instruments.
TINA™ and DesignSoft™ are trademarks of DesignSoft, Inc.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9141IDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9141ID	Samples
TLV9144IDR	ACTIVE	SOIC	D	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9144IDR	Samples
TLV9144IPWR	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9144PW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

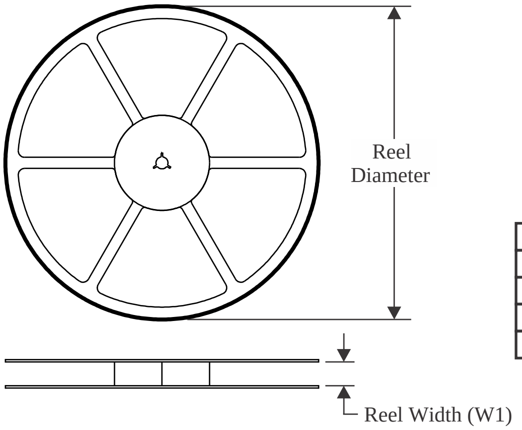
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

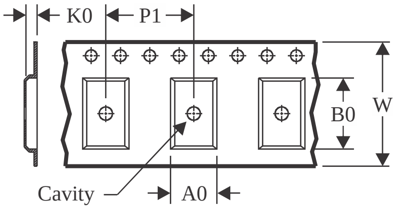
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

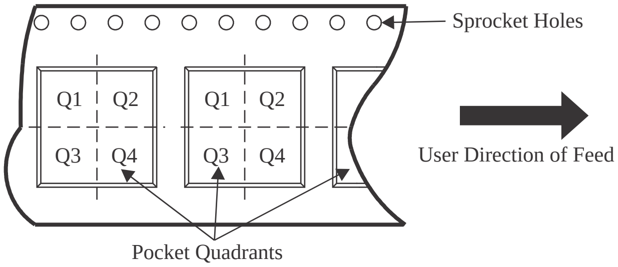


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

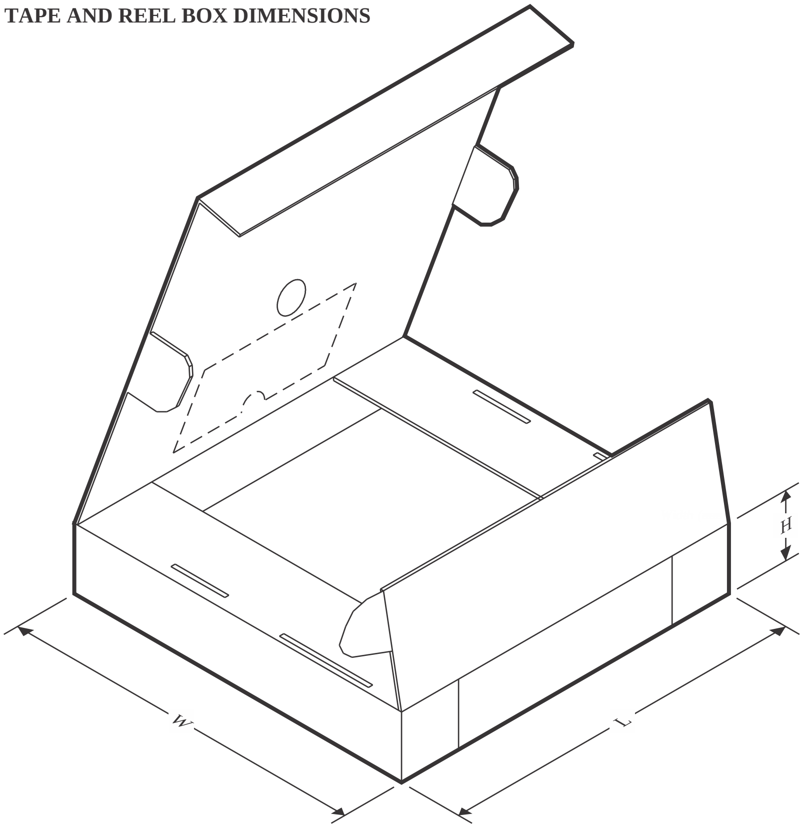
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

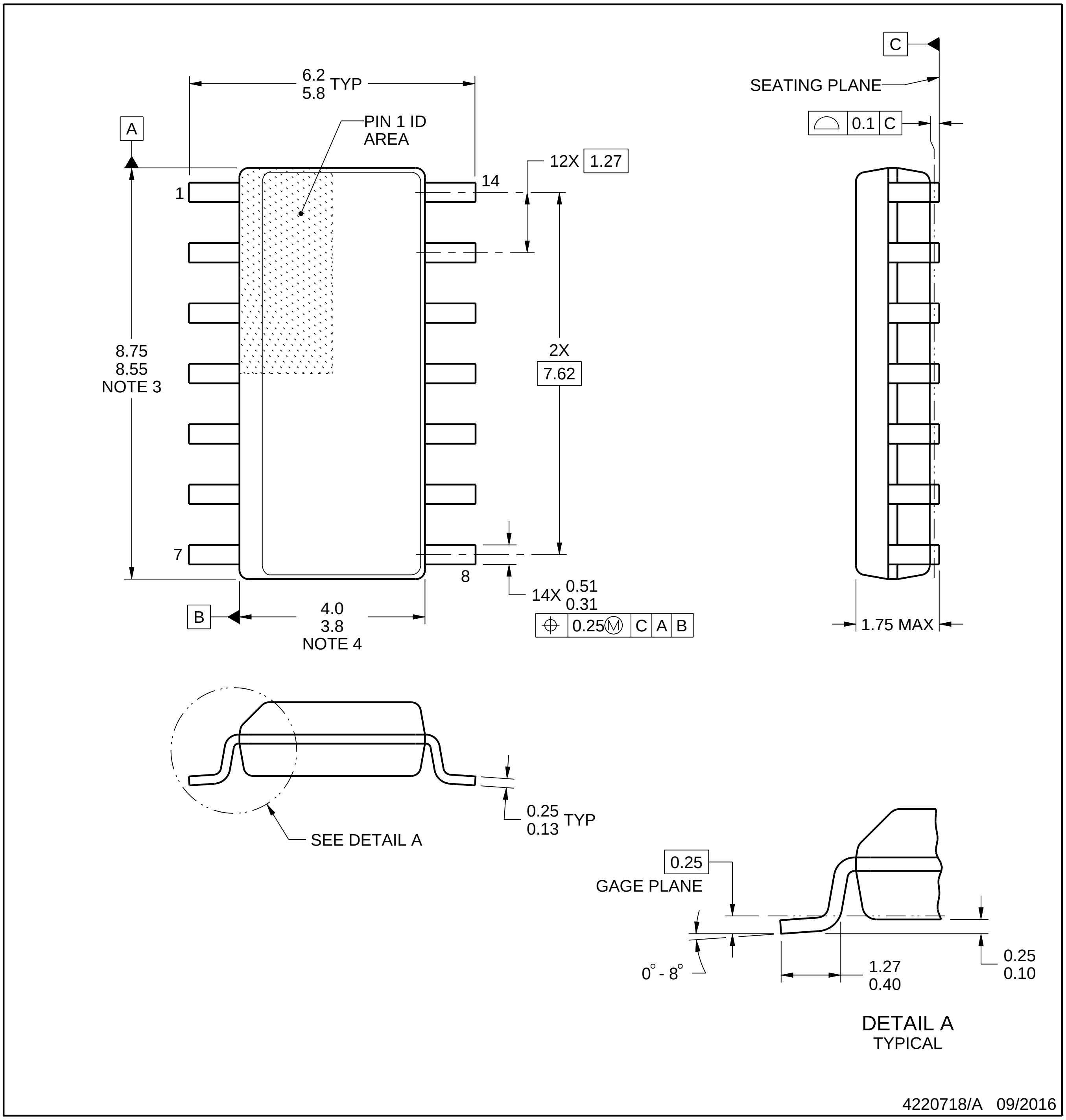
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9141IDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9144IDR	SOIC	D	14	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9144IPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



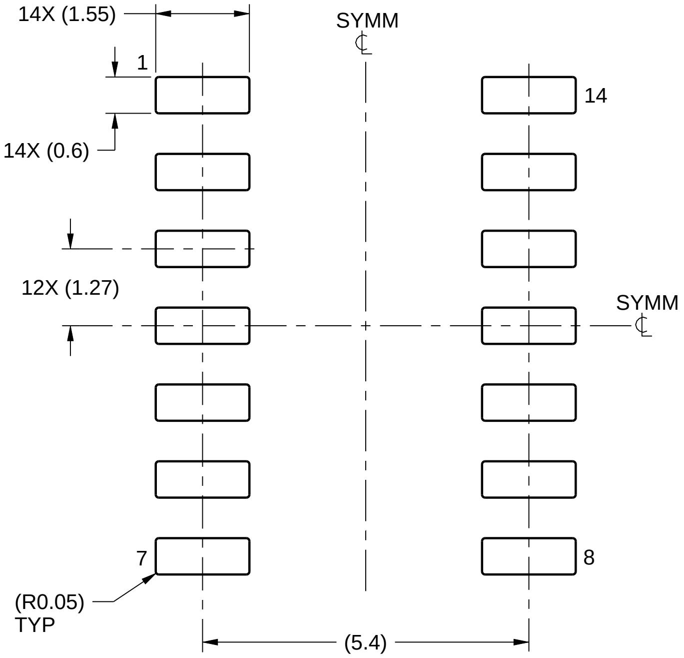
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9141IDR	SOIC	D	8	3000	340.5	338.1	20.6
TLV9144IDR	SOIC	D	14	3000	340.5	336.1	25.0
TLV9144IPWR	TSSOP	PW	14	3000	353.0	353.0	32.0

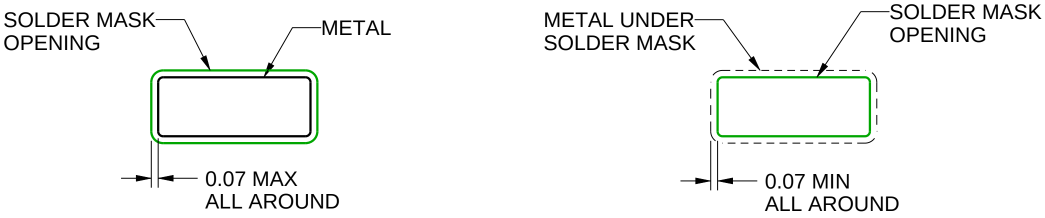


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED

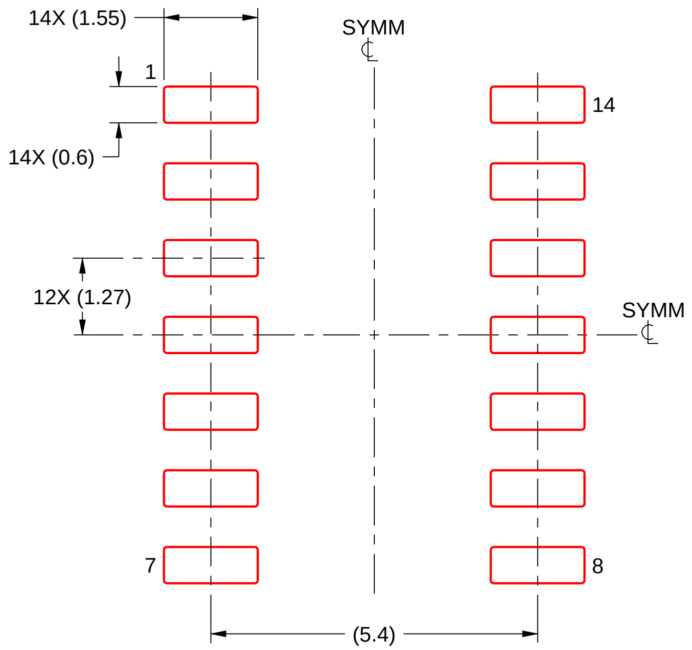
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

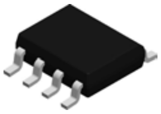


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

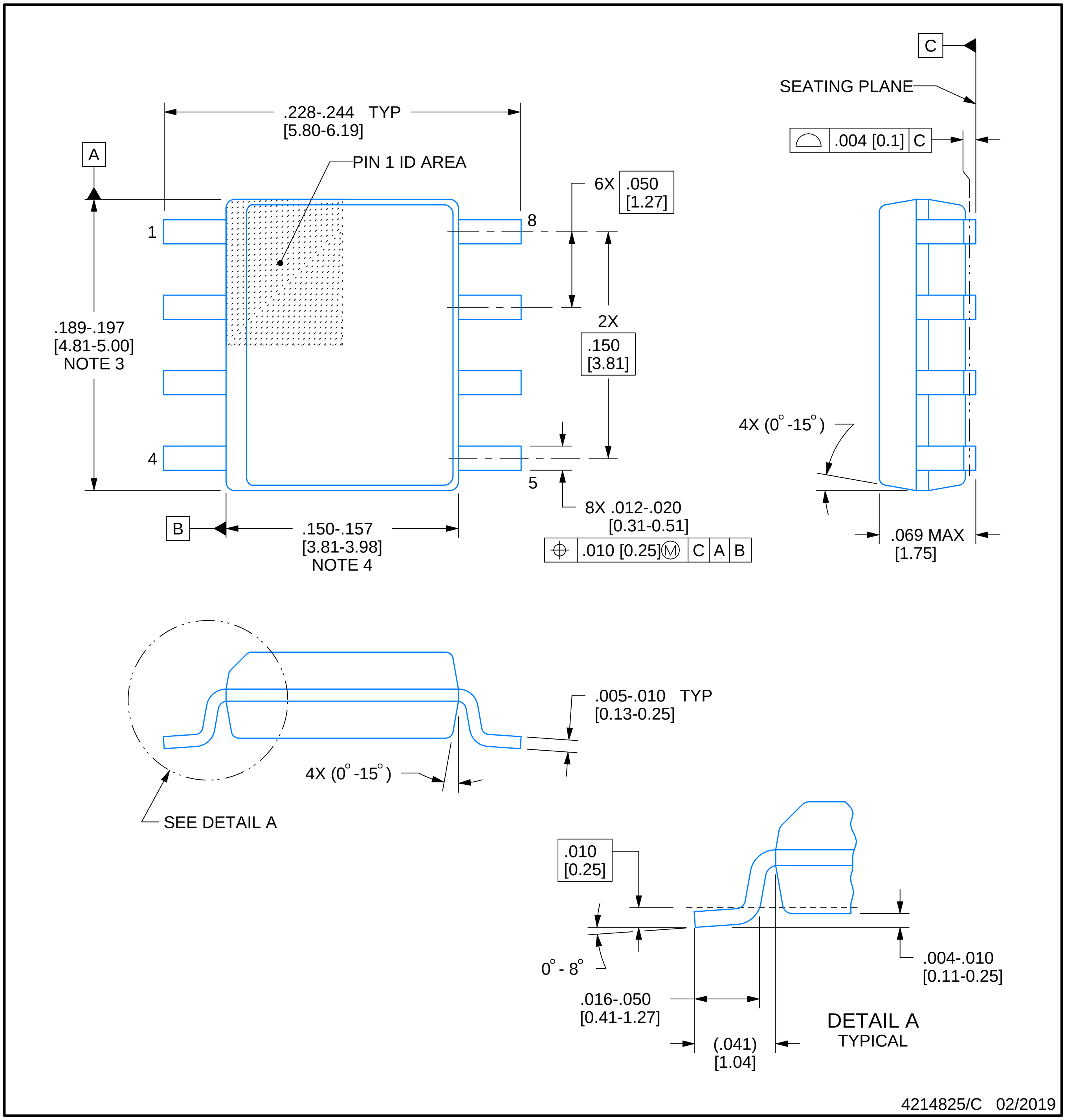


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

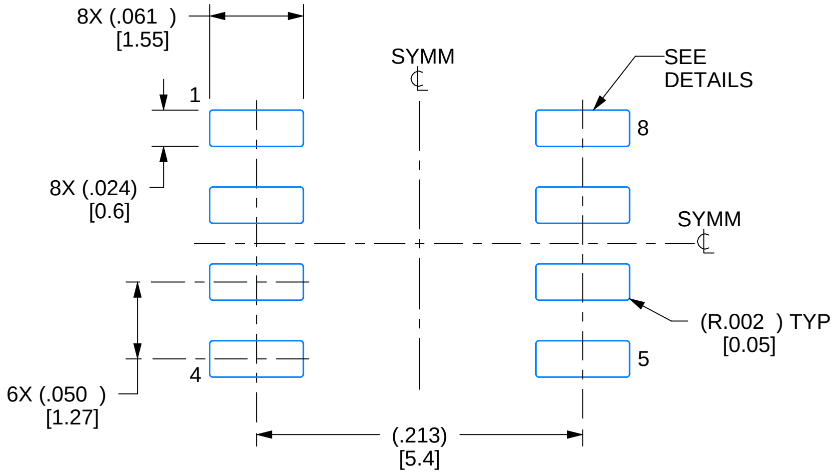
SMALL OUTLINE INTEGRATED CIRCUIT



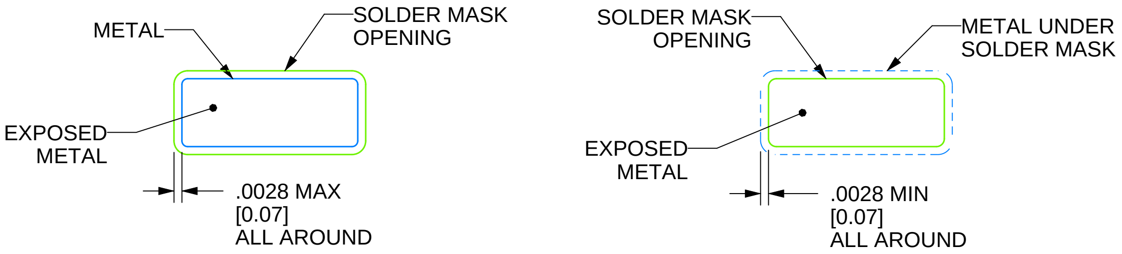
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



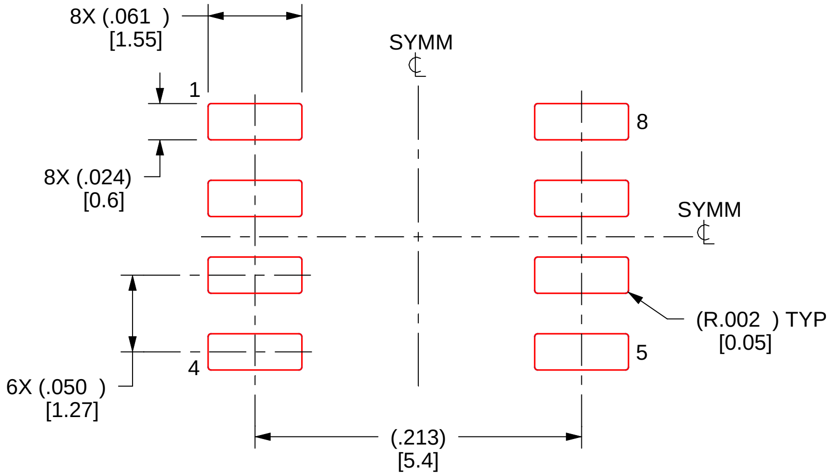
NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

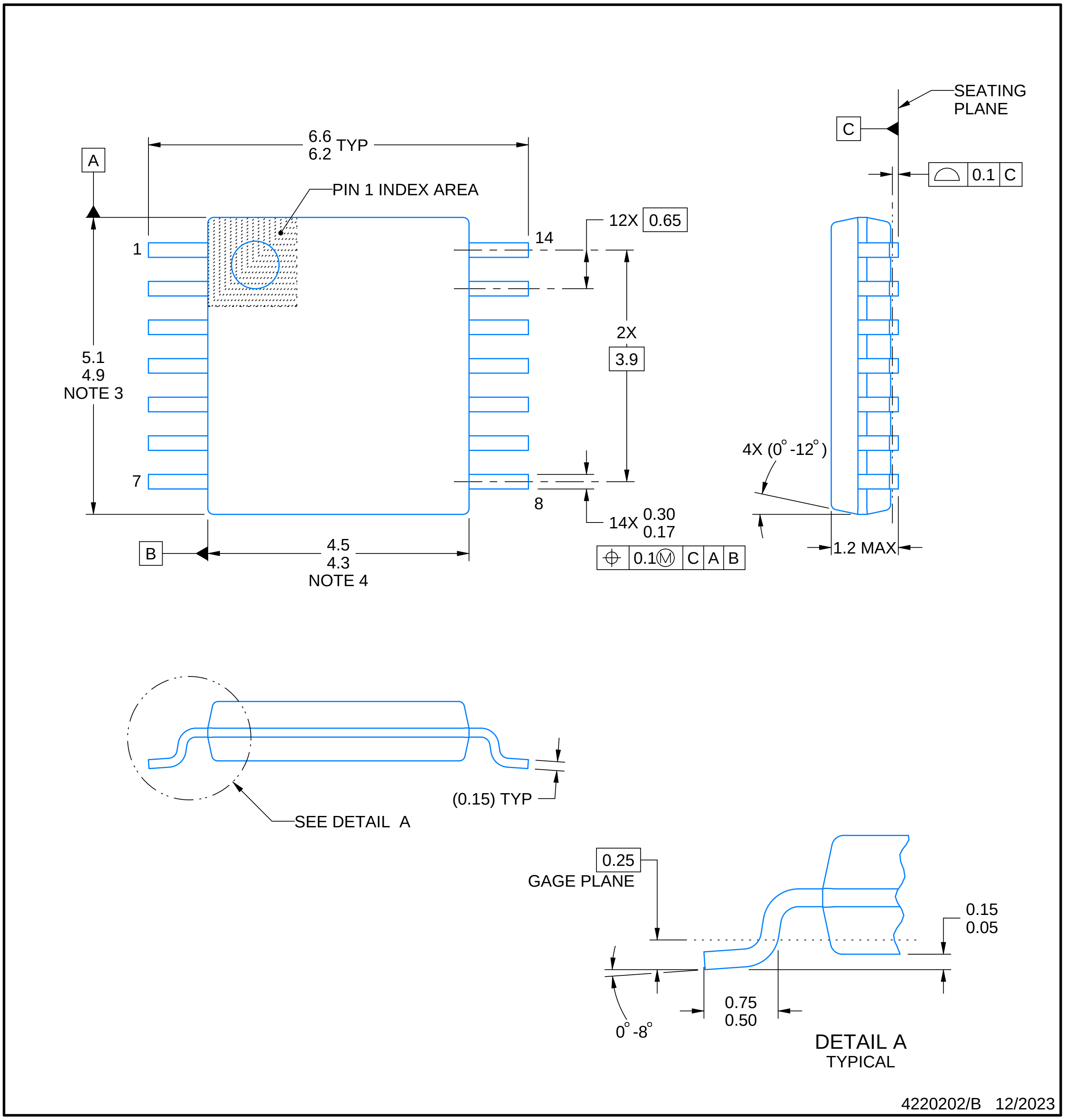
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

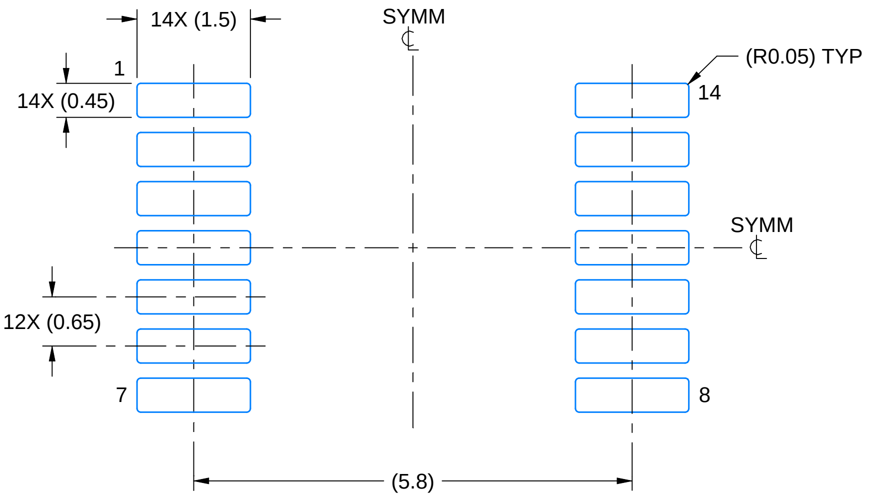
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

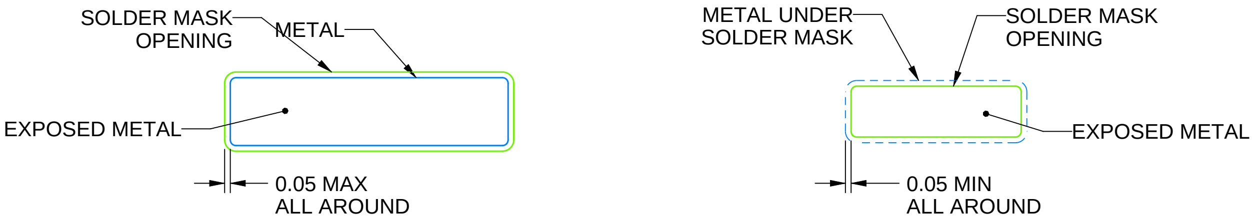


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



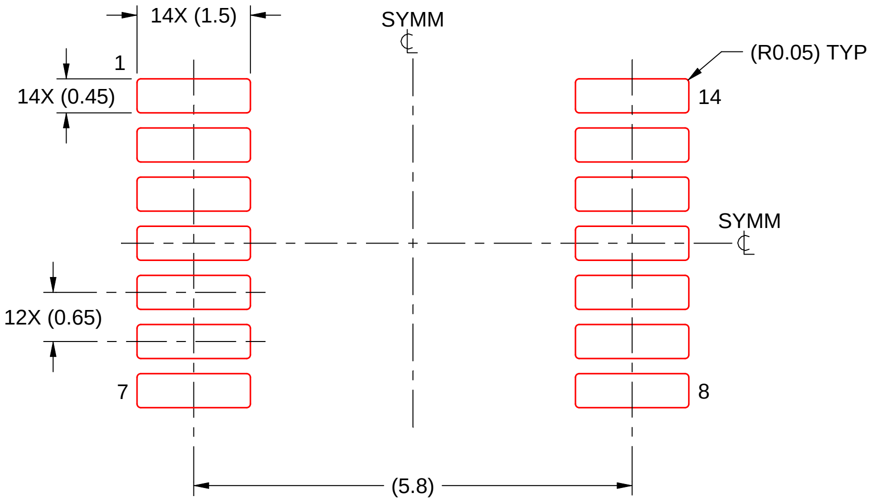
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated