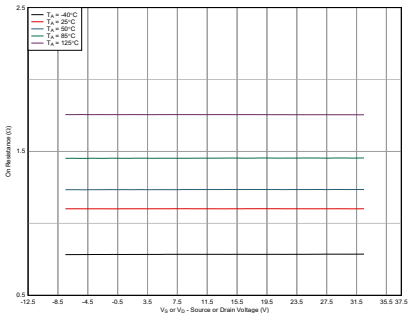
TMUX7612 50V, Low-RON, 1:1 (SPST), 4-Channel Precision Switches with 1.8V Logic

1 Features

- Dual supply range: ±4.5V to ±25V
- Single supply range: 4.5V to 50V
- Asymmetric dual supply support (For example: V_{DD} = 37.5V, V_{SS} = -12.5V)
- 1.8V logic compatible
- Precision performance:
  - Low on-resistance: 1.1Ω (typical)
  - Low capacitance: 27pF (typical)
  - Ultra-low on-resistance flatness: 0.0003Ω (typical)
  - High current support: 470mA (maximum)
  - Low on-leakage current: 3.7pA (typical), 0.3nA (maximum)
  - Low off-leakage current: 30pA (typical), 0.15nA (maximum)
  - Ultra-low charge injection: 2pC (typical)
- –40°C to +125°C operating temperature
- Rail-to-rail operation
- Bidirectional operation
- Break-before-make switching

2 Applications

- Semiconductor test equipment
- SSR and photorelay replacement
- Automated test equipment
- LCD test equipment
- Memory test equipment
- Programmable logic controllers (PLC)
- Factory automation and control
- Instrumentation: lab, analytical, and portable
- Data acquisition systems (DAQ)
- Optical test equipment



V_{DD} = 37.5 V, V_{SS} = -12.5 V

On-Resistance vs Source or Drain Voltage

3 Description

The TMUX7612 is a complementary metal-oxide semiconductor (CMOS) switch device with four independently selectable 1:1, single-pole, single-throw (SPST) switch channels. The device works with a single supply (4.5V to 50V), dual supplies (±4.5V to ±25V), or asymmetric supplies (such as V_{DD} = 37.5V, V_{SS} = –12.5V). The TMUX7612 supports bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins ranging from V_{SS} to V_{DD}.

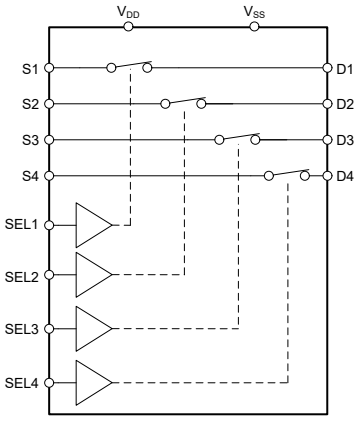
The switches of the TMUX7612 are controlled with appropriate logic control inputs on the SELx pins. The TMUX7612 features a special architecture which allows for ultra-low charge injection. This feature helps prevent unwanted coupling from the control input to the analog output of the device and reduces AC noise and offset errors.

The TMUX7612 is a part of the precision switches and multiplexers family of devices and have very low on and off leakage currents allowing them to be used in high precision measurement applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMUX7612	PW (TSSOP, 16)	5mm × 6.4mm
	RUM (WQFN, 16)	4mm × 4mm

(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TMUX7612
(SELx = Logic 1)

TMUX7612 Block Diagram

Table of Contents

4 Pin Configuration and Functions

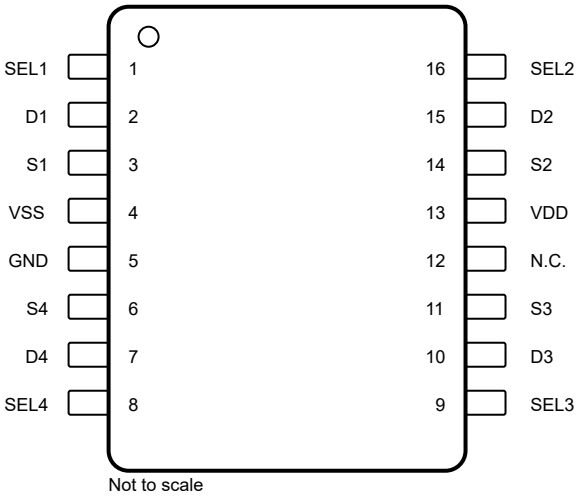


Figure 4-1. PW Package, 16-Pin TSSOP (Top View)

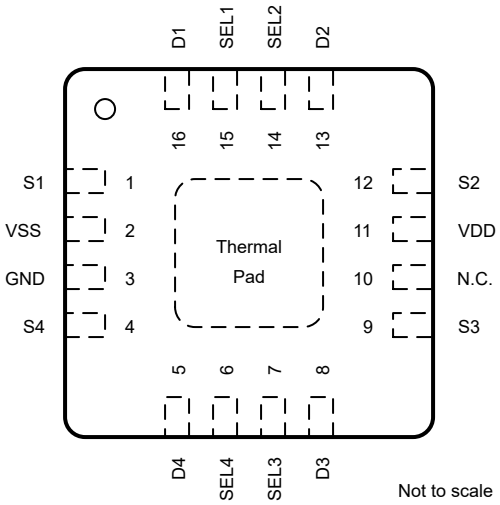


Figure 4-2. RUM Package, 16-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	TSSOP	WQFN		
D1	2	16	I/O	Drain pin 1. Can be an input or output.
D2	15	13	I/O	Drain pin 2. Can be an input or output.
D3	10	8	I/O	Drain pin 3. Can be an input or output.
D4	7	5	I/O	Drain pin 4. Can be an input or output.
GND	5	3	P	Ground (0 V) reference.
N.C.	12	10	—	No internal connection. Can be shorted to GND or left floating
S1	3	1	I/O	Source pin 1. Can be an input or output.
S2	14	12	I/O	Source pin 2. Can be an input or output.
S3	11	9	I/O	Source pin 3. Can be an input or output.
S4	6	4	I/O	Source pin 4. Can be an input or output.
SEL1	1	15	I	Logic control input 1, has internal pull-down resistor. Controls channel 1 state as provided in Table 7-1.
SEL2	16	14	I	Logic control input 2, has internal pull-down resistor. Controls channel 2 state as provided in Table 7-1.
SEL3	9	7	I	Logic control input 3, has internal pull-down resistor. Controls channel 3 state as provided in Table 7-1.
SEL4	8	6	I	Logic control input 4, has internal pull-down resistor. Controls channel 4 state as provided in Table 7-1.
VDD	13	11	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD and GND
VSS	4	2	P	Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10 µF between VSS and GND. In single-supply applications, this pin should be connected to ground.
Thermal Pad			—	The thermal exposed pad is connected internally. It is recommended that the pad be tied to VSS for best performance.

(1) I = input, O = output, I/O = input and output, P = power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
$V_{DD} – V_{SS}$	Supply voltage		53	V
V_{DD}		–0.5	53	V
V_{SS}		–32	0.5	V
V_{SEL}	Logic Supply Voltage	–0.5	53	V
I_{SEL}	Logic control input pin current (SEL pins)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, Dx)	V_{SS}–0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current(3)	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain current (Sx, Dx)		I_{DC} + 10 %(4)	mA
T_A	Ambient temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability,
functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Current* table for I_{DC} specifications.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC(1)		TMUX7612		UNIT
		RUM (QFN)	PW (TSSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.8	99.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.9	27.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.9	46.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.9	45.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.8	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Source or Drain Current through Switch

Current through the Switch	Test Conditions	T_J = 25°C	T_J = 50°C	T_J = 85°C	T_J = 105°C	T_J = 125°C	T_J = 135°C	T_J = 150°C	UNIT
I_{DC} (1)	V_{SS} to V_{DD} - 2.5V	470	470	470	309	143	100	60	mA
I_{peak} (2)	V_{SS} to V_{DD} - 2.5V	470	470	470	470	470	470	470	mA

(1) See ***Thermal Considerations*** section for more details
(2) Pulse current of 1ms with 10% Duty Cycle

5.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ (1)	Power supply voltage differential		4.5		50	V
V_{DD}	Positive power supply voltage		4.5		50	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)		V_{SS}		V_{DD}	V
V_{SEL}	Logic Supply Voltage	Logic supply voltage	0		44	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)				I_{DC} (2)	mA
T_A	Ambient temperature		–40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 4.5 V ≤ (V_{DD} – V_{SS}) ≤ 50 V, and the minimum V_{DD} is met.
(2) Refer to *Source or Drain Current* through Switch table for I_{DC} specifications.

5.6 Electrical Characteristics (Global)

Typical at V_{DD} = +15 V, V_{SS} = –15 V, V_L = 3.3V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
LOGIC INPUTS							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.005	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–2	–0.005		µA
T_{SD}	Thermal shutdown				165		°C
T_{SD_HYST}	Thermal shutdown hysteresis				15		°C
C_{IN}	Logic input capacitance		–40°C to +125°C		4		pF

5.7 Electrical Characteristics (±15 V Dual Supply)

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10% GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V I_D = –10 mA	25°C		1.1	1.4	Ω
			–40°C to +50°C			1.6	
			–40°C to +85°C			1.8	
			–40°C to +125°C			2.2	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V I_D = –10 mA	25°C		0.005		Ω
			–40°C to +50°C			0.045	
			–40°C to +85°C			0.055	
			–40°C to +125°C			0.060	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10 V to +10 V I_D = –10 mA	25°C		0.0003		Ω
			–40°C to +50°C			0.045	
			–40°C to +85°C			0.055	
			–40°C to +125°C			0.060	
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.006		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V	25°C	–0.15	0.03	0.15	nA
			–40°C to +50°C	–0.3		0.3	
			–40°C to +85°C	–0.65		0.65	
			–40°C to +125°C	–4		4	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V	25°C	–0.15	0.03	0.15	nA
			–40°C to +50°C	–0.3		0.3	
			–40°C to +85°C	–0.65		0.65	
			–40°C to +125°C	–4		4	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V	25°C	–0.3	0.0037	0.3	nA
			–40°C to +50°C	-0.4		0.4	
			–40°C to +85°C	–0.55		0.55	
			–40°C to +125°C	–4		4	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels(2)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V	25°C		10		pA
			–40°C to +50°C		13		
			–40°C to +85°C		22		
			–40°C to +125°C		32		
POWER SUPPLY							
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V All switches OFF	25°C		35	45	µA
			–40°C to +85°C			55	
			–40°C to +125°C			65	
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V All switches ON	25°C		435	480	µA
			–40°C to +85°C			520	
			–40°C to +125°C			545	
I_{SSQ}	V_{SS} quiescent supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V All switches OFF	25°C		15	20	µA
			–40°C to +85°C			25	
			–40°C to +125°C			40	

5.7 Electrical Characteristics (±15 V Dual Supply) (continued)

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10% GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V All switches ON	25°C		340	380	µA
			–40°C to +85°C			410	
			–40°C to +125°C			425	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.8 Switching Characteristics (±15 V Dual Supply)

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		2.0	2.5	µs
			–40°C to +85°C			2.75	µs
			–40°C to +125°C			3	µs
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		1.7	2.2	µs
			–40°C to +85°C			2.5	µs
			–40°C to +125°C			3	µs
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF	25°C		310		ns
			–40°C to +85°C	125			ns
			–40°C to +125°C	125			ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF	25°C		-2		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 100 kHz	25°C		–105		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–74		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 100 kHz	25°C		–114		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1MHz	25°C		–105		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V	25°C		180		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–0.095		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–80		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0 V R_L = 110 Ω , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0006		%
$C_{S(OFF)}$	Source off capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		27		pF
$C_{D(OFF)}$	Drain off capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		27		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		22		pF

5.9 Electrical Characteristics (±20 V Dual Supply)

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –15 V to +15 V I_D = –10 mA	25°C		1.1	1.4	Ω
			–40°C to +50°C			1.6	
			–40°C to +85°C			1.9	
			–40°C to +125°C			2.2	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –15 V to +15 V I_D = –10 mA	25°C		0.007		Ω
			–40°C to +50°C			0.04	
			–40°C to +85°C			0.05	
			–40°C to +125°C			0.06	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –15 V to +15 V I_D = –10 mA	25°C		0.006		Ω
			–40°C to +50°C			0.065	
			–40°C to +85°C			0.070	
			–40°C to +125°C			0.075	
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.005		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V	25°C	–0.16	0.012	0.16	nA
			–40°C to +50°C	-0.6	0.05	0.6	
			–40°C to +85°C	–5	0.3	5	
			–40°C to +125°C	–40	1.8	40	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V	25°C	–0.16	0.012	0.16	nA
			–40°C to +50°C	-0.6	0.05	0.6	
			–40°C to +85°C	–5	0.3	5	
			–40°C to +125°C	–40	1.8	40	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is on V_S = V_D = ±15 V	25°C	–0.35	0.0045	0.35	nA
			–40°C to +50°C	-0.45		0.45	
			–40°C to +85°C	–0.6		0.6	
			–40°C to +125°C	–6.5		6.5	
POWER SUPPLY							
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 22 V, V_{SS} = –22 V All switches OFF	25°C		35	45	µA
			–40°C to +85°C			55	
			–40°C to +125°C			75	
I_{DD}	V_{DD} supply current	V_{DD} = 22 V, V_{SS} = –22 V All switches ON	25°C		435	480	µA
			–40°C to +85°C			520	
			–40°C to +125°C			545	
I_{SSQ}	V_{SS} quiescent supply current	V_{DD} = 22 V, V_{SS} = –22 V All switches OFF	25°C		15	20	µA
			–40°C to +85°C			30	
			–40°C to +125°C			40	
I_{SS}	V_{SS} supply current	V_{DD} = 22 V, V_{SS} = –22 V All switches ON	25°C		340	400	µA
			–40°C to +85°C			425	
			–40°C to +125°C			450	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.10 Switching Characteristics (±20 V Dual Supply)

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		2	2.5	µs
			–40°C to +85°C			2.9	µs
			–40°C to +125°C			3	µs
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		1.8	2.2	µs
			–40°C to +85°C			2.5	µs
			–40°C to +125°C			2.8	µs
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF	25°C		320		ns
			–40°C to +85°C	150			ns
			–40°C to +125°C	150			ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF	25°C		-3		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 100 kHz	25°C		–105		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–76		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 100 kHz	25°C		–114		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1MHz	25°C		–105		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V,	25°C		200		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–0.093		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–76		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 20 V, V_{BIAS} = 0 V R_L = 110 Ω , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0003		%
$C_{S(OFF)}$	Source off capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		24		pF
$C_{D(OFF)}$	Drain off capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		24		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		21		pF

5.11 Electrical Characteristics (+37.5 V/–12.5 V Dual Supply)

V_{DD} = +37.5 V - 10%, V_{SS} = –12.5 V -10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +37.5 V - 10%, V_{SS} = –12.5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –7.5 V to 32.5 V I_D = –10 mA	25°C		1.1	1.35	Ω
			–40°C to +50°C			1.6	
			–40°C to +85°C			1.8	
			–40°C to +125°C			2.1	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –7.5 V to 32.5 V I_D = –10 mA	25°C		0.005		Ω
			–40°C to +50°C			0.055	
			–40°C to +85°C			0.065	
			–40°C to +125°C			0.07	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –7.5 V to 32.5 V I_D = –10 mA	25°C		0.006		Ω
			–40°C to +50°C			0.075	
			–40°C to +85°C			0.080	
			–40°C to +125°C			0.085	
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.006		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 37.5 V, V_{SS} = -12.5 V Switch state is off V_S = 32.5 V / –7.5 V V_D = –7.5 V / 32.5 V	25°C	–0.3	0.021	0.3	nA
			–40°C to +50°C	–0.8	0.07	0.8	
			–40°C to +85°C	–6	0.4	6	
			–40°C to +125°C	–50	2.9	50	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 37.5 V, V_{SS} = -12.5 V Switch state is off V_S = 32.5 V / –7.5 V V_D = –7.5 V / 32.5 V	25°C	–0.3	0.021	0.3	nA
			–40°C to +50°C	–0.8	0.07	0.8	
			–40°C to +85°C	–6	0.4	6	
			–40°C to +125°C	–50	2.9	50	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 37.5 V, V_{SS} = -12.5 V Switch state is on V_S = V_D = 32.5 V or –7.5 V	25°C	-0.35	0.02	0.35	nA
			–40°C to +50°C	-0.45		0.45	
			–40°C to +85°C	–1.1		1.1	
			–40°C to +125°C	–8		8	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels(2)	V_{DD} = 37.5 V, V_{SS} = -12.5 V Switch state is on V_S = V_D = 32.5 V or –7.5 V	25°C		1.1		pA
			–40°C to +50°C		2.1		
			–40°C to +85°C		4		
			–40°C to +125°C		12.1		
POWER SUPPLY							
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 37.5 V, V_{SS} = -12.5 V All switches OFF	25°C		38	50	µA
			–40°C to +85°C			60	
			–40°C to +125°C			75	
I_{DD}	V_{DD} supply current	V_{DD} = 37.5 V, V_{SS} = -12.5 V All switches ON	25°C		435	480	µA
			–40°C to +85°C			520	
			–40°C to +125°C			545	
I_{SSQ}	V_{SS} quiescent supply current	V_{DD} = 37.5 V, V_{SS} = -12.5 V All switches OFF	25°C		17	25	µA
			–40°C to +85°C			30	
			–40°C to +125°C			45	

5.11 Electrical Characteristics (+37.5 V/–12.5 V Dual Supply) (continued)

V_{DD} = +37.5 V - 10%, V_{SS} = –12.5 V -10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +37.5 V - 10%, V_{SS} = –12.5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{SS}	V_{SS} supply current	V_{DD} = 37.5 V, V_{SS} = -12.5 V All switches ON	25°C		340	380	µA
			–40°C to +85°C			400	
			–40°C to +125°C			430	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.12 Switching Characteristics (+37.5 V/–12.5 V Dual Supply)

V_{DD} = +37.5 V ± 10%, V_{SS} = –12.5 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +37.5 V ± 10%, V_{SS} = –12.5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		2.1	3	µs
			–40°C to +85°C			3.5	µs
			–40°C to +125°C			4	µs
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		1.74	2	µs
			–40°C to +85°C			2.1	µs
			–40°C to +125°C			2.5	µs
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF	25°C		350		ns
			–40°C to +85°C	310			ns
			–40°C to +125°C	300			ns
Q_{INJ}	Charge injection	V_S = 12.5 V, C_L = 100 pF	25°C		6.5		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V, f = 100 kHz	25°C		–105		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V, f = 1 MHz	25°C		–75		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V, f = 100 kHz	25°C		–110		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V, f = 1MHz	25°C		–100		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V,	25°C		200		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V, f = 1 MHz	25°C		–0.093		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–80		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0 V R_L = 110 Ω , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0005		%
$C_{S(OFF)}$	Source off capacitance to ground	V_S = 12.5 V, f = 1 MHz	25°C		24		pF
$C_{D(OFF)}$	Drain off capacitance to ground	V_S = 12.5 V, f = 1 MHz	25°C		24		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance to ground	V_S = 12.5 V, f = 1 MHz	25°C		21		pF

5.13 Electrical Characteristics (12 V Single Supply)

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 3 V to 9 V I_D = –10 mA	25°C		1.15	1.6	Ω
			–40°C to +50°C			1.75	
			–40°C to +85°C			2	
			–40°C to +125°C			2.3	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 3 V to 9 V I_D = –10 mA	25°C		0.005		Ω
			–40°C to +50°C			0.05	
			–40°C to +85°C			0.05	
			–40°C to +125°C			0.05	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 3 V to 9 V I_D = –10 mA	25°C		0.084		Ω
			–40°C to +50°C			0.13	
			–40°C to +85°C			0.15	
			–40°C to +125°C			0.16	
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.006		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 12 V, V_{SS} = 0 V Switch state is off V_S = 1 V / 10 V V_D = 10 V / 1 V	25°C	–0.07	0.0035	0.07	nA
			–40°C to +50°C	–0.16		0.16	
			–40°C to +85°C	–0.6		0.6	
			–40°C to +125°C	–12		12	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 12 V, V_{SS} = 0 V Switch state is off V_S = 1 V / 10 V V_D = 10 V / 1 V	25°C	–0.07	0.0027	0.07	nA
			–40°C to +50°C	–0.16		0.16	
			–40°C to +85°C	–0.6		0.6	
			–40°C to +125°C	–12		12	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 12 V, V_{SS} = 0 V Switch state is on V_S = V_D = 1 V or 10 V	25°C	–0.3	0.003	0.3	nA
			–40°C to +50°C	-0.4		0.4	
			–40°C to +85°C	–0.5		0.5	
			–40°C to +125°C	–6		6	
POWER SUPPLY							
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 12 V, V_{SS} = 0 V All switches OFF	25°C		30	40	µA
			–40°C to +85°C			45	
			–40°C to +125°C			55	
I_{DD}	V_{DD} supply current	V_{DD} = 12 V, V_{SS} = 0 V All switches ON	25°C		385	440	µA
			–40°C to +85°C			470	
			–40°C to +125°C			480	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

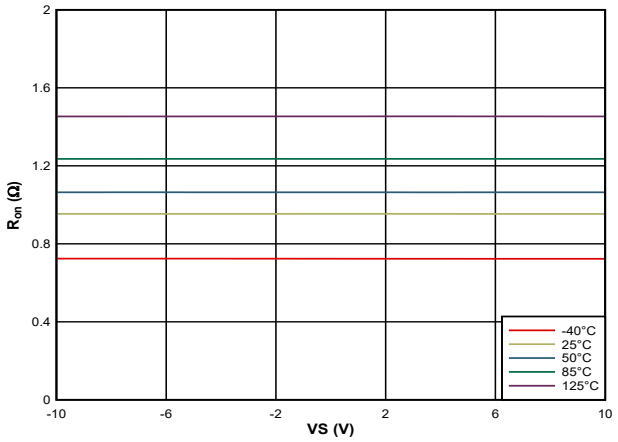
5.14 Switching Characteristics (12 V Single Supply)

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF	25°C		2	2.5	µs
			–40°C to +85°C			3	µs
			–40°C to +125°C			3.5	µs
t_{OFF}	Turn-off time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF	25°C		1.7	2.2	µs
			–40°C to +85°C			2.5	µs
			–40°C to +125°C			3	µs
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω, C_L = 35 pF	25°C		320		ns
			–40°C to +85°C	160			ns
			–40°C to +125°C	160			ns
Q_{INJ}	Charge injection	V_S = 6 V, C_L = 100 pF	25°C		4		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V, f = 100 kHz	25°C		–100		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V, f = 1 MHz	25°C		–70		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V, f = 100 kHz	25°C		–114		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V, f = 1MHz	25°C		–105		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V	25°C		165		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V, f = 1 MHz	25°C		–0.095		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–78		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6 V, V_{BIAS} = 6 V R_L = 110 Ω , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0095		%
$C_{S(OFF)}$	Source off capacitance to ground	V_S = 6 V, f = 1 MHz	25°C		37		pF
$C_{D(OFF)}$	Drain off capacitance to ground	V_S = 6 V, f = 1 MHz	25°C		37		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance to ground	V_S = 6 V, f = 1 MHz	25°C		27		pF

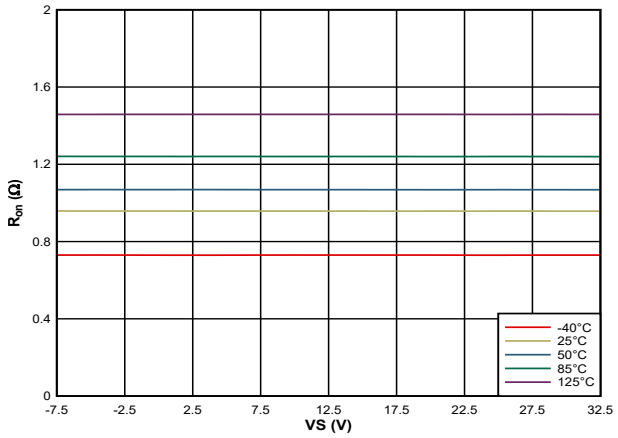
5.15 Typical Characteristics

at T_A = 25°C (unless otherwise noted)



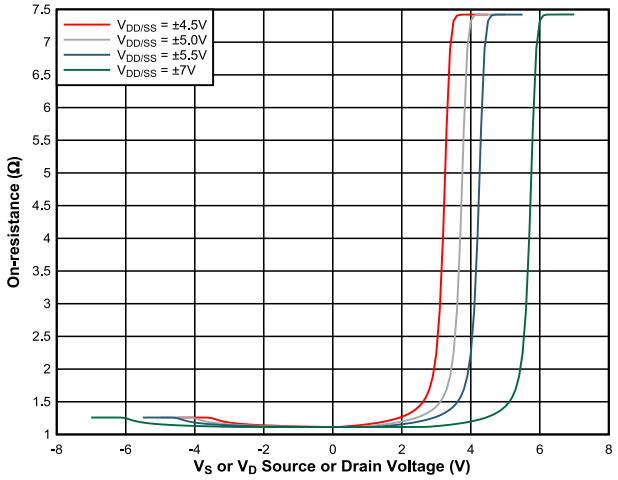
V_{DD}=15V, V_{SS}=-15V

Figure 5-1. On-Resistance vs Source or Drain Operational Voltage



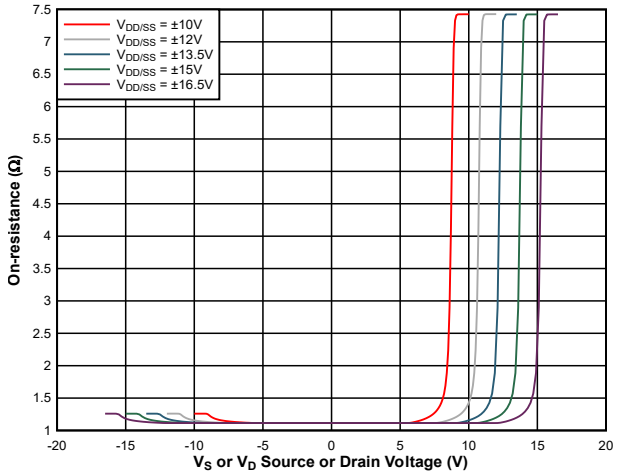
V_{DD}=37.5V, V_{SS} = -12.5V

Figure 5-2. On-Resistance vs Source or Drain Operational Voltage



T_A = 25°

Figure 5-3. On-Resistance vs Source or Drain Voltage for dual supply

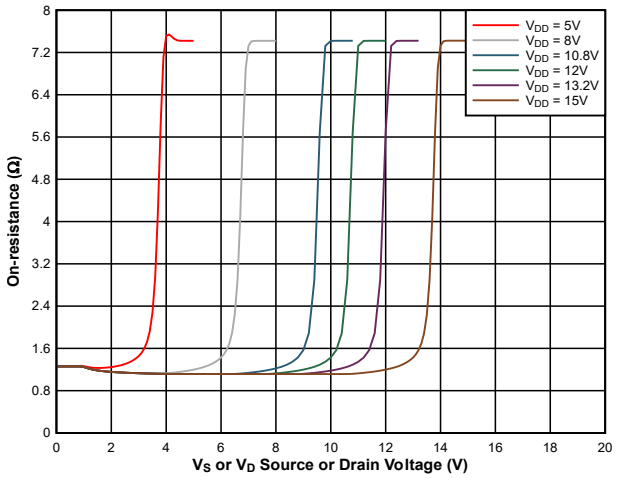


T_A = 25°

Figure 5-4. On-Resistance vs Source or Drain Voltage for dual supply

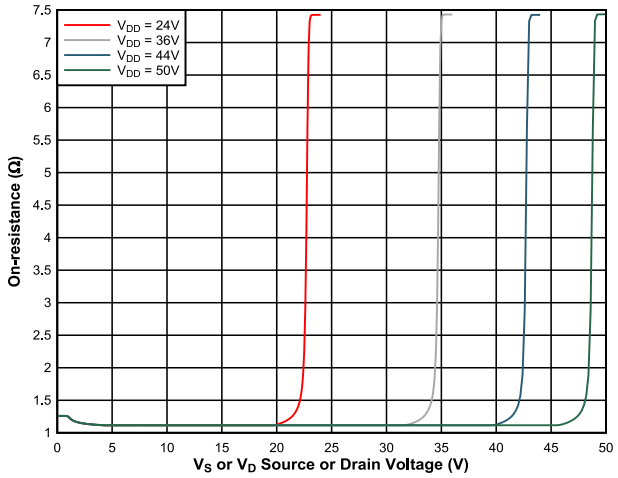
5.15 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



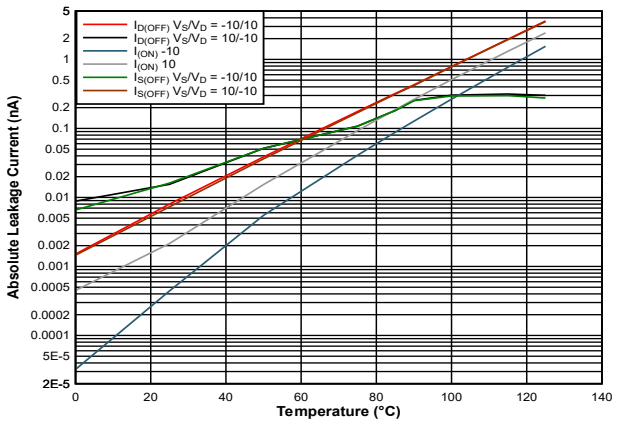
T_A = 25°

Figure 5-5. On-Resistance vs Source or Drain Voltage for single supply



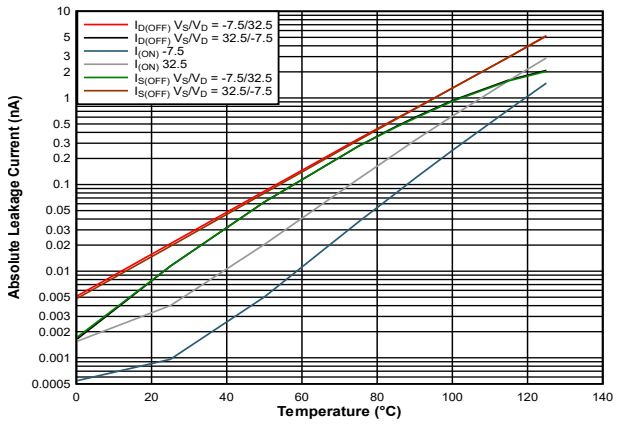
T_A = 25°

Figure 5-6. On-Resistance vs Source or Drain Voltage



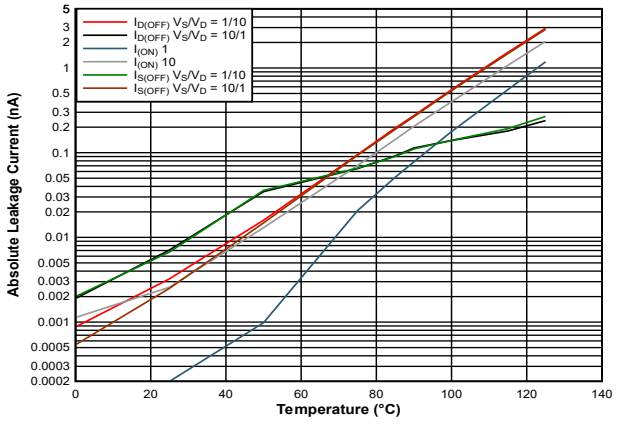
V_{DD} = 15V, V_{SS} = -15V

Figure 5-7. Leakage Current vs Temperature



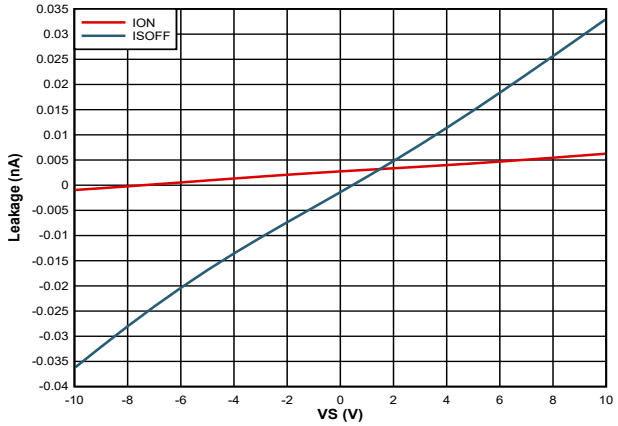
V_{DD} = 37.5V, V_{SS} = -12.5V

Figure 5-8. Leakage Current vs Temperature



V_{DD} = 12V, V_{SS} = 0V

Figure 5-9. Leakage Current vs Temperature

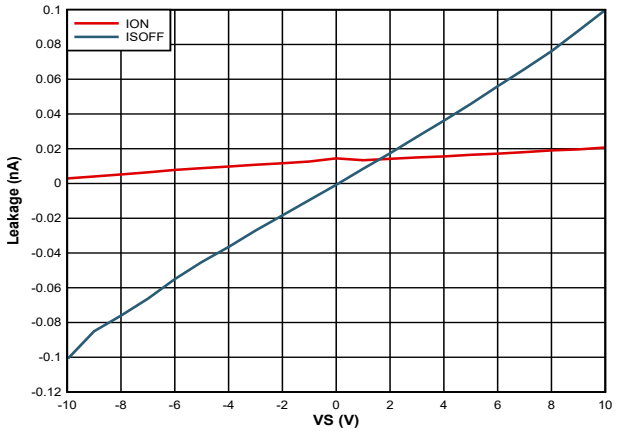


V_{DD} = 15V, V_{SS} = -15V, T_A=25°C

Figure 5-10. Leakage Current vs V_S

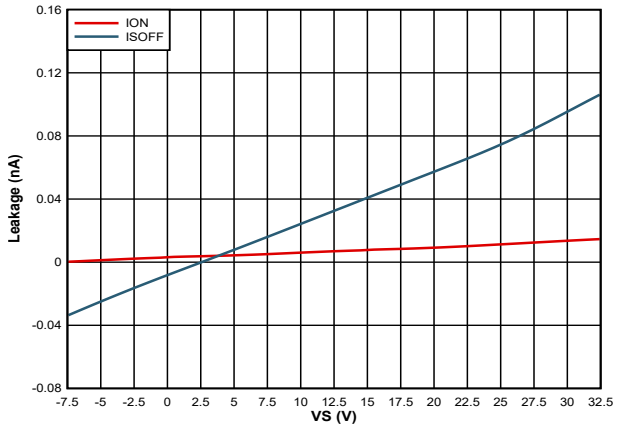
5.15 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



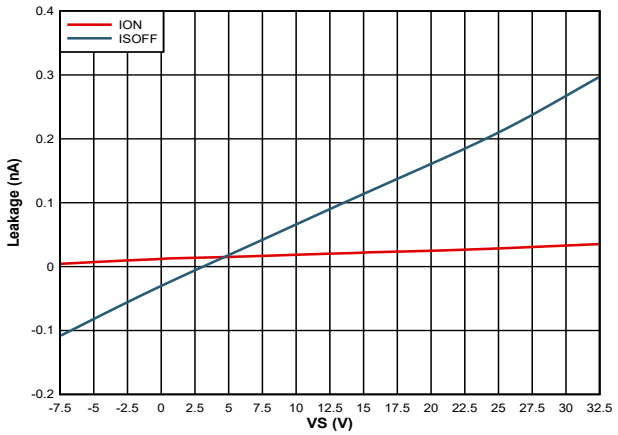
V_{DD} = 15V, V_{SS} = -15V, T_A=50°C

Figure 5-11. Leakage Current vs V_S



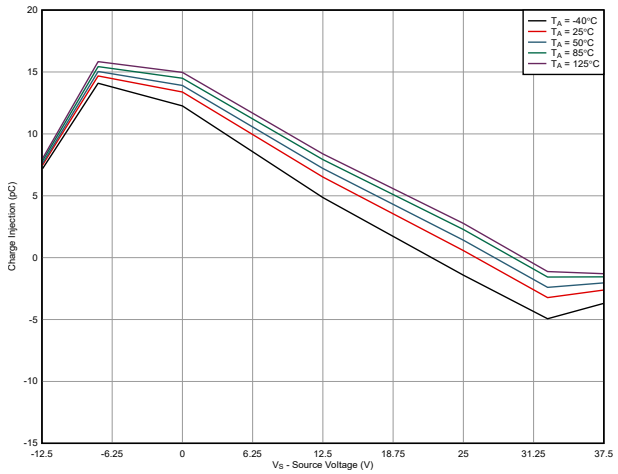
V_{DD} = 37.5V, V_{SS} = -12.5V, T_A=25°C

Figure 5-12. Leakage Current vs Temperature



V_{DD} = 37.5V, V_{SS} = -12.5V, T_A=50°C

Figure 5-13. Leakage Current vs Temperature



V_{DD} = 37.5V, V_{SS} = -12.5V

Figure 5-14. Charge Injection vs Source Voltage

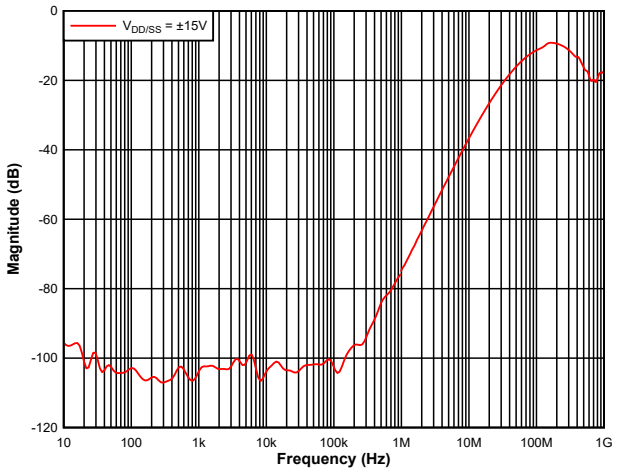


Figure 5-15. Off-Isolation vs Frequency

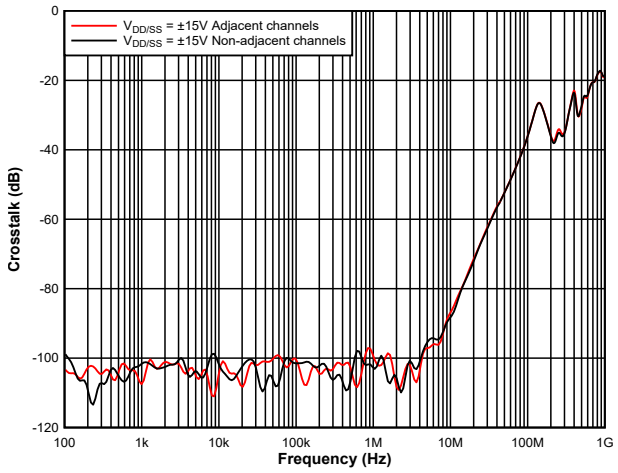


Figure 5-16. Crosstalk vs Frequency

5.15 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

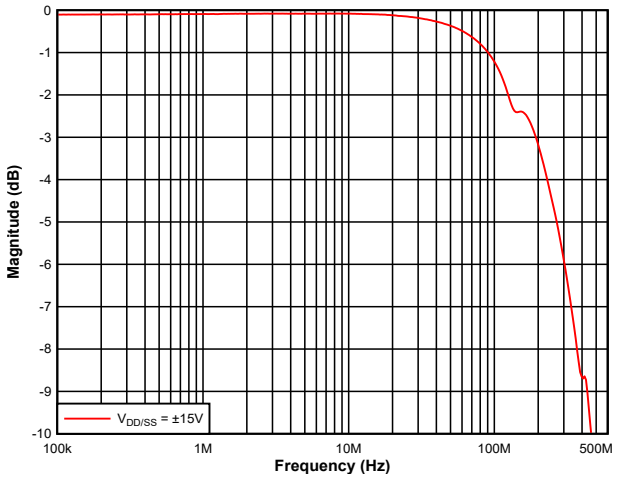


Figure 5-17. Bandwidth vs Frequency

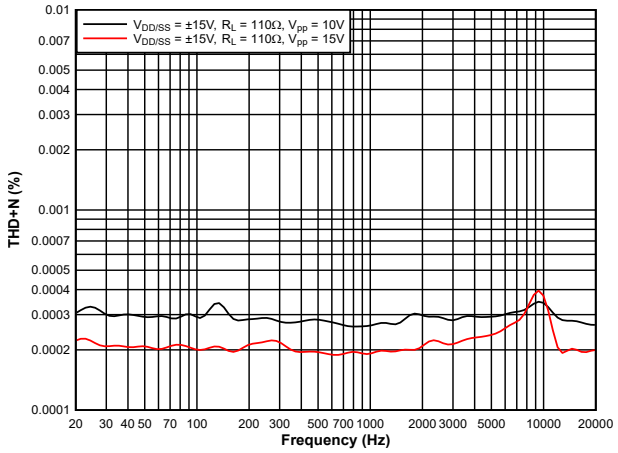


Figure 5-18. THD+N vs Frequency

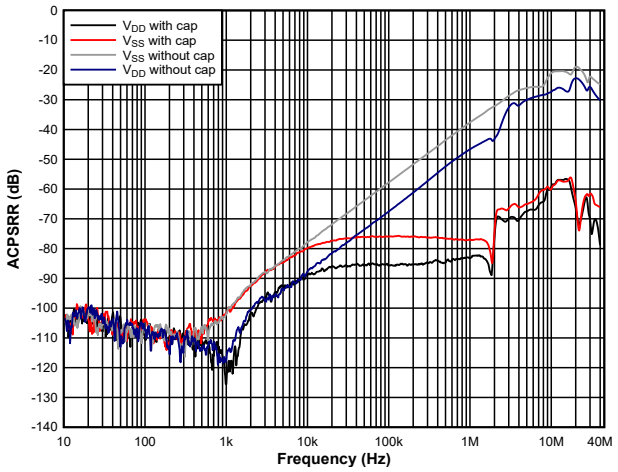
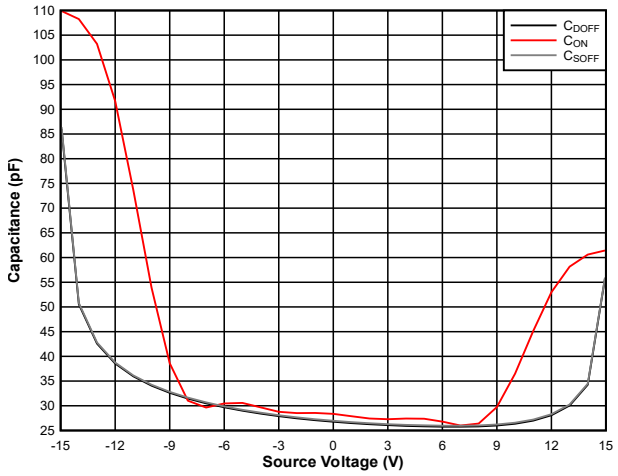


Figure 5-19. ACPSRR vs Frequency



V_{DD} = 15V, V_{SS} = -15V

Figure 5-20. Capacitance vs Source or Drain Voltage

6 Parameter Measurement Information

6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 6-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

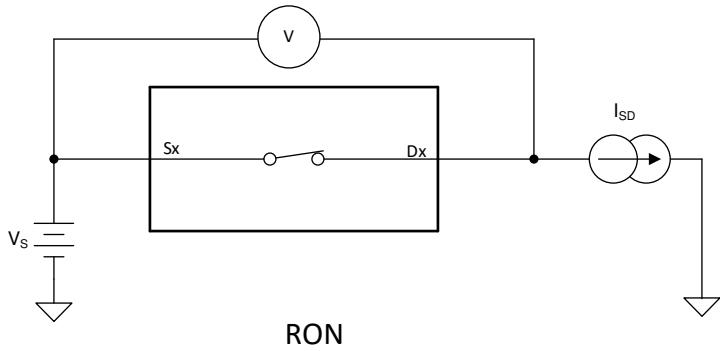


Figure 6-1. On-Resistance Measurement Setup

6.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 6-2 shows the setup used to measure both off-leakage currents.

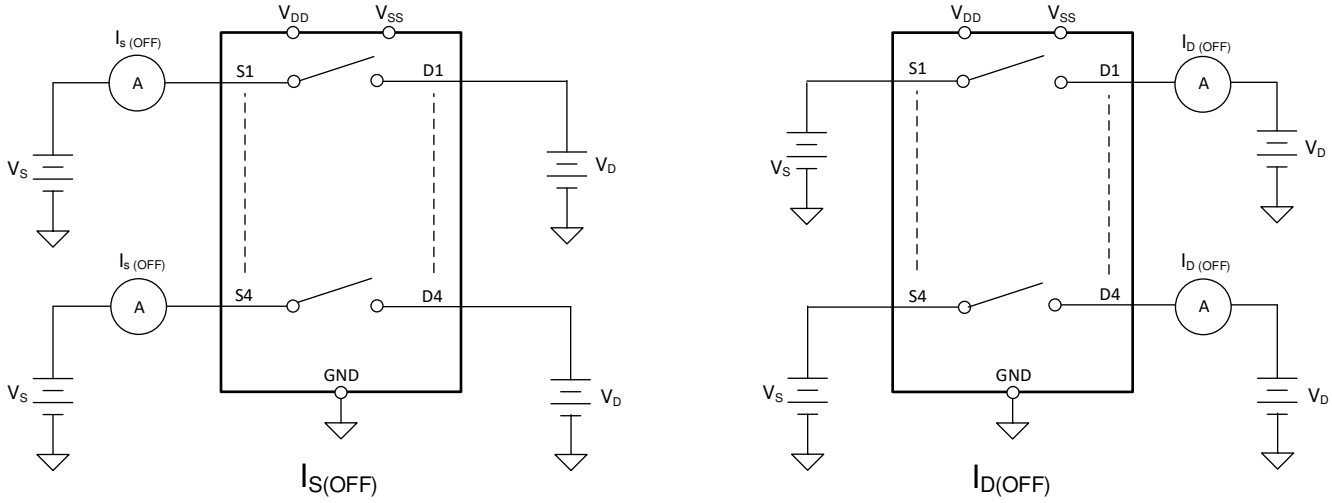


Figure 6-2. Off-Leakage Measurement Setup

6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 6-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

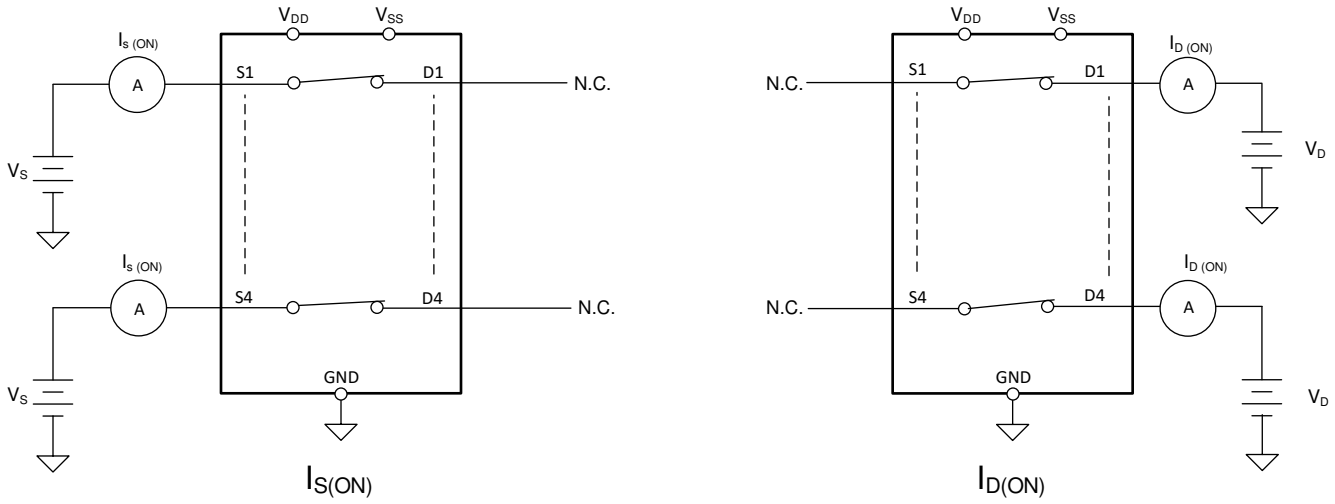


Figure 6-3. On-Leakage Measurement Setup

6.4 t_{ON} and t_{OFF} Time

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-4 shows the setup used to measure turn-on time, denoted by the symbol t_{ON}.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-4 shows the setup used to measure turn-off time, denoted by the symbol t_{OFF}.

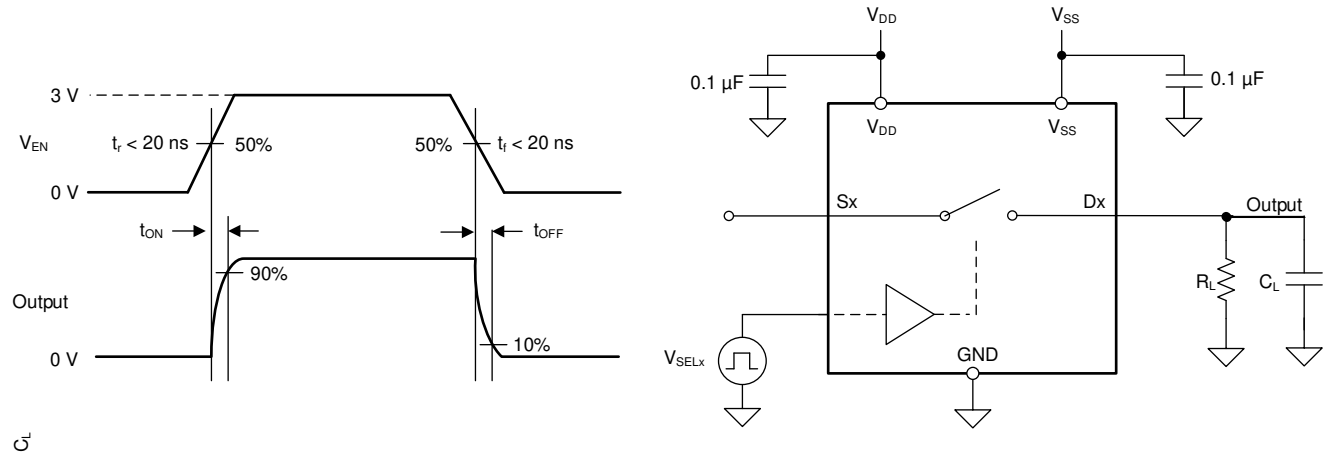


Figure 6-4. Turn-On and Turn-Off Time Measurement Setup

6.5 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 6-5 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

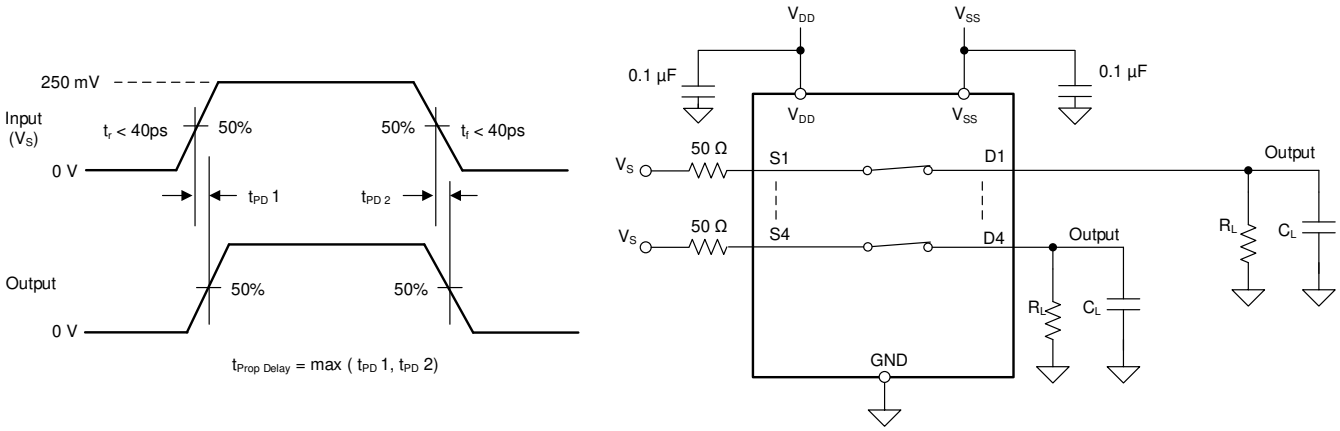


Figure 6-5. Propagation Delay Measurement Setup

6.6 Charge Injection

This device has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 6-6 shows the setup used to measure charge injection from source (Sx) to drain (Dx).

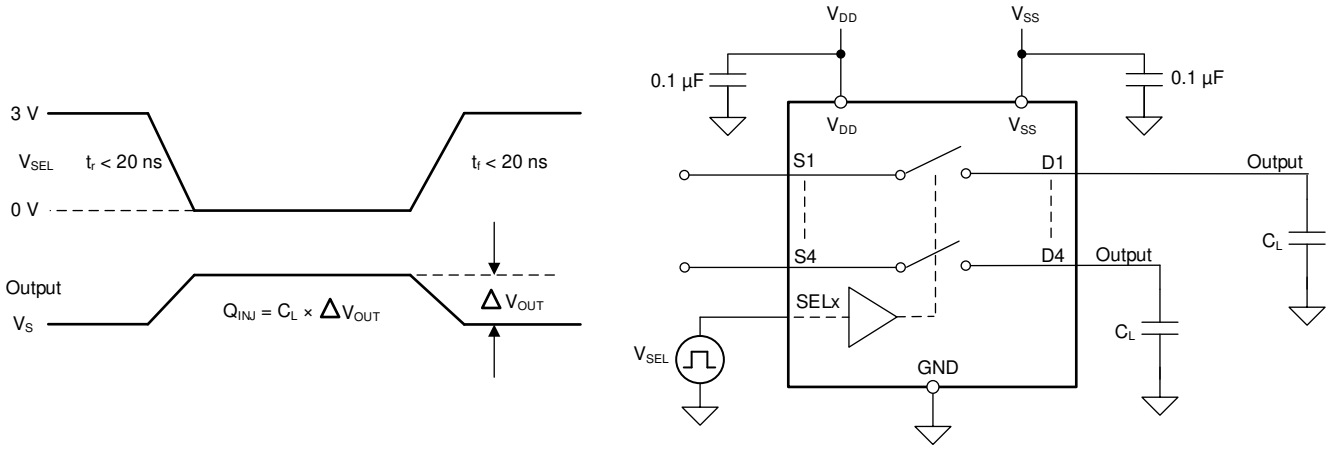
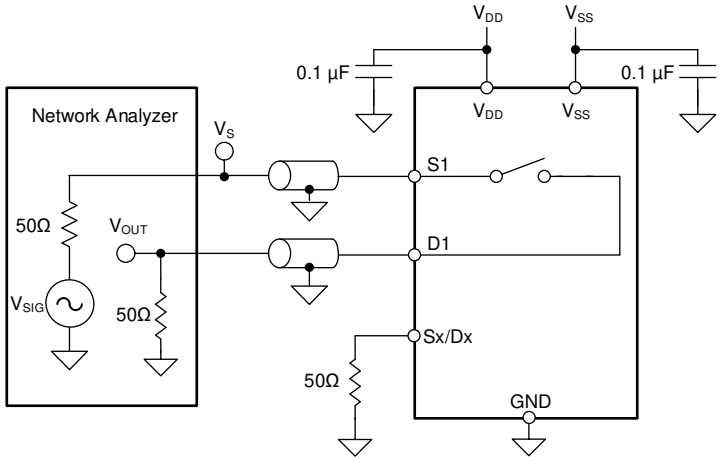


Figure 6-6. Charge-Injection Measurement Setup

6.7 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. Figure 6-7 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

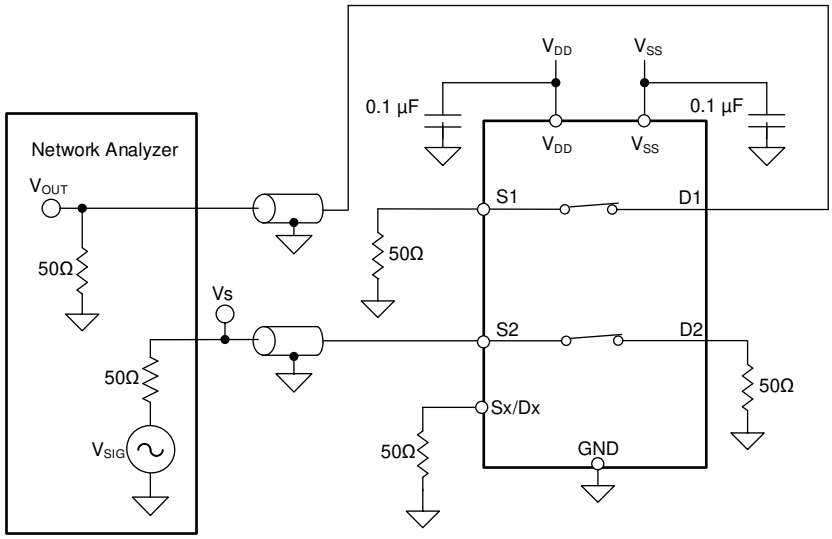


$$Off\ Isolation = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 6-7. Off Isolation Measurement Setup

6.8 Channel-to-Channel Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (Dx) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. Figure 6-8 shows the setup used to measure, and the equation used to compute crosstalk.

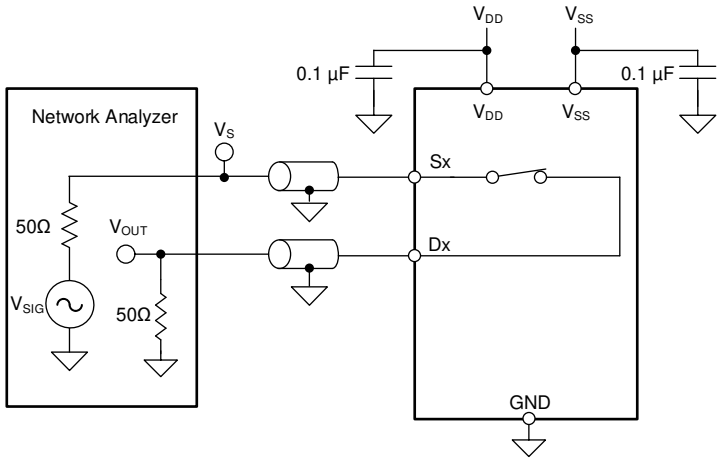


$$Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 6-8. Channel-to-Channel Crosstalk Measurement Setup

6.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. The characteristic impedance, Z_0, for the measurement is 50 Ω. Figure 6-9 shows the setup used to measure bandwidth.



$$Bandwidth = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 6-9. Bandwidth Measurement Setup

6.10 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.

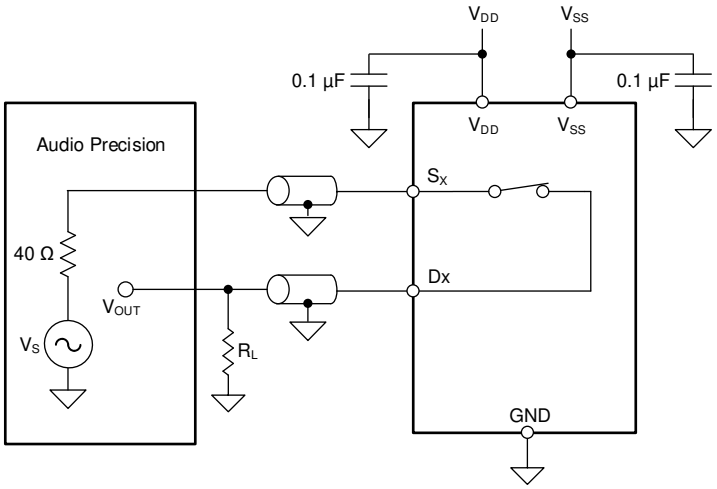
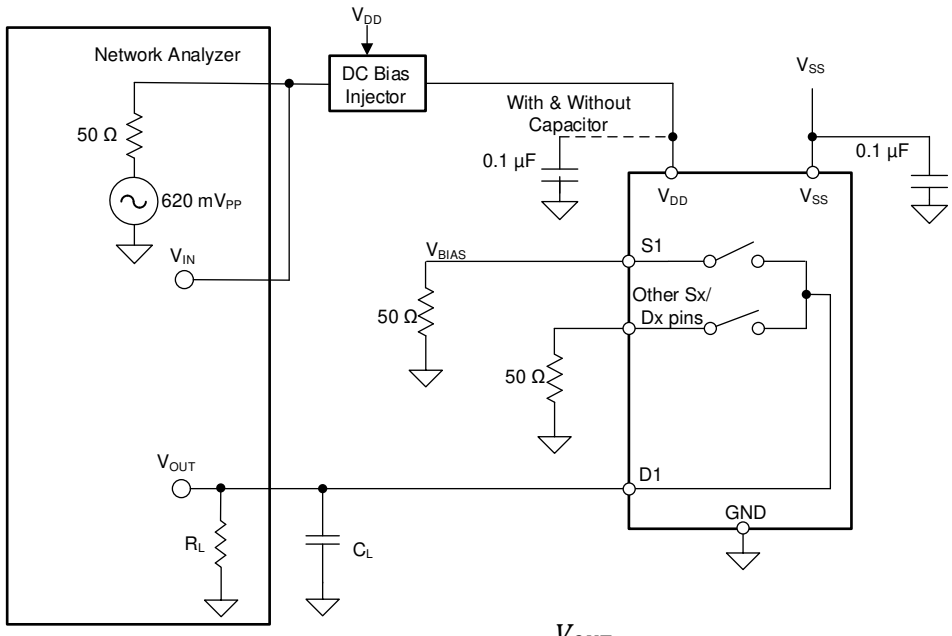


Figure 6-10. THD + N Measurement Setup

6.11 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 100 mV_{PP}. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.



$$PSRR = 20 \times Log \frac{V_{OUT}}{V_{IN}}$$

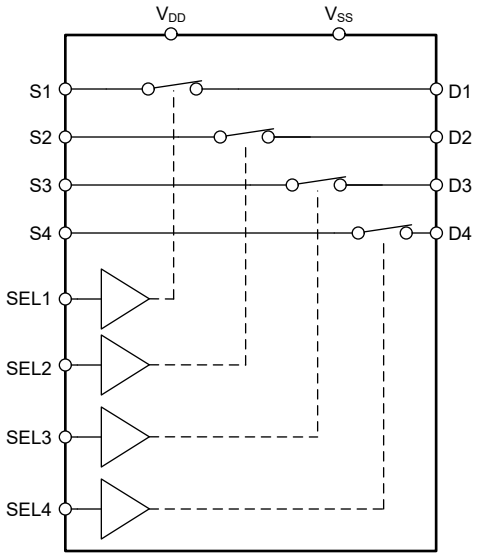
Figure 6-11. AC PSRR Measurement Setup

7 Detailed Description

7.1 Overview

TMUX7612 is a 1:1 (SPST), 4-channel switch. This device has four independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin. This device works well with dual supplies, a single supply, or asymmetric supplies such as V_{DD} = 37.5V, V_{SS} = –12.5V.

7.2 Functional Block Diagram



TMUX7612
(SELx = Logic 1)

7.3 Feature Description

7.3.1 Bidirectional Operation

The TMUX7612 conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has similar characteristics in both directions and supports both analog and digital signals.

7.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for TMUX7612 ranges from V_{SS} to V_{DD}.

7.3.3 1.8 V Logic Compatible Inputs

The TMUX7612 has 1.8-V logic compatible control for all logic control inputs. 1.8-V logic level inputs allows the TMUX7612 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

7.3.4 Flat On-Resistance

The TMUX7612 is designed with a special switch architecture to produce ultra-flat on-resistance (RON) across most of the switch input operating region. The flat RON response allows the device to be used in precision applications since the RON is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so unwanted noise is not produced from the device to affect sampling accuracy.

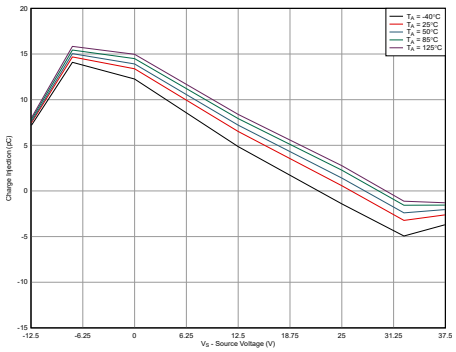
This architecture also keeps RON the same regardless of the supply voltage. The flattest on-resistance region extends roughly from 5 V above VSS to 5 V below VDD. As long as this headroom is maintained, the TMUX7612 exhibits an extremely linear response.

7.3.5 Power-Up Sequence Free

The TMUX7612 supports any power up sequencing. With the supply rails (VDD and VSS), any rail can be powered on first. Similarly, when powering down the supply rails can be powered down in any order.

7.3.6 Ultra-Low Charge Injection

The TMUX7612 contains specialized architecture to significantly reduce charge injection, which is consistent across supply and bias conditions. The result is a dramatic drop in AC noise when switching compared to other low on-resistance multiplexers or switches.

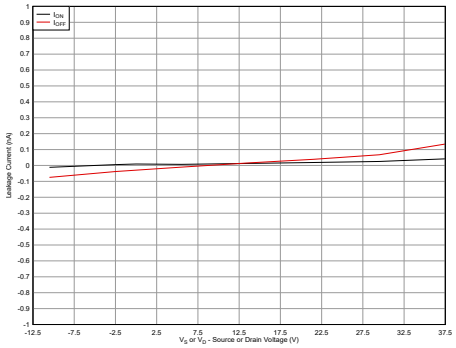


V_{DD} = 37.5 V, V_{SS} = -12.5 V

Figure 7-1. Charge Injection vs Source Voltage

7.3.7 Ultra-Low Leakage Current

The TMUX7612 provides extremely low on-leakage and off-leakage currents. This device is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents. Figure 7-2 shows typical leakage currents of the TMUX7612 devices versus source or drain voltage at V_{DD} = 32.5 V, V_{SS} = -12.5 V and 50°C. The typical performance seen here is less than 0.2 nA at 50°C, which enables the TMUX7612 to be used in a wide array of precision applications.



V_{DD} = 37.5 V, V_{SS} = -12.5 V

Figure 7-2. Leakage Current at 50°C vs Bias Voltage

7.4 Device Functional Modes

The TMUX7612 has four independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin. The control pins operate down to 1.8 V logic and can be as high as 44 V.

The TMUX7612 devices can be operated without any external components except for the supply decoupling capacitors. The SELx pins have internal pull-down resistors.

7.4.1 Truth Tables

Table 7-1 provides the truth table for TMUX7612.

Table 7-1. TMUX7612 Truth Table

SEL x (1)	CHANNEL x
0	Channel x OFF
1	Channel x ON

(1) x denotes 1, 2, 3, or 4 for the corresponding channel.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMUX7612 is a part of the precision switches and multiplexers family of devices. The device operates with dual supplies (±4.5 V to ±25V), a single supply (4.5 V to 50V), or asymmetric supplies (such as V_{DD} = 37.5 V, V_{SS} = –12.5 V), and offers a true rail-to-rail input and output signal range. The TMUX7612 offers a low R_{ON}, low on and off leakage currents and ultra-low charge injection performance. These features make the TMUX7612 a great option for high-performance and high-voltage industrial applications.

8.2 Typical Application

New generation LCD test equipment often requires simultaneous high-precision, high-voltage, multi-channel measurement capabilities and minimum channel-to-channel variation during measurement.

In LCD test systems, the parametric measurement unit (PMU) is tasked to measure device (DUT) LCD driver parametric information in terms of voltage and current. To measure current, voltage is applied at the DUT pin. To measure voltage, current is applied at the DUT pin. A 4-channel SPST switch can be used to select appropriate signals in the feedback path and measurement path in the two measurement modes. The PMU typically supports a voltage range of -12 V to 35 V and can be any combination of high or low current. An appropriate switch like the TMUX7612 with low on-resistance works well in these applications to increase the capability of higher current and even PMU ganging where multiple PMU channels are connected in parallel, allowing for a higher current output. Figure 8-1 shows a simplified diagram of such an implementation. The extremely flat on-resistance profile reduced the IR drop variation across the switch, enabling a much more streamlined calibration.

For calibration and diagnostics, the LCD test equipment also includes signals routed to the input path to confirm the system is calibrated across the life of a product or after installation. The multiplexer connects the selected signal to the appropriate pin. The TMUX7612 devices with very low RON (1.35 Ω typical) and on-leakage current (1 nA maximum) allows these devices to be used in precision measurement applications providing rail-to-rail operation suitable for high voltage testing.

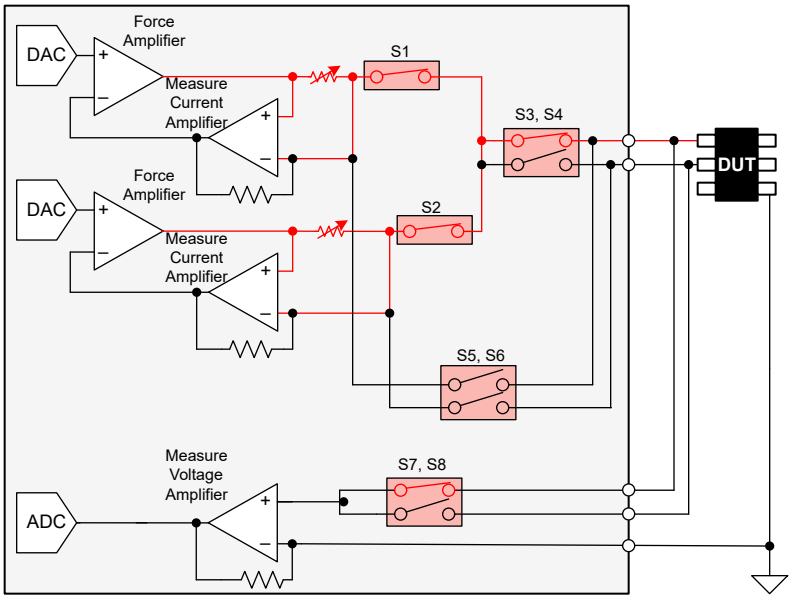


Figure 8-1. PMU Ganging Multiple Channels in Parallel

8.2.1 Detailed Design Procedure

Figure 9-1 shows one example of how two TMUX7612 can be used to gang two PMU channels together for higher current serial measurements while keeping the option for lower current parallel measurements. Here, switches S1 and S2 are used to gang the output current of the two force amplifiers in parallel to achieve a higher current output. The measure current amplifiers sense the current over the shunt resistors as a feedback to the force amplifier. S3 and S4 are used to select the DUT (device under test) channel. S7 and S8 are switched so that the correct DUT channel voltage can be measured by the measure voltage amplifier. Finally, S5 and S6 can be used when S1, S2, S3, and S4 are open to force current on both DUT channels in parallel if the higher current is not needed. This is only a two PMU channel solution but the amount of channels can be increased to any number by adding more switches.

The TMUX7612 can support 1.8-V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. All inputs to the switch must fall within the recommend operating conditions of the TMUX7612 including signal range and continuous current. For this design with a positive supply of 37.5 V on V_{DD}, and a negative supply of -12.5 V on V_{SS}, the signal range can be 37.5 V to -12.5 V. For the best linear performance, the signal range should be held within a 5 V headroom below the positive and above the negative supplies. The maximum continuous current (I_{DC}) can be up to 470 mA as shown in the *Recommended Operating Conditions* table for wide-range current measurement.

8.2.2 Design Requirements

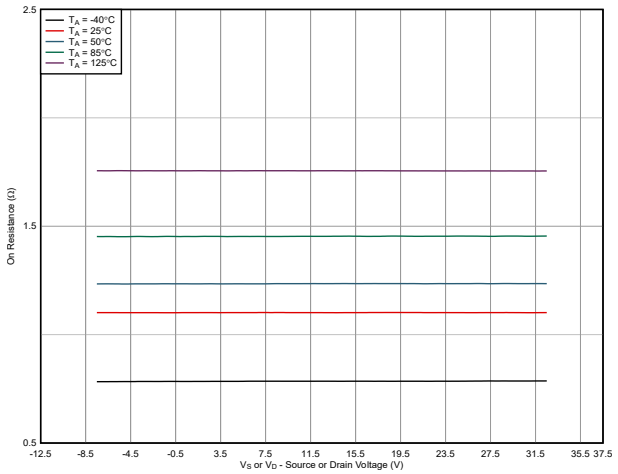
For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	37.5 V
Supply (V_{SS})	–12.5 V
Input / Output signal range	–12.5 V to 37.5 V (Rail-to-Rail operation)
	–10 V to 32.5 V (Best performance with headroom)
Max current through each channel	470 mA
Control logic thresholds	1.8 V compatible

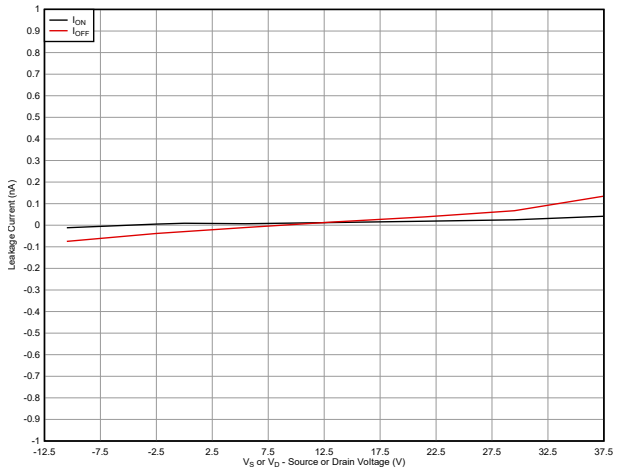
8.2.3 Application Curve

TMUX7612 has excellent linearity, leakage, and charge injection performance making them an excellent choice to minimize noise and offset errors for precision applications and very low current range measurements.



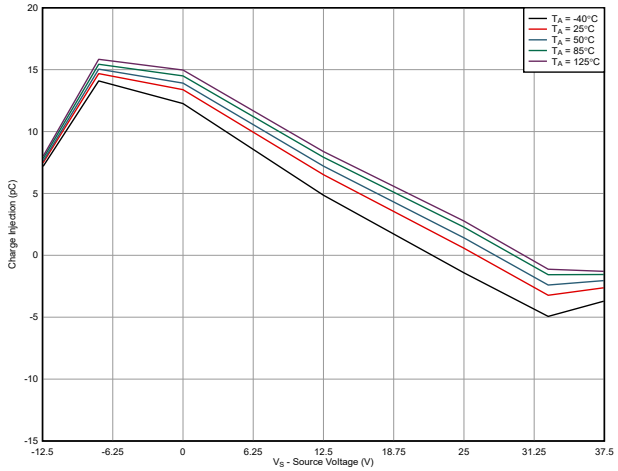
V_{DD} = 37.5 V, V_{SS} = -12.5 V

Figure 8-2. On-Resistance vs Source or Drain Voltage



V_{DD} = 37.5 V, V_{SS} = -12.5 V

Figure 8-3. Leakage Current vs Bias Voltage



V_{DD} = 37.5 V, V_{SS} = -12.5 V

Figure 8-4. Charge Injection vs Source Voltage

8.3 Thermal Considerations

For analog switches in many applications, several 100s of mA of current needs to be supported through the switch (from source to drain, or NO/NC to COM). Many devices already have a maximum current specified based on ambient temperature, but if a device specifies with junction temperature or you want to calculate for your specific use case (temperature, supply voltage, channels in parallel) you can use the following equations and scheme.

There are mainly 2 limitations to this maximum current:

1. Inherent metal limitations of the device
2. Thermal self-heating limitations

To calculate maximum current for your specific setup you need the following information:

- T_A = maximum ambient temperature
- $R_{\Theta JA}$ = package thermal coefficients
- R_{ON} = on resistance
- n = number of channels in parallel
- Limitations on maximum current based on junction temperature from the datasheet

Below is an example using TMUX7612 specifications:

Device maximum T_J=150°C

For this example we assume 20°C of self-heating at a maximum T_A=105°C and operating with 4 channels at once at ±15V. We can assume worst case R_{ON} = 2.2Ω. This number is taken from the maximum specified value at T_A = 125°C where T_J=125°C since the specification assumes no self-heating. Using the following equation we can calculate the maximum thermal limitation.

Similarly, you can calculate the T_J and total power dissipated in these examples with the following equations. Note there will be some small power dissipated from the supply current consumption of the device, which is ignored here.

$$T_J = R_{\theta JA} \times I^2 \times R_{ON} \times n + T_A \quad (1)$$

$$P_{total} = \frac{T_J - T_A}{R_{\theta JA}} \quad (2)$$

Pulse current can be calculated the same way, but using the duty cycle, d. Typically, pulse current is specified at a 10% duty cycle; however, do not exceed the maximum current provided in the pulse current table even with a shorter duty cycle.

$$I = \frac{1}{d}\sqrt{\frac{T_J - T_A}{R_{\theta JA} \times R_{ON} \times n}} \quad (3)$$

$$T_J = R_{\theta JA} \times (d \times I)^2 \times R_{ON} \times n + T_A \quad (4)$$

8.4 Power Supply Recommendations

The TMUX7612 device operates across a wide supply range of ±4.5 V to ±25V (4.5 V to 50V in single-supply mode). The device also performs well with asymmetrical supplies such as V_{DD} = 37.5 V and V_{SS} = –12.5 V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always make sure a solid ground (GND) connection is established before supplies are ramped.

8.5 Layout

8.5.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8-5 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

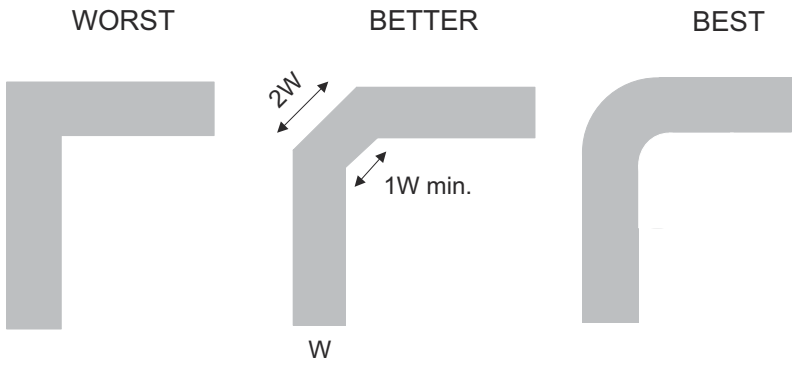


Figure 8-5. Trace Example

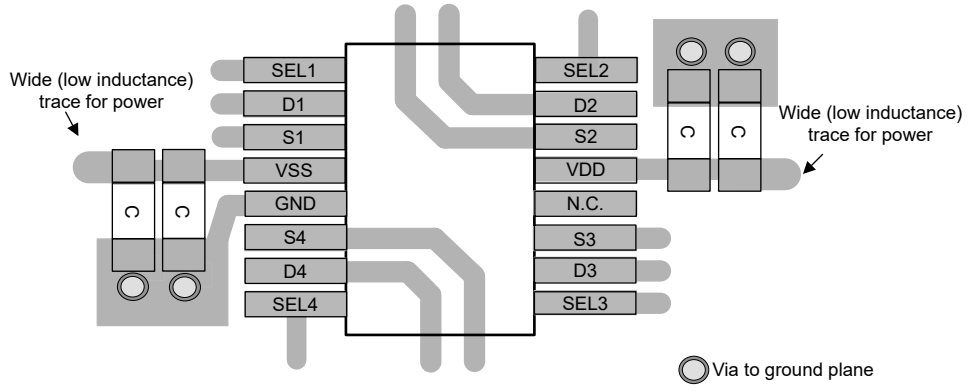
Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Figure 8-6 shows an example of a PCB layout with the TMUX7612.

Some key considerations are:

- For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD/VSS and GND. We recommend a 0.1 µF and 1 µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

8.5.2 Layout Example



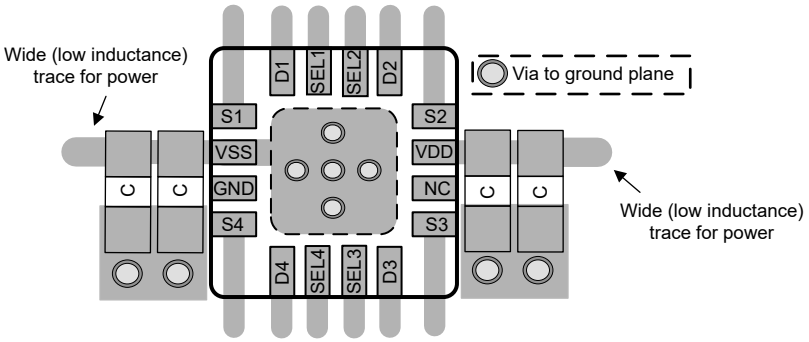


Figure 8-6. TMUX7612 Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *When to Replace a Relay with a Multiplexer* application brief
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment* application brief
- Texas Instruments, *Sample & Hold Glitch Reduction for Precision Outputs Reference Design* reference guide
- Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches* application brief
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application note
- Texas Instruments, *QFN/SON PCB Attachment* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

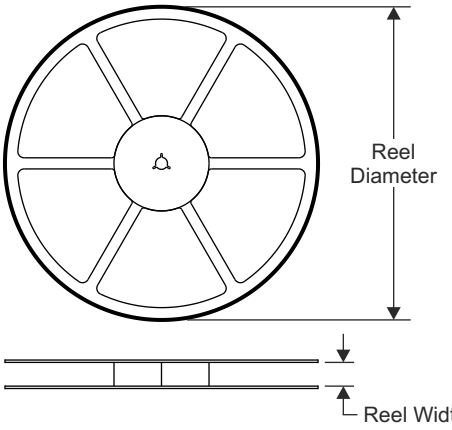
Changes from Revision * (August 2023) to Revision A (December 2024)	Page
• Changed the status from *Advanced Information* to *Production Data*	1

11 Mechanical, Packaging, and Orderable Information

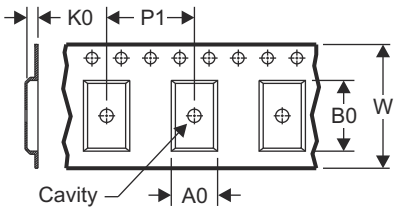
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

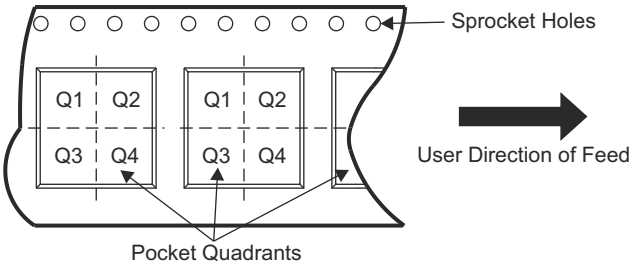


TAPE DIMENSIONS



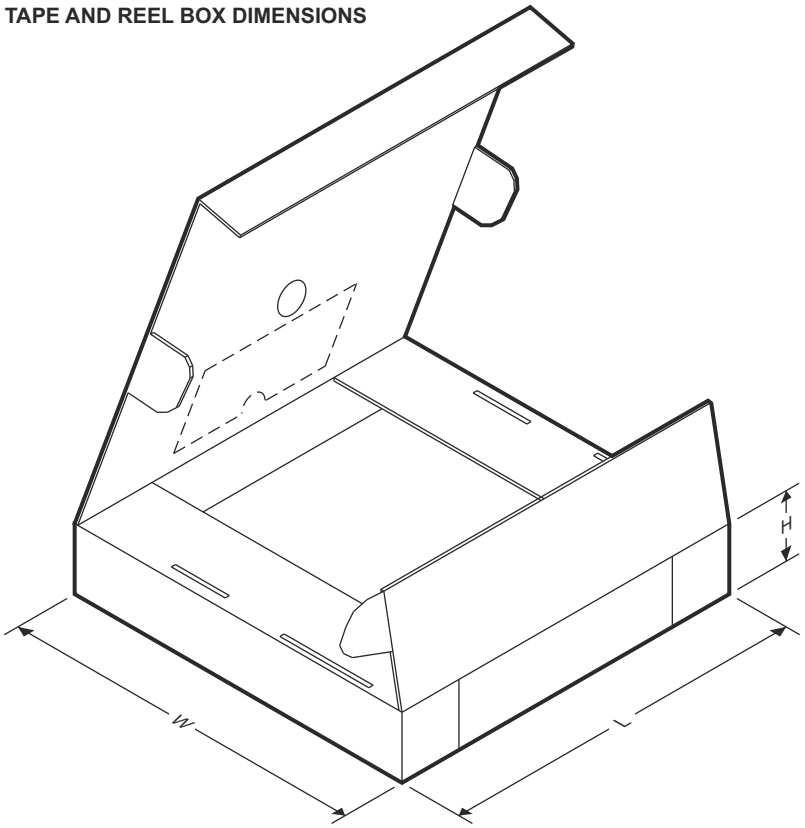
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTMUX7612PWR	TSSOP	PW	16	3000	330	12.4	6.90	5.60	1.60	8	12	Q1
PTMUX7612RUMR	WQFN	RUM	16	3000	330	12.4	4.25	4.25	1.15	8	12	Q2

TAPE AND REEL BOX DIMENSIONS



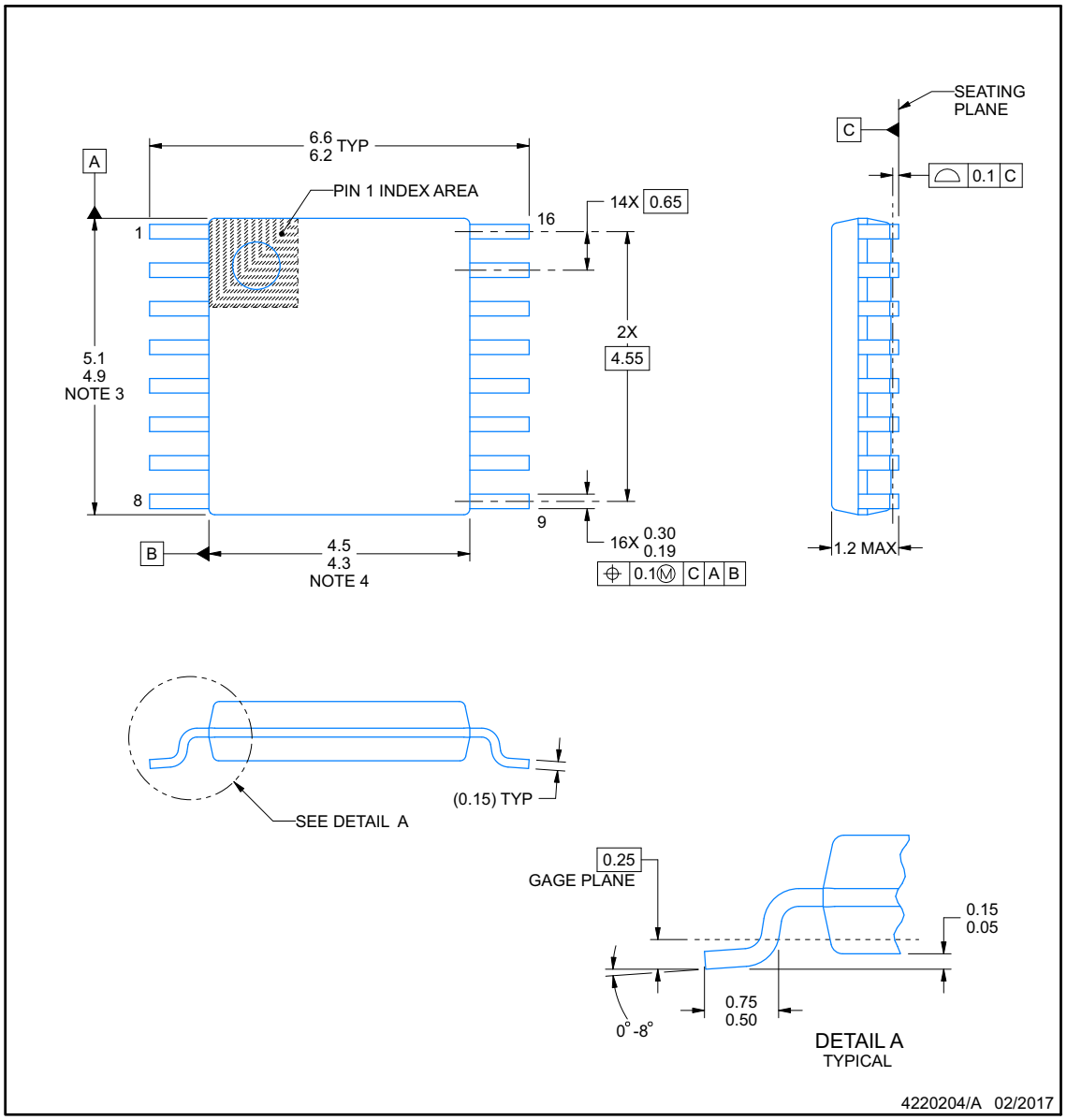
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTMUX7612PWR	TSSOP	PW	16	3000	367	367	35
PTMUX7612RUMR	WQFN	RUM	16	3000	360	360	36

11.2 Mechanical Data

PACKAGE OUTLINE

PW0016A — **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES:

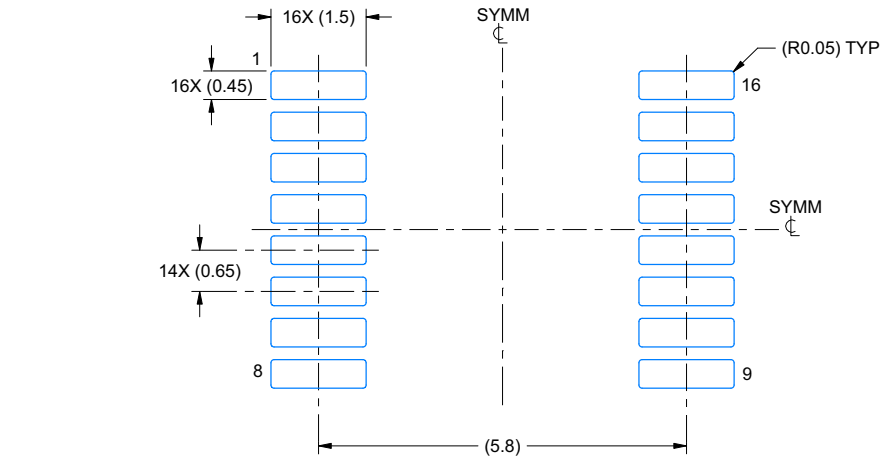
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

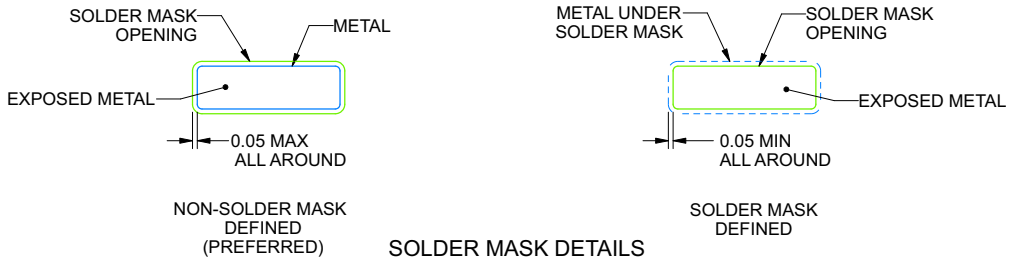
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

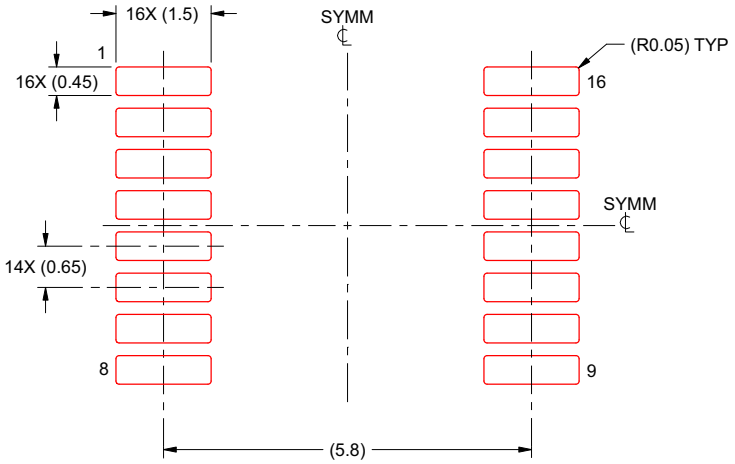
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

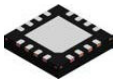
4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

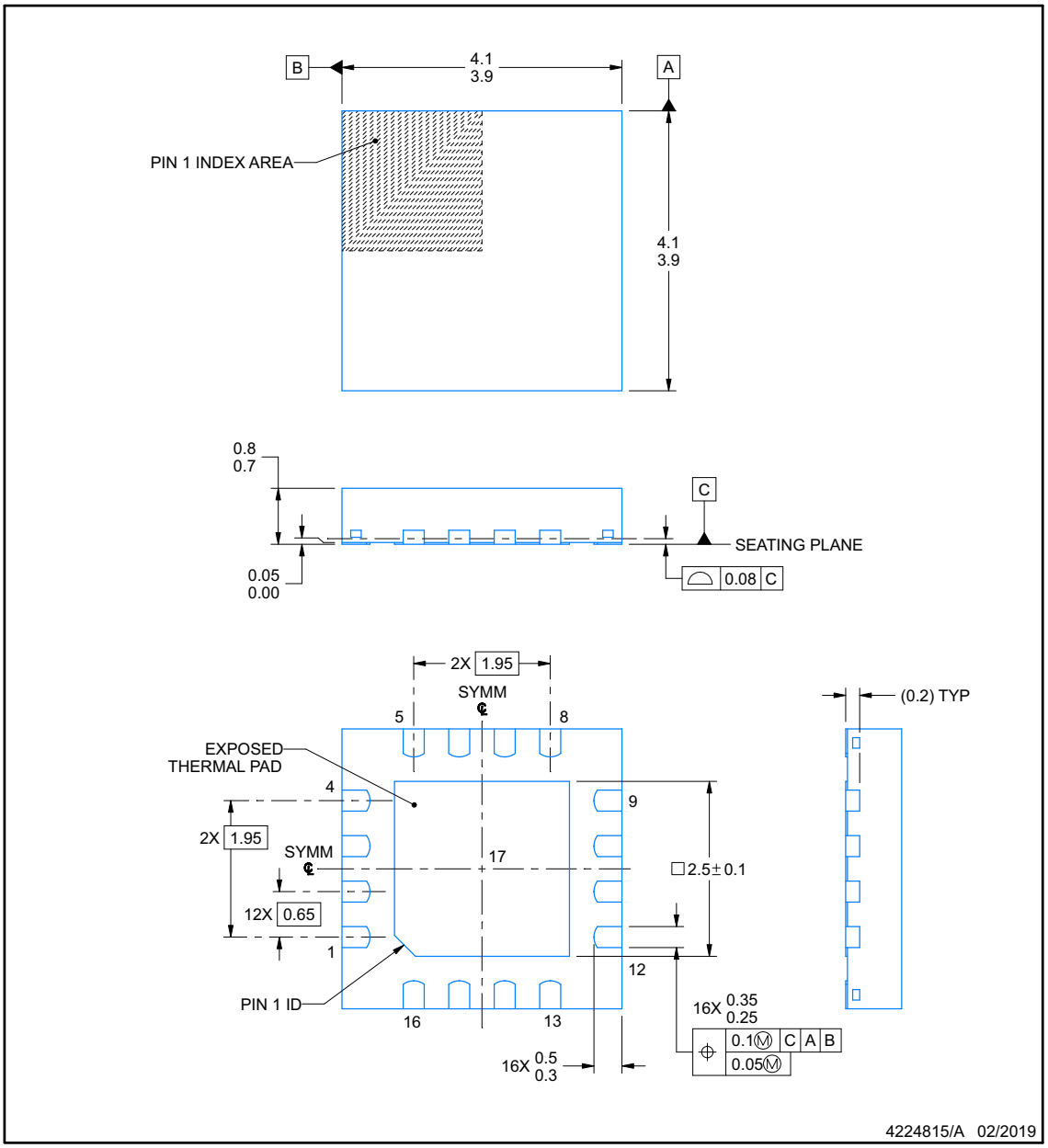
PACKAGE OUTLINE

RUM0016E



WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

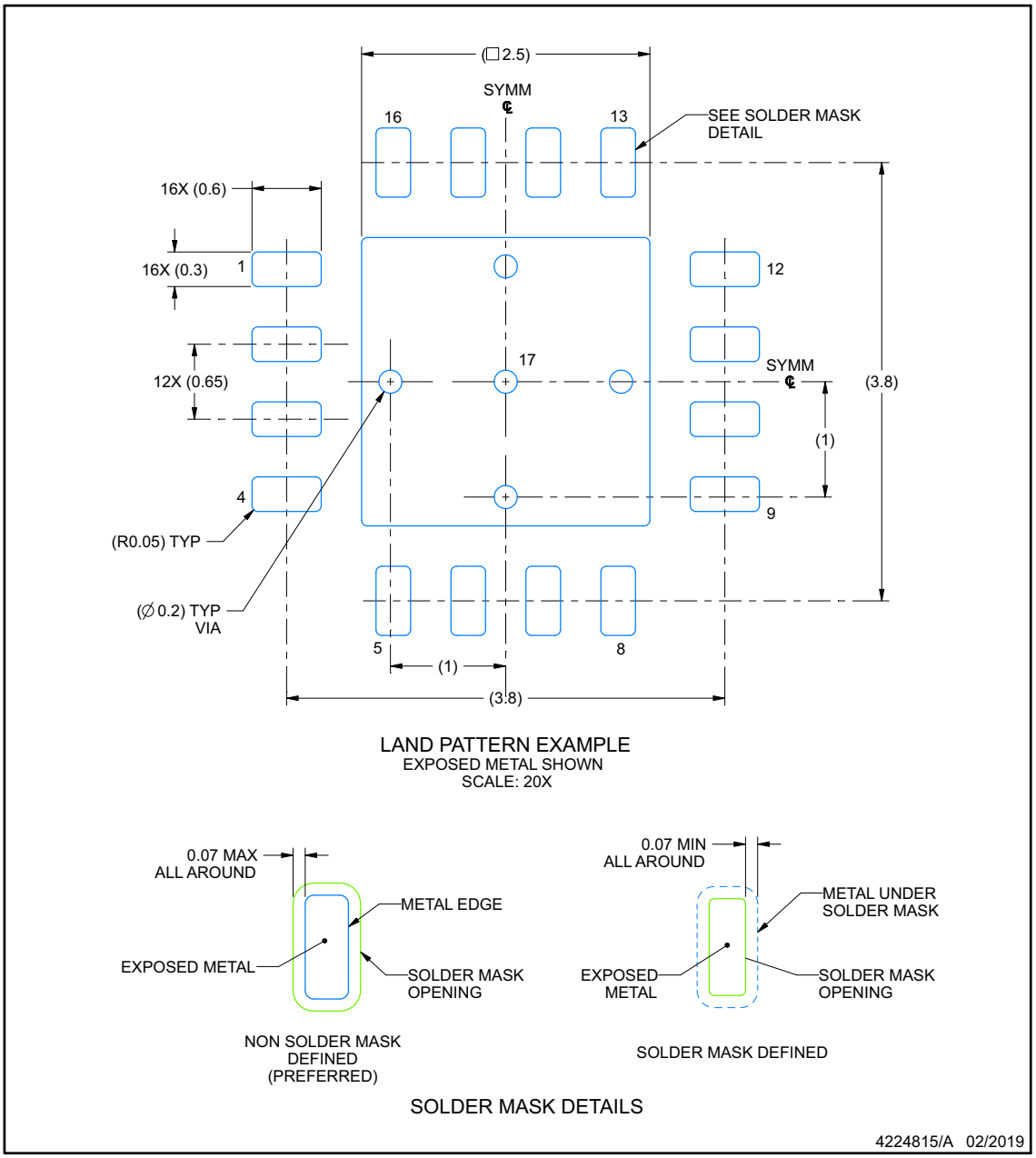
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RUM0016E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



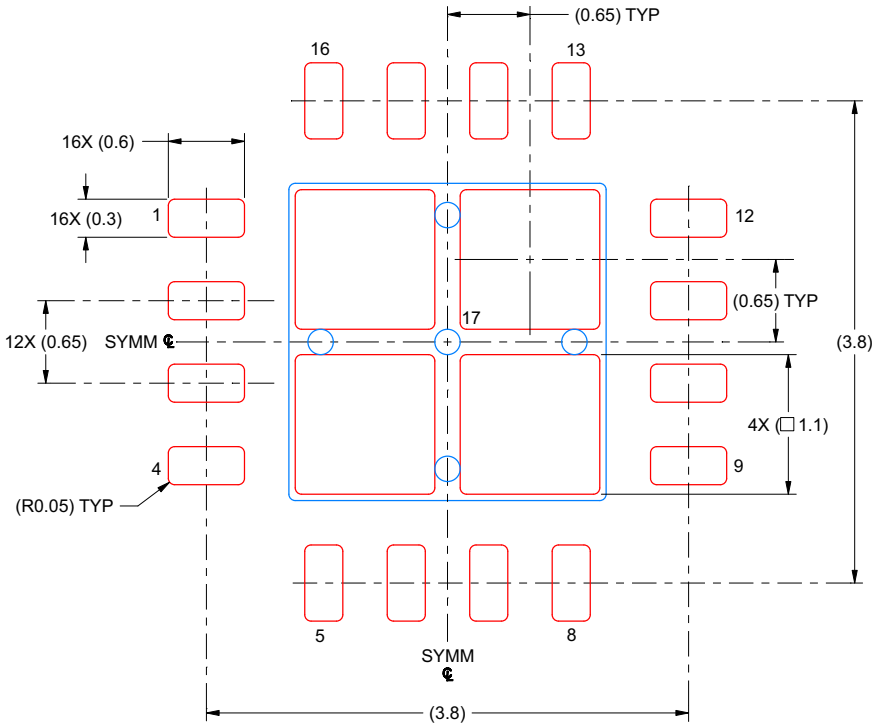
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUM0016E — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224815/A 02/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMUX7612PWR	ACTIVE	TSSOP	PW	16	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTMUX7612RUMR	ACTIVE	WQFN	RUM	16	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TMUX7612PWR	ACTIVE	TSSOP	PW	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7612	Samples
TMUX7612RUMR	ACTIVE	WQFN	RUM	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX 7612	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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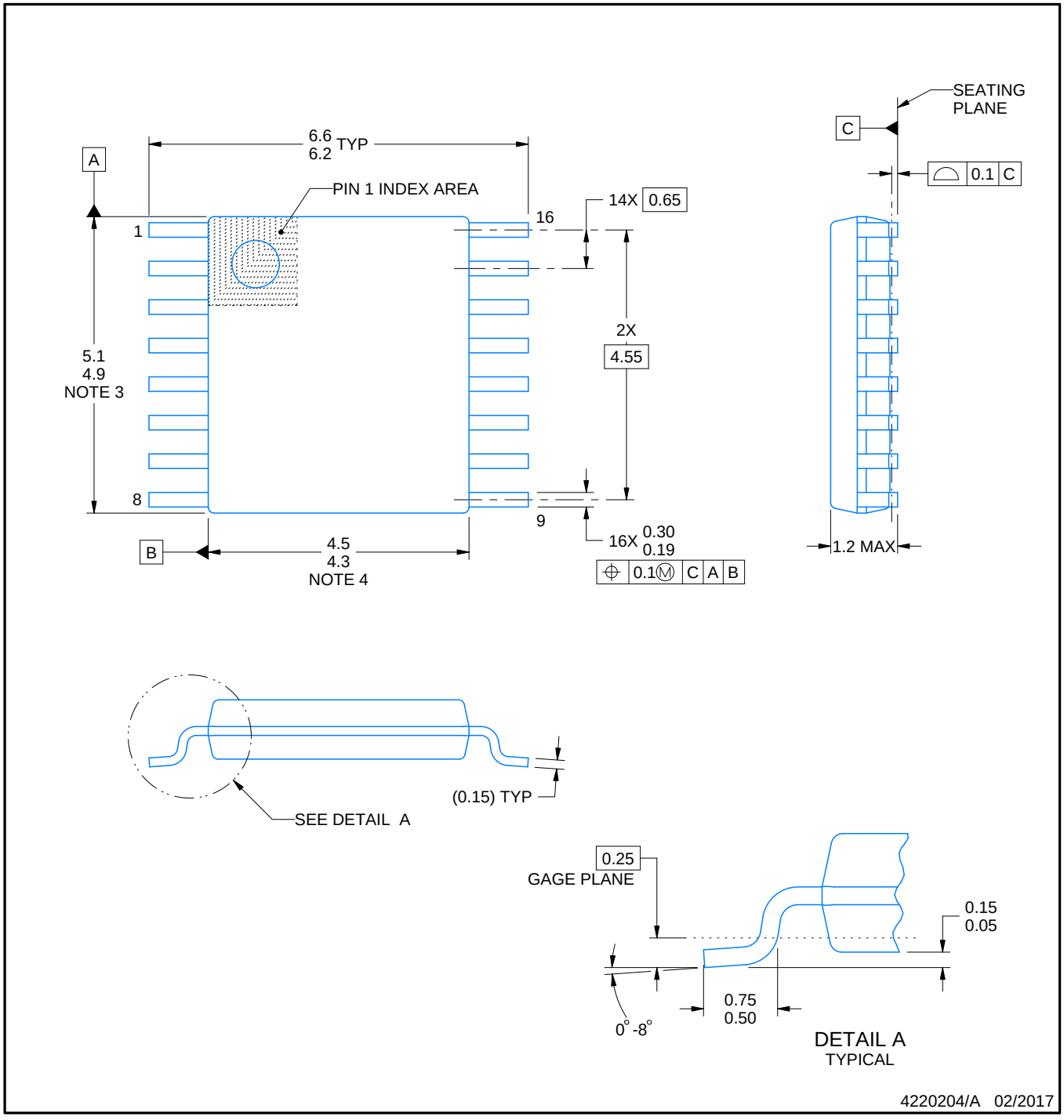
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

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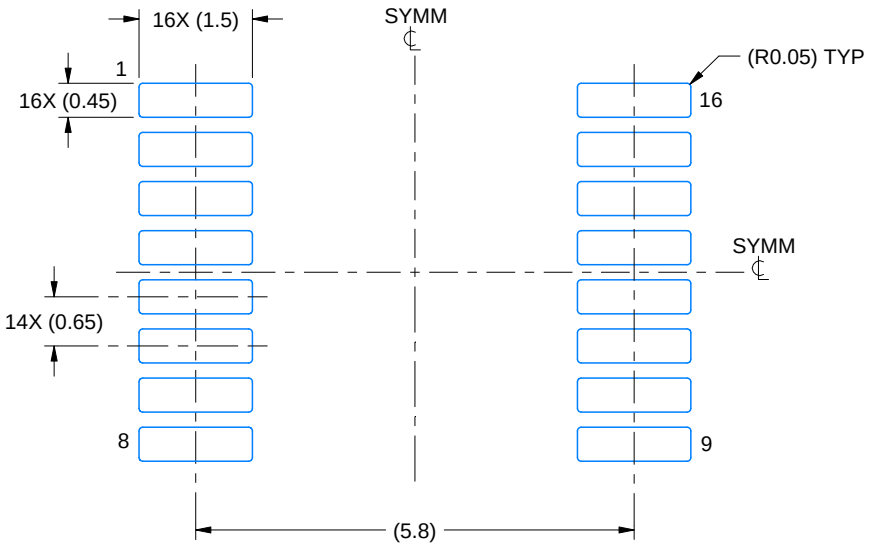
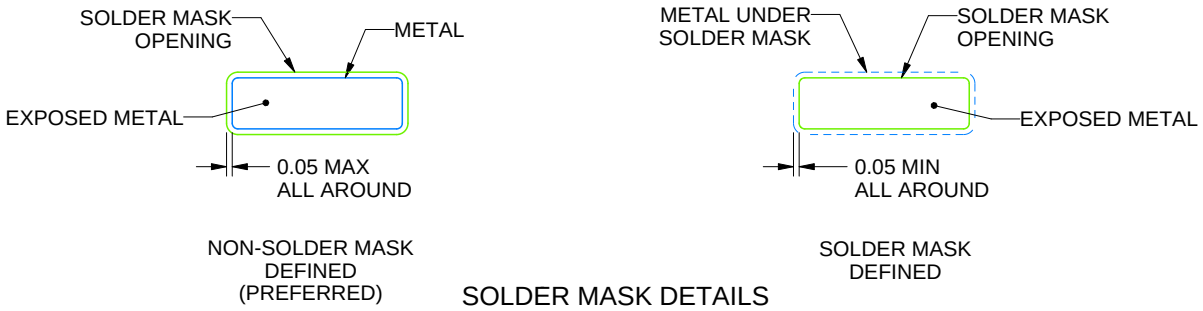
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

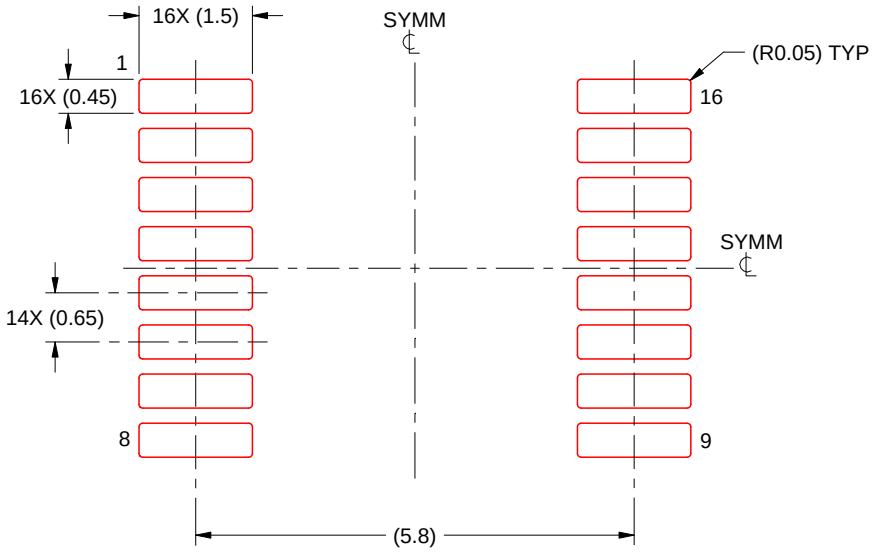


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

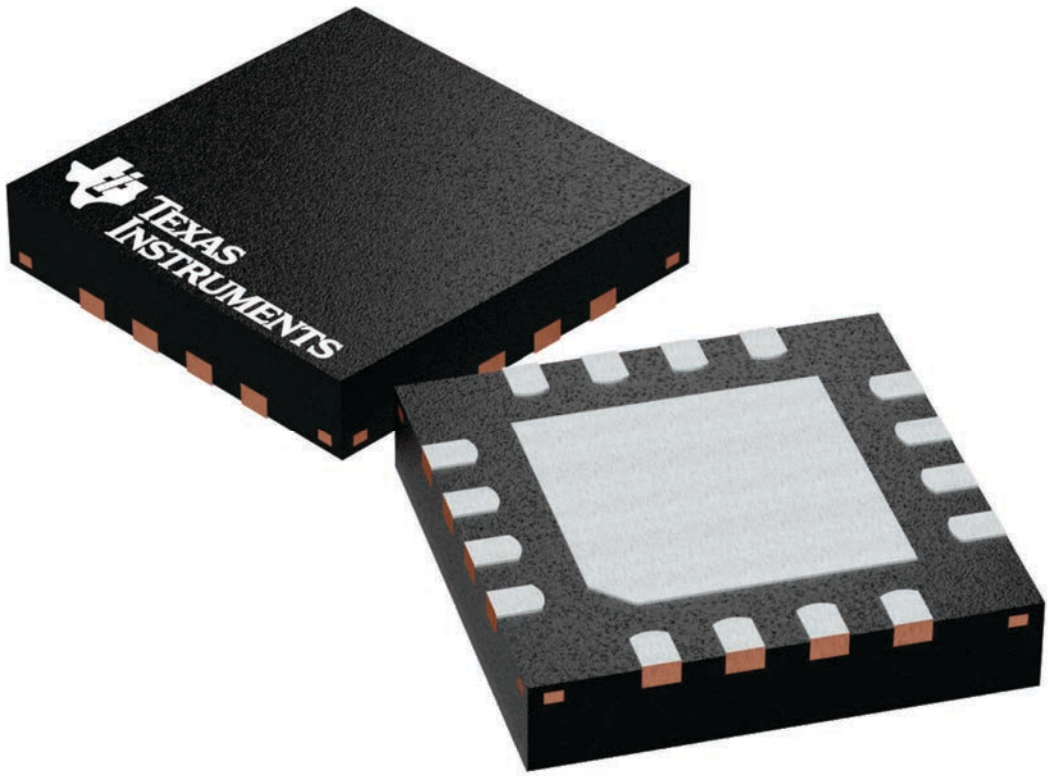
RUM 16

WQFN - 0.8 mm max height

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



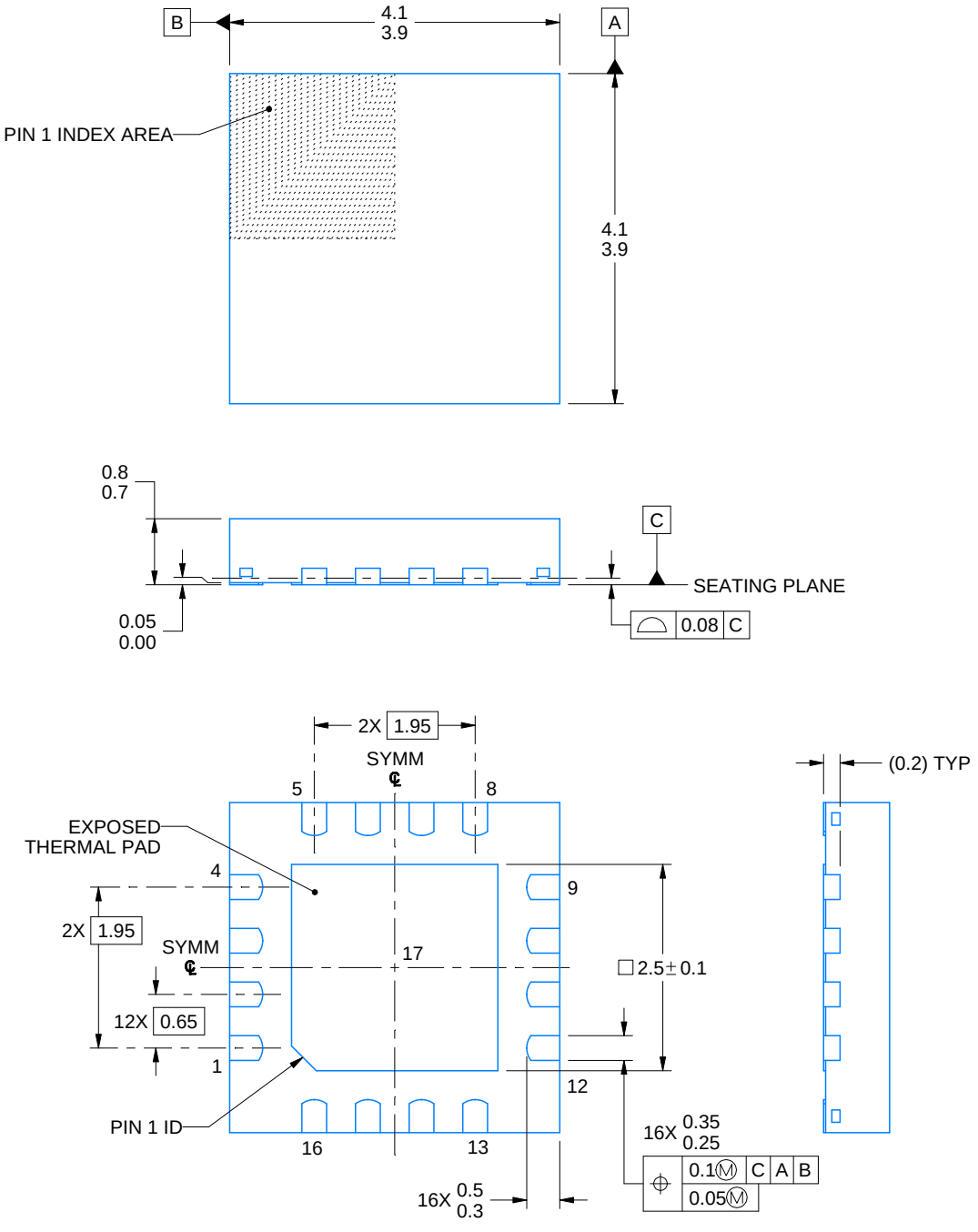
4224843/A

RUM0016E

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

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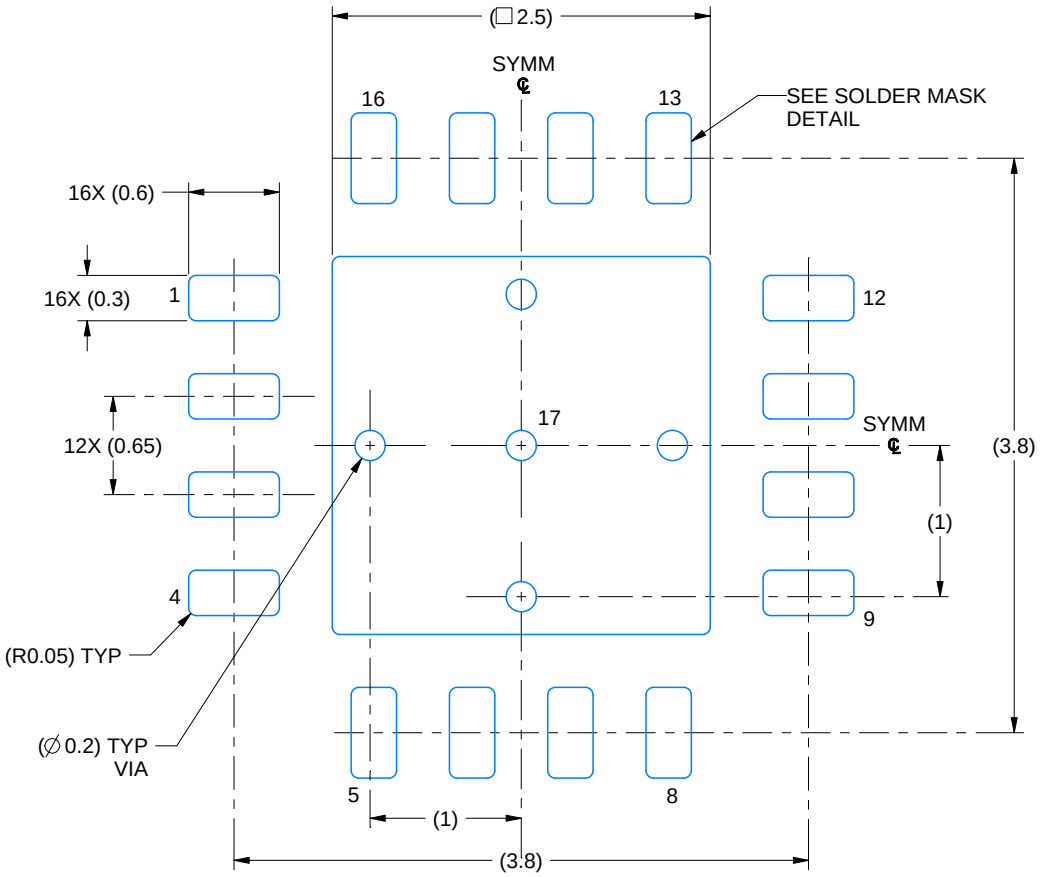
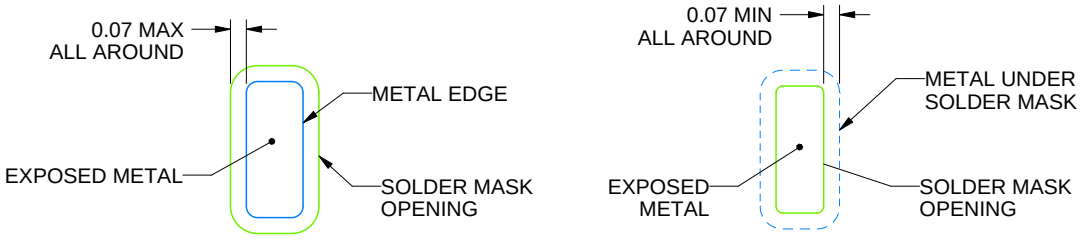
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224815/A 02/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
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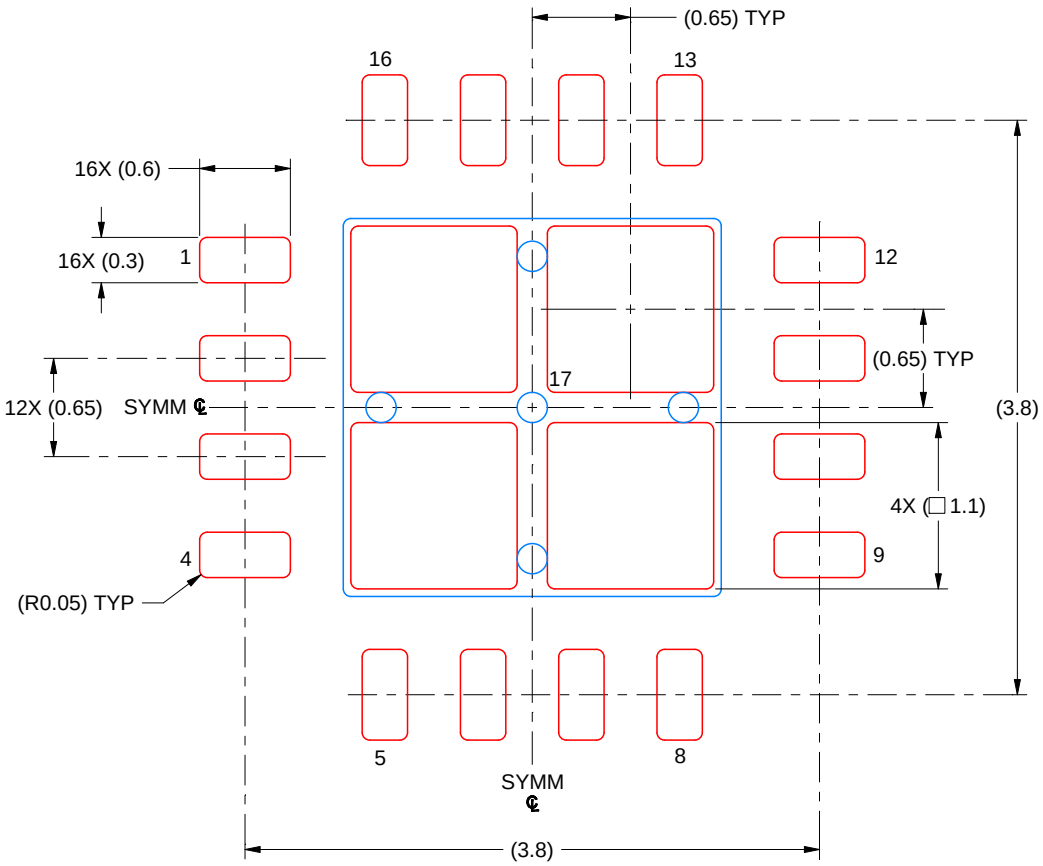

SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224815/A 02/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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