TPIC6A595 Power Logic 8-Bit Shift Register

1 Features

- Low $r_{DS(on)}$: 1Ω (Typical)
- Output short-circuit protection
- Avalanche energy: 75mJ
- Eight 350mA DMOS outputs
- 50V switching capability
- Devices are cascadable
- Low power consumption

2 Applications

- Instrumentation Clusters
- Tell-Tale Lamps
- LED Illumination and Controls
- Automotive Relay or Solenoids Drivers

3 Description

The TPIC6A595 is a monolithic, high-voltage, high-current power logic 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit, D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{\text{SRCLR}}$) is high. Write data and read data are valid only when RCK is low. When $\overline{\text{SRCLR}}$ is low, the input shift register is cleared. When output enable ($\overline{\text{G}}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{\text{G}}$ is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

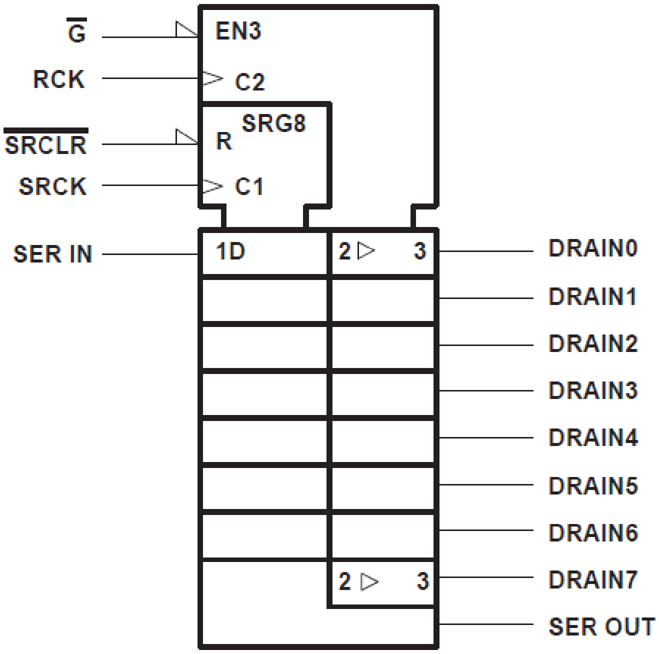
Outputs are low-side, open-drain DMOS transistors with output ratings of 50V and a 350mA continuous sink-current capability. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink current capability.

Separate power ground (PGND) and logic ground (LGND) terminals are provided to facilitate maximum system flexibility. All PGND terminals are internally connected, and each PGND terminal must be externally connected to power system ground in order to minimize parasitic impedence. A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logic and load circuits.

The TPIC6A595 is offered in a thermally-enhanced due-in-line (NE) package and a wide-body surface-mount (DW) package. The TPIC6A595 is characterized for operating over the operating case termperau range of -40 to 125°C.

Table 3-1. Device Information

PART MUMBER	PACKAGE	BODY SIZE(NOM)
TPIC6A595	PDIP(20)	24.00mm × 6.86mm
	SOIC(24)	15.40mm × 7.50mm



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Logic Symbol

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4 Pin Configuration and Functions

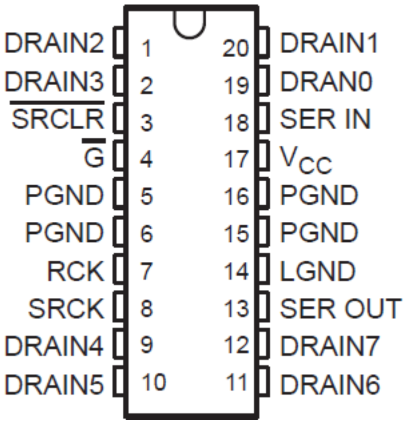


Figure 4-1. NE package 20-Pin PDIP Top View

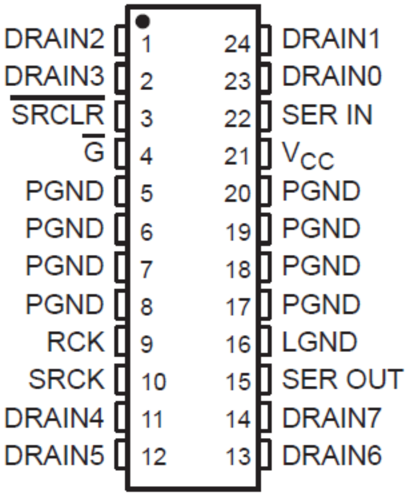


Figure 4-2. DW package 24-Pin SOIC Top View

Pin Function

Table 4-1. PDIP Pin Function

PIN		I/O	DESCRIPTION
Name	**NO.**		
DRAIN0	19	O	Open-drain output
DRAIN1	20		
DRAIN2	1		
DRAIN3	2		
DRAIN4	9		
DRAIN5	10		
DRAIN6	11		
DRAIN7	12		
$\overline{\text{G}}$	4	I	Output enable, active-low
PGND	5, 6, 15, 16	-	Power ground
LGND	14	-	Line ground
RCK	7	I	Register clock
SERIN	18	I	Serial data input
SEROUT	13	O	Serial data output
SRCK	8	I	Shift register clock
$\overline{\text{SRCLR}}$	3	I	Shift register clear, active-low
VCC	17	I	Power supply

Table 4-2. SOIC Pin Function

PIN		I/O	DESCRIPTION
Name	**NO.**		
DRAIN0	23	O	Open-drain output
DRAIN1	24		
DRAIN2	1		
DRAIN3	2		
DRAIN4	11		
DRAIN5	12		
DRAIN6	13		
DRAIN7	14		
$\overline{\text{G}}$	4	I	Output enable, active-low
PGND	5, 6, 7, 8, 17, 18, 19, 20	-	Power ground
LGND	16	-	Line ground
RCK	9	I	Register clock
SERIN	22	I	Serial data input
SEROUT	15	O	Serial data output
SRCK	10	I	Shift register clock
$\overline{\text{SRCLR}}$	3	I	Shift register clear, active-low
VCC	21	I	Power supply

5 Specifications

5.1 Absolute Maximum Ratings

over recommended operating case temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Logic supply voltage(2)			7	V
V_I	Logic input voltage range		-0.3	7	V
V_{DS}	Power DMOS drain-to-source voltage(3)			50	V
	Continuous source-drain diode anode current			1	A
	Pulsed source-drain diode anode current(4)			2	A
I_{DN}	Pulsed drain current, each output, all outputs on(4)	T_A = 25°C		1.1	A
I_{DN}	Continuous drain current, each output, all outputs on	T_A = 25°C		350	A
	Peak drain current, single output(4)	T_A = 25°C		1.1	A
E_{AS}	Single-pulse avalanche energy (see Figure 6-6)			75	mJ
I_{AS}	Avalanche current(5)			600	mA
	Continuous total dissipation		See Section 5.2		
T_C	Operating case temperature range		-40	125	℃
T_J	Operating virtual junction temperature range		-40	150	℃
T_{stg}	Storage temperature range		-65	150	℃
	Lead temperature 1,6mm (1/16 inch) from case for 10 seconds			260	℃

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to LGND and PGND.
(3) Each power DMOS source is internally connected to PGND.
(4) Pulse duration ≤ 100µs and duty cycle ≤ 2%.
(5) DRAIN supply voltage = 15V, starting junction temperature (T_{JS}) = 25°C, L = 210mH, I_{AS} = 600mA (see Figure 6-6).

5.2 Dissipation Rating Table

PACKAGE	T_C ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1750mW	14mW/°C	350mW
NE	2500mW	20mW/°C	500mW

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Logic supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	0.85 V_{CC}	VCC	V
V_{IL}	Low-level input voltage	0	0.15 V_{CC}	V
	Pulsed drain output current, T_C = 25°C, V_{CC} = 5V(1) (2)	−1.8	0.6	A
t_{su}	Setup time, SER IN high before SRCK↑ (seeFigure 6-2)	10		ns
t_h	Hold time, SER IN high after SRCK↑ (seeFigure 6-2)	10		ns
t_w	Pulse duration (see Figure 6-2)	20		ns
T_C	Operating case temperature	−40	125	°C

(1) Pulse duration ≤ 100µs and duty cycle ≤ 2%.
(2) Technique should limit $T_J - T_C$ to 10°C maximum.

5.4 Electrical Characteristics

V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1mA			50			V
V_{SD}	Source-to-drain diode forward voltage	I_F = 350mA	See(1)			0.8	1.1	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = − 20µA			V_{CC} − 0.1	V_{CC}		V
		I_{OH} = − 4mA			V_{CC} − 0.5	V_{CC} − 0.2		
V_{OL}	Low-level output voltage, SER OUT	I_{OL} = 20µA				0	0.1	V
		I_{OL} = 4mA				0.2	0.5	
I_{IH}	High-level input current	$V_I = V_{CC}$					1	µA
I_{IL}	Low-level input current	V_I = 0					−1	µA
$I_{O(chop)}$	Output current at which chopping starts	T_C = 25°C, See Figure 6-3 and Figure 6-4 (2)			0.6	0.8	1.1	A
I_{CC}	Logic supply current	I_O = 0	$V_I = V_{CC}$ or 0			0.5	5	mA
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5MHz, $V_I = V_{CC}$ or 0	I_O = 0, V_{CC} = 5V	C_L = 30pF, See Figure 5-1		1.3		mA
$I_{(nom)}$	Nominal current	$V_{DS(on)}$ = 0.5V, V_{CC} = 5V	$I_{(nom)} = I_D$	T_C = 85°C		350		mA
			See(2) (3) (4)					
I_D	Drain current, off-state	V_{DS} = 40V	T_C = 25°C			0.1	1	µA
		V_{DS} = 40V	T_C = 125°C			0.2	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 350mA	T_C = 25°C	See Figure 5-4 and Figure 5-5 (2) (3)		1	1.5	Ω
		I_D = 350mA	T_C = 125°C			1.7	2.5	
		I_D = 350mA	TC= 40°C					

(1) Pulse duration ≤ 100µs and duty cycle ≤ 2%
(2) Technique should limit $T_J - T_C$ to 10°C maximum.
(3) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
(4) Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5V at T_C = 85°C.

5.5 Switching Characteristics

V_{CC} = 5V, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$	C_L = 30pF	I_D = 350mA		30		ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	See Figure 6-1, Figure 6-2, and Figure 5-6			125		ns
tr	Rise time, drain output				60		ns
t_f	Fall time, drain output				30		ns
t_a	Reverse-recovery-current rise time	I_F = 350mA	di/dt = 20A/µs		100		ns
t_{rr}	Reverse-recovery time	See Figure 6-5 (1) (2)			300		ns

(1) Technique should limit $T_J - T_C$ to 10°C maximum.
(2) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

5.6 Thermal Resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case	DW	All eight outputs with equal power		10	°C/W
		NE			10	
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW	All eight outputs with equal power		50	°C/W
		NE			50	

5.7 Typical Characteristics

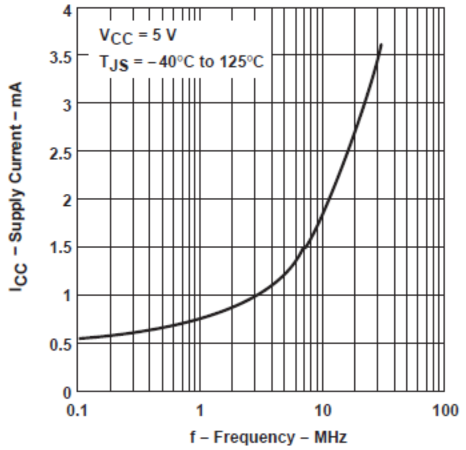


Figure 5-1. Supply Current vs Frequency

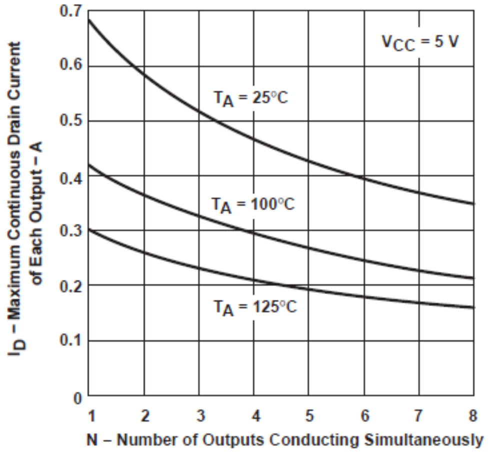


Figure 5-2. Maximum Continuous Drain Current of Each Output vs Number of Outputs Conducting Simultaneously

5.7 Typical Characteristics (continued)

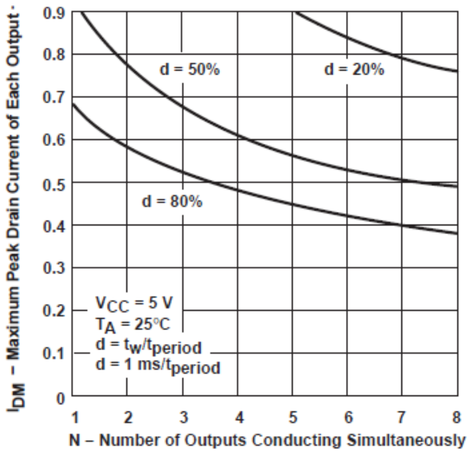


Figure 5-3. Maximum Peak Drain Current of Each Output vs Number of Outputs Conducting Simultaneously

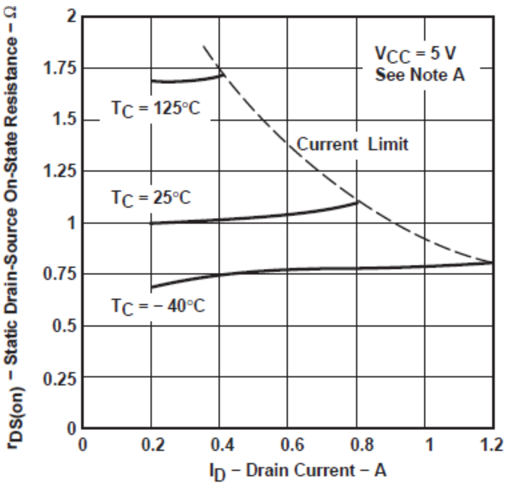


Figure 5-4. Static Drain-Source On-State Resistance vs Drain Current

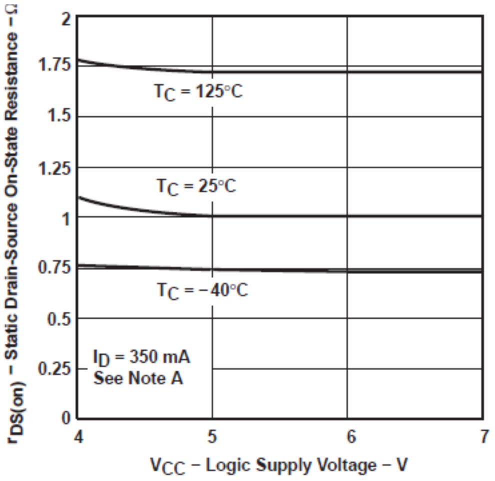


Figure 5-5. Static Drain-Source On-State Resistance vs Logic Supply Voltage

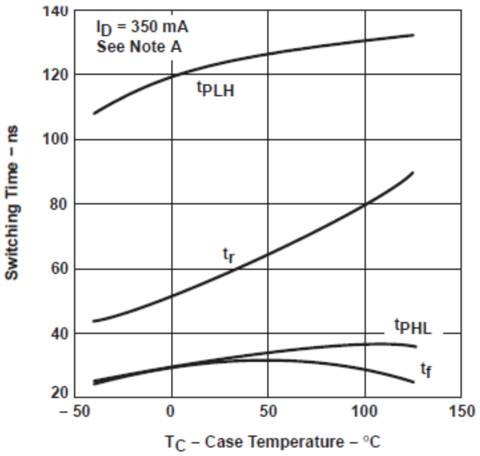
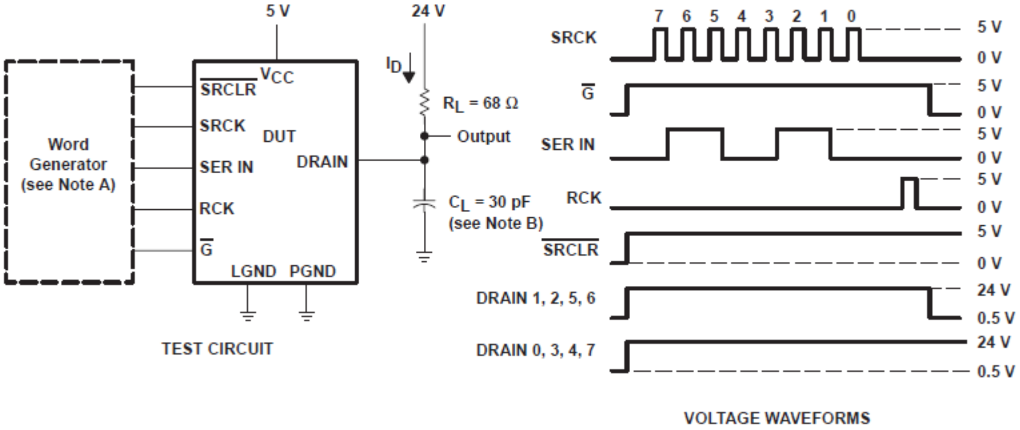


Figure 5-6. Switching Time vs Case Temperature

6 Parameter Measurement Information

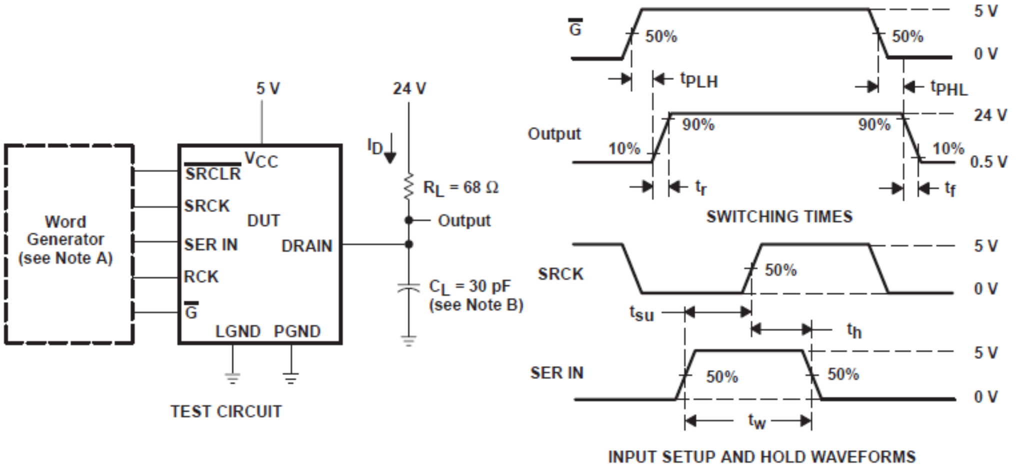


A. The word generator has the following characteristics: $t_r \le 10ns$, $t_f \le 10ns$, $t_w = 300ns$, pulsed repetition rate (PRR) = 5kHz, $Z_O = 50\Omega$.

B. C_L includes probe and jig capacitance.

C. Write data and read data are valid only when RCK is low

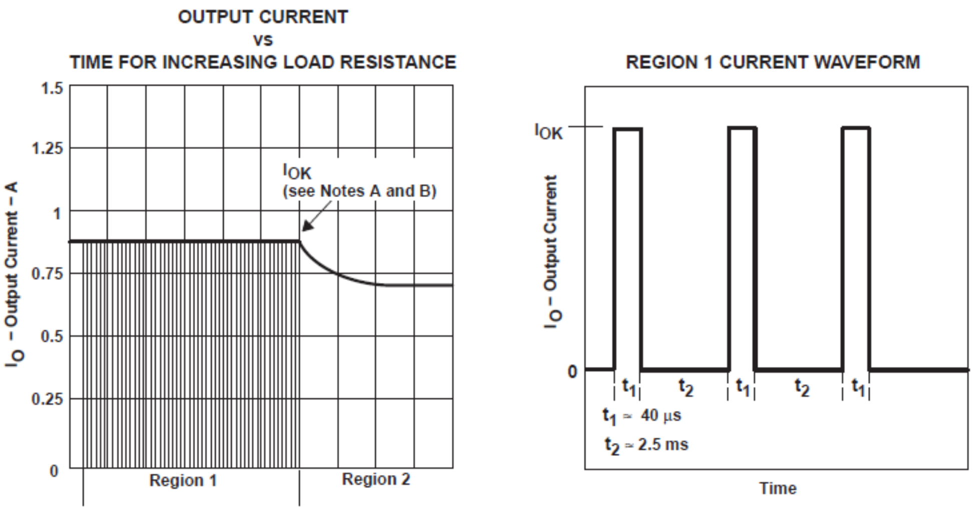
Figure 6-1. Resistive Load Operation



A. The word generator has the following characteristics: $t_r \le 10ns$, $t_f \le 10ns$, $t_w = 300ns$, pulsed repetition rate (PRR) = 5kHz, $Z_O = 50\Omega$.

B. C_L includes probe and jig capacitance.

Figure 6-2. Test Circuit, Switching Times, and Voltage Waveforms



First output current pulses after turn-on in chopping mode with resistive load.

A. Figure 6-4 illustrates the output current characteristics of the device energizing a load having initially low, increasing resistance, for example, an incandescent lamp. In region 1, chopping occurs and the peak current is limited to I_{OK}. In region 2, output current is continuous. The same characteristics occur in reverse order when the device energizes a load having an initially high, decreasing resistance.

B. Region 1 duty cycle is approximately 2%.

Figure 6-3. Chopping-Mode Characteristics

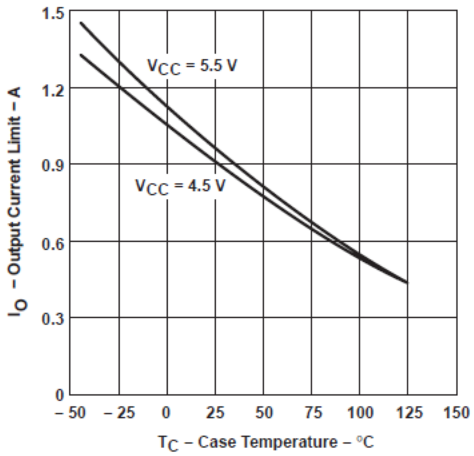
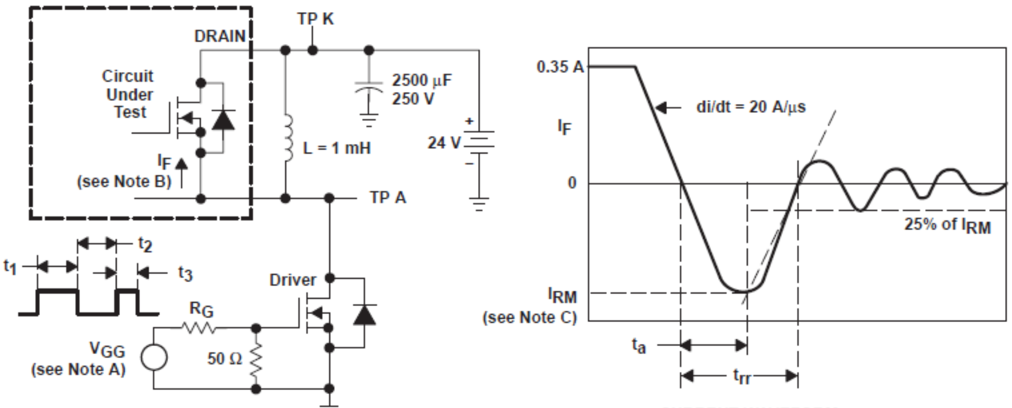


Figure 6-4. Output Current Limit vs Case Temperature



TEST CIRCUIT

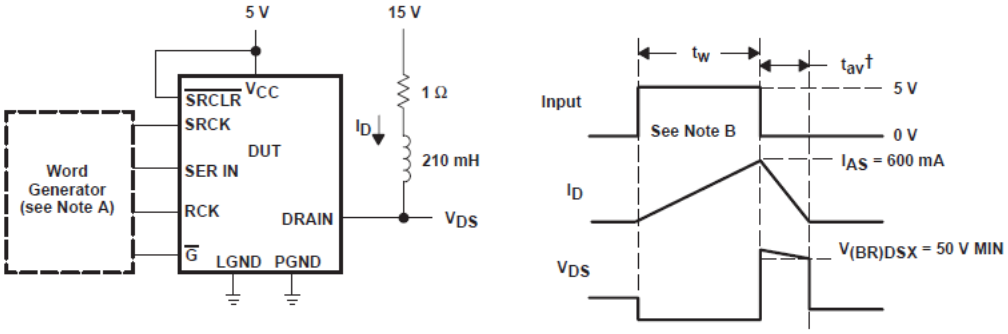
CURRENT WAVEFORM

A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20A/µs. A V_{GG} double-pulse train is used to set I_F = 0.35A, where t_1= 10µs, t_2 = 7µs, and t_3 = 3µs.

B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

C. I_{RM} = maximum recovery current.

Figure 6-5. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

A. † Non-JEDEC symbol for avalanche time.

B. The word generator has the following characteristics: $t_r \le$ 10ns, $t_f \le$ 10ns, Z_O = 50Ω.

C. Input pulse duration, t_w, is increased until peak current I_{AS} = 600mA. Energy test level is defined as E_{AS} = (I_{AS} x $V_{(BR)DSX}$ x t_{av})/2 = 75mJ.

Figure 6-6. Single-Pulse Avalanche Energy Test Circuit and Waveforms

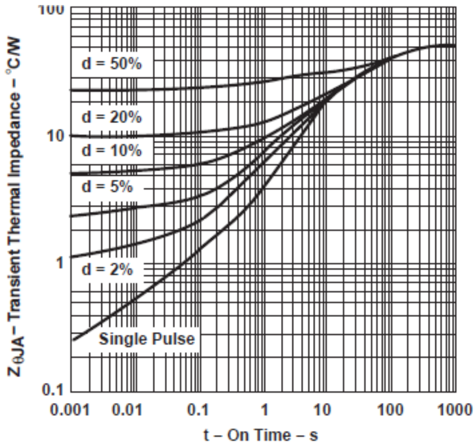


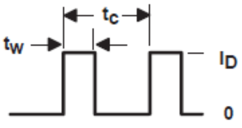
Figure 6-7. NE Package Transient Thermal Impedance vs On Time

The single-pulse curve represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left|\frac{t_w}{t_c}\right| R_{\theta JA} + \left|1 - \frac{t_w}{t_c}\right| Z_{\theta}(t_w + t_c) + Z_{\theta}(t_w) - Z_{\theta}(t_c) \tag{1}$$

where:

- $Z_{\theta}(t_w)$ = the single-pulse thermal impedance for $t = t_w$ seconds
- $Z_{\theta}(t_c)$ = the single-pulse thermal impedance for $t = t_c$ seconds
- $Z_{\theta}(t_w+t_c)$ = the single-pulse thermal impedance for $t = t_w + t_c$ seconds
- $d = t_w/t_c$

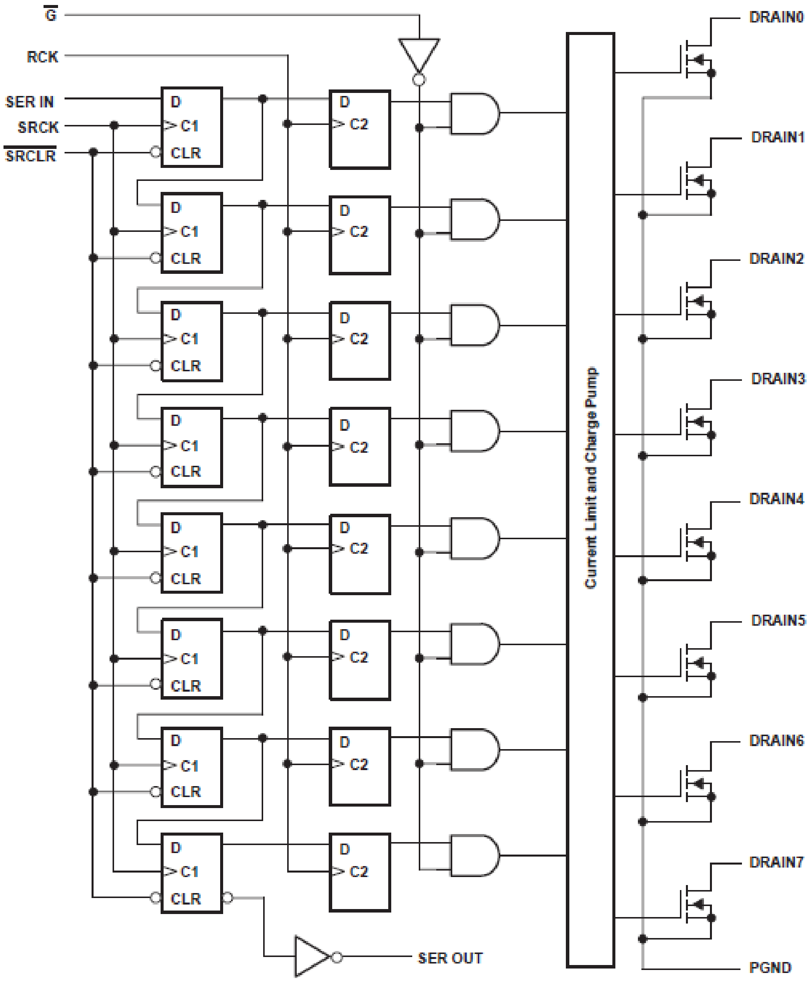


7 Detailed Description

7.1 Overview

The TPIC6A595 device is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection, so it can also drive relays, solenoids, and other medium-current or high-voltage loads.

7.2 Functional Block Diagram



Functional Block Diagram

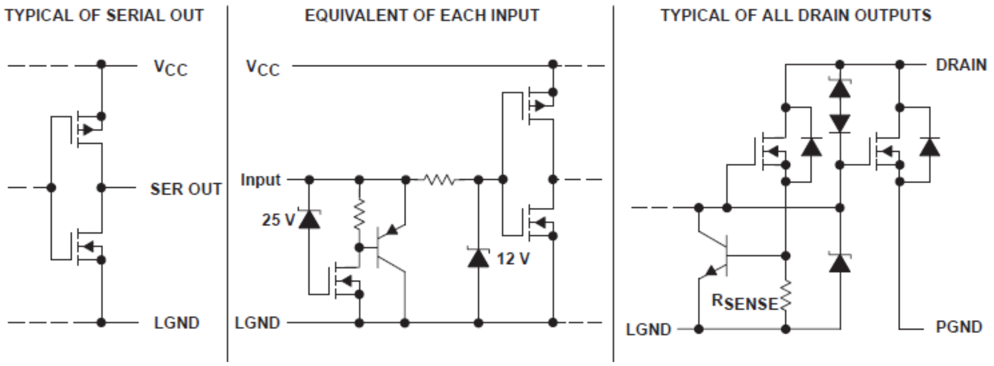


Figure 7-1. Functional Block Diagram (continued)

7.3 Feature description

7.3.1 Serial-In Interface

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. Write data and read data are valid only when RCK is low. The storage register transfers data to the output buffer when shift register clear ($\overline{\text{SRCLR}}$) is high.

7.3.2 Clear Register

A logical low on ($\overline{\text{SRCLR}}$) clears all registers in the device. TI suggests clearing the device during power up or initialization.

7.3.3 Output Control

Holding the output enable ($\overline{\text{G}}$) high holds all data in the output buffers low, and all drain outputs are off. Holding ($\overline{\text{G}}$) low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are OFF. When data is high, the DMOS transistor outputs have sink-current capability. This pin can also be used for global PWM dimming.

7.3.4 Cascaded Application

The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices. Connect the device (SER OUT) pin to the next device (SER IN) for daisy Chain.

7.3.5 Current Limit Function

Outputs are low-side, open-drain DMOS transistors with output ratings of 50V and a 350mA continuous sink current capability. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

8 Device Functional Modes

8.1 Operating with V_{cc} < 4.5V

This device works normally during 4.5V ≤ V_{cc} ≤ 5.5V, when operation voltage is lower than 4.5V, correct behavior of the device, including communication interface and current capability, is not assured.

8.2 Operating with 5.5V < V_{cc} ≤ 7V

The device works normally in this voltage range, but reliability issues can occur if the device works for a long time in this voltage range.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2005) to Revision C (March 2025)	**Page**
• Added Applications	1

Changes from Revision A (January 1995) to Revision B (May 2005)	**Page**
• Changed $\overline{\text{SRCLR}}$ timing diagram and changed title on Drain timing diagrams on Figure 6-1	8

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPIC6A595DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 125	TPIC6A595	
TPIC6A595DWG4	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 125	TPIC6A595	
TPIC6A595DWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6A595	Samples
TPIC6A595NE	ACTIVE	PDIP	NE	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TPIC6A595NE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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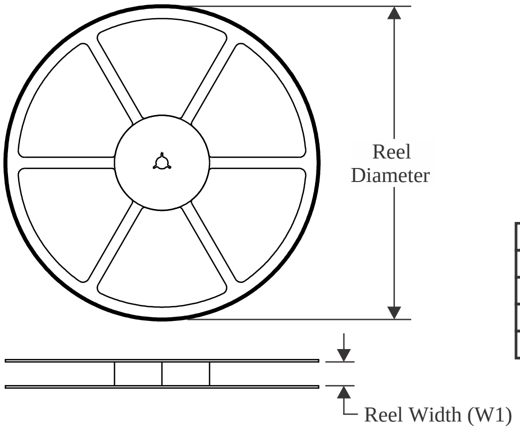
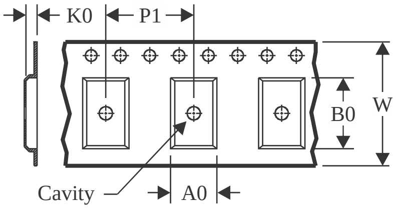
TAPE AND REEL INFORMATION

REEL DIMENSIONS

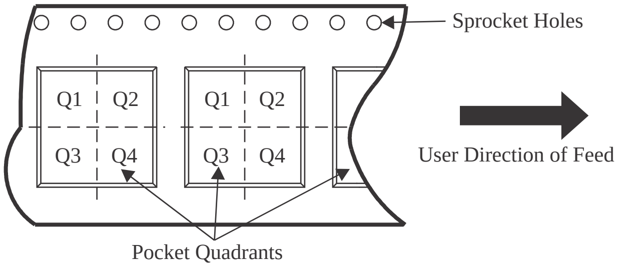


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

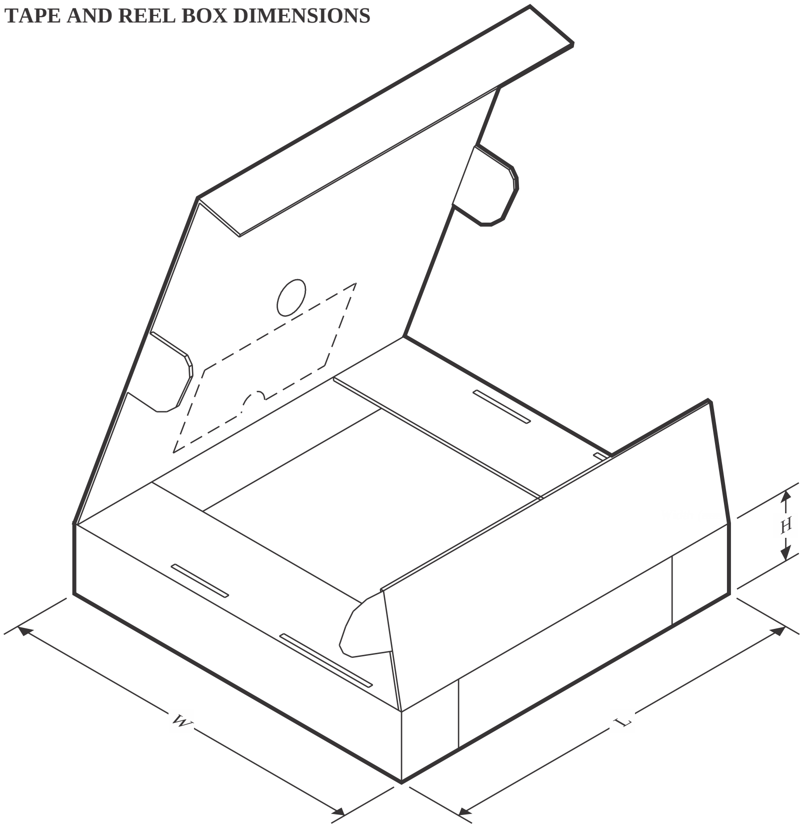
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC6A595DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
TPIC6A595DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

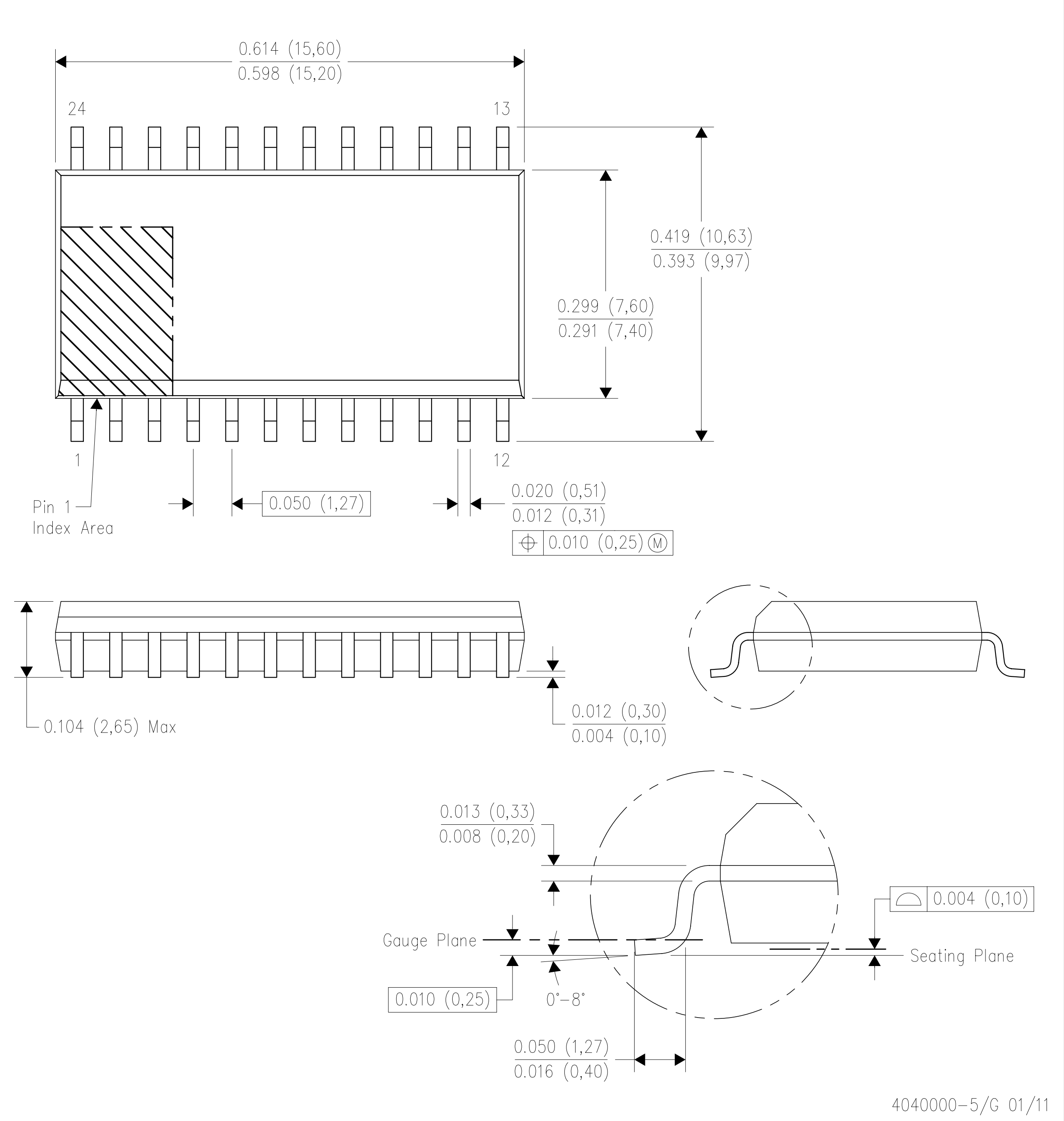
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC6A595DWR	SOIC	DW	24	2000	350.0	350.0	43.0
TPIC6A595DWR	SOIC	DW	24	2000	350.0	350.0	43.0

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–013 variation AD.

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