TPS38700S-Q1 Power-Supply Sequencer with I²C Support for Up to 6 Channels, 6 GPOs, and SYNC

1 Features

- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C
- Sequencing for state-of-the-art SoCs
  - Capable of sequencing up to 6 power rails
  - Power up/down timing sequence programmable via I2C
    - 125 us to 64 ms (in 125 us steps)
    - 500 us to 25 ms (in 500 us steps)
- System Robustness
  - Active-low open-drain NIRQ to latch system into safe state during operation error
  - Connect with a multichannel supervisor like the TPS389006-Q1 with Sync pin for full voltage monitoring & sequencing situations
  - Battery back-up function for diagnostic error reporting during power out events
  - Device thermal shutdown in high temperature environments

2 Applications

- Advanced driver assistance system (ADAS)
- Automotive camera modules
- FPGA power supply sequencing
- Microprocessor and microcontroller sequencing
- Multiple supply sequencing

3 Description

The TPS38700S-Q1 device is an integrated multichannel voltage sequencer with a window watchdog and I²C programmable available in a 24-pin 4 mm x 4 mm VQFN package.

This multichannel voltage sequencer is an excellent choice for systems that require precise power up and/or power down sequencing and can be interfaced with multichannel voltage supervisors. The device defaults to preprogrammed OTP options but the I²C can reprogram the power up and power down sequence, watchdog settings, and sequence timing options if needed.

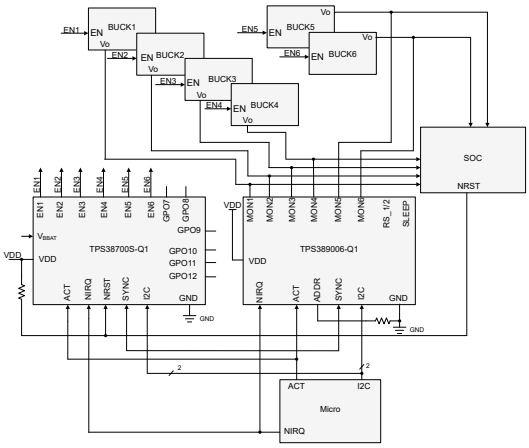
Flexible and programmable voltage rail sequencing capabilities, low quiescent current, and small footprint allow this device to meet most application requirements.

SYNC on the TPS38700S-Q1 allows designers to have more control over how their system powers up. The TPS38700S-Q1 acheives this by only firing the following enable signal when the current rail has powered up to an acceptable level with the use of the SYNC signal. In addition TPS38700S-Q1 allows for custom delay options. TPS38700S-Q1 is designed to be used with the TPS389006-Q1.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TPS38700S-Q1	VQFN (24)	4 mm x 4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Multichannel Voltage Sequencer and Monitor

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2023	*	Initial Release

5 Device Comparison

Figure 5-1 shows the device nomenclature of the TPS38700S-Q1 device. See Table 12-1 for more information regarding device ordering codes. Contact TI sales representatives or on TI's E2E forum for details and availability of other options; minimum order quantities apply.

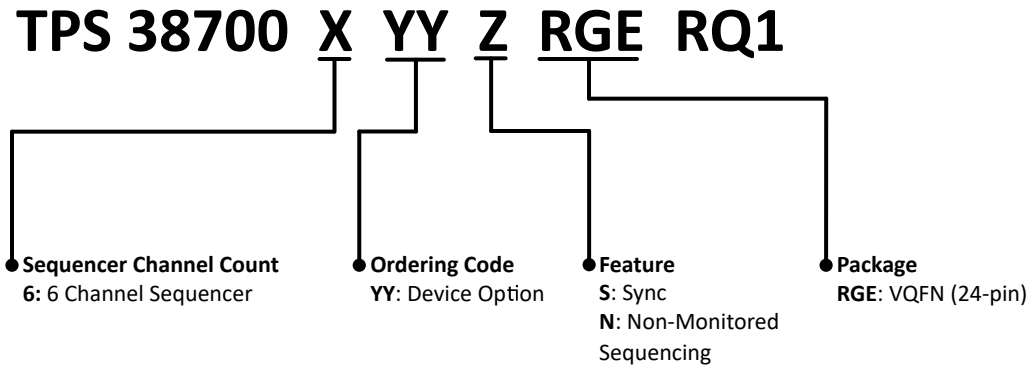

Figure 5-1. TPS38700S-Q1 Device Nomenclature

6 Pin Configuration and Functions

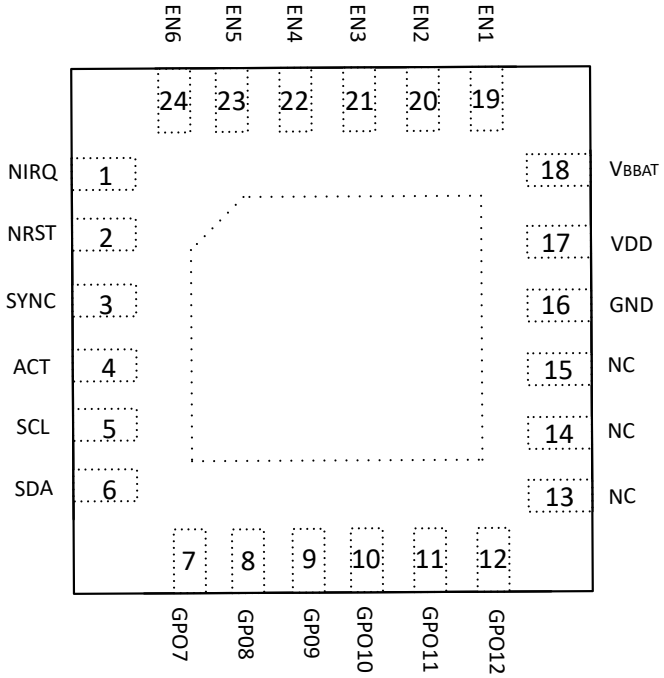

Figure 6-1. RGE Package
24-Pin VQFN
TPS38700 Top View

Table 6-1. Pin Functions

PIN		I / O	DESCRIPTION
NO.	TPS38700S-Q1 NAME		
1	NIRQ	O	Interrupt Pin (open-drain, active-low)
2	NRST	O	Reset Pin (open-drain, active-low)
3	SYNC	I	Active low input needed for enabling and disabling voltage rails during the Power Up and Power Down sequences. For more information check out Section 8.1 and Section 8.3.2.
4	ACT	I	ACT pin (logic high starts power up sequence, logic low starts power down sequence)
5	SCL	I	I2C clock pin
6	SDA	I / O	I2C data pin
7	GPO7	O	GPO7 (open-drain)
8	GPO8	O	GPO8 (open-drain)
9	GPO9	O	GPO9 (open-drain)
10	GPO10	O	GPO10 (open-drain)
11	GPO11	O	GPO11 (open-drain)
12	GPO12	O	GPO12 (open-drain)
13	NC	NA	Leave pin open circuit. Do not connect to anything.
14	NC	NA	Leave pin open circuit. Do not connect to anything.
15	NC	NA	Leave pin open circuit. Do not connect to anything.
16	GND	-	Ground
17	VDD	-	Power supply
18	V_{BBAT}	-	Backup battery supply. For more information on the backup state check out Section 8.3.4.
19	EN1	O	Enable 1 (open-drain)
20	EN2	O	Enable 2 (open-drain)
21	EN3	O	Enable 3 (open-drain)
22	EN4	O	Enable 4 (open-drain)
23	EN5	O	Enable 5 (open-drain)
24	EN6	O	Enable 6 (open-drain)

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VDD, V_{BBAT}	–0.3	6	V
Voltage	GPOx	-0.3	6	V
Voltage	SCL, SDA (OTP=3.3V)	-0.3	5.5	V
Temperature (2)	Continuous total power dissipation	See the Thermal Information		
	Operating junction temperature, T_J	-40	150	°C
	Operating free-air temperature, T_A	-40	125	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond values listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VDD	Supply pin voltage	2.2		5.5	V
V_{BBAT}	Battery back up	1.8		5.5	V
I_{NRST}, I_{NIRQ}, I_{ENx}	Pin Currents	0		±1	mA
GPOx	Pin voltage	0		5.5	V
SCL, SDA	Pin Voltage (OTP=3.3V)	0		4	V
R_{UP}	Pull-up resistor (Open Drain configuration)	10		100	kΩ
T_J	Junction temperature (free-air temperature)	-40		125	℃

7.4 Thermal Information

THERMAL METRIC(1)		TPS38700x-Q1 RGE (VQFN) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At 2.2 V ≤ VDD ≤ 5.5 V, NRST/NIRQ Voltage = 10 kΩ to VDD, NRST/NIRQ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C, typical conditions at VDD= 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common Parameters						
VDD	Input supply voltage		2.2		5.5	V
V_{BBAT}	Backup battery voltage range		1.85		5.5	V
UVLO_VDDR	UVLO VDD	Rising threshold			2.2	V
UVLO_VDDF	UVLO VDD	Falling threshold/switch over to V_{BBAT}	1.90		2	V
UVLO_V_{BBAT}	UVLO Battery backup	Falling threshold			1.85	V
POR	Power ON reset voltage, all outputs guaranteed to be stable above this value	Falling threshold			1.39	V
I_{DD}	Supply current into VDD pin ACT=High	VDD ≤ 5.5 V, power up sequence complete		45	75	µA
I_{DD}	Supply current into VDD pin ACT=Low	VDD ≤ 5.5 V ,power down sequence complete		35	60	µA
I_{BBAT}	Supply current from V_{BBAT}	V_{BBAT} ≤ 5.5 V		35	60	µA
I_{LKG_NRST}	Output leakage current (NRST)	VDD=V_{NRST} = 5.5 V			300	nA
I_{LKG_NIRQ}	Output leakage current (NIRQ)	VDD=V_{NIRQ} = 5.5 V			300	nA
ACT_L	Logic Low input				0.36	V
ACT_H	Logic high input		0.84		VDD - 0.2	V
SYNC_H	Input High	Io = 1mA	1.1			V
SYNC_L	Input Low	Io = 1mA			0.36	V
ACT	Internal Pull down			100		kΩ
NRST	Output Low	Open-Drain (10 kΩ pull up)			0.1	V
NIRQ	Output Low	Open-Drain (10 kΩ pull up)			0.1	V
ENx	Output Low	Open-Drain (10 kΩ pull up)			0.1	V
GPOx	Output Low	Open-Drain (10 kΩ pull up)			0.1	V
OSC	Internal oscillator tolerance		-5		5	%
$I_{lkg(BBAT)}$	Leakge current from V_{BBAT}	V_{BBAT} > 1.85V			300	nA
TSD	Thermal Shutdown			165		℃

7.5 Electrical Characteristics (continued)

At 2.2 V ≤ VDD ≤ 5.5 V, NRST/NIRQ Voltage = 10 kΩ to VDD, NRST/NIRQ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C, typical conditions at VDD= 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TSD Hysterisis	Thermal Shutdown Hysteresis			25		℃
I2C Electrical Specifications						
C_B	Capacitive load for SDA and SCL				400	pF
SDA, SCL	Low Threshold, OTP = 3.3 V				0.84	V
SDA, SCL	Low Threshold, OTP = 3.3 V		2.31			V
SDA	Output Low with 3 mA sink current				0.2	V

7.6 Timing Requirements

At 2.2 V ≤ VDD ≤ 5.5 V, NIRQ/NRST Voltage = 10 kΩ to VDD, NIRQ/NRST load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C, typical conditions at VDD = 3.3 V.

			MIN	NOM	MAX	UNIT
Common parameters						
t_{D_ENx}	ENx toggle delay from start of time slot	From start of time slot			10	µs
$t_{D\_ENx,y}$	Delay between 2 subsequent EN in same time slot				1	µs
t_{NRST_EN}	ENx delay from NRST in Emergency Shutdown	Sequence 2	200			ns
t_{D_NRST}	NRST assertion latency from falling edge of ACT pin below VIL or falling edge of VDD pin below VDD_{min}				25	µs
t_{D_NIRQ}	Fault detection to NIRQ assertion latency				25	µs
t_{No_BIST}	POR to ready without BIST	including OTP load with ECC			2.5	ms
I2C Timing Characteristics						
f_{SCL}	Serial clock frequency (1)	Standard mode			100	kHz
f_{SCL}	Serial clock frequency (1)	Fast mode			400	kHz
f_{SCL}	Serial clock frequency (1)	Fast mode +			1	MHz
t_{LOW}	SCL low time (1)	Standard mode	4.7			µs
t_{LOW}	SCL low time (1)	Fast mode	1.3			µs
t_{LOW}	SCL low time (1)	Fast mode +	0.5			µs
t_{HIGH}	SCL high time (1)	Standard mode	4			µs
t_{HIGH}	SCL high time (1)	Fast Mode	1			µs
t_{HIGH}	SCL high time (1)	Fast mode +	0.26			µs
t_{SU_DAT}	Data setup time (1)	Standard mode	250			ns
t_{SU_DAT}	Data setup time (1)	Fast mode	100			ns
t_{SU_DAT}	Data setup time (1)	Fast mode +	50			ns
t_{HD_DAT}	Data hold time (1)	Standard mode	10		3450	ns
t_{HD_DAT}	Data hold time (1)	Fast mode	10		900	ns
t_{HD_DAT}	Data hold time (1)	Fast mode +	10			ns
t_{SU_STA}	Setup time for a Start or Repeated Start condition (1)	Standard mode	4.7			µs
t_{SU_STA}	Setup time for a Start or Repeated Start condition (1)	Fast mode	0.6			µs
t_{SU_STA}	Setup time for a Start or Repeated Start condition (1)	Fast mode +	0.26			µs
t_{HD_STA}	Hold time for a Start or Repeated Start condition (1)	Standard mode	4			µs
t_{HD_STA}	Hold time for a Start or Repeated Start condition (1)	Fast mode	0.6			µs

7.6 Timing Requirements (continued)

At 2.2 V ≤ VDD ≤ 5.5 V, NIRQ/NRST Voltage = 10 kΩ to VDD, NIRQ/NRST load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C, typical conditions at VDD = 3.3 V.

			MIN	NOM	MAX	UNIT
t_{HD_STA}	Hold time for a Start or Repeated Start condition (1)	Fast mode +	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition (1)	Standard mode	4.7			µs
t_{BUF}	Bus free time between a STOP and START condition (1)	Fast mode	1.3			µs
t_{BUF}	Bus free time between a STOP and START condition (1)	Fast mode +	0.5			µs
t_{SU_STO}	Setup time for a Stop condition (1)	Standard mode	4			µs
t_{SU_STO}	Setup time for a Stop condition (1)	Fast mode	0.6			µs
t_{SU_STO}	Setup time for a Stop condition (1)	Fast mode +	0.26			µs
t_{rDA}	Rise time of SDA signal (1)	Standard mode			1000	
t_{rDA}	Rise time of SDA signal (1)	Fast mode	20		300	ns
t_{rDA}	Rise time of SDA signal (1)	Fast mode +			120	ns
t_{fDA}	Fall time of SDA signal (1)	Standard mode			300	ns
t_{fDA}	Fall time of SDA signal (1)	Fast mode	1.4		300	ns
t_{fDA}	Fall time of SDA signal (1)	Fast mode +	6.5		120	ns
t_{rCL}	Rise time of SCL signal (1)	Standard mode			1000	ns
t_{rCL}	Rise time of SCL signal (1)	Fast mode	20		300	ns
t_{rCL}	Rise time of SCL signal (1)	Fast mode +			120	ns
t_{fCL}	Fall time of SCL signal (1)	Standard mode			300	ns
t_{fCL}	Fall time of SCL signal (1)	Fast mode	6.5		300	ns
t_{fCL}	Fall time of SCL signal (1)	Fast mode +	6.5		120	ns
t_{SP}	Pulse width of SCL and SDA spikes that are suppressed (1)	Standard mode, Fast mode and Fast mode +			50	ns

(1) Guaranteed by design

7.7 Typical Characteristics

At T_A = 25°C, V_{DD} = 3.3 V, and R_{PU} = 10 kΩ, unless otherwise noted.

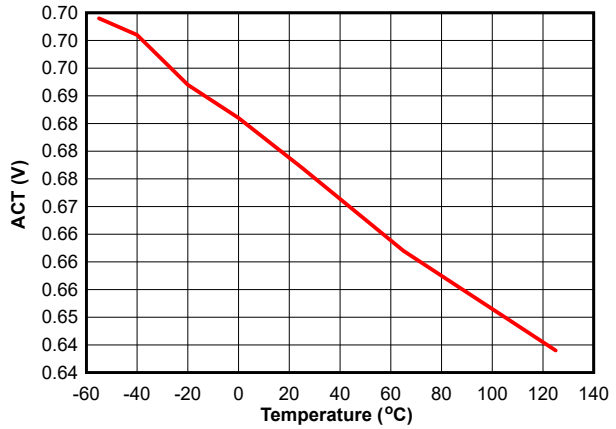

Figure 7-1. ACT Logic High Threshold Voltage vs. Temperature

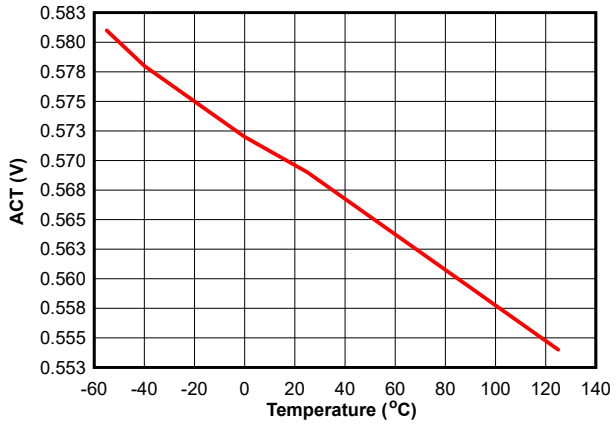

Figure 7-2. ACT Logic Low Threshold Voltage vs. Temperature

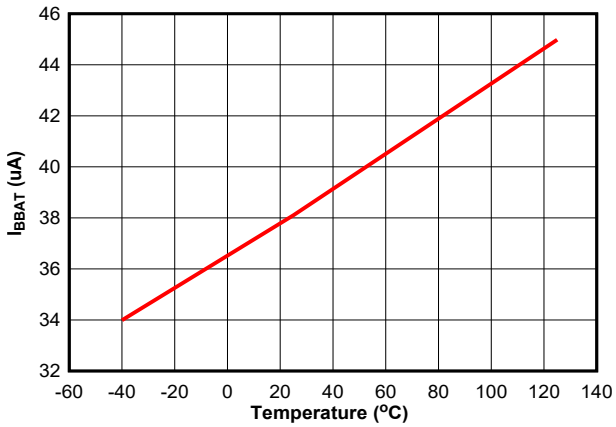

Figure 7-3. I_{BBAT} vs. Temperature

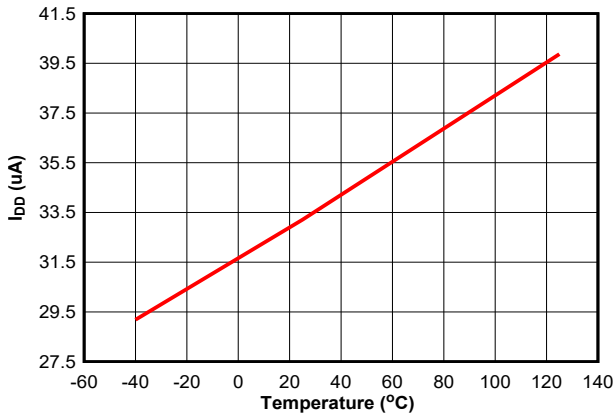

Figure 7-4. I_{DD} Shutdown Current vs. Temperature

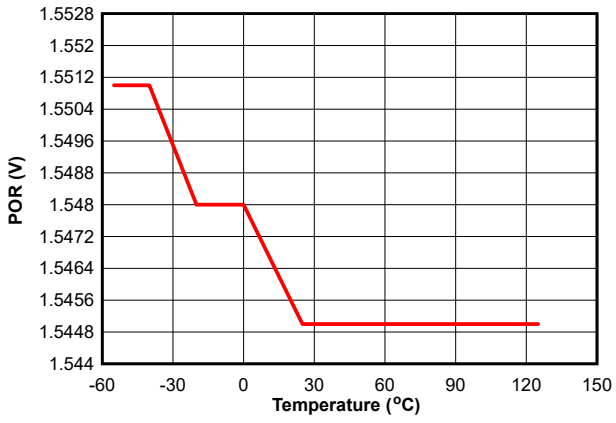

Figure 7-5. V_{POR} vs. Temperature

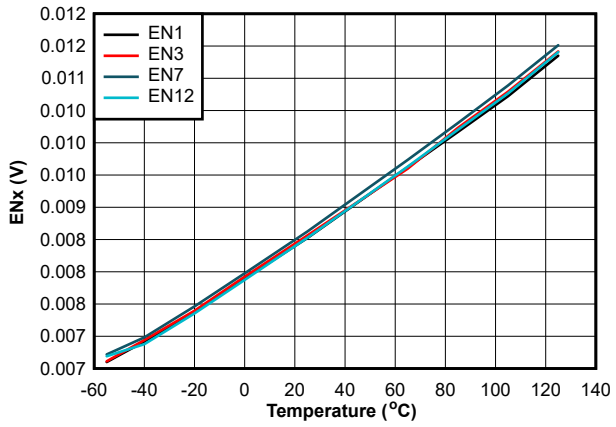

Figure 7-6. ENx Logic Low Output Voltage vs. Temperature

8 Detailed Description

8.1 Overview

When designing a complicated system with many power rails, you must not overlook how and when rails are turned on. Sequencing sub-systems can be implemented in various ways. Theoretically a system can chain PGOOD signals from Power IC's to the enable subsequent power rails. This is not recommended, however, as there's no easy way to disable the system once it's been turned on.

TPS38700S-Q1 operates similarly to a PGOOD based protocol, but is able to bypass the powering down dilemma by having a handshake based PGOOD protocol with SYNC for both sequencing up and down. TPS38700S-Q1 waits for the SYNC signal from the TPS389006-Q1 Device indicating the voltage met a UV PGOOD or OFF threshold before firing the next signal.

Another way a system can also implement sequencing is with a blind firing approach. The blind firing approach turns on subsequent rails after a small time delay regardless of whether or not the rails power on. This can be useful in systems where power rails don't have any critical voltage dependencies, but the order of how the rails are turned on and off is important. You can implement a Non-Monitored sequencing approach like this with the **N** OTP variant ofTPS38700S-Q1.

TPS38700S-Q1 is a versatile part that can be configured for multiple ways. The part can be ordered as a pure sequencer, pure GPO expander, or combination sequencer & GPOs. Sequencing outputs can be assigned to ACT pin. These sequencing outputs can be factory configured for default values and subsequently changed via I^2C on power-up before sending ACT pin high.

The TPS38700S-Q1 is capable of various I^2C logic levels. A full featured Graphical User Interface (GUI) is available for download in the product folder. Contact a Texas Instruments representative for custom configured part queries.

The TPS38700S-Q1 is AEC-Q100 qualified for automotive applications and has been characterized from -40ºC to +125ºC.

8.2 Functional Block Diagram

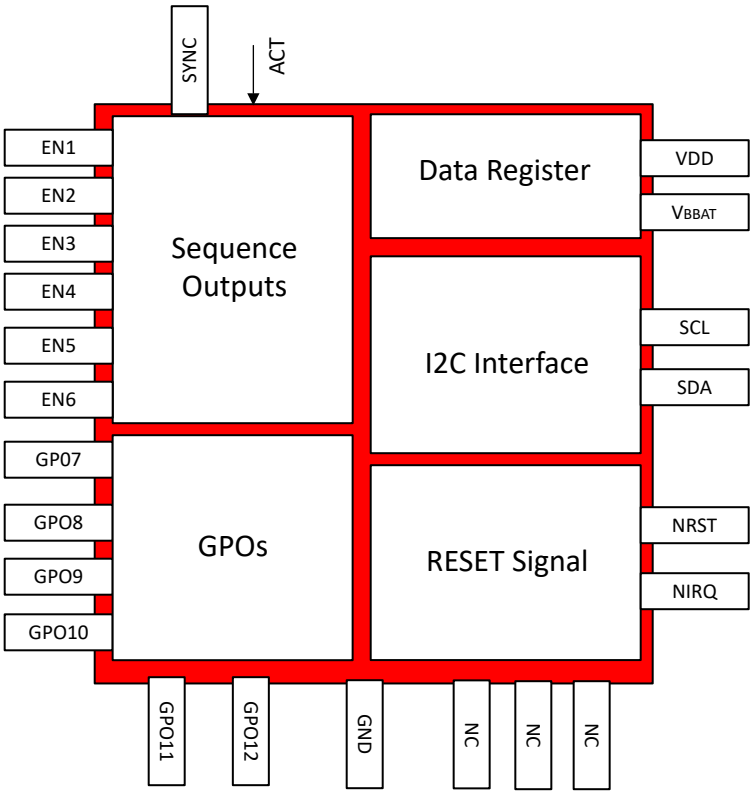

Figure 8-1. TPS38700S-Q1 Block Diagram

8.3 Feature Description

8.3.1 Device State Diagram

The TPS38700S-Q1 state diagrams shown in Figure 8-2 show the flow of operation.

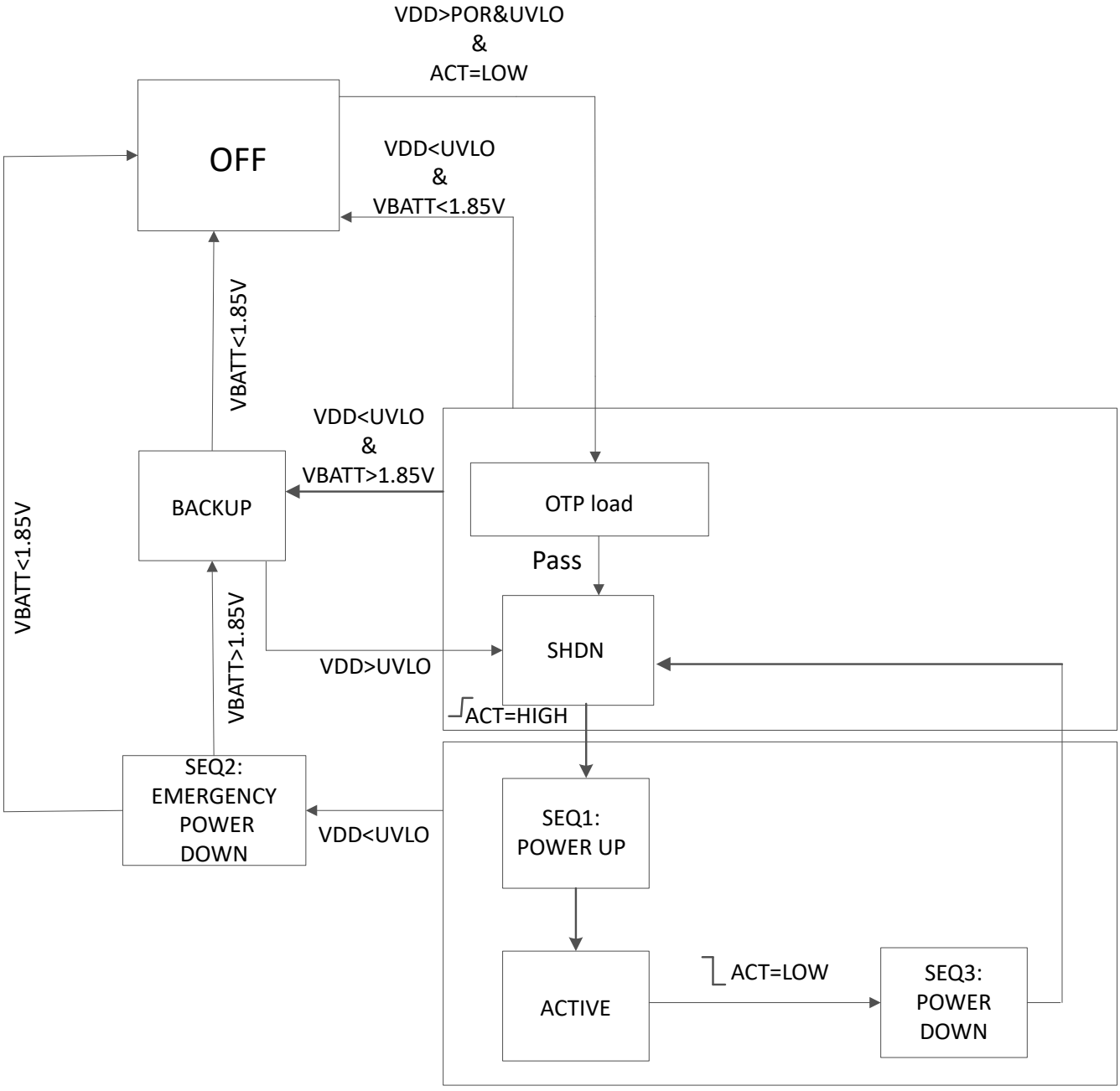

Figure 8-2. TPS38700S-Q1 State Diagram

8.3.2 Sync Functionality

A typical implementation of the sync functionality of the TPS38700S-Q1 is shown in Figure 8-3. TPS38700S-Q1 and TPS389006-Q1 can be used together by tying SYNC pins together in order to ensure that sequential voltage rails are dependent on earlier voltage rails successfully powering up or powering down.

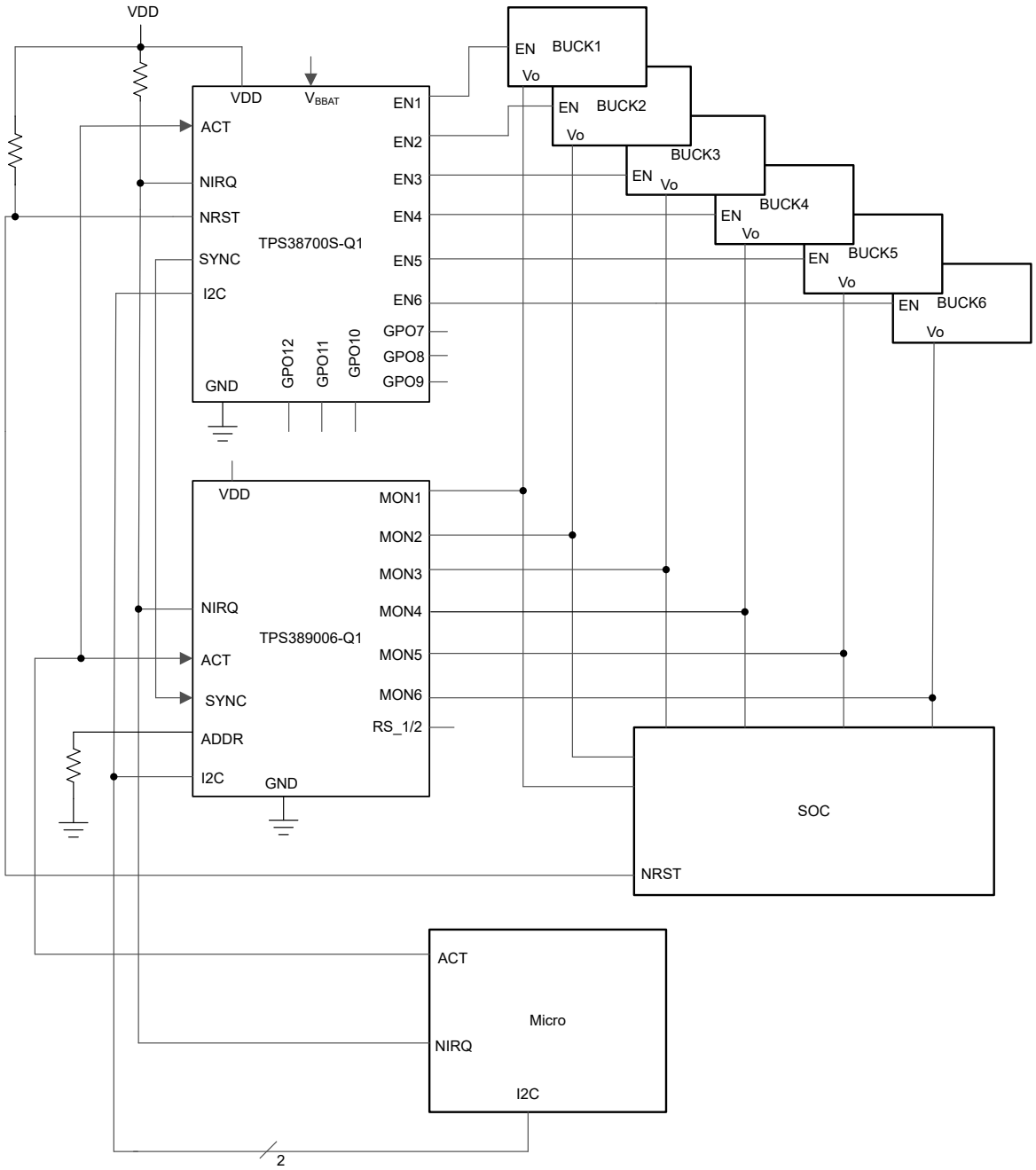

Figure 8-3. TPS38700S Voltage Sequencer Design Block Diagram

SYNC is an active low input on the TPS38700S-Q1 which causes EN pins to toggle on when sequencing up or off when sequencing down. TPS389006-Q1 will send an active low signal when the desired voltage threshold is monitored. For more information on how sequence logging works and how TPS389006-Q1 tags power rails with SYNC check out the TPS389006-Q1 data sheet.

8.3.3 Transitioning Sequences

The sequences of the device are described in Section 8.3.3.1 through Section 8.3.3.3 with timing diagrams showing the main signals involved in each sequence.

8.3.3.1 Power Up

When ACT is driven high, the first EN signal is turned on by TPS38700S-Q1. Then, the MON voltage rises and triggers TPS389006-Q1 to send the first SYNC signal which causes TPS38700S-Q1 to turn on the second EN voltage. This process repeats until all Enable voltages turn on. After the final EN signal is turned on, NRST deactivates after the RST_DLY time. A successful power up sequence is shown in Figure 8-4 using the circuit shown in Figure 9-1. Note that the TPS389006-Q1 defaults to using UV thresholds for sending the SYNC pulse when sequencing up.

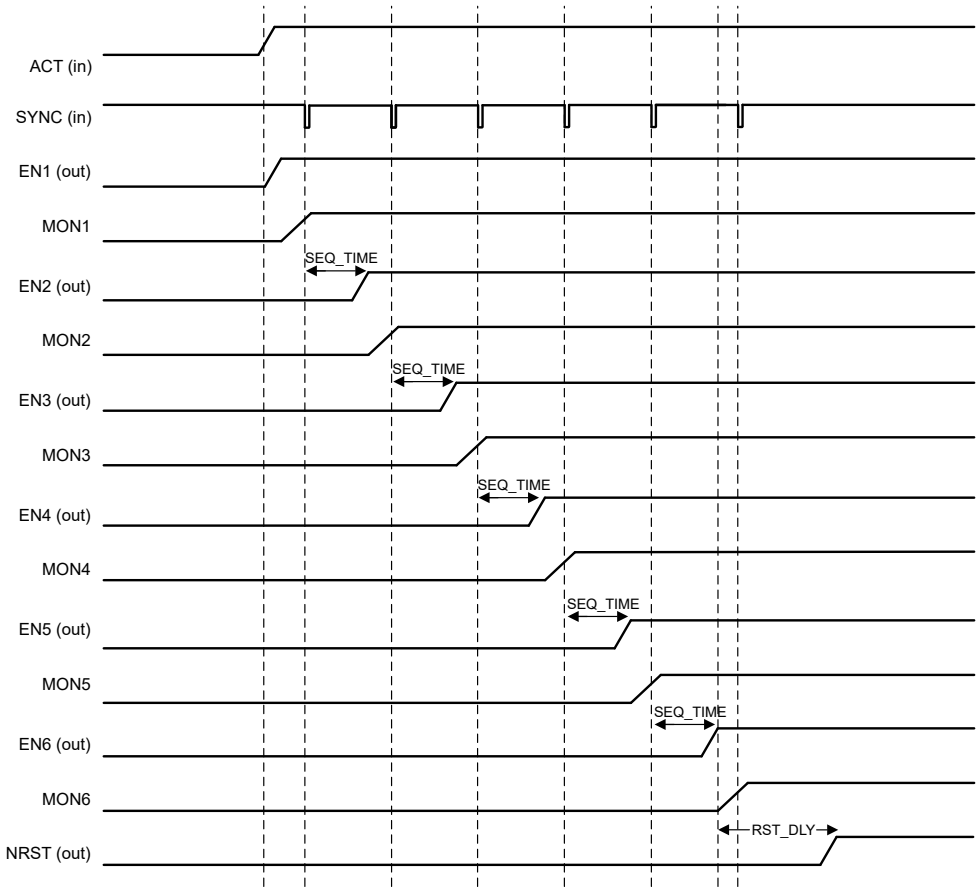

Figure 8-4. TPS38700S Power Up with SYNC

8.3.3.2 Power Down

A similar sequence of events happens when ACT is driven low. Immediately the first EN signal in the down sequence is driven low. This triggers TPS389006-Q1 by having the MON voltage drop below a threshold and send a SYNC signal. The SYNC signal causes TPS38700S-Q1 to turn off the second EN signal. This process also repeats until all voltages have been turned off. By default SYNC voltage thresholds for TPS389006-Q1 are based on the OFF voltage. The voltage thresholds can be changed to UV voltage thresholds for both sequencing up and down. A successful power down sequence is shown in Figure 8-5 using the circuit shown in Figure 9-1. Note that the TPS389006-Q1 defaults to using OFF voltage threshold (MONx<140mV) for sending the SYNC pulse when sequencing down.

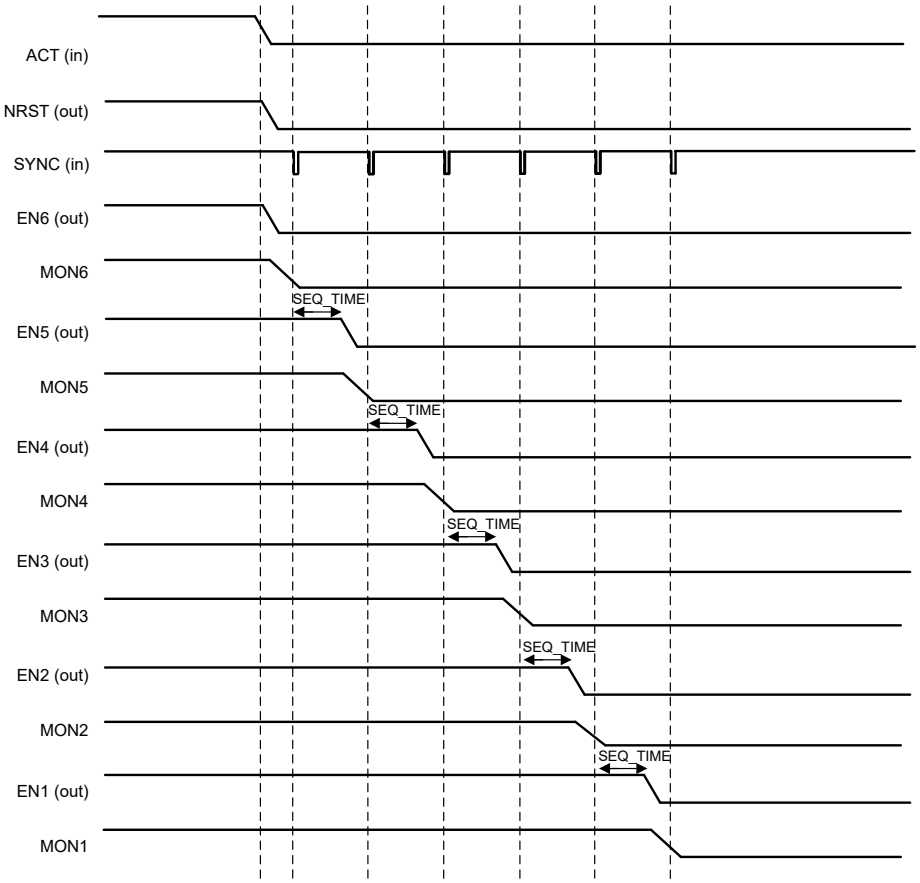

Figure 8-5. TPS38700S Power Down with SYNC

Note that TPS38700S-Q1 must finish sequencing (either up or down) before starting a new sequence.

8.3.3.3 Emergency Power Down

In case of emergency power down (VDD drops below UVLO), a best effort approach is taken to assert NRST before pulling ENx and NIRQ down.

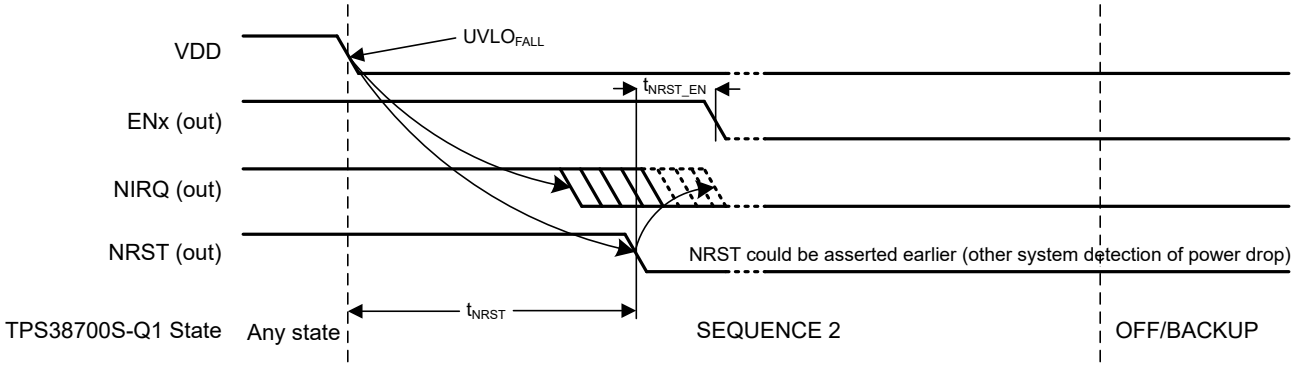

Figure 8-6. Emergency Power Down

8.3.4 BACKUP State

In the BACKUP state only the battery is supplying power to the device, however the device must have gone through a VDD supplied state (and loaded configuration data) in order to enter this state. If no VDD supplied state has occurred, then the TPS38700S-Q1 stays in the "OFF or Battery Installed" state, from which it will exit only with a valid VDD supply. I^{2}C commincation with TPS38700S-Q1 is possible when in this state.

When in BACKUP state, the TPS38700S-Q1 pins are in the following state:

- ENx = Low (de-asserted)
- NRST = Low (asserted)
- ACT input is ignored.

Upon exiting from the BACKUP state, the last configuration is active and the device enters the SHDN state.

8.3.5 Thermal Shutdown (TSD) State

In the TSD state TPS38700S-Q1 reduces functionality to only support I²C commincation. Upon exiting from the TSD state, the last configuration is active and the device enters the SHDN state.

When in BACKUP state, the TPS38700S-Q1 pins are in the following state:

- ENx = Low (de-asserted)
- NRST = Low (asserted)
- ACT input is ignored.

Note that the F_TSD bit in Table 8-4 will be set high. The F_TSD bit will stay high even if TPS38700S-Q1 leaves the TSD state, but can be manually cleared.

8.3.6 I²C

TPS38700S-Q1 follows the I²C protocol (up to 1MHz) to manage communication with host devices such as a MCU or System on Chip (SoC). I²C is a two wire communication protocol implmented using two signals, clock (SCL) and data (SDA). The host device is the primary controller of communication. TPS38700S-Q1 responds over the data line during read or write operations as defined by I²C protocol. Both SCL and SDA signals are open drain topology and can be used in a wired-OR configuration with other devices to share the communication bus. Both SCL and SDA pins need an external pull up resistor to supply voltage (10 kΩ recommended).

Figure 8-7 shows the timing relationship between SCL and SDA lines to transfer 1 byte of data. SCL line is always controlled by host. To transfer 1 byte data, host needs to send 9 clocks on SCL. 8 clocks for data and 1 clock for ACK or NACK. SDA line is controlled by either the host or TPS38700S-Q1 based on the read or write operation. Figure 8-8 and Figure 8-9 highlight the communication protocol flow and which device controls SDA line at various instances during active communication.

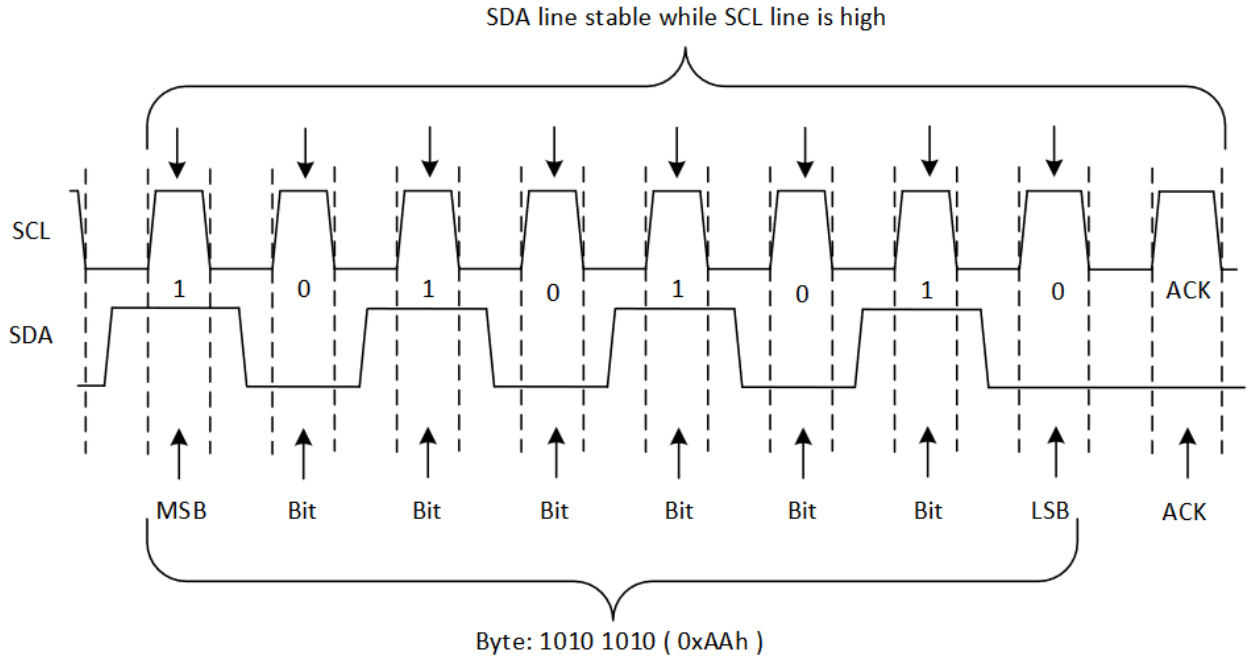

Figure 8-7. SCL to SDA Timing for 1 Byte Data Transfer

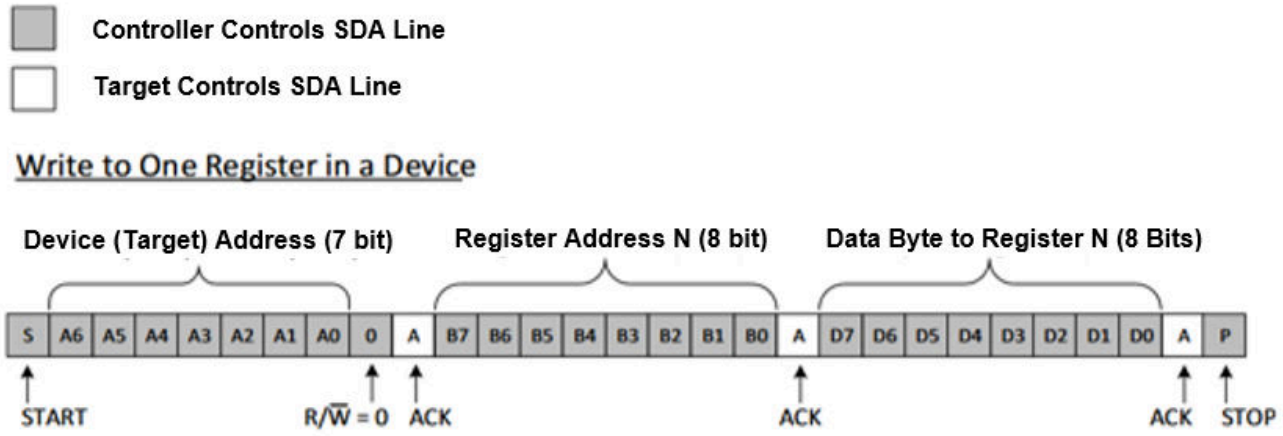

Figure 8-8. I²C Write Protocol

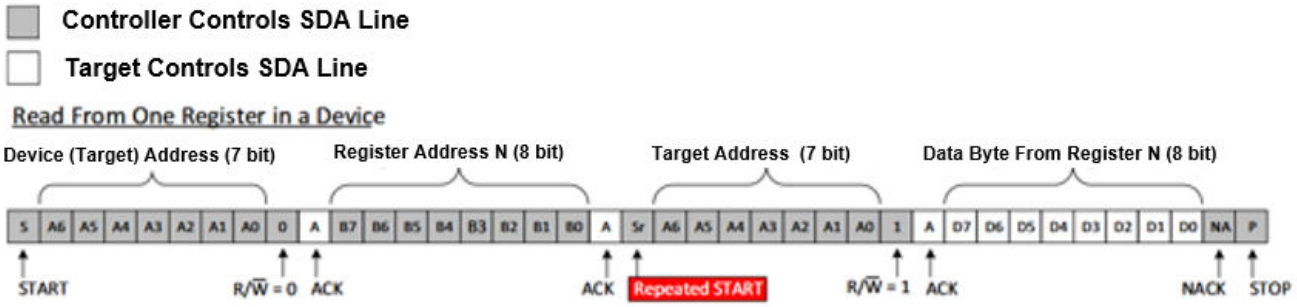

Figure 8-9. I²C Read Protocol

Before initiating communication over I²C protocol, host needs to confirm the I²C bus is available for communication. Monitor the SCL and SDA lines, if any line is pulled low, the I²C bus is occupied. Host needs to wait until the bus is available for communication. Once the bus is available for communication, the host can initiate read or write operation by issuing a START condition. Once the I²C communication is complete, release the bus by issuing STOP command. Figure 8-10 shows how to implement START and STOP condition.

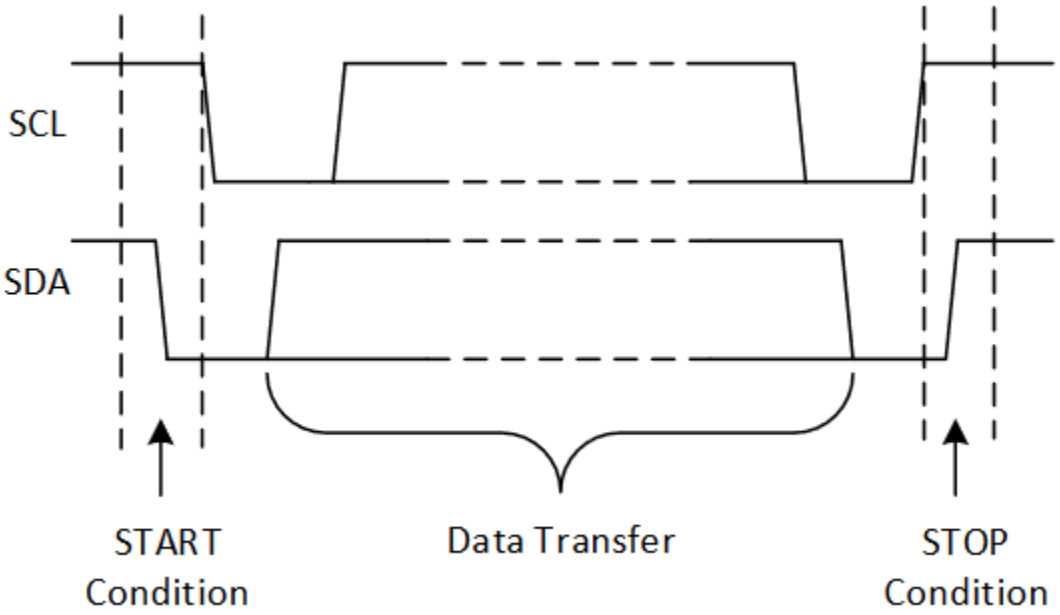

Figure 8-10. I²C START and STOP Condition

8.3.6.1 I²C

Refer to Table 8-1 for the I²C register map overview. Note that "PSEQ" refers to TPS38700S-Q1 and is used enhance table readability.

Table 8-1. I²C Register Categories and Associated Details

TYPE	BITS	DESCRIPTION	RANGE / FUNCTION OR STATUS	WHO TOGGLES THEM?	WHO ELSE CAN WRITE TO THEM?	WHAT GETS AFFECTED DUE TO THIS BIT?
OTP bits R	VENDORID[7:0]	TI defined	TI defined	OTP option	None	None
	MODEL_REV[7:0]	TI defined	TI defined	OTP option	None	None
	TARGET_ID[7:0]	TI defined	TI defined	OTP option	None	I²C
Interrupt info bits RW1C	F_INTERR	Internal fault	No internal fault / Internal fault detected	Interrupt	Any of the interrupts generated; Can be cleared by writing 1	NIRQ
	EM_PD (1)	Emergency Power down	No emergency PD / shutdown caused by emergency PD	PSEQ	PSEQ; SOC	NRST; NIRQ
	F_EN	Enable output pin fault	No faults detected / fault detected	EN readback-PSEQ	PSEQ; SOC	NIRQ; NRST
	F_NRSTIRQ	Reset or Interrupt pin fault	No faults detected / fault detected	Reset readback-PSEQ	PSEQ; SOC	NIRQ
	F_LDO	LDO fault	No faults detected / fault detected	BIST	BIST; SOC	NIRQ; NRST
	F_TSD	Thermal shutdown fault	No faults detected / fault detected	TSD	TSD; SOC	NIRQ; NRST
	F_RT_CRC	Runtime CRC register fault	No faults detected / fault detected	CRC	SOC	NIRQ
Status bits R	ST_NIRQ	Current state of NIRQ output	NIRQ asserted / not asserted	Interrupt	None	None
	ST_NRST	Current state of NRST output	NRST asserted / not asserted	Interrupt; NRSTstate change	None	None
	ST_ACTSHDN	Current state of ACT input	ACT pin driven Low or High	PSEQ	None	None
	ST_PSEQ[1:0]	Current state of PSEQ	SHDNx, Power Up, Power Down, invalid, Active	PSEQ	None	None
	STDR1	Current drive state of GPO12 to GPO9	Sequencer is driving EN Low or High	PSEQ	None	None
	STDR2	Current drive state of GPO7,8 to EN1	Sequencer is driving EN Low or High	PSEQ	None	None
CONTROL R/W	FORCE_INT	Force NIRQ low	NIRQ contolled by faults / register	SOC	SOC	NRST
	FORCE_ACT	Force PSEQ Active state		PSEQ	SOC can clear it; but not set it	PSEQ
	RST_DLY[3:0]	Reset Delay	0.1 ms to 128 ms	SOC	None	PSEQ

Table 8-1. I²C Register Categories and Associated Details (continued)

TYPE	BITS	DESCRIPTION	RANGE / FUNCTION OR STATUS	WHO TOGGLES THEM?	WHO ELSE CAN WRITE TO THEM?	WHAT GETS AFFECTED DUE TO THIS BIT?
PSEQ	USLOT[3:0]	Power Up time slots	125 µs / 2.5 s	SOC	None	PSEQ
	DSLOT[3:0]	Power Down time slots	125 µs / 2.5 s	SOC	None	PSEQ
	SSTEP	Slot step multiplier	250 µs / 1000 µs	SOC	None	PSEQ
	PU[3:0][12:1]	Power Up Sequence	ENx not mapped / ENx mapped	SOC	None	PSEQ
	PD[3:0][12:1]	Power Down Sequence	ENx not mapped / ENx mapped	SOC	None	PSEQ
PROT	WRK	Work set register lock	0 / 1	SOC only 1	None	Write function to those register groups
	SEQS	SEQS set register lock	0 / 1	SOC only 1	None	Write function to those register groups
	SEQP	SEQP set register lock	0 / 1	SOC only 1	None	Write function to those register groups
	SEQC	SEQC set register lock	0 / 1	SOC only 1	None	Write function to those register groups
	CTL	CTL set register lock	0 / 1	SOC only 1	None	Write function to those reg groups

(1) Presence of fault reporting functionality dependent on part configuration.

8.4 Register Map Table

Table 8-2. Register Map Table

RSVD = Reserved

ADDR	NAME	R/W	MSB	6	5	4	3	2	1	LSB	DEFAULT	GROUP
0x00 - 0x0F: Vendor info and vendor usage registers												
0x00	Model Rev	R	Device Model (Bits 3-7)					Vendor ID (Bits 0-2)				
0x01	Revision	R	Silicon_Rev		OTP_Rev							
0x02 … 0x0F	RSVD		Vendor defined or other IC information									
0x10 - 0x1F: Interrupts and Status registers												
0x10	INT_SRC1	RW1C	F_INTERNAL	EM_PD	RSVD	RSVD	RSVD	F_EN	RSVD	F_NRSTIRQ	0x00	
0x11	INT_SRC2	RW1C	F_VENDOR	RSVD	F_RT_CRC	RSVD	F_LDO	F_TSD	RSVD	RSVD	0x00	
0x12	INT_VENDOR	RW1C	Vendor specific internal fault flags								0x00	
0x13	CTL_STAT	R	RSVD	ST_VBBAT	ST_NIRQ	ST_NRST	RSVD	ST_ACTSHDN	ST_PSEQ[1:0]		0x00	
0x14	EN_STDR1	R	RSVD				STDR_GPO12	STDR_GPO11	STDR_GPO10	STDR_GPO9	0x00	
0x15	EN_STDR2	R	STDR_GPO8	STDR_GPO7	STDR_EN6	STDR_EN5	STDR_EN4	STDR_EN3	STDR_EN2	STDR_EN1	0x00	
0x16	EN_STRD1	R	RSVD				STRD_GPO12	STRD_GPO11	STRD_GPO10	STRD_GPO9	0x00	
0x17	Table 8-10	R	STRD_GPO8	STRD_GPO7	STRD_EN6	STRD_EN5	STRD_EN4	STRD_EN3	STRD_EN2	STRD_EN1	0x00	
0x18 … 0x19	RSVD		RSVD									
0x1A	Table 8-11	R	RSVD	RSVD	RSVD	RSVD	ACTSHDN	RSVD	RSVD	RSVD	0x00	
0x1B … 0x1F	RSVD		RSVD									
0x20 - 0x2F: Configuration Registers												
0x20 … 0x26	RSVD	R	RSVD								NVM	
0x27	RSVD	R/W	RSVD								NVM	CTL
0x28	CTL_1	R/W	RSVD				FORCE_INT	FORCE_ACT	RSVD	RSVD	NVM	WRK
0x29	Table 8-14	R/W	RST_DLY[3:0]				RSVD		RSVD	RSVD	NVM	CTL
0x2B	IEN_VENDOR	R/W	Vendor specifc internal fault enables								NVM	CTL
0x2C … 0x2F	RSVD		RSVD									
0x30 - 0x38: Sequencing Registers												

Table 8-2. Register Map Table (continued)

RSVD = Reserved

ADDR	NAME	R/W	MSB	6	5	4	3	2	1	LSB	DEFAULT	GROUP
0x30	SEQ_CFG	R/W	RSVD							SSTEP	NVM	SEQC
0x31	SEQ_USLOT	R/W	TIME[7:0]								NVM	SEQC
0x32	SEQ_DSLOT	R/W	TIME[7:0]								NVM	SEQC
0x33	PWR_EN1	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x34	PWR_EN2	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x35	PWR_EN3	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x36	PWR_EN4	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x37	PWR_EN5	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0x38	PWR_EN6	R/W	PU[3:0]				PD[3:0]				NVM	SEQP
0xF0 - 0xFF: Protection registers												
0xF0	PROT1	R/W	RSVD	WRK	SEQS	SEQP	SEQC	WDT	RSVD	CTL	0x00	
0xF1	PROT2	R/W	RSVD	WRK	SEQS	SEQP	SEQC	WDT	RSVD	CTL	0x00	
0xF2 … 0xF8	RSVD		RSVD									
0xF9	I2CADDR	R	RSVD	ADDR_I2C_NVM[6:0]							NVM	
0xFA … 0xFF	RSVD		RSVD									

8.4.1 Register Descriptions

Table 8-3. INT_SRC1

Address: 0x10

Description: Interrupt Source register. If F_INTERNAL, then INT_SRC2 register provides further information.

POR Value: 0x00

Access: Read and write 1 to clear. Writing 0 has no effect; writing 1 to a bit which is already at 0 has no effect.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7	F_INTERNAL	Internal Fault (ORed value of all bits in INT_SRC2): 0 = No internal fault detected 1 = Internal fault detected. Further detail flagged in INT_SRC2. This bit is cleared by clearing the bits in INT_SRC2.
6	EM_PD	Emergency Power Down: 0 = No emergency power-down event 1 = Shutdown caused by emergency power-down (Sequence 2). Write-1-to-clear will clear the bit. The bit will be set again on next emergency power-down.
3	RSVD	RSVD
2	F_EN	Enable Output Pin Fault: 0 = No short to supply or ground detected. 1 = Short to supply or ground detected. Write-1-to-clear will clear the bit only if the fault condition is also removed.
1	RSVD	RSVD
0	F_NRSTIRQ	Reset or Interrupt Pin Fault: 0 = No fault detected on NRST or NIRQ. 1 = Low resistance path to supply detected on either NRST or NIRQ. Write-1-to-clear will clear the bit only if the fault condition is also removed.

INT_SRC1 represents the reason that NIRQ was asserted. When the host processor receives NIRQ, it may read this register to quickly determine the source of the interrupt. If this register is clear, then TPS38700S-Q1 did not assert NIRQ.

Table 8-4. INT_SRC2

Address: 0x11

Description: Interrupt Source register for internal errors.

POR Value: 0x00

Access: Read and write 1 to clear. Writing 0 has no effect; writing 1 to a bit which is already at 0 has no effect.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7	F_VENDOR	Vendor specific internal fault. Details reported in INT_VENDOR. This bit represents the ORed value of all bits in INT_VENDOR. 0 = No fault reported in INT_VENDOR 1 = Fault reported in INT_VENDOR This bit is cleared by clearing the bits in INT_VENDOR.
6	RSVD	Reserved

Table 8-4. INT_SRC2 (continued)

Address: 0x11

Description: Interrupt Source register for internal errors.

POR Value: 0x00

Access: Read and write 1 to clear. Writing 0 has no effect; writing 1 to a bit which is already at 0 has no effect.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
5	F_RT_CRC	Runtime register CRC Fault: 0 = No fault detected. 1 = Register CRC fault detected. Write-1-to-clear will clear the bit. The bit will be set again during next register CRC check if a fault is detected.
3	F_LDO	LDO Fault: 0 = No LDO fault detected. 1 = LDO fault detected. If internal LDO is used, this flag is to indicate fault. If internal LDO is not used, this flag must be reserved. Write-1-to-clear will clear the bit only if the fault condition is also removed.
2	F_TSD	Thermal Shutdown: 0 = No thermal shutdown. 1 = Thermal shutdown occurred since last read. Write-1-to-clear will clear the bit only if the fault condition is also removed.

Table 8-5. INT_VENDOR

Address: 0x12

Description: Vendor Specific Internal Interrupt Status register.

POR Value: 0x00

Access: Read and write 1 to clear. Writing 0 has no effect; writing 1 to a bit which is already at 0 has no effect.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:0	FAULTS[7:0]	Vendor specific internal faults flags.

Table 8-6. CTL_STAT

Address: 0x13

Description: TPS38700S-Q1 Status register for control pins and internal state.

POR Value: 0x00

Access: Read only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:6	RSVD	Reserved
5	ST_NIRQ	Current state of NIRQ Output: 0 = NIRQ pin asserted low by TPS38700S-Q1. 1 = NIRQ pin not asserted low by TPS38700S-Q1.

Table 8-6. CTL_STAT (continued)

Address: 0x13

Description: TPS38700S-Q1 Status register for control pins and internal state.

POR Value: 0x00

Access: Read only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
4	ST_NRST	Current state of NRST Output: 0 = NRST pin asserted low by TPS38700S-Q1. 1 = NRST pin not asserted low by TPS38700S-Q1.
3	RSVD	RSVD
2	ST_ACTSHDN	Current state of ACT input: 0 = ACT pin driven low (Shutdown) by system. 1 = ACT pin driven high (Active) by system.
1:0	ST_PSEQ[1:0]	00b: SHDNx, Power Up, Power Down 01b: NA 10b: Invalid combination 11b: ACTIVE

Table 8-7. EN_STDR1

Address: 0x14

Description: Current drive status of Enable Pins.

POR Value: 0x00

Access: Read only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	RSVD	Reserved
3:0	STDR_GPO[12:9]	Current drive state of GPO[X]: 0 = TPS38700S-Q1 is driving GPO[X] Low. 1 = TPS38700S-Q1 is driving or allowing to float GPO[X] High.

Table 8-8. EN_STDR2

Address: 0x15

Description: Current drive status of Enable Pins.

POR Value: 0x00

Access: Read only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:0	STDR_EN[6:1] GPO[8:7]	Current drive state of GPO[X]: 0 = TPS38700S-Q1 is driving GPO[X] Low. 1 = TPS38700S-Q1 is driving or allowing to float GPO[X] High.

Table 8-9. EN_STRD1

Address: 0x16

Description: Current read status of Enable Pins.

POR Value: 0x00

Access: Read only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	RSVD	Reserved
3:0	STRD_GPO[12:9]	Current read state of GPO[X]: 0 = TPS38700S-Q1 is reading GPO[X] Low. 1 = TPS38700S-Q1 is reading GPO[X] High.

Table 8-10. EN_STRD2

Address: 0x17

Description: Current read status of Enable Pins.

POR Value: 0x00

Access: Read only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:0	STRD_EN[6:1] GPO[8:7]	Current read state of GPO[X]: 0 = TPS38700S-Q1 is reading GPO[X] Low. 1 = TPS38700S-Q1 is reading GPO[X] High.

Table 8-11. LAST_RST

Address: 0x1A

Description: Reason of last NRST assertion or shutdown. NRST assertion and shutdown occur in Sequence 2 and Sequence 3.

The register is maintained as long as VDD and/or VBBAT is present. An emergency shutdown triggering Sequence 2 is already recorded in INT_SRC1.EM_PD register bit, so it does not need to be stored in this register. The host is expected to read this register as part of the first actions taken upon power ON.

The register is overwritten with new relevant data on next NRST assertion or shutdown.

POR Value: 0x00

Access: Read Only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7	RSVD	Reserved
5	RSVD	Reserved
3	ACTSHDN	NRST/Shutdown due to ACT asserted Low (shutdown). 0 = Last NRST/Shutdown assertion was not due to ACT Low. 1 = Last NRST/Shutdown assertion was due to ACT Low.
1	RSVD	Reserved
0	RSVD	Reserved

Table 8-12. GP_OUT

Address: 0x25

Description: Set General Purpose Output state for sequencing pins EN[12:9]. GPO is enabled through AF_IN_OUT and EN_ALT_F registers.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if CTL group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	RSVD	Reserved
3	GPO12	GPO12 General Purpose Output. Only used when PWR_EN12 is cleared. 0 = GPO12 pin driven low. 1 = GPO12 pin driven high.
2	GPO11	GPO11 General Purpose Output. Only used when PWR_EN11 is cleared. 0 = GPO11 pin driven low. 1 = GPO11 pin driven high.
1	GPO10	EN10 General Purpose Output. Only used when PWR_EN10 is cleared. 0 = EN10 pin driven low. 1 = EN10 pin driven high.
0	GPO9	GPO9 General Purpose Output. Only used when PWR_EN9 is cleared. 0 = GPO9 pin driven low. 1 = GPO9 pin driven high.

Table 8-13. CTL_1

Address: 0x28

Description: Interrupt and State SW control.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if CTL group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	RSVD	Reserved
3	FORCE_INT (1)	Force NIRQ low: 0 = NIRQ pin controlled by INT_SRCx register faults. 1 = NIRQ pin forced low.

(1) FORCE_INT is used by software for periodic check for internal or external short to VDD on NIRQ pin.

Table 8-14. CTL_2

Address: 0x29

Description: Miscellaneous configuration.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if CTL group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION	
7:4	RST_DLY[3:0]	Power up sequence: NRST remains asserted until RST_DLY[3:0] after last ENx assert.	
		0000b = 0.1 ms 0001b = 0.2 ms 0010b = 0.4 ms 0011b = 0.8 ms 0100b = 1.6 ms 0101b = 3.2 ms 0110b = 6.4 ms 0111b = 12.8 ms	1000b = 1 ms 1001b = 2 ms 1010b = 4 ms 1011b = 8 ms 1100b = 16 ms 1101b = 32 ms 1110b = 64 ms 1111b = 128 ms
		Power down sequence: NRST asserted within t_{NRST} of ACT= Low.	
3:2	RSVD	RSVD	

Table 8-15. IEN_VENDOR

Address: 0x2B

Description: Vendor Specific Internal Interrupt Enable register.

POR Value: 0x00 or load from NVM.

Access: Read/Write. Read-only if CTL group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:0	FAULTS[7:0]	Vendor specific internal faults enables.

Table 8-16. SEQ_CFG

Address: 0x30

Description: Sequencing configuration.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if SEQ group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:1	RSVD	Reserved
0	SSTEP	Sequencing time slot step size selection for SEQ_USLOT and SEQ_DSLOT: 0 = Time slot step size t_{SSTEP} = 250 µs 1 = Time slot step size t_{SSTEP}= 1000 µs

Table 8-17. SEQ_USLOT

Address: 0x31

Description: Power Up sequencing time slot configuration.

POR Value: Loaded from NVM.

Access: Read/Write. Read only if SEQ group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:0	TIME[7:0]	Sets time slot between sequencing points on power-up: t_{USLOT} = SEQ_USLOT.TIME[7:0] × t_{SSTEP} + t_{SMIN} with t_{SSTEP} set by SEQ_CFG.SSTEP and t_{SMIN} = t_{SSTEP}/2 For the case where SEQ_CFG.SSTEP = 0, refer to Table 8-18. For the case where SEQ_CFG.SSTEP = 1, refer to Table 8-19.

Table 8-18. SEQ_CFG.SSTEP = 0

PARAMETER	SYMBOL	MIN (-6%)	TYPICAL	MAX (+6%)	UNIT
Slot step size	t_{SSTEP}	235	250	265	µs
Min slot time (0x00)	t_{SMIN}	117.5	125	132.5	µs
Max slot time (0xFF)	t_{SMAX}	60042.5	63875	67707.5	µs

Table 8-19. SEQ_CFG.SSTEP = 1

PARAMETER	SYMBOL	MIN (-6%)	TYPICAL	MAX (+6%)	UNIT
Slot step size	t_{SSTEP}	940	1000	1060	µs
Min slot time (0x00)	t_{SMIN}	470	500	530	µs
Max slot time (0xFF)	t_{SMAX}	240170	255500	270830	µs

Table 8-20. SEQ_DSLOT

Address: 0x32

Description: Power Down sequencing time slot configuration.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if SEQ group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:0	TIME[7:0]	Sets time slot between sequencing points on power-down: t_{DSLOT} = SEQ_DSLOT.TIME[7:0] × t_{SSTEP} + t_{SMIN} with t_{SSTEP} set by SEQ_CFG.SSTEP and t_{SMIN} = t_{SSTEP}/2 See Table 8-17 for setting details.

Table 8-21. PWR_EN[12:1]

Address: PWR_EN1 (0x33) - PWR_EN12 (0x3E) (Twelve 8-bit registers).

Description: Power Up/ Down sequence definition by assignment of EN[12:1] to one of fifteen time slots.

Slot=1 is the earliest slot that can be selected and it indicates that the ENx pin will toggle in the first SEQ_USLOT.TIME or SEQ_DSLOT.TIME after the triggering event.

POR Value: Loaded from NVM.

Access: Read/Write. Read-only if SEQ group is protected.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7:4	PU[3:0]	Power Up Sequence: 0 = ENx pin not mapped to sequence. ENx maintains previous state, unless entering BACKUP or FAILSAFE state (ENx is pulled low in those states). 1 = ENx pin mapped to first time slot (first up). 15 = ENx pin mapped to last time slot (last up).
3:0	PD[3:0]	Power Down Sequence: 0 = ENx pin not mapped to sequence. ENx maintains previous state, unless entering BACKUP or FAILSAFE state (ENx is pulled low in those states). 1 = ENx pin mapped to first time slot (first down). 15 = ENx pin mapped to last time slot (last down).

Table 8-22. PROT1, PROT2

Address: 0xF0, 0xF1

Description: Protection selection registers. In order to write-protect a register group, the host must set the relevant bit in both registers.

POR Value: 0x00

Access: Read/Write.

For security, these registers need to have POR value=0x00 and become read-only once set until power cycle.

Once set to 1, they cannot be cleared to 0 by the host; a power cycle (VDD=0) is required to write different registers configurations.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7	RSVD	Reserved
6	WRK	0 = Working registers are writable. 1 = Writes to working registers are ignored.
5	RSVD	RSVD
4	SEQP	0 = Power Sequence registers are writable. 1 = Writes to Power Sequence registers are ignored.
3	SEQC	0 = Sequence slot configuration registers are writable. 1 = Writes to Sequence slot configuration registers are ignored.
2	RSVD	RSVD
1	RSVD	RSVD
0	CTL	0 = Control registers are writable. 1 = Writes to control registers are ignored.

Table 8-23. I2CADDR

Address: 0xF9

Description: I^2C address.

POR Value: Loaded from NVM.

Access: Read-Only.

Back to Register Map Table.

BIT	NAME	DESCRIPTION
7	RSVD	Reserved
6:0	ADDR_NVM[6:0]	I^2C target device address. Set in NVM.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Modern SOC and FPGA devices typically need multiple power rails to provide power to the different blocks within the respective SOC or FPGA. Accurate voltage level and timing requirements are common and must be met to maintain proper operation of these devices. By utilizing TPS38700S-Q1 along with a multichannel voltage supervisor like the TPS389006-Q1, the power up and power down sequencing requirements as well as the core voltage requirements of the target SOC or FPGA can be met. This design can also assist in meeting the strict timing requirements for an SOC or FPGA .

9.2 Typical Application

9.2.1 Automotive Multichannel Sequencer and Monitor

A typical application for the TPS38700S-Q1 is shown in Figure 9-1. TPS38700S-Q1 is used to provide the proper voltage sequencing for the target SOC device by providing enable signals to the DC/DC converters shown. These DC/DC converters are used to generate the appropriate voltage rails for the SOC. A mulitchannel voltage monitor like the TPS389006-Q1 is used to monitor the voltage rails as these rails power up and power down to ensure that the correct sequence occurs in both occasions. After a rail successfully powers up, a SYNC pulse will be need to be sent to TPS38700S-Q1 in order to bring up the subsequent power rail. A microcontroller is also used to provide ACT, NIRQ, and I^2C commands to the TPS38700S-Q1 and the multichannel voltage monitor. The ACT signal from the microcontroller determines when the TPS38700S-Q1 enters into ACTIVE or SHDN states while the NIRQ pin of the TPS38700S-Q1 acts as an interrupt pin that is set when a fault has occurred. For instance, if an external device pulls the NRST pin low, then the TPS38700S-Q1 will trigger an interrupt through the NIRQ pin. I^2C is used to communicate the type of fault to the host microcontroller. The host microcontroller can clear the fault by writing 1 to the affected register. The power rails for the microcontroller are not shown in Figure 9-1 for simplicity.

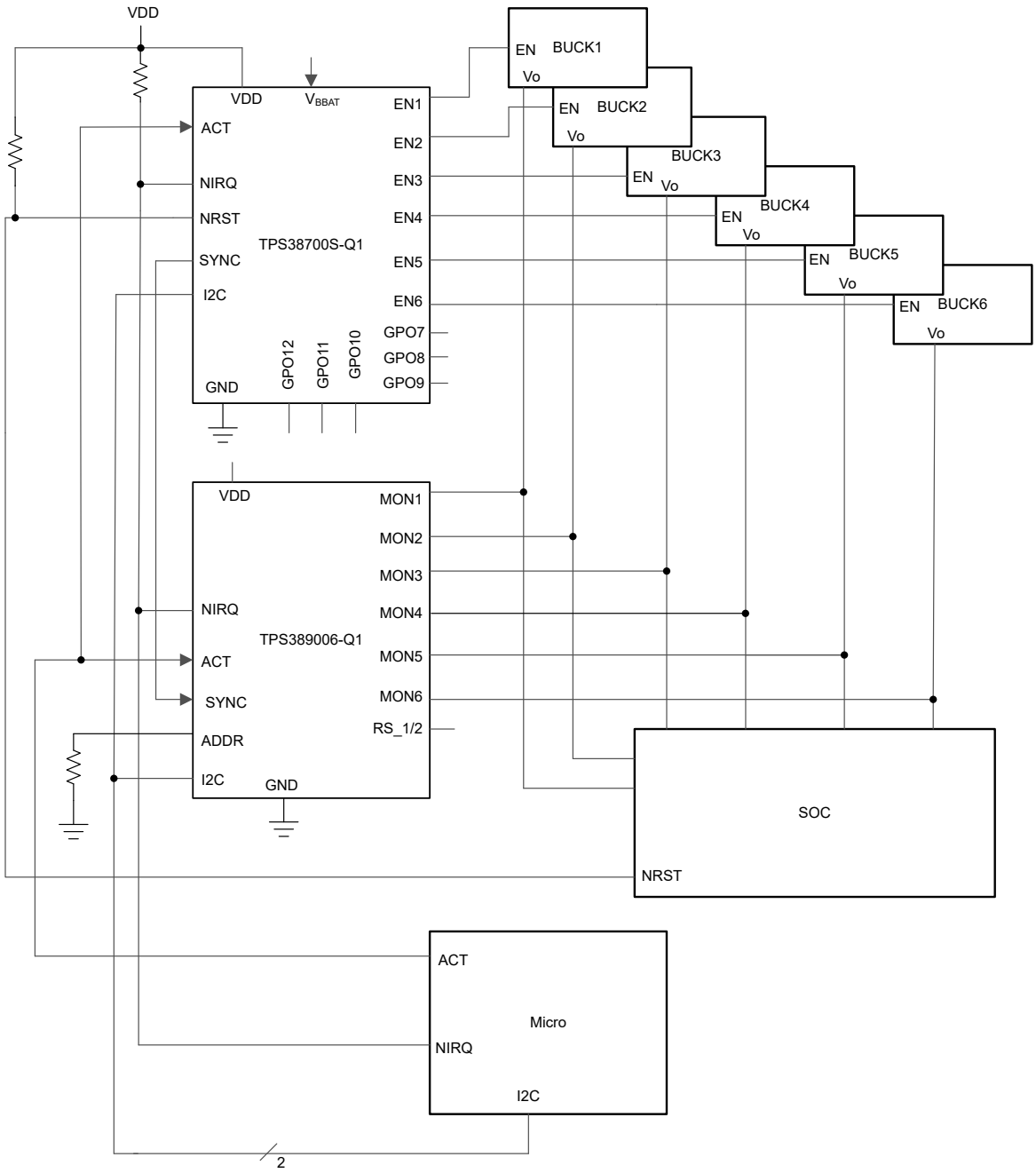

Figure 9-1. TPS38700S Voltage Sequencer Design Block Diagram

9.2.2 Design Requirements

- Eight different voltage rails supplied by DC/DC converters need to be properly sequenced in this design. The sequence order and timing requirements are outlined in Table 9-1.
- Emergency power down functionality is optional.
- Backup battery power supply required. This must be stepped down to a maximum value of 5.5 V in order to comply with the absolute maximum ratings of the V_{BBAT} pin.
- All detected failures in sequencing should be reported via an external hardware interrupt signal.
- All detected failures should be logged in internal registers and be accessible to an external processor via I^2C.

Table 9-1. Power Up and Power Down Sequence Requirement

ENABLE CHANNEL	POWER UP SEQUENCE POSITION	POWER DOWN SEQUENCE POSITION	TIME BETWEEN POWER UP SIGNALS (µs)	TIME BETWEEN POWER DOWN SIGNALS (µs)
EN1	1	4	625	625
EN2	1	1	625	625
EN3	2	3	625	625
EN4	2	3	625	625
EN5	3	2	625	625
EN6	4	1	625	625

9.2.3 Detailed Design Procedure

- TPS38700S-Q1 device comes preprogrammed with the power up, power down sequences shown in Table 9-1.
- NIRQ and NRST pins both require a pull up resistor in the range of 10 kΩ to 100 kΩ.
- SDA and SCL lines require pull up resistors in the range of 10 kΩ.
- The microcontroller is used to clear fault interrupts reported through the NIRQ interrupt pin and the INT_SCR1 and INT_SCR2 registers. The interrupt flags can only be cleared by the host mircontroller with a write-1-to-clear operation; interrupt flags are not automatically cleared if the fault condition is no longer present.

9.2.4 Test Implementation

The TPS38700S-Q1 SYNC feature can be demonstrated in a simple test setup with the TPS389006-Q1. For this test, you need the TPS38700Q1EVM-Q1 and the TPS389006Q1EVM-Q1. Replace U1 on the TPS38700Q1EVM with the orderable part TPS38700603SRGERQ1. Replace the U1 on TPS389006Q1EVM with orderable part TPS38900603NRTERQ1. The orderable part TPS38900603NRTERQ1 has initial conditions set such that TPS38700603SRGERQ1 enable voltages meet the UV thresholds to trigger SYNC pulses by default. Connect the system as shown in Figure 9-2. Connect ACT and VDD to two separate power supplies. Configure the settings over I2C as needed. However, note that power cycling the evaluation modules sets the conditions back to default. If you enable ACT and have done everything correctly, then no LED's should be turned on. If something goes wrong, then either NIRQ on TPS389006-Q1 or NRST on TPS38700S-Q1 will be set low.

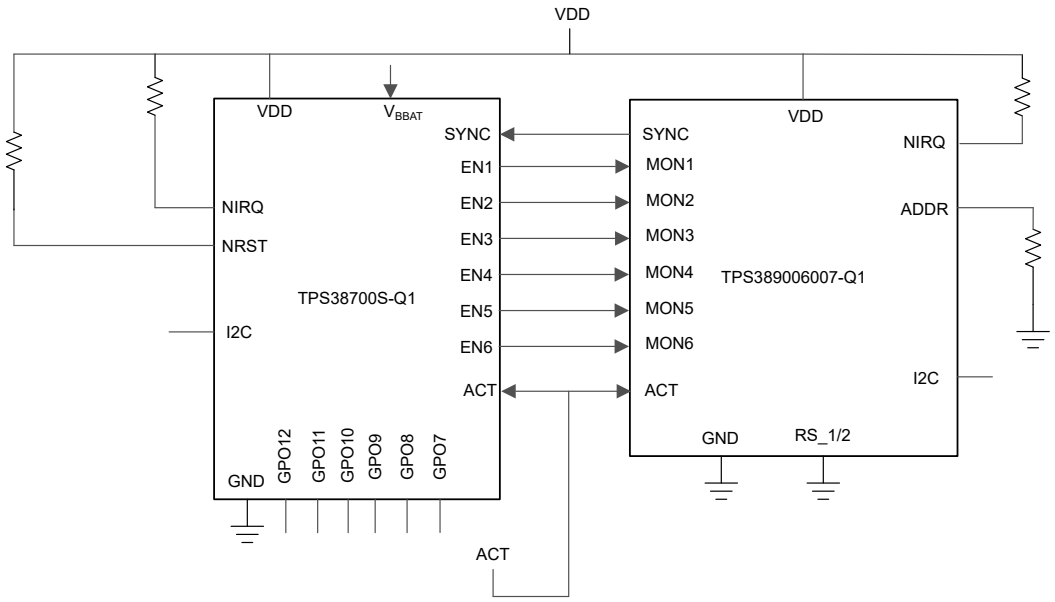

Figure 9-2. TPS38700S SYNC Test Implementation

Toggling high ACT makes the waveform of the enable voltages look like Figure 9-3 If the waveform does not look that, then to debug check and make sure that everything is connected properly. If the system is connected properly, then verify the I^2C address values are what you expect the values to be. For example check if the status register of MON1 of TPS389006007-Q1 reads the TPS38700S-Q1 EN voltage output in the Fusion Digital Power Tool.

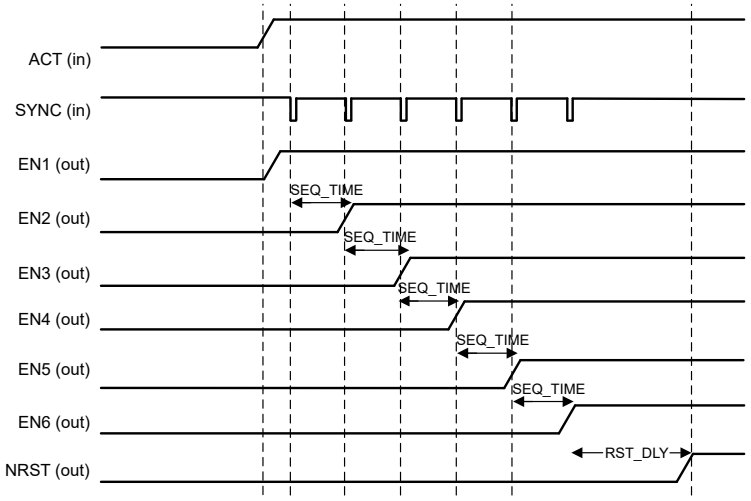

Figure 9-3. TPS38700S SYNC Sequence Up Test Implementation Waveform

Figure 9-3 shows how the device behaves when ACT is toggled off. Note that there's no delay between when the system detects the ACT falling edge and when NRST and EN6 start sequencing down.

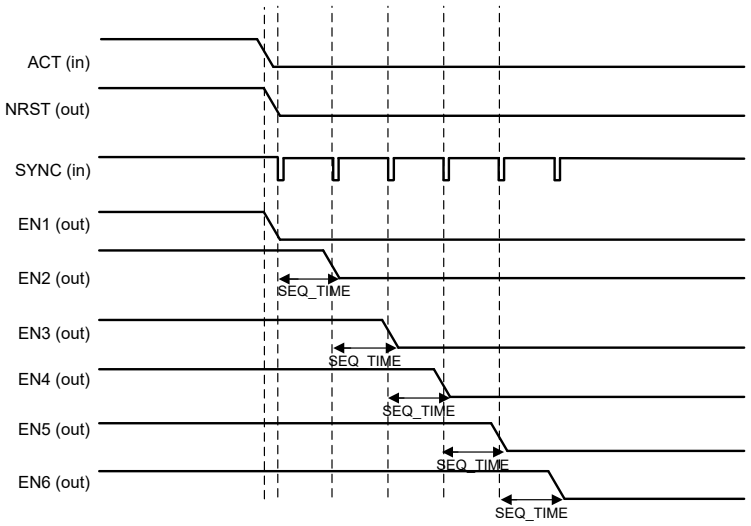

Figure 9-4. TPS38700S SYNC Sequence Down Test Implementation Waveform

9.2.5 Application Curves

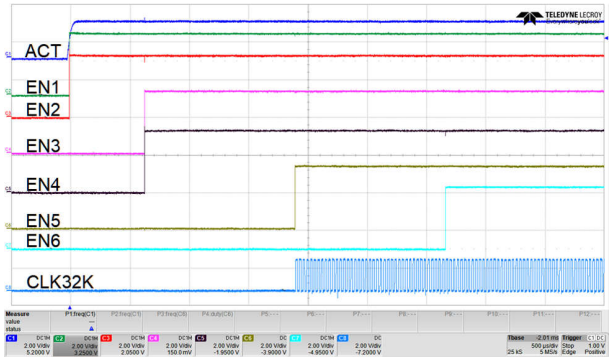

Figure 9-5. Power Up Sequence

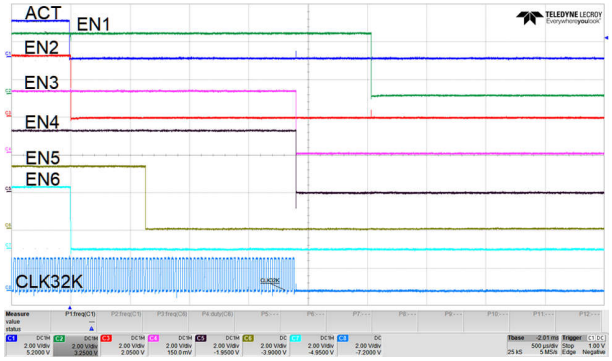

Figure 9-6. Power Down Sequence

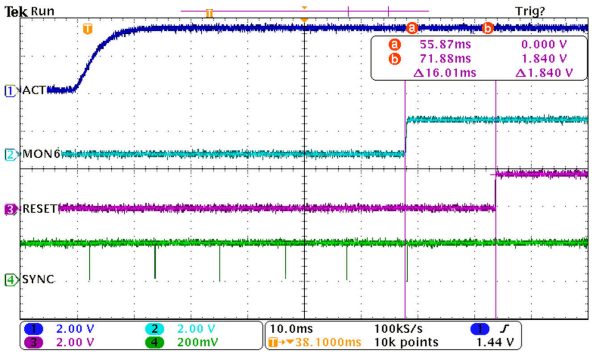

Figure 9-7. Power Up Sequence with SYNC

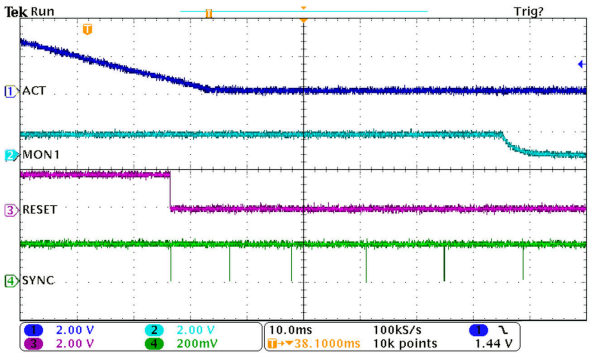

Figure 9-8. Power Down Sequence with SYNC

10 Power Supply Recommendations

10.1 Power Supply Guidelines

This device is designed to operate from an input supply with a voltage range between 2.2 V to 5.5 V. It has a 6 V absolute maximum rating on the VDD pin as well as on the V_{BBAT} pin. It is good analog practice to place a 0.1-µF to 1-µF capacitor between the VDD pin and the GND pin depending on the input voltage supply noise. If the voltage supply providing power to VDD is susceptible to any large voltage transients that exceed maximum specifications, additional precautions must be taken.

11 Layout

11.1 Layout Guidelines

- Place the external components as close to the device as possible. This configuration prevents parasitic errors from occurring.
- Do not use long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC circuit and create ringing with peak voltages above the maximum VDD voltage.
- Do not use long traces of voltage to the sense pin. Long traces increase parasitic inductance and cause inaccurate monitoring and diagnostics.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

11.2 Layout Example

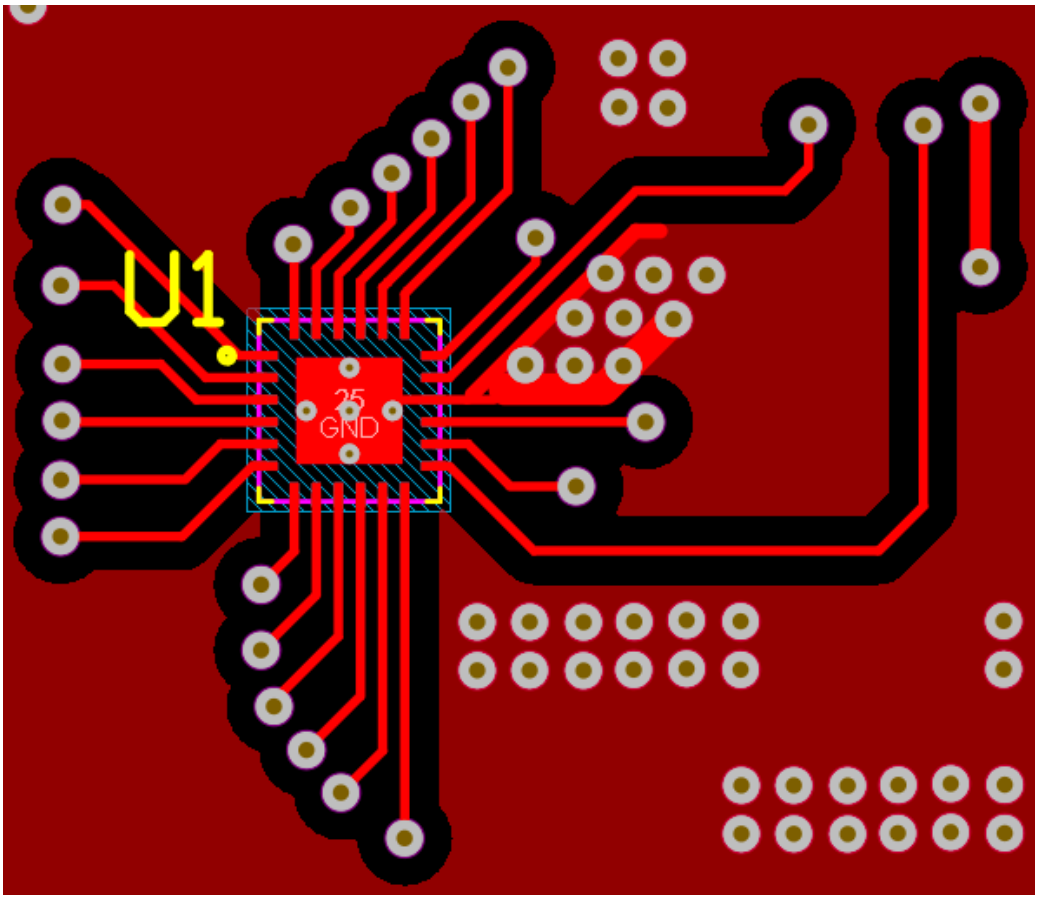

Figure 11-1. Recommended Layout

12 Device and Documentation Support

12.1 Device Nomenclature

Table 12-1 shows how to decode the function of the device based on the device ordering code, while Figure 5-1 shows the sequence configuration based on the device ordering code. See Figure 5-1 for more information regarding how to decode the device part number.

Table 12-1. Device Comparison Table

ORDERING CODE	FUNCTIONS	EN PINS DEFAULT	GPO	TIME SLOT (µsec)	I²C ADDR.	RESET DELAY (msec)	I²C PULL-UP VOLTAGE (V)
TPS38700603SRGERQ1	Sequencer, GPO	Open-drain	Open-Drain	625	3C	16	3.3

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

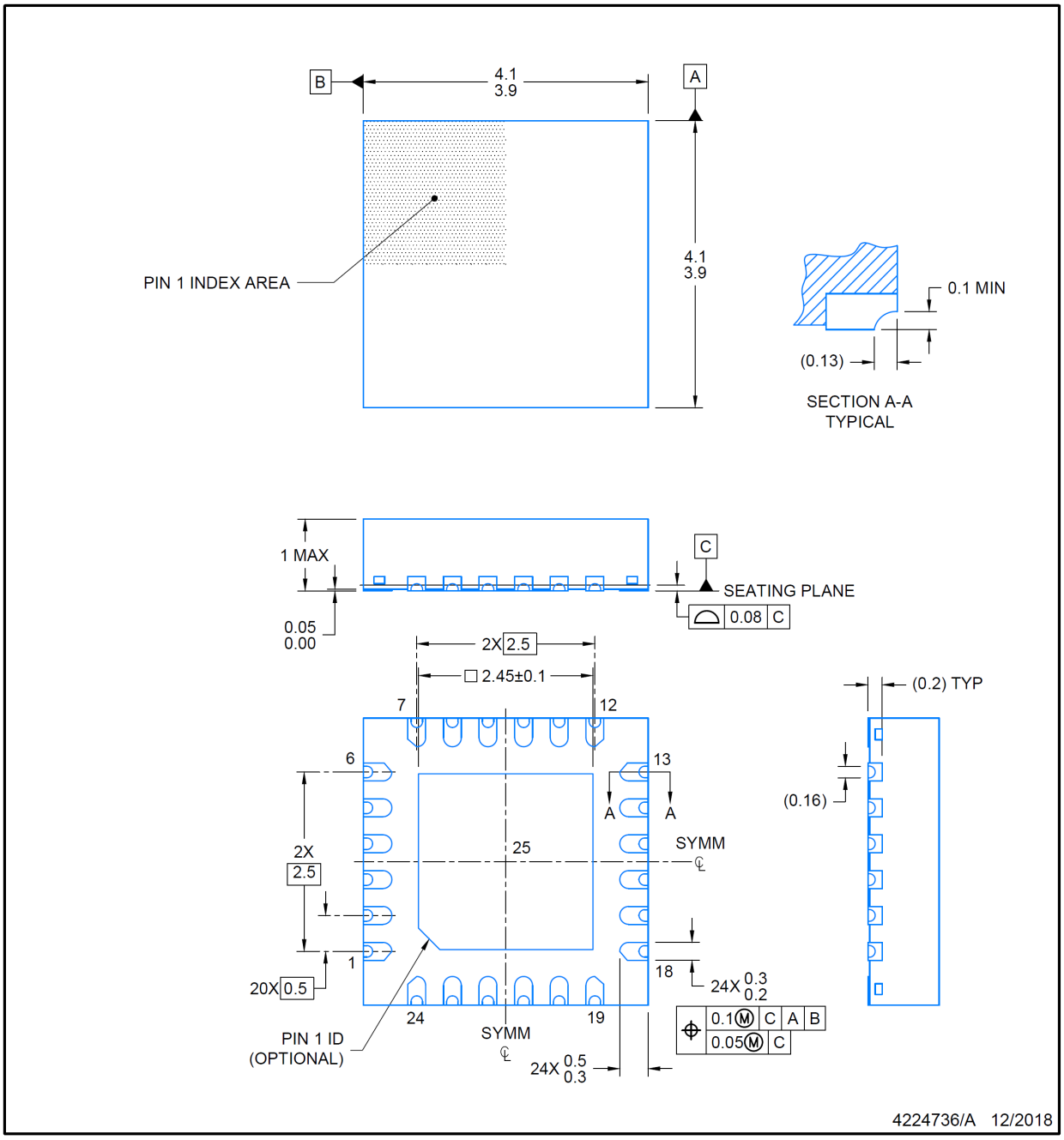
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RGE0024N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

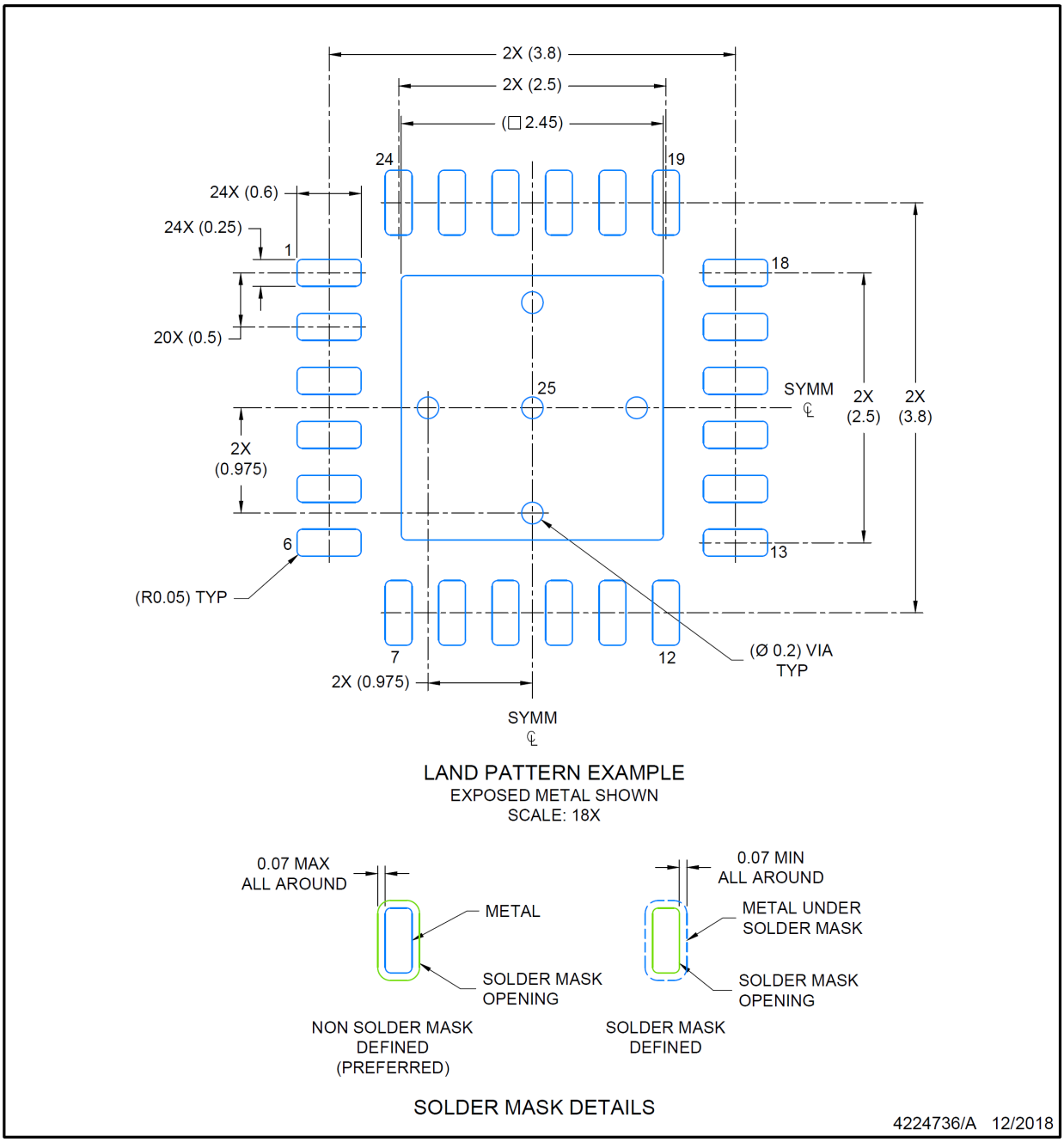
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGE0024N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

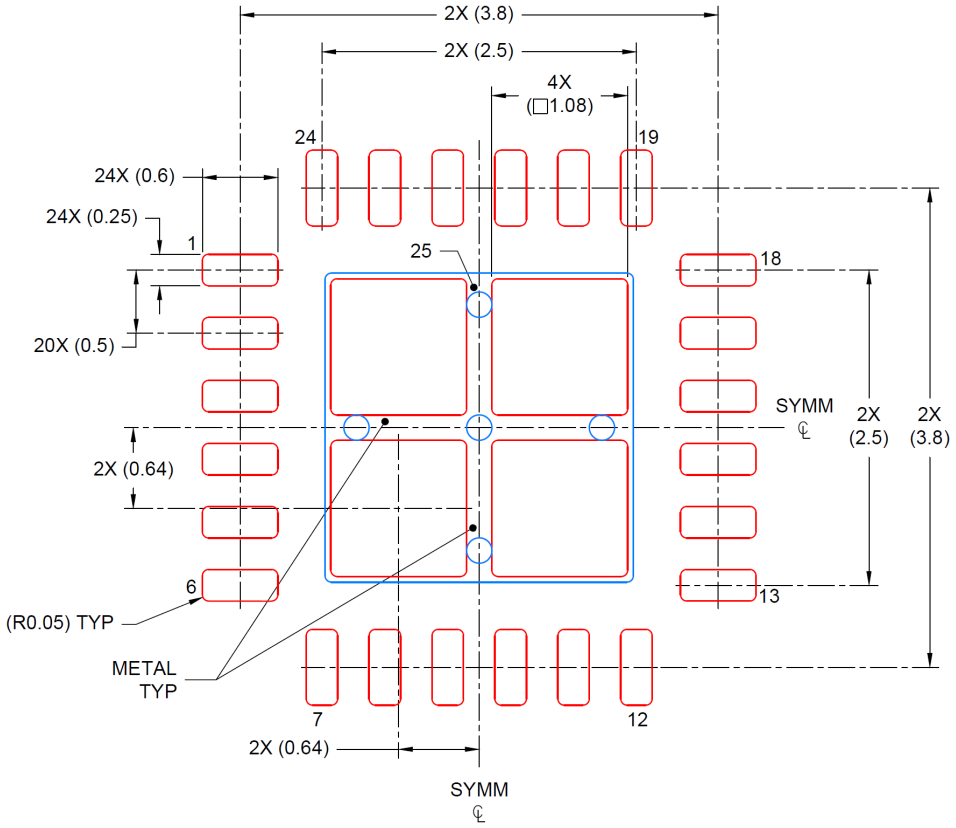
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS38700603SRGERQ1	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T387006 03SQA1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

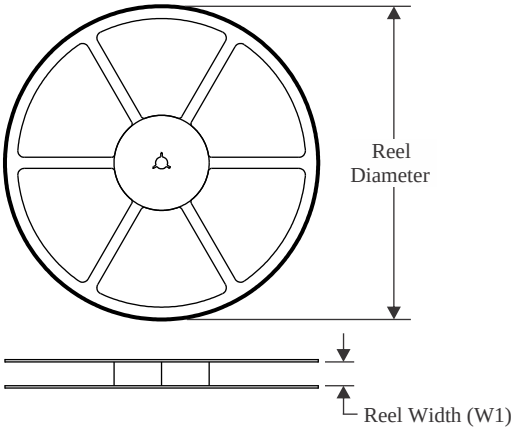
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

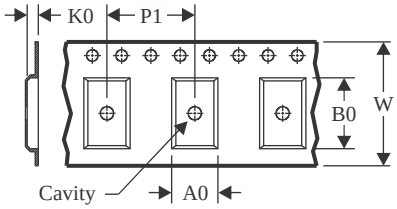
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

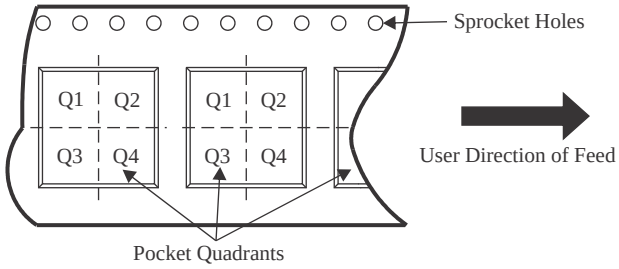


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

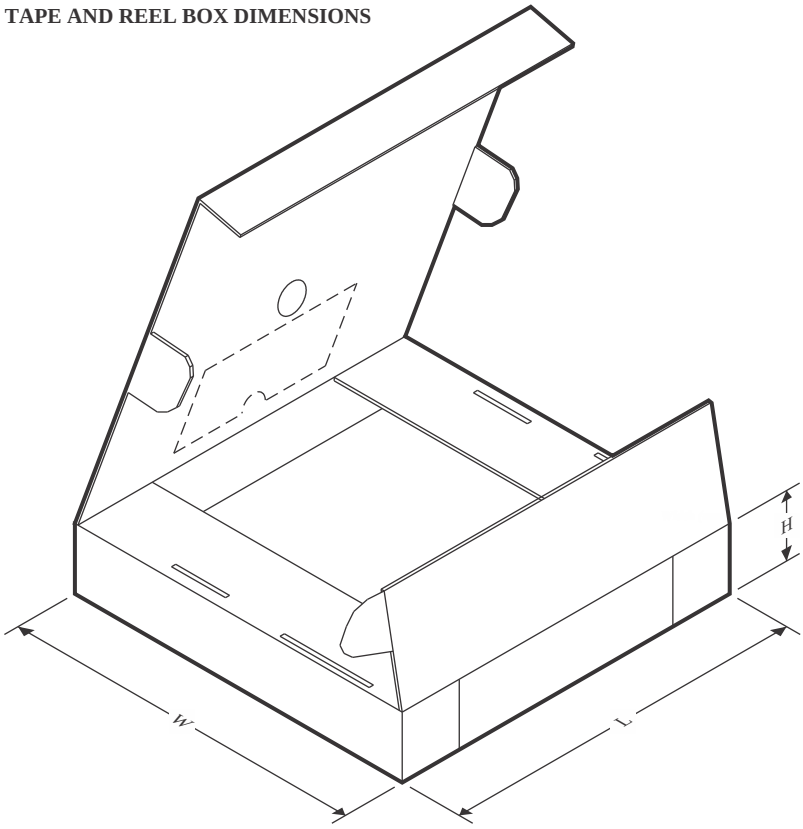
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS38700603SRGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



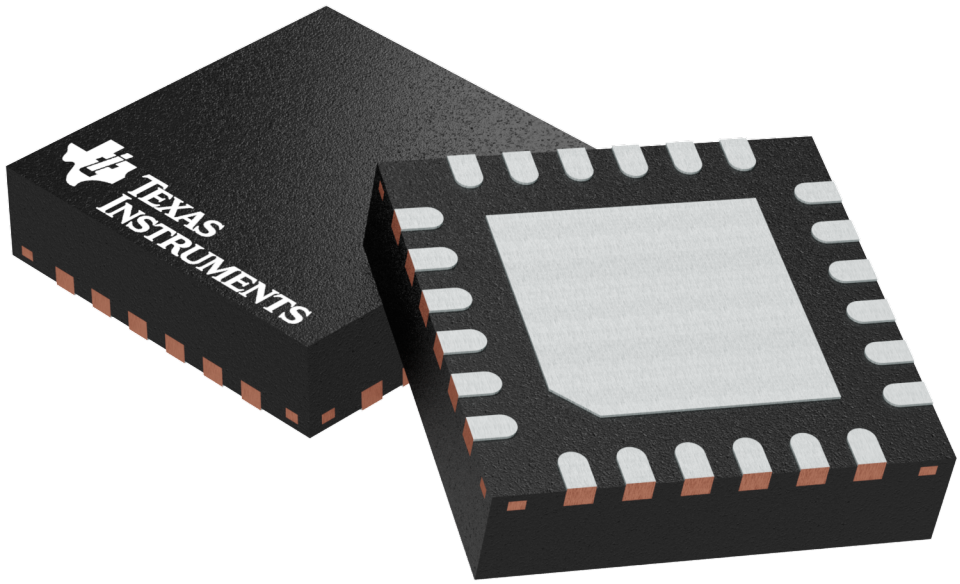
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS38700603SRGERQ1	VQFN	RGE	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

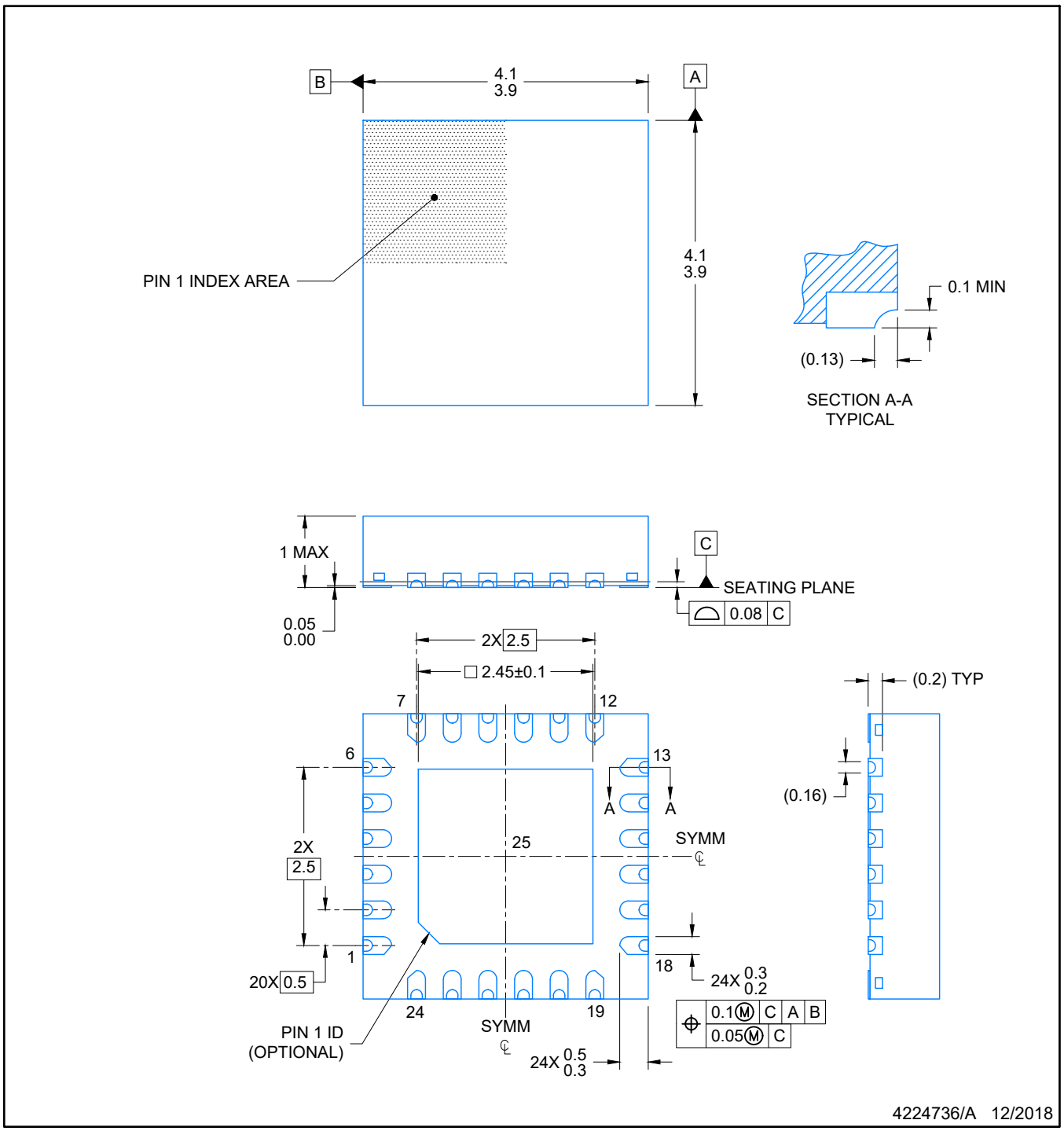
RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H



NOTES:

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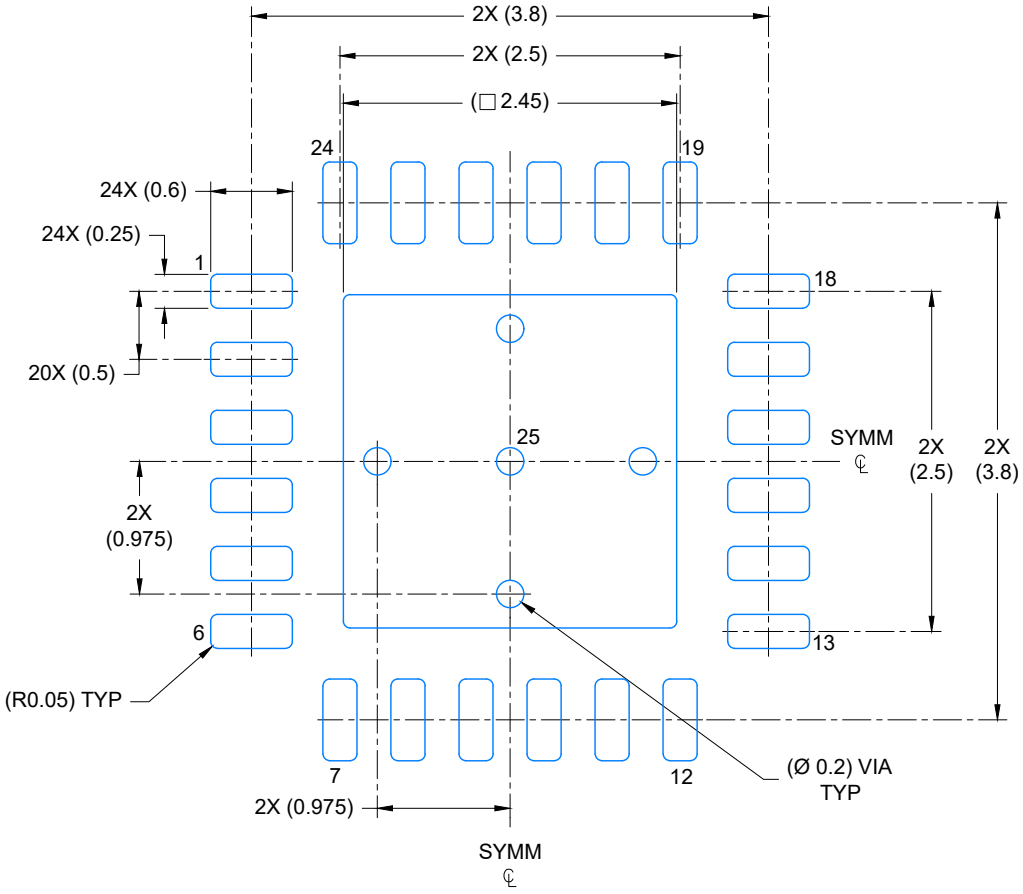
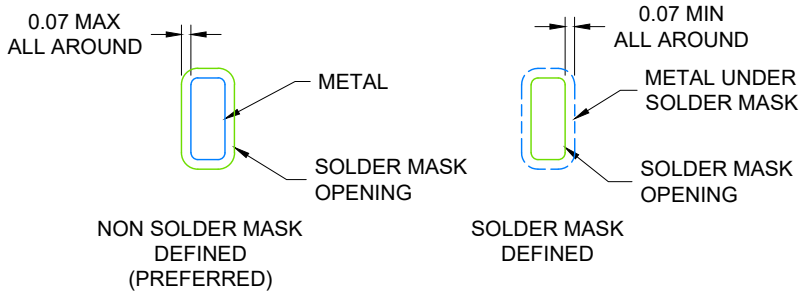
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X



SOLDER MASK DETAILS

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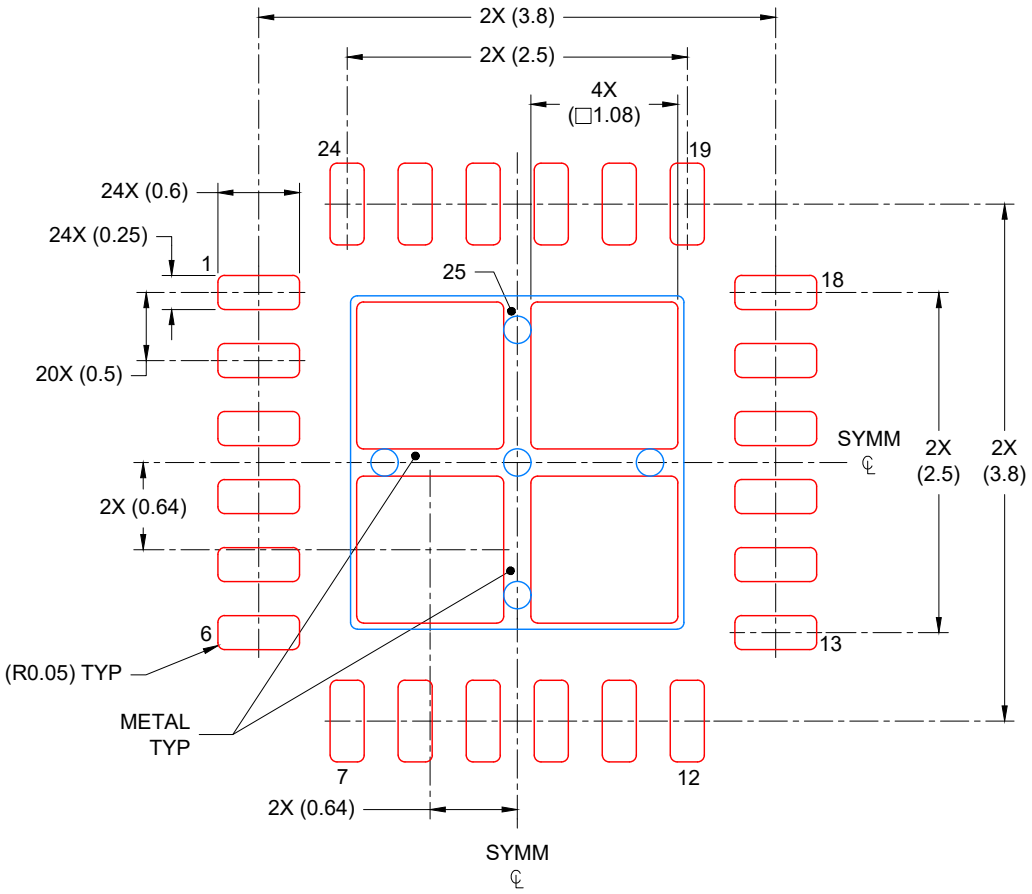
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 18X

4224736/A 12/2018

NOTES: (continued)

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