TPS61199 White-LED Driver for LCD Monitor Backlighting

1 Features

- 8-V to 30-V Input Voltage
- Integrated High-Power Boost Controller
- Adaptive Boost Output for LED Voltages
- Drive up to Eight LED Strings in Parallel
- Maximum 70 mA for Each LED String
- 3% Current Matching Between Strings
- 5000:1 PWM Dimming Ratio at 200 Hz
- MOSFET Overcurrent Protection
- Programmable LED Short Protection
- Adjustable LED Open Protection
- Thermal Shutdown Protection
- 20-Pin SO Package and TSSOP Package With PowerPAD™

2 Applications

- Monitor LCD Backlight
- LCD TV Backlight
- General LED Lighting

3 Description

The TPS61199 provides highly integrated solutions for large size LCD backlighting. This device integrates a current-mode boost controller and eight current sinks for driving up to eight LED strings with multiple LEDs in series. Each string has an independent current regulator with current matching between strings reaching 3% regulation accuracy. The device automatically adjusts the output voltage of the boost converter to provide only the voltage required by the LED string with the largest forward voltage drop plus the minimum required voltage at the IFBx pin of that string, thereby optimizing efficiency of the driver.

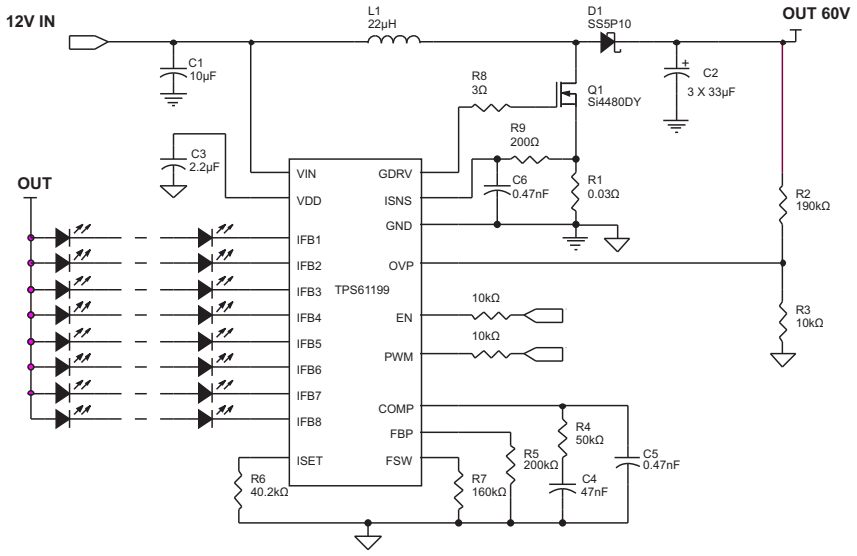
The TPS61199 provides PWM brightness dimming with an external PWM signal. The signal of the PWM maximum frequency can be as high as 22 kHz. Dimming ratios up to 5000:1 can be achieved with a 200-Hz PWM signal. The TPS61199 integrates overcurrent protection for the switch FET, soft start-up, LED short protection, LED open protection, and overtemperature shutdown protection. The TPS61199 device is available in 20-pin SO and HTSSOP packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61199	SO (20)	12.60 mm × 5.30 mm
	HTSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2011) to Revision B **Page**

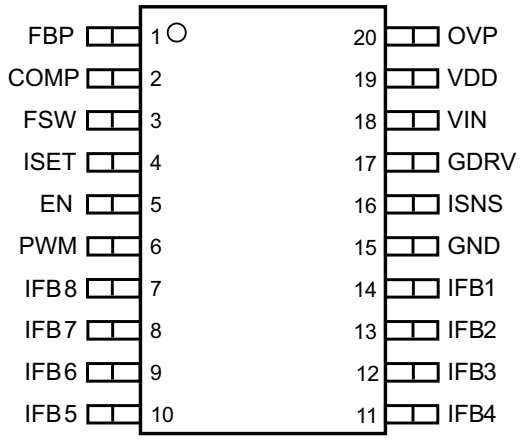
- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; delete *Device Comparison* table - info in POA ... 1

Changes from Original (December 2010) to Revision A **Page**

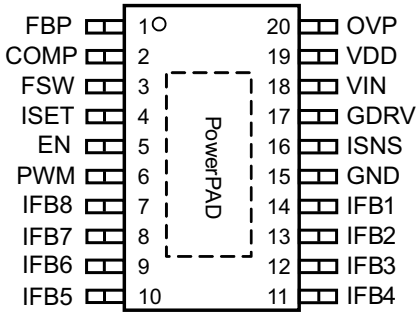
- Changed to Rev A, May 2011 ... 1
- Changed from 65 mA to 70 mA in fifth list Item of Features ... 1
- Changed ABS MAX table MAX column, row 1 to 33 and the 4th row to 3.6 ... 4
- Changed Electrical Characteristics table, Current Regulation, I_{IFB_max} spec MIN value from 65 to 70 mA ... 5
- Changed values in ELEC CHAR TABLE, OSCILLATOR section, first 2 rows 0.66, 0.8, 0.94 and 0.44, 0.5, 0.56 ... 5
- Changed values in ELEC CHAR TABLE, PROTECTION section, first row to min 2.77, max 3.13 ... 5
- Added a paragraph: Fs (in kHz) = 80,000 / R7 (in kΩ) ... 9
- Changed 65 mA to 70 mA in paragraph in *Program LED Full-Scale Current* ... 10
- Changed 65 mA to 70 mA in paragraph in *Drive High Current LED* ... 10
- Added ListItem number 4 to OrderedList under Protection section ... 10
- Changed or added the paragraph *Current Sense and Current Sense Filtering* ... 14

5 Pin Configuration and Functions

NS Package
20-Pin SO
Top View



PWP Package
20-Pin HTSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
COMP	2	Output	Loop compensation pin. Connect an RC network to make loop stable (see *Loop Consideration*).
EN	5	Input	Enable/disable pin — high = device is enabled; low = device is disabled.
FBP	1	Output	LED short-across protection threshold program pin (see *Protection*)
FSW	3	Output	Boost switching frequency selection pin. Connect a resistor to set the frequency between 300 kHz to 800 kHz.
GDRV	17	Output	External Switch MOSFET gate driver output pin
GND	15	Ground	Ground pin
IFB1 to IFB8	7, 8, 9, 10, 11 12, 13, 14	Input	Regulated current sink input pins.
ISET	4	Output	Full-scale LED current selection pin; connect a resistor to program LED current for each string
ISNS	16	Input	External MOSFET current sense positive input pin
OVP	20	Input	Overvoltage protection pin (see *Protection*)
PWM	6	Input	PWM dimming signal input pin. The frequency must be in the range of 100 Hz to 22 kHz.
VDD	19	Output	Internal regulator output pin. Connect a 2.2-µF capacitor between this pin to GND.
VIN	18	Input	Supply input pin. This pin can be tied to a voltage different from the power stage input.
PowerPAD – HTTSOP package		—	The PowerPAD pad must be soldered to the ground. If possible, use thermal vias to connect to top and internal ground plane layers for ideal power dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Pin VIN(2)	–0.3	33	V
	Pin IFB1 to IFB8(2)	–0.3	30	
	Pin EN and PWM(2)	–0.3	20	
	Pin ISET, ISNS and OVP(2)	–0.3	3.6	
	All other pins(2)	–0.3	7	
Continuous power dissipation		See *Thermal Information*		
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–65	50	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control procedures.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	NOM	MAX	UNIT
Inductor, L1	10	22	47	µH
Input capacitor, C1	10			µF
Output capacitor, C2	10	33	100	µF
PWM dimming frequency, f_{PWM}	0.1		22	KHz
Rising/falling edge of PWM signal, t_{PWM}			1	µsec
Boost regulator switching frequency, f_{BOOST}	300		800	kHz
Operating ambient temperature, T_A	–40		85	°C

(1) Customers must verify the component values in their application if the values are different from the recommended values.

6.4 Thermal Information

THERMAL METRIC(1)		TPS61199 NS (SO) 20 PINS	TPS61199 PWP (HTSSOP) 20 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	69.4	46.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.4	48.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.3	22.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.0	3.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.8	13.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics

V_{IN} = 12 V; T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
VIN	Input voltage range		8		30	V
V_{UVLO_VIN}	Undervoltage lockout threshold	V_{IN} falling		6.5	7	V
V_{VIN_SYS}	VIN hysteresis	V_{IN} rising		300		mV
I_{Q_VIN}	Operating quiescent current into VIN	EN = high; PWM = low; no switching, V_{IN} = 30 V			1.5	mA
I_{SD}	Shutdown current				10	µA
VDD	Internal regulation voltage	Output current of V_{DD} = 15 mA	5.7	6	6.3	V
EN and PWM						
V_H	Logic high threshold on EN, PWM	V_{IN} = 8 V to 30 V	2			V
V_L	Logic low threshold on EN, PWM	V_{IN} = 8 V to 30 V			0.8	V
R_{PD}	Pulldown resistor on EN, PWM		400	800	1600	kΩ
CURRENT REGULATION						
V_{ISET}	ISET pin voltage		1.204	1.229	1.253	V
K_{ISET}	Current multiple $I_{IFB(AVG)}$ / I_{SET}	I_{ISET} = 30 µA; IFB = 450 mV		1990		
IFB	Current accuracy to $I_{IFB(AVG)}$	I_{ISET} = 30 µA; IFB = 450 mV	–2%		2%	
$IFB_{(BR)}$ (1)	Current matching	I_{ISET}= 30 µA; IFB = 450 mV			3%	
IFB_{leak}	IFB pin leakage current	IFB voltage = 30 V; PWM = low	10	25	45	µA
I_{IFB_max}	Current sink max output current	IFB = 450 mV	70			mA
OSCILLATOR						
f_{OSC}	Switching frequency	R = 100 kΩ	0.66	0.8	0.94	MHz
		R = 160 kΩ	0.44	0.5	0.56	
V_{FSW}	FSW pin reference voltage			1.229		V
$Duty_{max}$	Maximum duty cycle	F_{SW} = 500 kHz	90%	94%		
t_{skip}	Minimum pulse width for skip cycle mode			200		ns
GATE DRIVER and OVERCURRENT LIMIT						
$R_{GDRV(SRC)}$	Gate driver impedance when sourcing	V_{GDRV} = 6 V, I_{GDRV} = 20 mA		2		Ω
$R_{GDRV(SNK)}$	Gate driver impedance when sinking	V_{GDRV} = 6 V, I_{GDRV} = 20 mA		1.5		Ω
V_{ISNS}	Switch current limit detection threshold	V_{IN} = 8 V to 30 V	120	160	180	mV
PROTECTION						
V_{CLAMP}	Output overvoltage threshold at OVP pin		2.77	2.95	3.13	V
I_{FBP}	LED short across protection bias current multiple I_{FBP}/I_{ISET}	VFBP = 1 V	0.23	0.25	0.27	
V_{OVP_IFB}	IFB overvoltage threshold		26.5		29.5	V
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			150		°C

(1) Current matching = (I_{MAX} – I_{MIN}) / I_{AVG}

6.6 Typical Characteristics

Typical Application as test circuit, and L = CDRH127/HPNP- 220M, R6 = 41kΩ, unless otherwise noted

DESCRIPTION		FIGURES
Dimming linearity	17 LEDs in series; V_{IN} = 12 V	Figure 1
Dimming with short on time	17 LEDs in series; V_{IN} = 12 V	Figure 2
Current matching	17 LEDs in series; V_{IN} = 12 V	Figure 3
Dimming waveform	17 LEDs in series; V_{IN} = 12 V; 200 Hz with 1% duty cycle	Figure 4
Dimming waveform	17 LEDs in series; V_{IN} = 12 V; 22 kHz with 5% duty cycle	Figure 5
Startup waveform	17 LEDs in series; V_{IN} = 12 V; 200 Hz with 50% duty cycle	Figure 6
Shutdown waveform	17LEDs in series; V_{IN} = 12 V; 200 Hz with 50% duty cycle	Figure 7
Dimming efficiency	17 LEDs in series; 200 Hz dimming frequency	Figure 9
Dimming efficiency	13 LEDs in series; 200 Hz dimming frequency	Figure 10

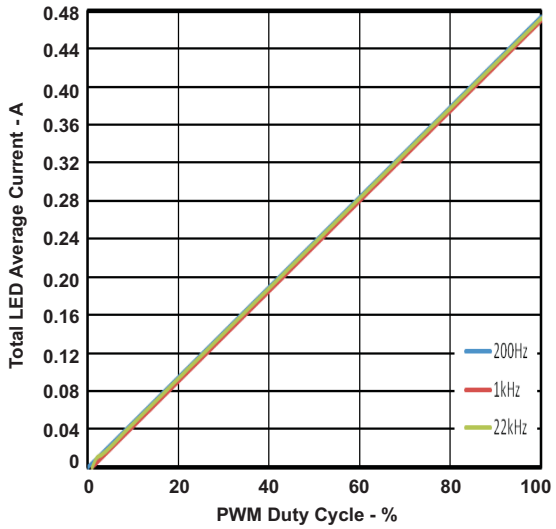


Figure 1. Dimming Linearity

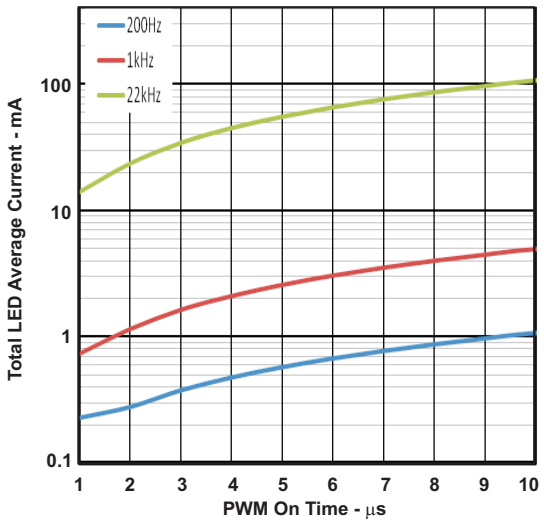


Figure 2. Dimming With Short On Time

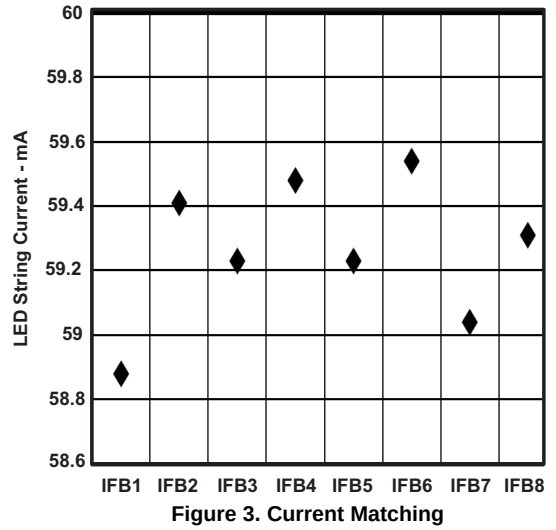


Figure 3. Current Matching

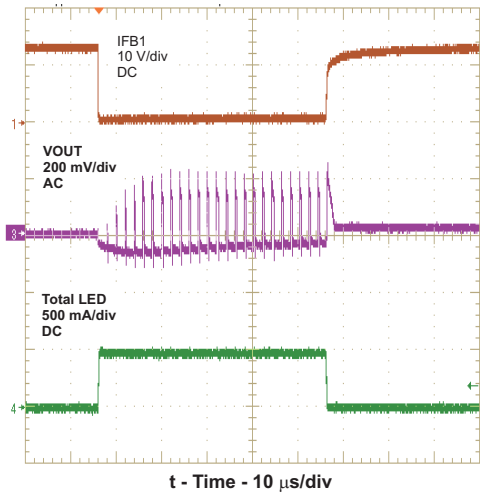


Figure 4. Dimming Waveforms

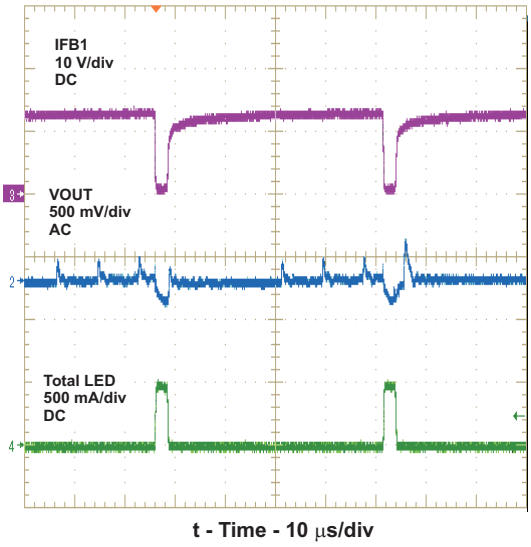


Figure 5. Dimming Waveforms

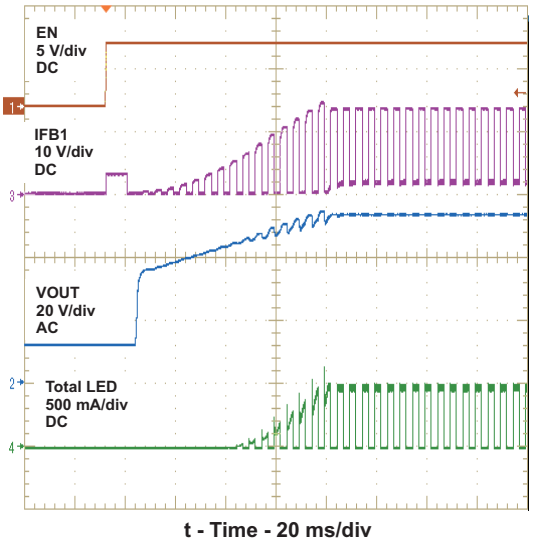


Figure 6. Start-Up Waveform

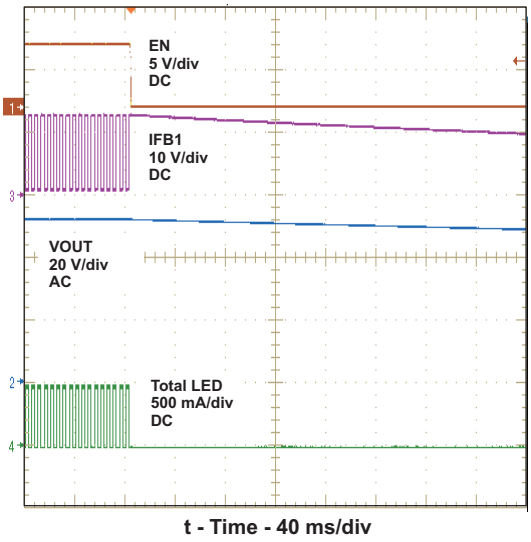


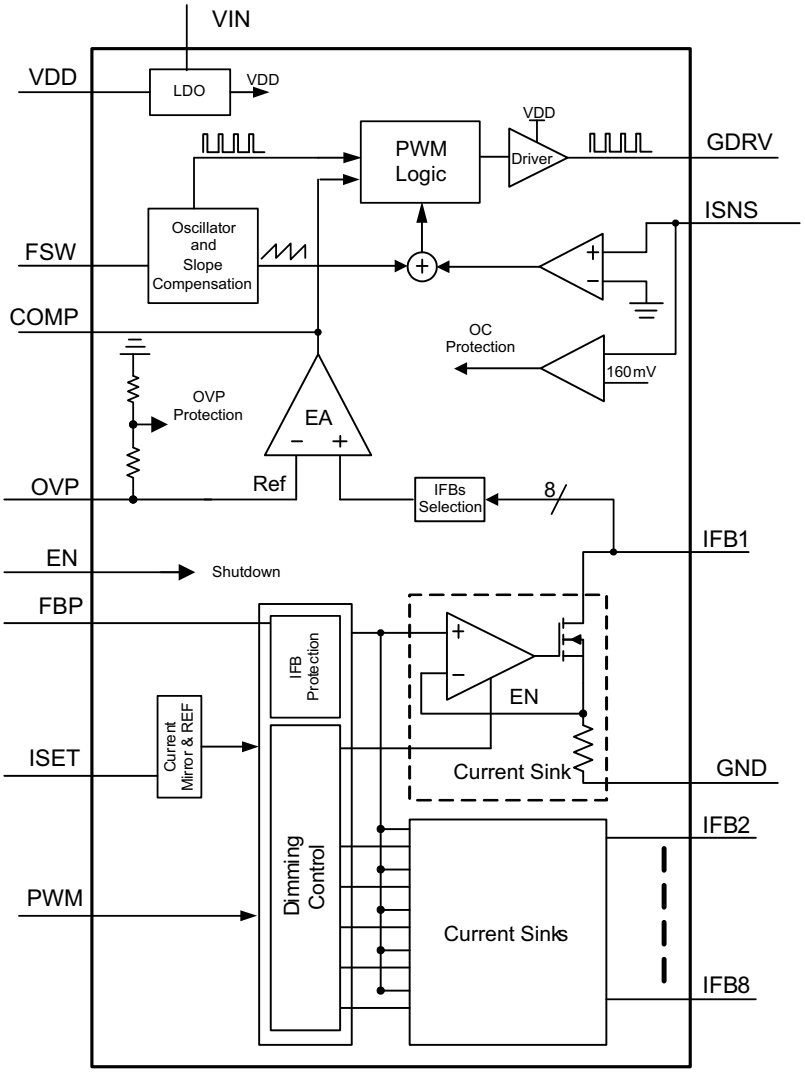
Figure 7. Shutdown Waveform

7 Detailed Description

7.1 Overview

The TPS61199 provides a highly integrated solution for large-size LCD TV backlight with high precision pulse width modulation (PWM) dimming resolution up to 5000:1. This device is a current-mode boost controller driving up to eight LED strings in parallel. The input voltage range for the device is from 8 V to 30 V. See *Functional Block Diagram* and *Typical Application*.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Supply Voltage

The TPS61199 has a built-in linear regulator to supply the device analog and logic circuitry. The VDD pin, output of the regulator, must be connected to a 2.2-µF bypass capacitor. VDD only has a current sourcing capability of 15 mA. VDD voltage is ready after the EN pin is pulled high.

7.3.2 Boost Controller

A boost controller is shown at the top of the *Functional Block Diagram*. The TPS61199 regulates the output voltage with current mode pulse width modulation (PWM) control. The control circuitry turns on an external switch FET at the beginning of each switching cycle. The input voltage is applied across the inductor and stores the energy as the inductor current ramps up. During this portion of the switching cycle, the load current is provided by the output capacitor. When the inductor current rises to the threshold set by the *Error Amplifier* (EA) output, the switch FET is turned off and the external Schottky diode is forward biased. The inductor transfers stored energy to replenish the output capacitor and supply the load current. This operation repeats each switching cycle. The switching frequency is programmed by the external resistor.

A ramp signal from the oscillator is added to the current ramp to provide slope compensation, shown in the *Oscillator and Slope Compensation* block. The duty cycle of the converter is then determined by the *PWM Logic* block which compares the EA output and the slope compensated current ramp. The feedback loop regulates the OVP pin to a reference voltage generated by the minimum voltage across the IFB pins. The output of the EA is connected to the COMP pin. An external RC compensation network must be connected to the COMP pin to optimize the feedback loop for stability and transient response.

The device consistently adjusts the boost output voltage to account for any changes in LED forward voltages. In the event that the boost controller is not able to regulate the output voltage due to the minimum pulse width (t_{skip} in *Electrical Characteristics*), the device enters pulse skip mode. In this mode, the device keeps the power switch off for several switching cycles to prevent the output voltage from rising above the regulated voltage. This operation typically occurs in light load condition or when the input voltage is higher than the output voltage.

7.3.3 Switching Frequency

The TPS61199 switching frequency can be programmed between 300 kHz to 800 kHz by a external resistor (R7 in *Typical Application*). Table 1 shows the recommended values for the resistance.

$$Fs\ (\text{in kHz}) = 80{,}000 / R7\ (\text{in k}\Omega) \quad (1)$$

Table 1. Recommended Value For Resistance

R7	F_{SW}
100 kΩ	800 kHz
160 kΩ	500 kHz

7.3.4 Enable and Undervoltage Lockout

The TPS61199 is enabled with the soft-start when the EN pin voltage is higher than 2 V; a voltage of less than 0.8 V disables the device.

An undervoltage lockout protection feature is provided. When the voltage at VIN pin is less than 7 V, the device is switched off. The device resumes the operation once the voltage at VIN pin recovers adjusted for hysteresis (see V_{VIN_SYS} in *Electrical Characteristics*).

7.3.5 Start-Up

The TPS61199 has integrated soft-start circuitry to avoid any inrush current during start-up. During the start-up period, the output voltage rises step-by-step from the minimum voltage of LED string in 100-mV increments, shown in Figure 6. The soft-start time depends on the load and the output capacitor.

7.3.6 Unused LED String

If the application requires fewer than eight LED strings, the TPS61199 simply requires shorting the unused IFB pin to ground. The device detects the voltage less than 0.3 V and immediately disables the string during start-up. Refer to Figure 11.

7.3.7 Program LED Full-Scale Current

The eight current sink regulators embedded in the TPS61199 can be configured to provide up to a maximum of 70 mA per string. The current must be programmed to the expected full-scale LED current by the ISET pin resistor (R6 in Typical Application) using Equation 2.

$$I_{LED} = \frac{V_{ISET}}{R6} \times K_{ISET} \quad (2)$$

where

- K_{ISET} = Current multiple (1990 typical, in *Electrical Characteristics*)
- V_{ISET} = ISET pin voltage (1.229 V typical, in *Electrical Characteristics*)

7.3.8 PWM Dimming

LED brightness dimming is set by applying an external PWM signal of 100 Hz to 22 kHz to the PWM pin. Varying the PWM duty cycle from 0% to 100% adjusts the LED from minimum to maximum brightness respectively. The minimum on time of the LED string is 1 µsec; thus the TPS61199 has a dimming ratio of 5000:1 at 200 Hz. Refer to Figure 2 for dimming ratio in other dimming frequency.

When the PWM voltage is pulled low, the device will turn off the LED strings and keep the boost converter output at the same level as when PWM is high. Thus, the TPS61199 limit the output ripple due to the load transient that occurs during PWM dimming.

7.3.9 Drive High Current LED

For applications requiring LEDs rated for more than 70 m A, it is acceptable to tie two or more IFB pins together as shown in Figure 12.

7.4 Device Functional Modes

7.4.1 Protection

1. Switch current limit protection using the ISNS pin

   The TPS61199 monitors the inductor current through the voltage across a sense resistor (R1 in *Typical Application*) in order to provide current limit protection. During the switch FET on period, when the voltage at ISNS pin rises above 160 mV (V_{ISNS} in *Electrical Characteristics*), the device turns off the FET immediately and does not turn it back on until the next switch cycle. The switch current limit is equal to 160 mV / R1.

2. LED open protection

   When one of the LED strings is open, the boost output rises to the clamp threshold voltage (see 5. *Output overvoltage protection using the OVP pin*). The device detects the open string by sensing no current on the corresponding IFB pin. As a result, the device deactivates the open IFB pin and removes it from the voltage feedback loop. Afterwards, the output voltage returns to the voltage required for the connected WLED strings. The IFB pin currents of the connected strings remain in regulation during this process.

   If all the LED strings are open, the device repeatedly attempts to restart until the fault is cleared.

3. LED short-across protection using the FBP pin

   If one or several LEDs short in one string, the corresponding IFB pin voltage rises but continues to sink the LED current, causing increased device power dissipation. To protect the device, the TPS61199 provides a programmable LED short-across protection feature with threshold voltage that can be programmed by properly sizing the resistor on the FBP pin (see R5 in *Typical Application*) using Equation 3.

   $$V_{LED\_short} = \frac{R5}{R6} \times 1.229V \quad (3)$$

   If any IFB pin voltage exceeds the threshold (V_{LED_short}), the device turns off the corresponding current sink and removes this IFB pin from the output voltage regulation loop. Current regulation of the remaining IFB pins is not affected.

   If the voltage on all the IFB pins exceed the threshold, the device repeatedly attempts to restart until the fault is cleared.

4. IFB overvoltage protection

Device Functional Modes (continued)

When any of IFB pin reaches the threshold (V_{OVP_IFB}), the device stops switching immediately to protect from damage. The device re-starts when IFB pin voltage falls below the threshold. The time delay depends on how quickly IFB voltage can fall. It is usually determined by the amount of output capacitance and load.

5. Output overvoltage protection using the OVP pin:

   Use a resistor divider to program the clamp threshold voltage as follows:

   (a) Compute the maximum output voltage by multiplying the maximum forward voltage ($V_{FWD(MAX)}$) and number (n) of series LEDs. Add 1V to account for regulation and resistor tolerances and load transients.

$$V_{OUTMAX} = V_{FLED\_MAX} \times \text{Number} + 1V \tag{4}$$

   (b) The recommended bottom feedback resistor (R3 in *Typical Application*) at 10 k. Calculate the top resistor (R2 in *Typical Application*) using Equation 5:

$$R2 = \left(\frac{V_{OUTMAX} + 1V}{2.95V} - 1 \right) \times R3 \tag{5}$$

   When the device detects that the OVP pin exceeds 2.95 V, indicating that the output voltage has exceeded the clamp threshold voltage, the device clamps the output voltage to the set threshold.

   When the OVP pin voltage is higher than 3 V, indicating that the output is higher than the clamp threshold voltage due to transients or high voltage noise spike coupling from external circuits, the device shuts down the boost controller until the output drops below the clamp threshold voltage.

6. Output short-to-ground protection

   When the inductor peak current reaches twice the switch current limit in each switch cycle, the device immediately disables the boost controller until the fault is cleared. This protects the device and external components from damage if the output is shorted to ground.

7. Thermal Protection

   When the device junction temperature is over 150°C, the thermal protection circuit is triggered and shuts down the device immediately. The device automatically restarts when the junction temperature falls back to less than 150°C, with approximate 15°C hysteresis.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61199 is designed for LCD TV backlighting. It is a current-mode boost controller driving up to eight LED strings in parallel. The input voltage range for the device is from 8 V to 30 V. Its switching frequency is programmed by an external resistor from 300 kHz to 800 kHz.

The TPS61199 has a built-in linear regulator, which steps down the input voltage to the VDD voltage for powering the internal circuitry. An internal soft start circuit is implemented to work with an external capacitor to adjust the soft start-up time to minimize the in-rush current during boost converter start-up.

8.2 Typical Application

The TPS61199 is configured as a simple boost converter to drive the single string with the LEDs when the boost ratio of the output voltage to the input voltage is less than 6.

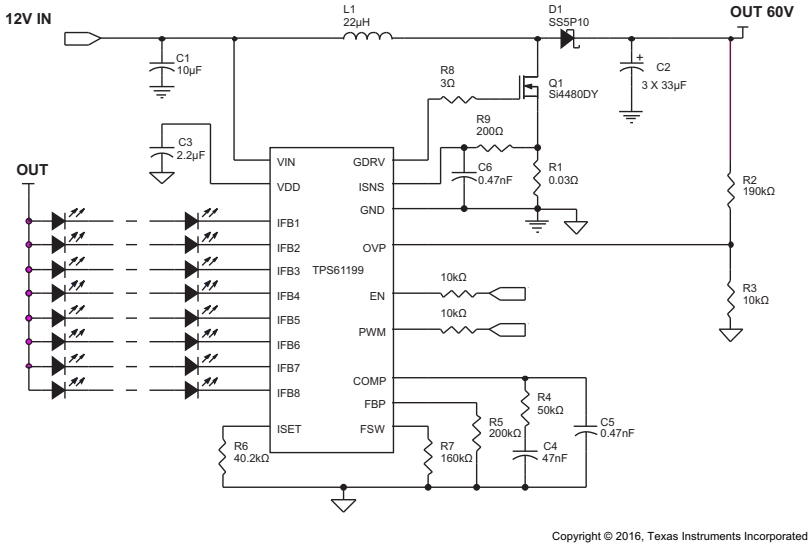


Figure 8. TPS61199 Typical Application

8.2.1 Design Requirements

For typical LED-driver applications, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	8 V to 30 V
Output voltage	60 V
Output current	60 mA
Programmable switching frequency	300 kHz to 800 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection

The TPS61199 is designed to work with inductor values between 10 µH to 47 µH. Running the controller at higher switching frequencies allows the use of smaller and/or lower profile inductors in the 10-µH range. Running the controller at slower switching frequencies requires the use of larger inductors, near 47 µH, to maintain the same inductor current ripple but may improve overall inefficiency due to smaller switching losses. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation. In a boost regulator, the inductor peak current can be calculated with Equation 6 and Equation 7.

$$I_{L_{Peak}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} + \frac{I_{PP}}{2} \quad (6)$$

$$\Delta I_L = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}} \right) \times F_{SW}} \quad (7)$$

where

- V_{OUT} = output voltage
- I_{OUT} = total LED current
- V_{IN} = input voltage
- η = power conversion efficiency, use 85% for TPS61199 applications
- L = inductor value
- F_{SW} = switching frequency

Select an inductor with a saturation current over the calculated peak current. To calculate the worst case inductor peak current, use the minimum input voltage, maximum output voltage, and maximum total LED current. Select an inductor with a saturation current at least 30% higher the calculated peak current to account for load transients when dimming. Table 3 lists the recommended inductors

Table 3. Recommended Value For Inductors

DEVICE	L (µH)	DCR (mΩ)	I_{SAT} (A)	SIZE (L × W × H mm)	MANUFACTURER
CDRH127/HPNP-220M	22	48.8	5.6	12.5 × 12.5 × 8.0	Sumida
SLF12575T- 220M	22	26.3	4	12.5 × 12.5 × 7.5	TDK
#B953AS-220M	22	46	3.6	12.8 × 12.8 × 6.8	TOKO

8.2.2.2 Schottky Diode

The TPS61199 demands a high-speed rectification for optimum efficiency. Ensure that the average and peak current ratings of the diode exceed the output LED current and inductor peak current. In addition, the reverse breakdown voltage of the diode must exceed the application output voltage. Therefore, TI recommends the VISHAY SS5P9.

8.2.2.3 Switch MOSFET and Gate Driver Resistor

The TPS61199 demands a power N-MOSFET (see Q1 in *Typical Application*) as a switch. The voltage and current rating of the MOSFET must be higher than the application output voltage and the inductor peak current. The applications benefits from the addition of a resistor (see R8 in *Typical Application*) connected between the GDRV pin and the gate of the switching MOSFET. With this resistor, the load regulation between LED dimming on and off period and EMI are improved. TI recommends a 3-Ω resistor value. The TPS61199 exhibits lower efficiency when the resistor value is above 3 Ω.

8.2.2.4 Current Sense and Current Sense Filtering

R1 determines the correct overcurrent limit protection. To choose the right value of R1, start with the total system power needed P_{OUT}. Input current Iin = P_{OUT} / (V_{IN} × efficiency). Efficinecy can be estimated from Figure 10. The second step is to calculate the inductor ripple current based on the inductor value L.

$$dIL = V_{IN} \times D / (fs \times L)$$

where

- $D = 1 - V_{IN} / V_{OUT}$ (8)

Thus, the peak current Ipk = Iin + dIL/2. The maximum R1 can now be calculated as

$$R1 = VISNS / Ipk \quad (9)$$

TI recommends adding 20% or more margin to account for component variations.

A small filter placed on the ISNS pin improves performance of the converter (see R9 and C6 in *Typical Application*). The time constant of this filter should be approximately 100 ns. The range of R9 must be from about 100 Ω to 1 kΩ for best results. Locate C6 as close as possible to the ISNS pin to provide noise immunity.

8.2.2.5 Output Capacitor

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability of the whole system. This ripple voltage is related to the capacitance of the capacitor and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$V_{ripple_C} = \frac{D_{MAX} \times I_{OUT}}{F_{SW} \times C_{OUT}}$$

where

- $V_{ripplec}$ is the peak to peak output ripple
- D_{MAX} is the duty cycle of the boost converter.
- D_{MAX} is equal to approximately ($V_{OUT\_MAX} - V_{IN\_MIN}$) / V_{OUT_MAX} in applications. (10)

Care must be taken when evaluating the derating of a capacitor under DC bias. The DC bias can also significantly reduce capacitance. Ceramic device capacitors can loss as much as 50% of its capacitance at its rated voltage. Therefore, leave the margin on the voltage rating to ensure adequate capacitance in the recommendation table.

The ESR impact on the output ripple must be considered as well if tantalum or electrolytic capacitors are used. Assuming there is enough capacitance such that the ripple due to the capacitance can be ignored, the ESR needed to limit the V_{ripple} is:

$$V_{ripple_{ESR}} = I_{L_{Peak}} \times ESR \quad (11)$$

Ripple current flowing through the ESR of a capacitor causes power dissipation in the capacitor. This power dissipation causes a temperature increase internal to the capacitor. Excessive temperature can seriously shorten the expected life of a capacitor. Capacitors have ripple current ratings that are dependent on ambient temperature and must not be exceeded. Therefore, three electrolytic capacitors (UPW2A330MPD6, Nichicon) in parallel reduces the total ESR, shown as in *Typical Application*.

In a typical application, the output requires a capacitor in the range of 10 µF to 100 µF. The output capacitor affects the small signal control loop stability of the boost converter. If the output capacitor is below the range, the boost regulator may potentially become unstable.

8.2.2.6 Loop Consideration

The COMP pin on the TPS61199 is used for external compensation, allowing the loop response to be optimized for each application. The COMP pin is the output of the internal transconductance amplifier. The external resistor R4, along with ceramic capacitors C4 and C5, are connected to the COMP pin to provide poles and zero. The poles and zero, along with the inherent pole and zero in a peak current mode control boost converter, determine the closed loop frequency response. This is important to converter stability and transient response. For most of the applications, the recommended values of 10 kΩ for R4, 100 nF for C4 and 470 pF for C5 are sufficient. For applications with different components or requirements, see *Description Compensating the Current Mode Boost Control Loop* for guidance on selecting different compensation components.

8.2.3 Application Curves

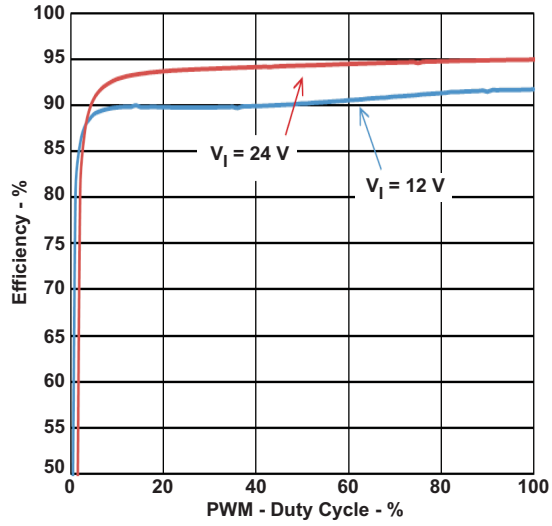


Figure 9. Dimming Efficiency

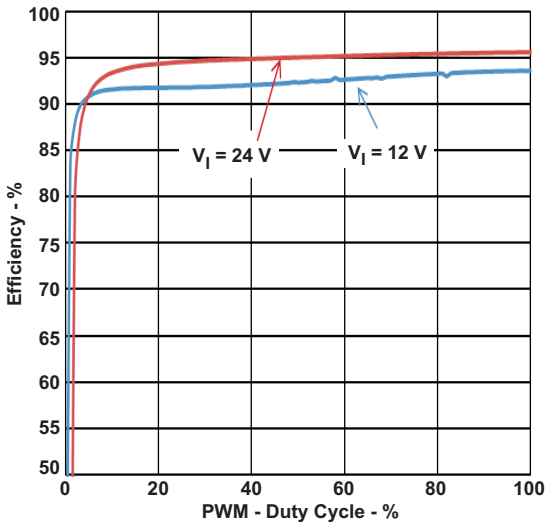


Figure 10. Dimming Efficiency

8.2.4 Additional Application Circuits

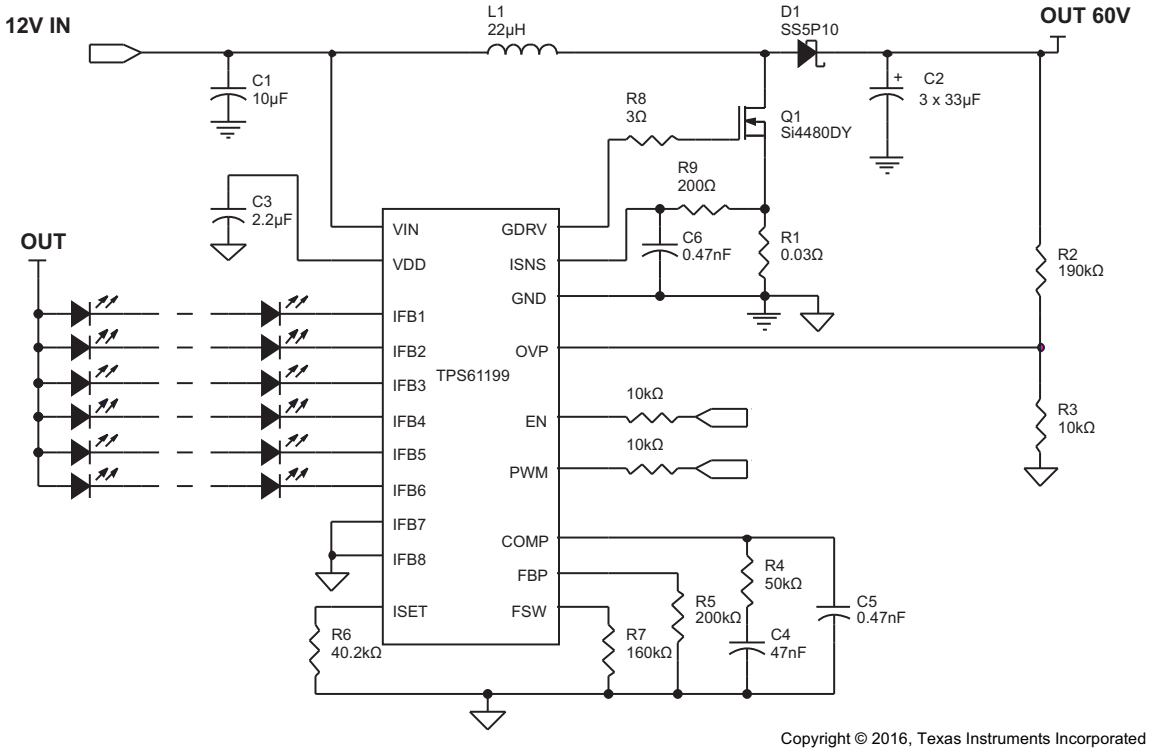


Figure 11. Six LED Strings Application

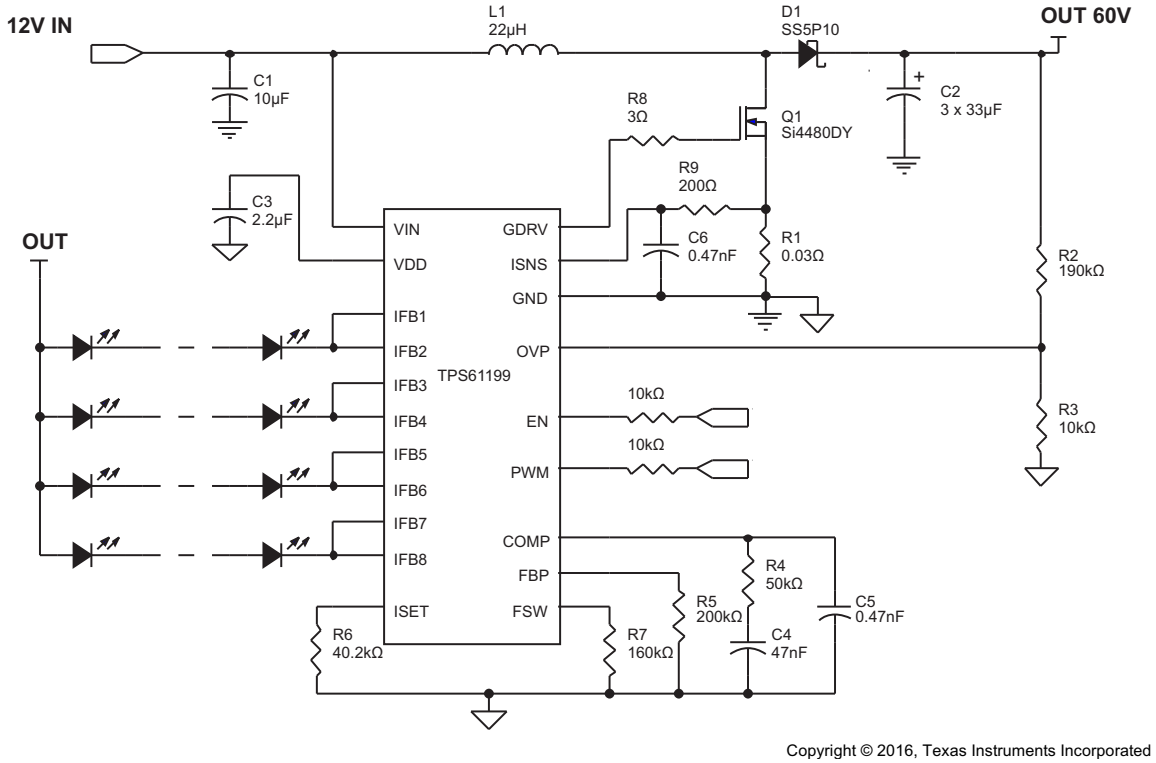


Figure 12. Four LED Strings With 130-mA Current Application

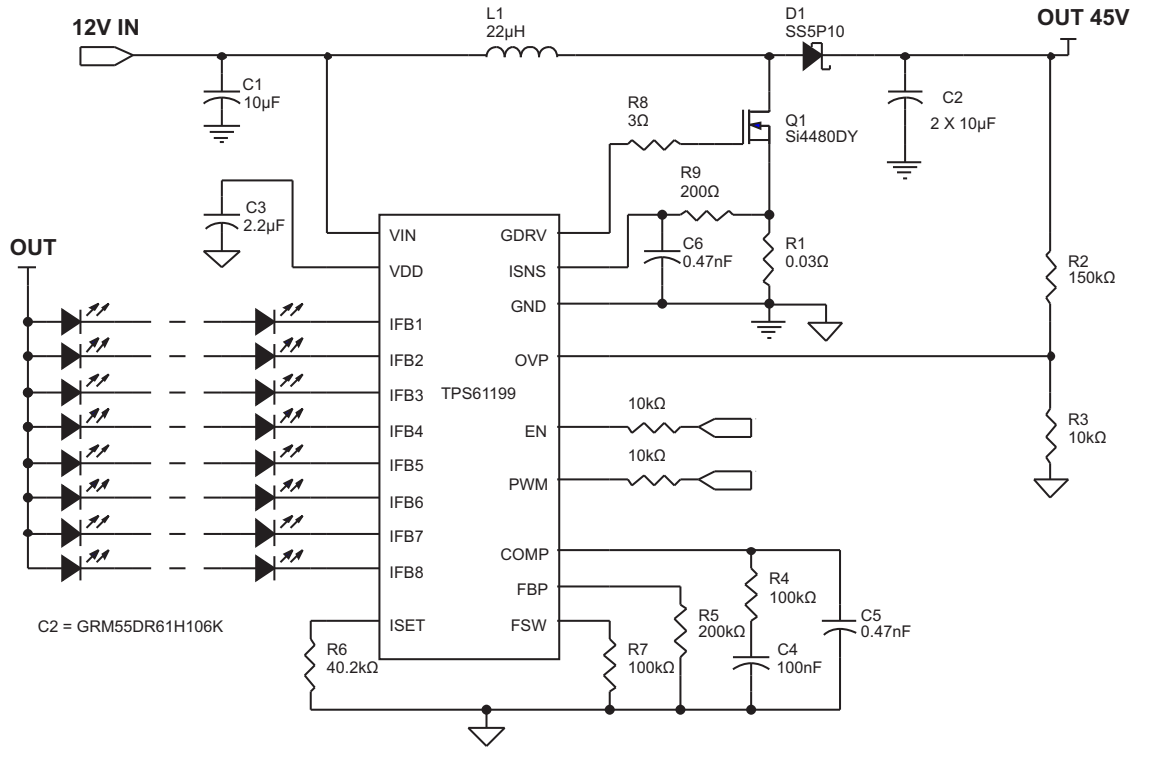


Figure 13. 112-LED Driver Application With Ceramic Output Capacitor

9 Power Supply Recommendations

The TPS61199 requires a single-supply input voltage. This voltage can range from 8 V to 30 V and be able to supply enough current for a given application.

10 Layout

10.1 Layout Consideration

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The VDD capacitor, C3 (see *Typical Application*) is the filter and noise decoupling capacitor for the internal linear regulator powering the internal digital circuits. Place C3 as close as possible between the VDD and GND pins to prevent any noise insertion to digital circuits. The switch node at the drain of Q1 carries high current with fast rising and falling edges. Therefore, the connection between this node to the inductor and the Schottky diode must be kept as short and wide as possible. It is also beneficial to have the ground of the output capacitor C2 close to the GND pin since there is large ground return current flowing between them. When laying out signal grounds, TI recommends using short traces separate from power ground traces, connecting them together at a single point, for example on the thermal pad in the PWP package. Resistors R5, R6, and R7 in *Typical Application* are LED short-protection threshold current setting and switching frequency programming resistors. To avoid unexpected noise coupling into the pins and affecting the accuracy, these resistors must be close to the pins with short and wide traces to GND. In the PWP package, the thermal pad must be soldered onto the PCB and connected to the GND pin of the device. Additional thermal via can significantly improve power dissipation of the device.

10.2 Layout Example

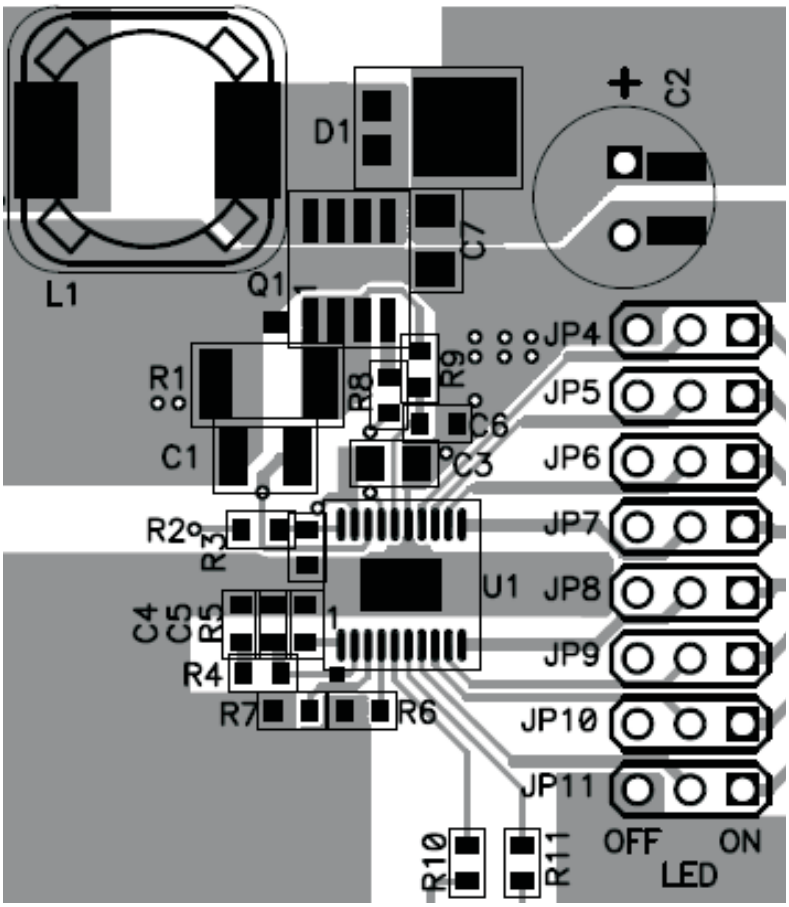


Figure 14. Recommended TPS61199 PCB Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Related Documentation

For additional information, see the following:

Description Compensating the Current Mode Boost Control Loop

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61199NSR	ACTIVE	SOP	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS61199	Samples
TPS61199PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS61199	Samples
TPS61199PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS61199	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

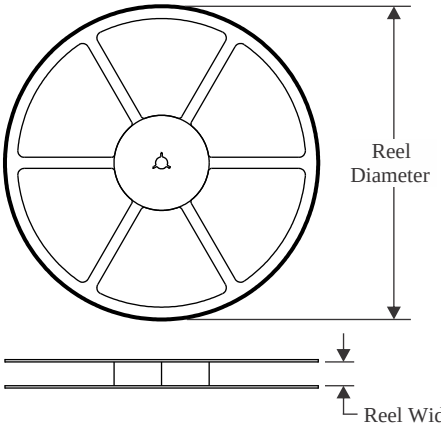
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

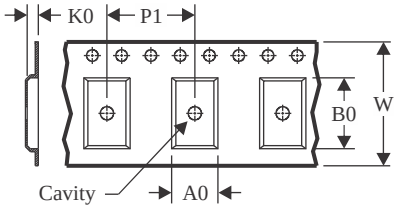
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

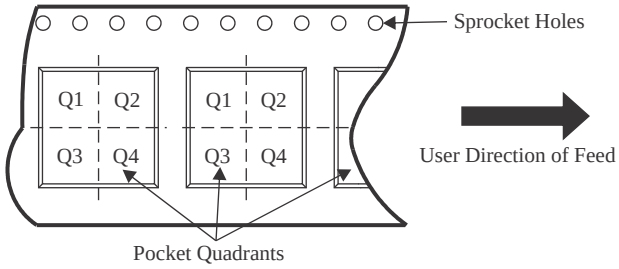


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

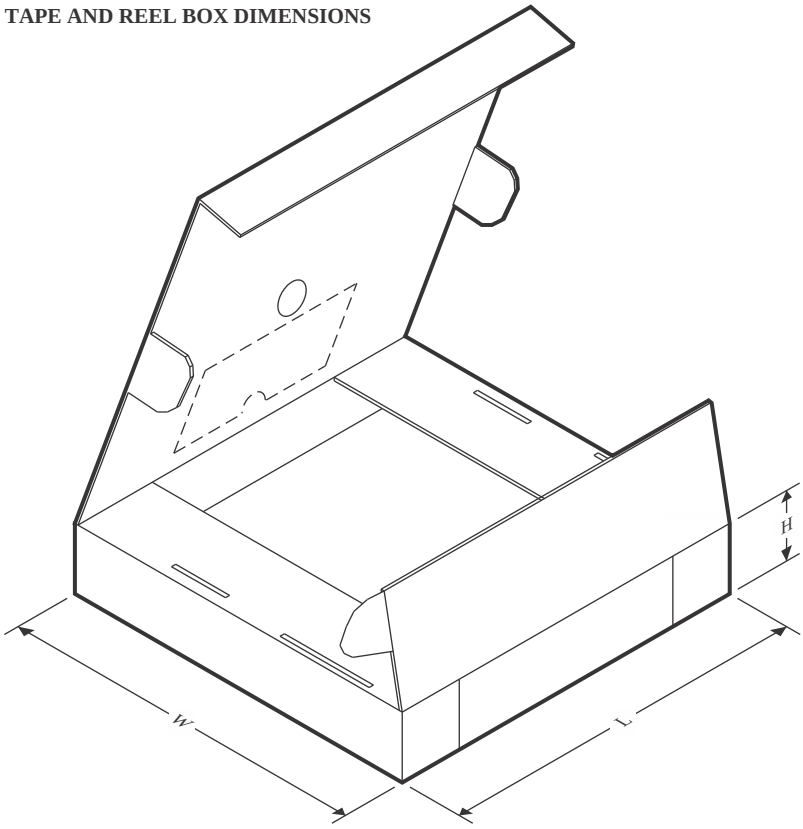
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61199NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
TPS61199PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

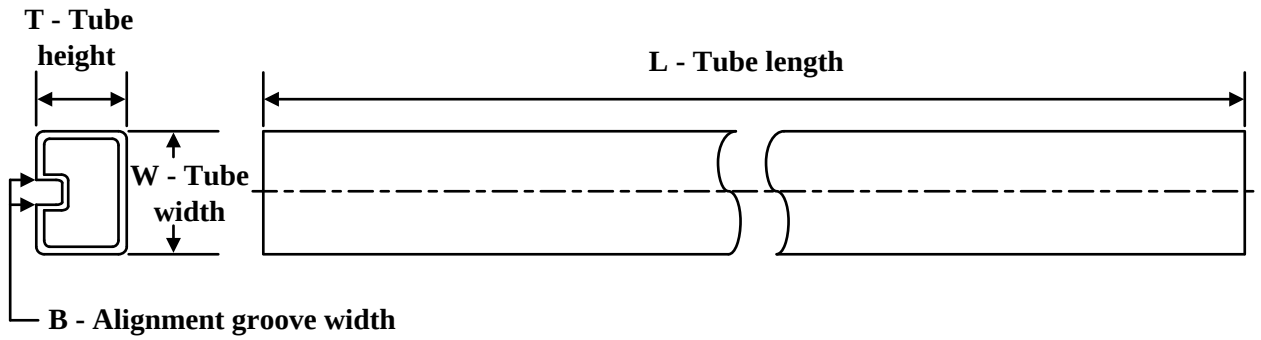
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61199NSR	SOP	NS	20	2000	367.0	367.0	45.0
TPS61199PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

TUBE



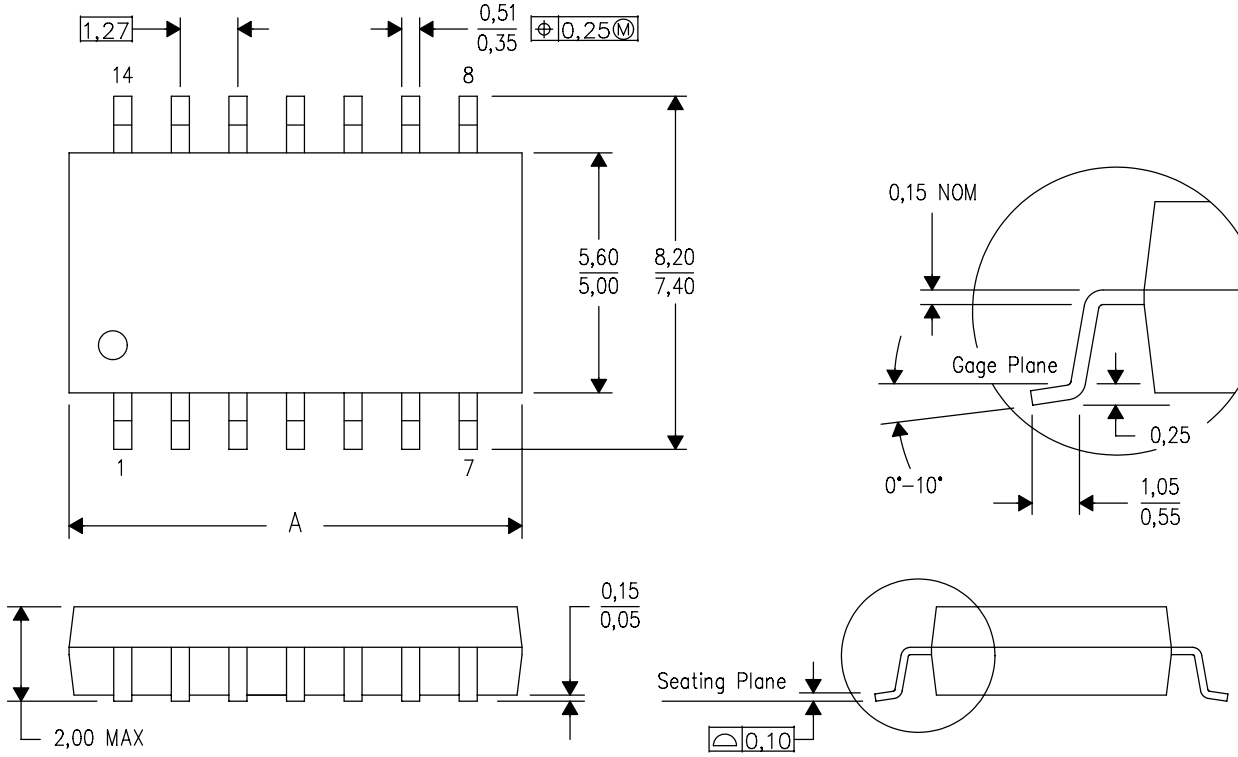
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS61199PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

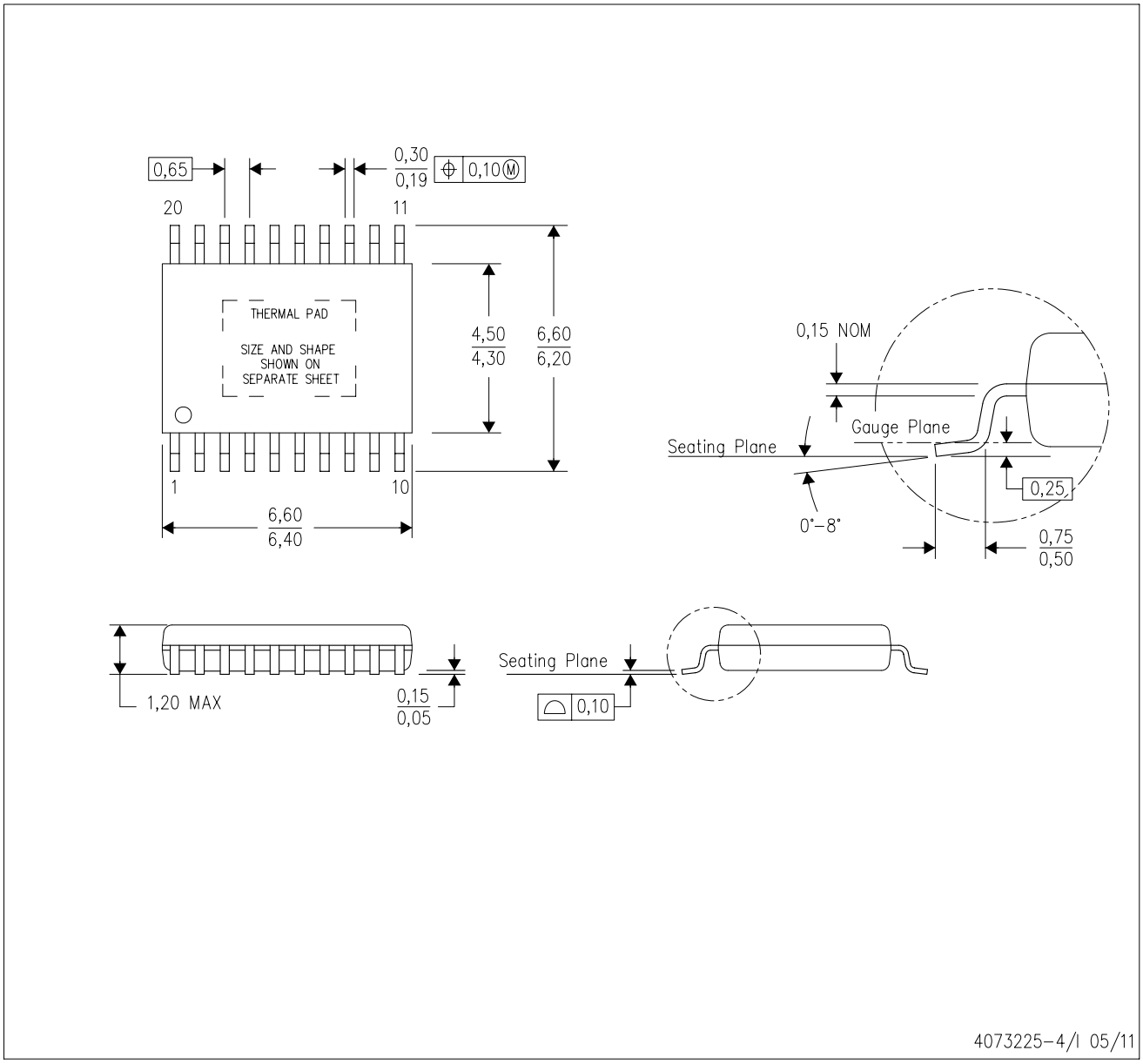


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

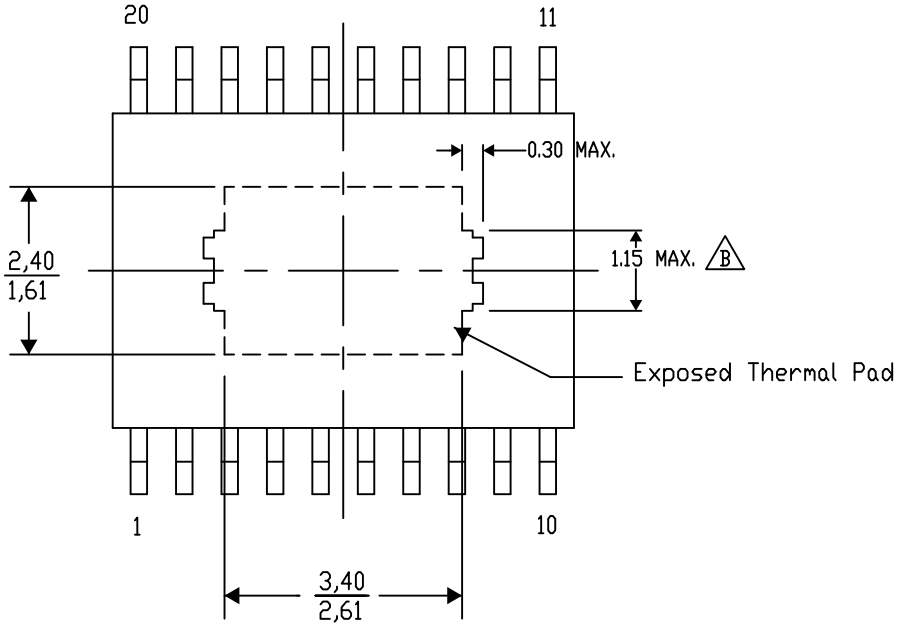
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

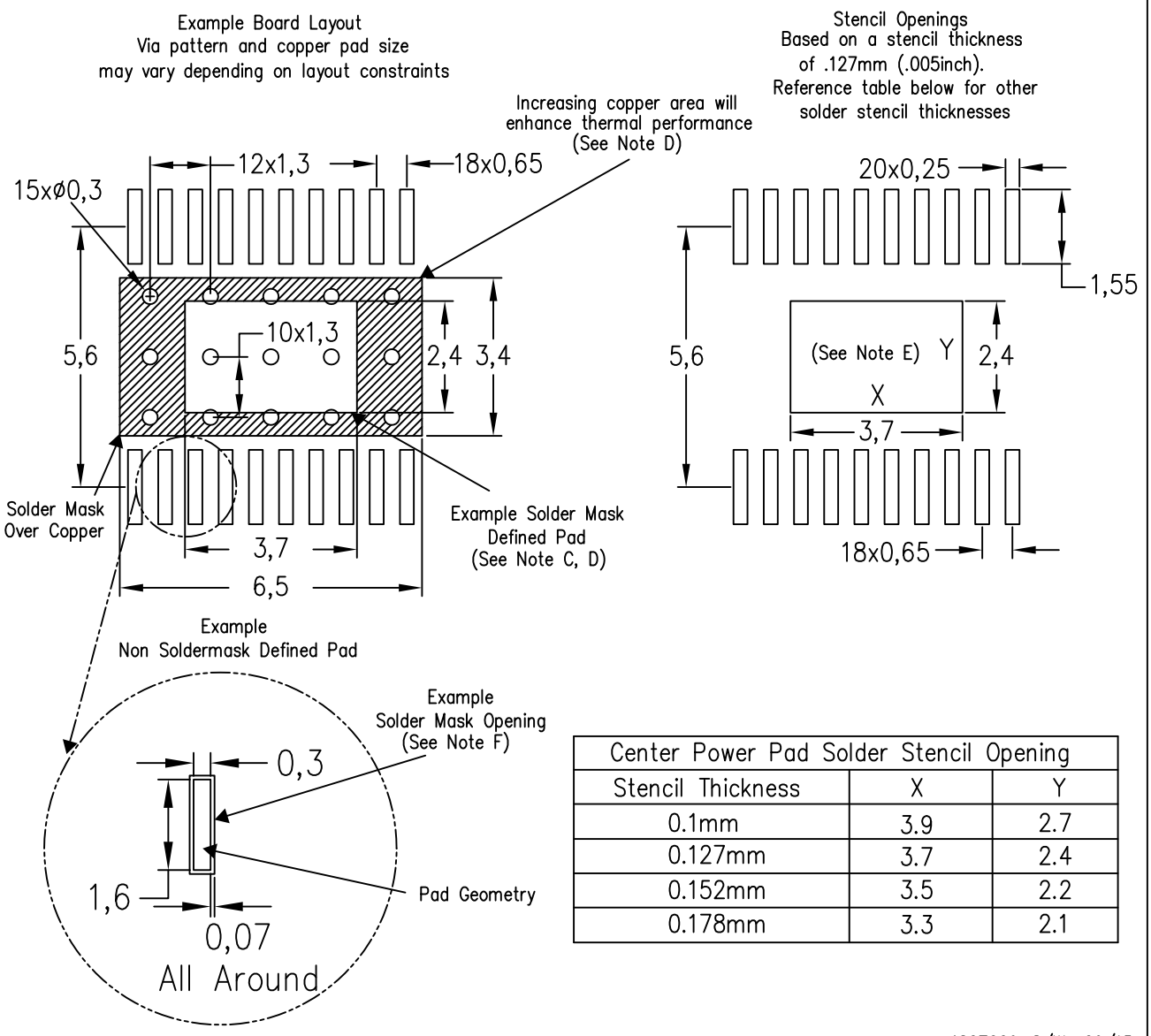
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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