TPS62441-Q1, TPS62442-Q1
SLUSDN9B – NOVEMBER 2021 – REVISED JULY 2022

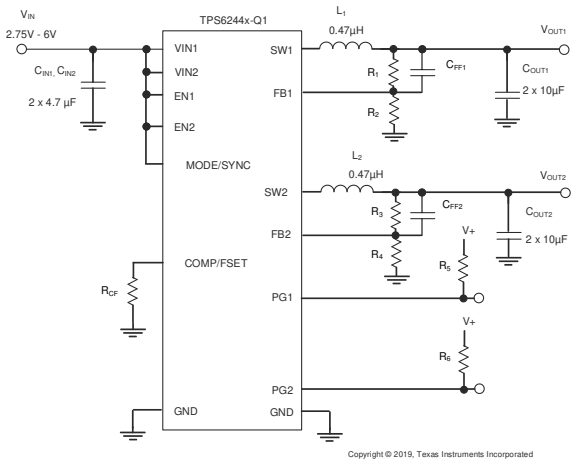
TPS6244x-Q1 2.75-V to 6-V Dual Step-Down Converter with Adjustable Frequency in a QFN Package

1 Features

- AEC-Q100-qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Input voltage range: 2.75 V to 6 V
- Dual-channel output, output voltage from 0.6 V to 5.5 V
- Output voltage accuracy ±1% (PWM operation)
- Forced PWM or PWM and PFM operation
- Adjustable switching frequency of 1.8 MHz to 4 MHz
- Two precise ENABLE inputs allow:
  - User-defined undervoltage lockout
  - Exact sequencing
- Two power-good outputs with window comparator
- 180° phase shifted operation
- 100% duty cycle mode
- Active output discharge
- Optional spread spectrum clocking
- Optional foldback overcurrent protection
- T_J = –40°C to +150°C
- 2.3-mm × 2.7-mm QFN package with wettable flanks

2 Applications

- ADAS camera and ADAS sensor fusion
- Surround view ECU
- Hybrid and reconfigurable cluster
- Infotainment head unit and digital cockpit
- Telematics control unit



Schematic

3 Description

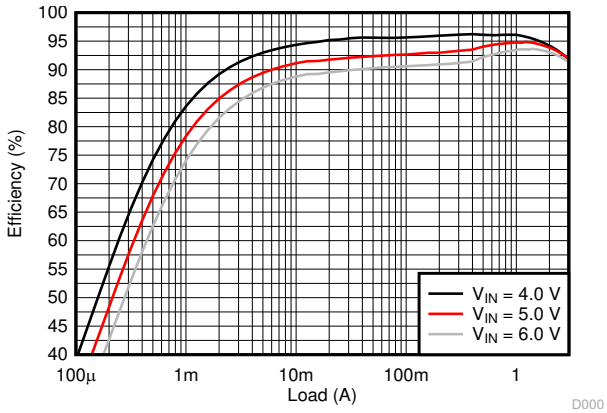
The TPS6244x-Q1 is a family of pin-to-pin dual 1-A, dual 2-A or 3-A, and 1-A high-efficiency and easy-to-use synchronous step-down DC/DC converters. They are based on a peak current mode control topology. The devices are designed for automotive applications such as infotainment and advanced driver assistance systems. Low resistive switches allow up to 3-A continuous output current and a total maximum output current up to 4 A at high ambient temperature. The switching frequency is externally adjustable from 1.8 MHz to 4 MHz and can also be synchronized to an external clock from 2 MHz to 4 MHz. In PWM and PFM mode, the TPS6244x-Q1 automatically enters power save mode at light loads to maintain high efficiency across the whole load range. The TPS6244x-Q1 provides a 1% output voltage accuracy in PWM mode, which helps design a power supply with high output voltage accuracy.

The TPS6244x-Q1 is available as an adjustable voltage version, packaged in a VQFN package.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS62441-Q1	VQFN-HR	2.30 mm × 2.70 mm
TPS62442-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Efficiency vs Output Current, V_{OUT} = 3.3 V, PWM and PFM, f_{SW} = 2.25 MHz

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2022) to Revision B (July 2022)	Page
• Removed preview note	3

Changes from Revision * (November 2021) to Revision A (June 2022)	Page
• Changed document status from Advance Information to Production Data	1

5 Device Comparison Table

Device Number	Features	Foldback Current Limit	Output Voltage
TPS62441QWRQRRQ1	2 × 1-A output current V_{OUT} discharge	OFF	Adjustable
TPS62442QWRQRRQ1	2 × 2-A or 3-A and 1-A output current V_{OUT} discharge	OFF	Adjustable

6 Pin Configuration and Functions

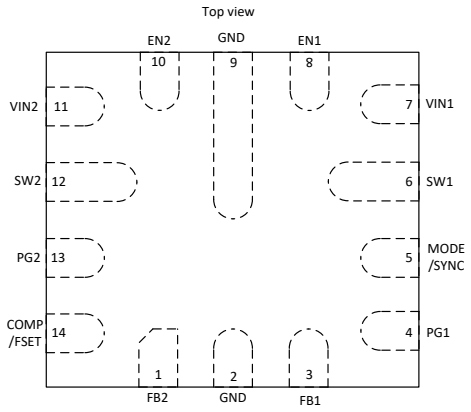


Figure 6-1. 14-Pin VQFN-HR RQR Package

Table 6-1. Pin Functions

Pin		Type(1)	Description
Name	NO.		
EN1	8	I	This pin is the enable pin of converter 1. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
EN2	10	I	This pin is the enable pin of converter 2. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
FB1	3	I	Voltage feedback input for converter 1. Connect the resistive output voltage divider to this pin.
FB2	1	I	Voltage feedback input for converter 2. Connect the resistive output voltage divider to this pin.
PG1	4	O	Open-drain power-good output of converter 1
PG2	13	O	Open-drain power-good output of converter 2
SW1	6		This pin is the switch pin of converter 1 and is connected to the internal power MOSFETs.
SW2	12		This pin is the switch pin of converter 2 and is connected to the internal power MOSFETs.
MODE/SYNC	5	I	The device runs in PFM and PWM mode when this pin is pulled low. When the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected. The mode pin can also be used to synchronize the device to an external frequency. See the electrical characteristics for the detailed specification for the digital signal applied to this pin for external synchronization.
COMP/FSET	14	I	Device compensation and frequency set input. A resistor from this pin to GND defines the compensation of the control loop as well as the switching frequency if not externally synchronized. Do not leave this pin floating.
VIN1	7	—	Power supply input. Make sure the input capacitor is connected as close as possible between pin VIN1 and GND. Connect VIN1 to VIN2.
VIN2	11	—	Power supply input. Make sure the input capacitor is connected as close as possible between pin VIN2 and GND. Connect VIN2 to VIN1.
GND	2, 9	—	Ground pins. The GND pins are internally connected.

(1) I = input; O = output

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN1, VIN2	–0.3	6.5	V
	SW1, SW2 (DC)	–0.3	V_{IN} + 0.3	
	SW1, SW2 (AC, less than 10 ns)(3)	–3	10	
	FB1, FB2	–0.3	4	
	PG1, PG2, COMP/FSET	–0.3	V_{IN} + 0.3	
	EN1, EN2, MODE/SYNC	– .3	6.5	
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground pin.
(3) While switching

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C6	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN1}, V_{IN2}	Input voltage range	2.75		6	V
V_{OUT1}, V_{OUT2}	Output voltage range	0.6		5.5	V
L_1, L_2	Effective inductance	0.32	0.47	0.9	µH
C_{OUT1}, C_{OUT2}	Effective output capacitance(1)	8	10	200	µF
C_{IN1}, C_{IN2}	Effective input capacitance on each pin(1)		10		µF
R_{CF}		4.5		100	kΩ
I_{SINK_PG}	Sink current at PG pin	0		2	mA
T_J	Junction temperature	–40		150	°C

(1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer's DC bias curves for the effective capacitance versus DC voltage applied. Further restrictions can apply. Please see the feature description for COMP/FSET for the output capacitance versus compensation setting and output voltage.

7.4 Thermal Information

THERMAL METRIC[1]		(JEDEC)	(EVM)	UNIT
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.7	53.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.8	n/a	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.1	n/a	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.5	1.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.9	20.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Over operating junction temperature range (T_J = –40°C to +150°C) and V_{IN} = 2.75 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN1 or EN2 = V_{IN}, no load, device is not switching, T_J = 25°C, MODE = GND, one converter enabled			27	µA
I_Q	Quiescent current	EN1 or EN2 = V_{IN}, no load, device is not switching, MODE = GND, one converter enabled		22	66	µA
I_Q	Quiescent current	EN1 = EN2 = V_{IN}, no load, device is not switching, T_J = 25°C, MODE = GND, both converters enabled			38	µA
I_Q	Quiescent current	EN1 = EN2 = V_{IN}, no load, device is not switching, MODE = GND, both converters enabled		33	80	µA
I_{SD}	Shutdown current	EN1 = EN2 = low, at T_J = 25°C			2	µA
I_{SD}	Shutdown current	EN1 = EN2 = GND, nominal value at T_J = 25°C, maximum value at T_J = 150°C		1.5	26	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} rising	2.5	2.6	2.75	V
		V_{IN} falling	2.3	2.5	2.6	V
T_{JSD}	Thermal shutdown threshold	T_J rising		170		°C
	Thermal shutdown hysteresis	T_J falling		15		°C
CONTROL AND INTERFACE						
$V_{EN,IH}$	Input-threshold voltage at EN1, EN2, rising edge		1.06	1.1	1.15	V
$V_{EN,IL}$	Input-threshold voltage at EN1, EN2, falling edge		0.96	1.0	1.05	V
$I_{EN,LKG}$	Input leakage current into EN1, EN2	V_{IH} = V_{IN} or V_{IL} = GND			450	nA
V_{IH}	High-level input-threshold voltage at MODE/SYNC		1.1			V
V_{IL}	Low-level input-threshold voltage at MODE/SYNC				0.3	V
I_{LKG}	Input leakage current into MODE/SYNC				700	nA
t_{Delay}	Enable delay time	Time from ENx high to device starts switching, V_{IN} applied already	110	200	300	µs
t_{Delay}	Enable delay time if one converter already enabled	Time from ENx high to device starts switching, V_{IN} applied already		100		µs

7.5 Electrical Characteristics (continued)

Over operating junction temperature range (T_J = –40°C to +150°C) and V_{IN} = 2.75 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{Ramp}	Output voltage ramp time	Time from device starts switching to power good; the device is not in current limit	0.7	1.1	1.5	ms
f_{SYNC}	Frequency range on MODE/SYNC pin for synchronization		2		4	MHz
	Resistance from COMP/FSET to GND for logic low	Internal frequency setting with f = 2.25 MHz	0		2.5	kΩ
	Voltage on COMP/FSET for logic high	Internal frequency setting with f = 2.25 MHz		V_{IN}		V
V_{TH_PG}	UVP power-good threshold voltage; DC level	Rising (%V_{FB})	94%	96.5%	99%	
V_{TH_PG}	UVP power-good threshold voltage; DC level	Falling (%V_{FB})	92%	94.5%	97%	
V_{TH_PG}	OVP power-good threshold voltage; DC level	Rising (%V_{FB})	104%	107%	110%	
	OVP power-good threshold voltage; DC level	Falling (%V_{FB})	102%	104.5%	107%	
$V_{PG,OL}$	Low-level output voltage at PG	I_{SINK_PG} = 2 mA		0.07	0.3	V
$I_{PG,LKG}$	Input leakage current into PG	V_{PG} = 5 V			100	nA
t_{PG}	PG deglitch time	For a high-level to low-level transition on the power-good output		40		µs
OUTPUT						
V_{FB1}, V_{FB2}	Feedback voltage			0.6		V
$I_{FB1,LKG}$, $I_{FB2,LKG}$	Input leakage current into FB	V_{FB} = 0.6 V		1	80	nA
V_{FB1}, V_{FB2}	Feedback voltage accuracy	PWM, $V_{IN} \geq V_{OUT}$ + 1 V	–1%		1%	
V_{FB1}, V_{FB2}	Feedback voltage accuracy	PFM, $V_{IN} \geq V_{OUT}$ + 1 V, $V_{OUT} \geq$ 1.5 V, $C_{o,eff} \geq$ 22 µF, L = 0.47 µH	–1%		2.5%	
V_{FB1}, V_{FB2}	Feedback voltage accuracy	PFM, $V_{IN} \geq V_{OUT}$ + 1 V, 1 V ≤ V_{OUT} < 1.5 V, $C_{o,eff} \geq$ 47 µF, L = 0.47 µH	–1%		2.5%	
	Load regulation	PWM		0.05		%/A
	Line regulation	PWM, I_{OUT} = 1 A, $V_{IN} \geq V_{OUT}$ + 1 V		0.02		%/V
R_{DIS}	Output discharge resistance			50	150	Ω
f_{SW}	PWM switching frequency range	See the FSET pin functionality about setting the switching frequency.	1.8	2.25	4	MHz
f_{SW}	PWM switching frequency	With COMP/FSET tied to GND or V_{IN}	2.025	2.25	2.475	MHz
f_{SW}	PWM switching frequency tolerance	Using a resistor from COMP/FSET to GND	–16%		17%	
$t_{on,min}$	Minimum on time of high-side FET	$V_{IN} \geq$ 3.3 V		50	75	ns
$t_{on,min}$	Minimum on time of low-side FET			30		ns
$R_{DS(ON)}$	High-side FET on-resistance	$V_{IN} \geq$ 5 V		55	100	mΩ
	Low-side FET on-resistance	$V_{IN} \geq$ 5 V		25	50	mΩ
	High-side MOSFET leakage current	V_{IN} = 6 V; $V_{(SW)}$ = 0 V		1	86	µA
	Low-side MOSFET leakage current	$V_{(SW)}$ = 6 V		1	205	µA
I_{LIMH}	High-side FET switch current limit	DC value, for the TPS62442; V_{IN} = 3 V to 6 V	3.8	4.7	5.5	A

7.5 Electrical Characteristics (continued)

Over operating junction temperature range (T_J = –40°C to +150°C) and V_{IN} = 2.75 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIMH}	High-side FET switch current limit	DC value, for the TPS62441; V_{IN} = 3 V to 6 V	2.1	2.6	3.1	A
I_{LIMNEG}	Low-side FET negative current limit	DC value		–1.8		A

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
$f_{(SYNC)}$	Synchronization clock frequency range (MODE/SYNC)	Nominal f_{SW} determined through COMP/FSET	f_{SW} + 10%		f_{SW} + 40%	MHz
$D_{(SYNC)}$	Synchronization clock duty cycle range (MODE/SYNC)		45%		55%	

7.7 Typical Characteristics

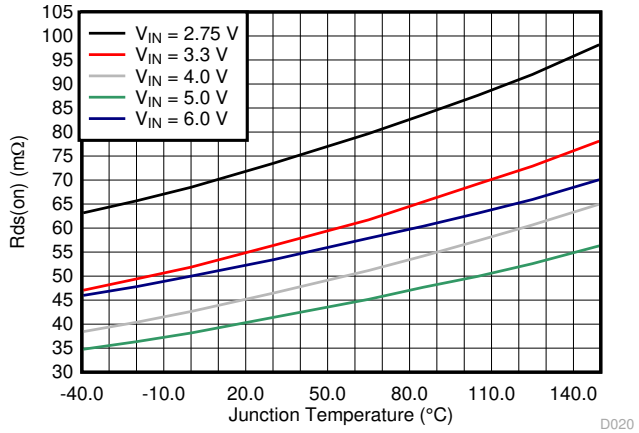


Figure 7-1. $R_{ds(on)}$ of High-Side Switch

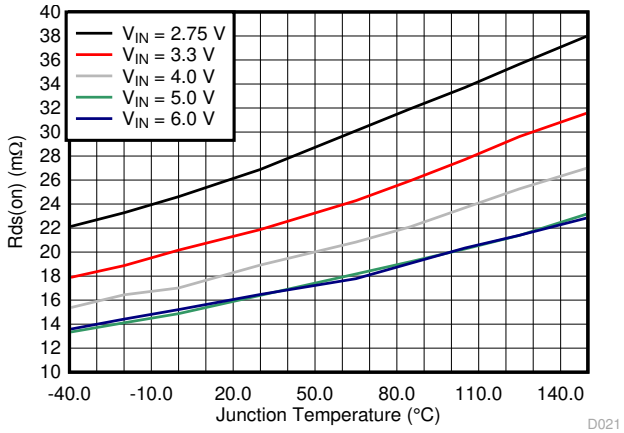


Figure 7-2. $R_{ds(on)}$ of Low-Side Switch

8 Parameter Measurement Information

8.1 Schematic

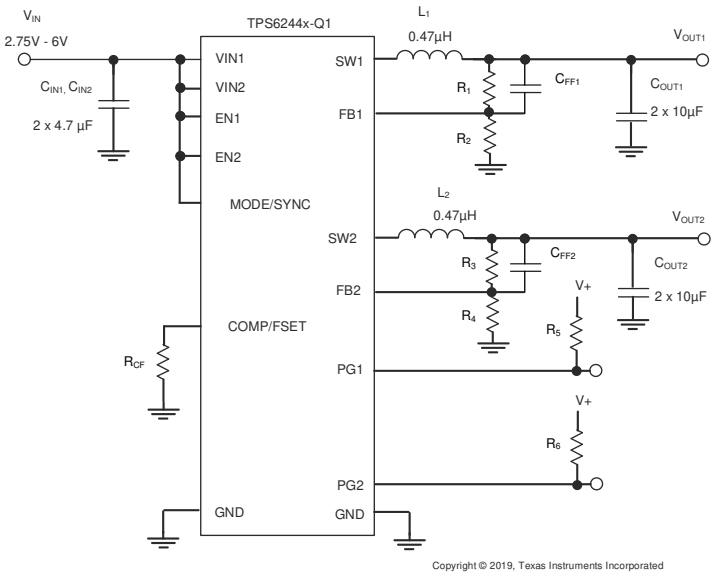


Figure 8-1. Measurement Setup

Table 8-1. List of Components

Reference	Description	Manufacturer(1)
IC	TPS62442QWRQRRQ1	Texas Instruments
L1, L2	2 × 0.47-µH inductor DFE252012PD-R47M-P2	Murata
C_{IN1}, C_{IN2}	2 × 4.7 µF / 6.3 V	Murata
C_{OUT1}, C_{OUT2}	2 × 10 µF / 6.3 V	Murata
R_{CF}	8.06 kΩ	Any
C_{FF1}, C_{FF2}	10 pF	Any
R_1	Depending on V_{OUT}	Any
R_2	Depending on V_{OUT}	Any
R_3	Depending on V_{OUT}	Any
R_4	Depending on V_{OUT}	Any
R_5, R_6	100 kΩ	Any

(1) See the *Third-Party Products Disclaimer*.

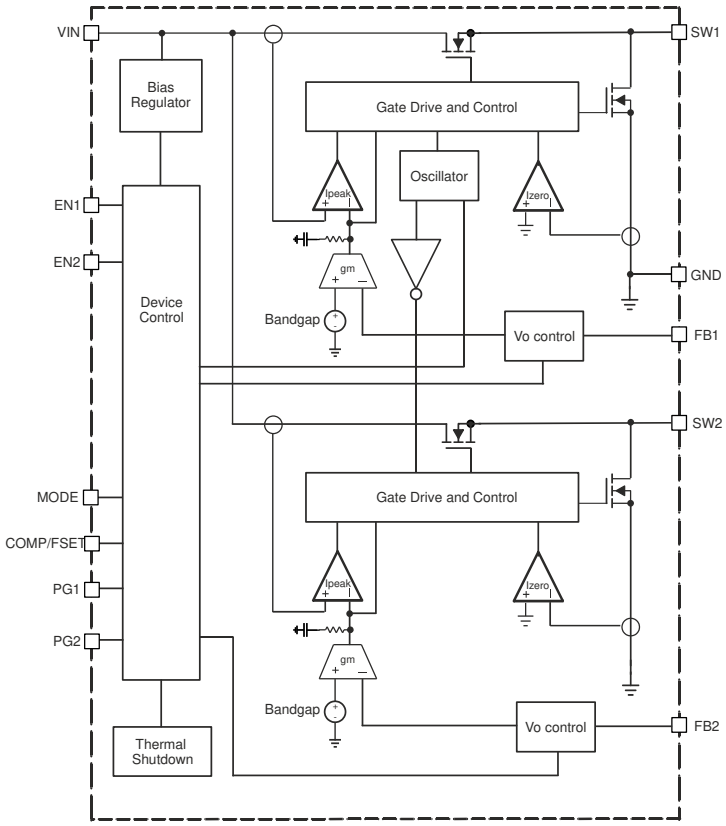
9 Detailed Description

9.1 Overview

The TPS6244x-Q1 synchronous dual switch mode power converters are based on a peak current mode control topology. The control loop is internally compensated. To optimize the bandwidth of the control loop to the wide range of output capacitance that can be used with TPS6244x-Q1, the internal compensation has two settings. See Section 9.3.2. One out of the two compensation settings is chosen either by a resistor from COMP/FSET to GND, or by the logic state of this pin. The regulation network achieves fast and stable operation with small external components and low-ESR ceramic output capacitors. The devices can be operated without a feedforward capacitor on the output voltage divider, however, using a typically 10-pF feedforward capacitor improves transient response.

The devices support forced fixed-frequency PWM operation with the MODE pin tied to a logic high level. The frequency is defined as either 2.25 MHz internally fixed when COMP/FSET is tied to GND or VIN or in a range of 1.8 MHz to 4 MHz defined by a resistor from COMP/FSET to GND. Alternatively, the devices can be synchronized to an external clock signal in a range from 2 MHz to 4 MHz, applied to the MODE pin with no need for additional passive components. External synchronization can only be used when there is a resistor from COMP/FSET to GND. When COMP/FSET is directly tied to GND or VIN, the TPS6244x-Q1 cannot be synchronized externally. The TPS6244x-Q1 allows for a change from internal clock to external clock during operation. When the MODE pin is set to a logic low level, the device operates in power save mode (PFM) at low output current and automatically transfers to fixed frequency PWM mode at higher output current. In PFM mode, the switching frequency decreases linearly based on the load to sustain high efficiency down to very low output current. When a converter switches from PFM to PWM operation, there can be a maximum delay of one clock cycle because in this case, the converter has to synchronize to the other converter to achieve 180 degrees phase shift.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Precise Enable (EN)

The voltage applied at EN1 and EN2 is compared to a 1.1-V fixed threshold for a rising voltage, which allows the user to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The precise enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the input of EN1 and EN2.

The enable input threshold for a falling edge is typically 100 mV lower than the rising edge threshold. The TPS6244x-Q1 starts operation when the rising threshold is exceeded. For proper operation, the enable (EN) pin must be terminated and must not be left floating. Pulling the enable pin low forces the device into shutdown, with a shutdown current of typically 1.5 µA. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off.

The enable delay time is defined from EN1 or EN2 going high to when the converter starts switching. The converter is enabled first, the internal bandgap is started, and bias currents and configuration bits are read, so its start-up delay time is longer than the converter being enabled when this is already done.

9.3.2 COMP/FSET

This pin allows to set three different parameters:

- Internal compensation settings for the control loop (two settings available)
- The switching frequency in PWM mode from 1.8 MHz to 4 MHz
- Enable and disable spread spectrum clocking (SSC)

A resistor from COMP/FSET to GND changes the compensation as well as the switching frequency. The change in compensation allows the user to adopt the device to different values of output capacitance. Place the resistor close to the pin to keep the parasitic capacitance on the pin to a minimum. The compensation setting is sampled at start-up of the converter, so a change in the resistor during operation only has an effect on the switching frequency, but not on the compensation.

To save external components, the pin can also be directly tied to VIN or GND to set a pre-defined setting. Do not leave the pin floating.

The switching frequency has to be selected based on the input voltage and the output voltage to meet the specifications for the minimum on time and minimum off time.

Example: V_{IN} = 5 V, V_{OUT} = 1 V --> duty cycle = 1 V / 5 V = 0.2

- --> $t_{on,min}$ = 1 / fs × 0.2
- --> $f_{sw,max}$ = 1 / $t_{on,min}$ × 0.2 = 1 / 0.075 µs × 0.2 = 2.67 MHz

The compensation range has to be chosen based on the minimum capacitance used. The capacitance can be increased from the minimum value as given in Table 9-1, up to the maximum of 200-µF effective capacitance in both compensation ranges. If the capacitance of an output changes during operation, for example, when load switches are used to connect or disconnect parts of the circuitry, the compensation has to be chosen for the minimum capacitance on the output. With large output capacitance, the compensation must be done based on that large capacitance to get the best load transient response. Compensating for large output capacitance but placing less capacitance on the output can lead to instability.

The switching frequency for the different compensation setting is determined by the following equations.

For compensation (comp) setting 1 with spread spectrum clocking (SSC) disabled:

$$R_{CF}(k\Omega) = \frac{18\ MHz \times k\Omega}{fs(MHz)} - 0.18\ k \quad (1)$$

For compensation (comp) setting 1 with spread spectrum clocking (SSC) enabled:

$$R_{CF}(k\Omega) = \frac{60\ MHz \times k\Omega}{fs(MHz)} - 0.6\ k \quad (2)$$

For compensation (comp) setting 2 with spread spectrum clocking (SSC) disabled:

$$R_{CF}(k\Omega) = \frac{180\ MHz \times k\Omega}{fs(MHz)} - 1.8\ k \quad (3)$$

Table 9-1. Switching Frequency, Compensation, and Spread Spectrum Clocking

R_{CF}	Compensation	Switching Frequency	Minimum Output Capacitance For V_{OUT} < 1 V	Minimum Output Capacitance For V_{OUT} < 3.3 V	Minimum Output Capacitance For V_{OUT} ≥ 3.3 V
10 kΩ .. 4.5 kΩ	for smallest output capacitance (comp setting 1) SSC disabled	1.8 MHz (10 kΩ) .. 4 MHz (4.5 kΩ) according to Equation 1	11 µF	7 µF	5 µF
33 kΩ .. 18 kΩ	for smallest output capacitance (comp setting 1) SSC enabled	1.8 MHz (33 kΩ) .. 4 MHz (18 kΩ) according to Equation 2	11 µF	7 µF	5 µF
100 kΩ .. 45 kΩ	for best transient response (larger output capacitance) (comp setting 2) SSC disabled	1.8MHz (100 kΩ) ..4 MHz (45 kΩ) according to Equation 3	30 µF	18 µF	15 µF
tied to GND	for smallest output capacitance (comp setting 1) SSC disabled	internally fixed 2.25 MHz	11 µF	7 µF	5 µF
tied to V_{IN}	for best transient response (larger output capacitance) (comp setting 2) SSC enabled	internally fixed 2.25 MHz	30 µF	18 µF	15 µF

Refer to Section 10.1.2.2.2 for further details on the output capacitance required depending on the output voltage.

A too-high resistor value for R_{CF} is decoded as "tied to V_{IN}," a value below the lowest range as "tied to GND." The minimum output capacitance in Table 9-1 is for capacitors close to the output of the device. If the capacitance is distributed, a lower compensation setting can be required.

9.3.3 MODE/SYNC

When MODE/SYNC is set low, the device operates in PWM or PFM mode, depending on the output current. The MODE/SYNC pin allows the user to force PWM mode when set high. The pin also allows the user to apply an external clock in a frequency range from 2 MHz to 4 MHz for external synchronization. Similar to COMP/FSET, the specifications for the minimum on time and minimum off time have to be observed when setting the external frequency. The external synchronization frequency applied on the MODE/SYNC pin must be 10% to 40% higher than the nominal internal switching frequency set by R_{CF} (calculated with Equation 1 to Equation 3). Ensuring this makes sure that, if the external clock fails, the converter can continue normal operation with the internal switching frequency in a range where the compensation settings are still valid. When there is no resistor from COMP/FSET to GND but the pin is pulled high or low, external synchronization is not possible. If the device is externally synchronized, both converters are forced to run on that clock frequency preserving 180° phase relation. The internally generated spread spectrum clocking is turned off while running on an external clock.

9.3.4 Spread Spectrum Clocking (SSC)

The device offers spread spectrum clocking as an option. When SSC is enabled, the switching frequency is modulated in a triangular manner when in PWM mode using the internal clock. The frequency variation is typically between the nominal switching frequency and up to 20% above the nominal switching frequency set

by R_{CF}. When the device is externally synchronized by applying a clock signal to the MODE/SYNC pin, the TPS6244x-Q1 follows the external clock and the internal spread spectrum block is turned off. SSC is also disabled during soft start and PFM mode.

9.3.5 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the power FETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage trips below the threshold for a falling supply voltage.

9.3.6 Power-Good Output (PG)

Power good is an open-drain output driven by a window comparator. PG is held low when the device is:

- Disabled
- In undervoltage lockout
- In thermal shutdown
- In soft start

When the output voltage is in regulation hence, within the window defined in the electrical characteristics, the output is high impedance.

Table 9-2. PG Status

EN	Device Status	PG State
X	V_{IN} < 2 V	undefined
low	V_{IN} ≥ 2 V	low
high	2 V ≤ V_{IN} ≤ UVLO OR in thermal shutdown OR V_{OUT} is not in regulation OR device in soft start	low
high	V_{OUT} in regulation	high impedance

9.3.7 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 170°C (typical), the device goes into thermal shutdown. Both the high-side and low-side power FETs of both converters are turned off and PG goes low. When T_J decreases below the hysteresis amount of typically 20°C, the converters resume normal operation, beginning with soft start. When both converters are in a PFM pause, the thermal shutdown is not active. After the PFM pause, the device needs up to 9 µs to detect a too high junction temperature. If the PFM burst is shorter than this delay, the device does not detect a too high junction temperature. As long as one converter is in PWM, thermal shutdown is always active.

9.4 Device Functional Modes

9.4.1 Pulse Width Modulation (PWM) Operation

The TPS6244x-Q1 has two operating modes. Forced PWM mode is discussed in this section and PWM and PFM as discussed in Section 9.4.2.

With the MODE/SYNC pin set to high, the TPS6244x-Q1 operates with pulse width modulation in continuous conduction mode (CCM). The switching frequency is either defined by a resistor from the COMP pin to GND or by an external clock signal applied to the MODE/SYNC pin. With an external clock applied to MODE/SYNC, the TPS6244x-Q1 follows the frequency applied to the pin. The frequency needs to be in a range the device can operate at, taking the minimum on time into account.

9.4.2 Power Save Mode Operation (PWM and PFM)

When the MODE/SYNC pin is low, power save mode is allowed. The device operates in PWM mode as long as the peak inductor current is above the PFM threshold of approximately 0.8 A. When the peak inductor current drops below the PFM threshold, the device starts to skip switching pulses. In power save mode, the switching frequency decreases with the load current maintaining high efficiency.

9.4.3 100% Duty-Cycle Operation

The duty cycle of a buck converter operated in PWM mode is given as D = V_{OUT} / V_{IN}. The duty cycle increases as the input voltage comes close to the output voltage and the off time gets smaller. When the minimum off time of 30 ns (typical) is reached, the TPS6244x-Q1 skips switching cycles while it approaches 100% mode. In 100% mode, the device keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the target. In 100% mode, the low-side switch is turned off. The maximum dropout voltage in 100% mode is the product of the on-resistance of the high-side switch plus the series resistance of the inductor and the load current.

9.4.4 Current Limit and Short Circuit Protection

The TPS6244x-Q1 is protected against overload and short circuit events. The converter is not switching with the fixed frequency when in current limit. The converter resumes the fixed-frequency operation when the converter leaves current limit condition. If the inductor current exceeds the current limit, I_{LIMH}, the high-side switch is turned off and the low-side switch is turned on to ramp down the inductor current. The high-side switch turns on again only if the current in the low-side switch has decreased below the low-side current limit, which can cause bursts or single pulses between the high-side and low-side current limit. Due to internal propagation delay, the actual current can exceed the static current limit. The dynamic current limit is given as:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_L}{L} \cdot t_{PD} \tag{4}$$

where

- I_{LIMH} is the static current limit as specified in the electrical characteristics.
- L is the effective inductance at the peak current.
- V_L is the voltage across the inductor (V_{IN} – V_{OUT}).
- t_{PD} is the internal propagation delay of typically 50 ns.

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_{IN} - V_{OUT}}{L} \cdot 50ns \tag{5}$$

9.4.5 Foldback Current Limit and Short Circuit Protection

Foldback current limit and short circuit protection are valid for devices where foldback current limit is enabled.

When the TPS6244x-Q1 detects current limit for more than 1024 subsequent switching cycles, the device reduces the current limit from its nominal value to typically 1.3 A (TPS62441-Q1) and 1.45 A (TPS62442-Q1). Foldback current limit is left when the current limit indication goes away. If device operation continues in current limit, it would, after 3072 switching cycles, try again for full current limit for 1024 switching cycles.

9.4.6 Output Discharge

The purpose of the discharge function is to ensure a defined down-ramp of the output voltage when the device is being disabled but also to keep the output voltage close to 0 V when the device is off. The output discharge feature is only active once the TPS6244x-Q1 has been enabled at least once since the supply voltage was applied. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active is typically 2 V. Output discharge is not activated during a current limit or foldback current limit event.

9.4.7 Soft Start

The internal soft-start circuitry controls the output voltage slope during start-up, which avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high impedance power sources or batteries. When EN1 and EN2 are set high, the device starts switching after t_{Delay}. The output voltage is ramped with a slope defined by t_{Ramp}.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Programming the Output Voltage

The output voltage of the TPS6244x-Q1 is adjustable. The device can be programmed for output voltages from 0.6 V to 5.5 V using a resistor divider from VOUT to GND. The voltage at the FB pin is regulated to 600 mV. The value of the output voltage is set by the selection of the resistor divider from Equation 6. Choose resistor values that allow a current of at least 6 µA, meaning the value of R_2 must not exceed 100 kΩ. Lower resistor values are recommended for the highest accuracy and most robust design.

$$R_1 = R_2 \cdot \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \tag{6}$$

10.1.2 External Component Selection

10.1.2.1 Inductor Selection

The TPS6244x-Q1 is designed for a nominal 0.47-µH inductor with a switching frequency of typically 2.25 MHz. Larger values can be used to achieve a lower inductor current ripple but they can have a negative impact on efficiency and transient response. Smaller values than 0.47 µH cause a larger inductor current ripple, which causes larger negative inductor current in forced PWM mode at low or no output current. For a higher or lower nominal switching frequency, the inductance must be changed accordingly.

The inductor selection is affected by several effects like the following:

- Inductor ripple current
- Output ripple voltage
- PWM-to-PFM transition point
- Efficiency

In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 7 calculates the maximum inductor current.

$$I_{L(\max)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \tag{7}$$

$$\Delta I_{L(\max)} = \frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}{L \min} \cdot \frac{1}{f_{SW}} \tag{8}$$

where

- $I_{L(max)}$ is the maximum inductor current.
- $\Delta I_{L(max)}$ is the peak-to-peak inductor ripple current.
- Lmin is the minimum inductance at the operating point.

Table 10-1. Typical Inductors

Type	Inductance [µH]	Current [A](1)	For Device	Nominal Switching Frequency	Dimensions [L × B × H] mm	Manufacturer(2)
XEL3520-801ME	0.80 µH, ±20%	2.0	TPS62441-Q1	2.25 MHz	3.5 × 3.2 × 2.0	Coilcraft
XEL3520-561ME	0.56 µH, ±20%	2.4	TPS62441-Q1	2.25 MHz	3.5 × 3.2 × 2.0	Coilcraft
XEL3515-561ME	0.56 µH, ±20%	4.5	TPS62442-Q1	2.25 MHz	3.5 × 3.2 × 1.5	Coilcraft
XFL3012-681ME	0.68 µH, ±20%	2.1	TPS62441-Q1	2.25 MHz	3.0 × 3.0 × 1.2	Coilcraft
XPL2010-681ML	0.68 µH, ±20%	1.5	TPS62441-Q1	2.25 MHz	2 × 1.9 × 1	Coilcraft
DFE252012PD-R68M	0.68 µH, ±20%	see data sheet	TPS62442-Q1	2.25 MHz	2.5 × 2 × 1.2	Murata
DFE252012PD-R47M	0.47 µH, ±20%	see data sheet	TPS62442-Q1	2.25 MHz	2.5 × 2 × 1.2	Murata
DFE201612PD-R68M	0.68 µH, ±20%	see data sheet	TPS62441-Q1	2.25 MHz	2 × 1.6 × 1.2	Murata
DFE201612PD-R47M	0.47 µH, ±20%	see data sheet	TPS62442-Q1	2.25 MHz	2 × 1.6 × 1.2	Murata

(1) Lower of I_{RMS} at 20°C rise or I_{SAT} at 20% drop.
(2) See the *Third-Party Products Disclaimer*.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. TI recommends adding a margin of approximately 20%. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well.

10.1.2.2 Capacitor Selection

10.1.2.2.1 Input Capacitor

For most applications, 10-µF nominal is sufficient and is recommended. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low-ESR multilayer ceramic capacitor (MLCC) is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins.

10.1.2.2.2 Output Capacitor

The architecture of the TPS6244x-Q1 allows the use of tiny ceramic output capacitors with low-equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, use X7R or X5R dielectric. Using a higher value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode. By changing the device compensation with a resistor from COMP/FSET to GND, the device can be compensated in three steps based on the minimum capacitance used on the output. The maximum capacitance is 200 µF in any of the compensation settings.

10.2 Typical Application

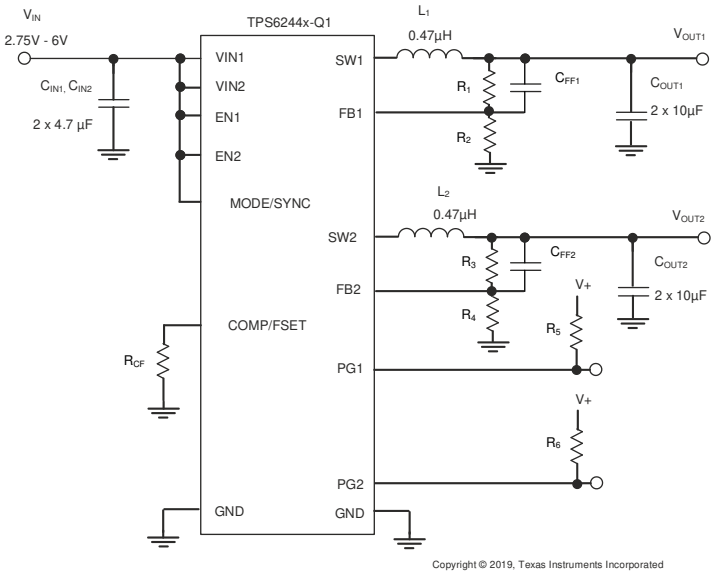


Figure 10-1. Typical Application Schematic

10.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

10.2.2 Detailed Design Procedure

$$R_1 = R_2 \cdot \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \tag{9}$$

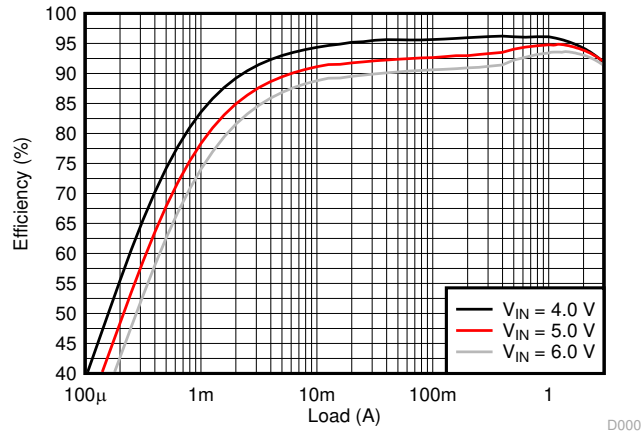
With V_{FB} = 0.6 V:

Table 10-2. Setting the Output Voltage

Nominal Output Voltage V_{OUT}	R_1, R_3	R_2, R_4	C_{FF1}, C_{FF2}	Exact Output Voltage
0.8 V	16.9 kΩ	51 kΩ	10 pF	0.7988 V
1.0 V	20 kΩ	30 kΩ	10 pF	1.0 V
1.1 V	39.2 kΩ	47 kΩ	10 pF	1.101 V
1.2 V	68 kΩ	68 kΩ	10 pF	1.2 V
1.5 V	76.8 kΩ	51 kΩ	10 pF	1.5 V
1.8 V	80.6 kΩ	40.2 kΩ	10 pF	1.803 V
2.5 V	47.5 kΩ	15 kΩ	10 pF	2.5 V
3.3 V	88.7 kΩ	19.6 kΩ	10 pF	3.315 V

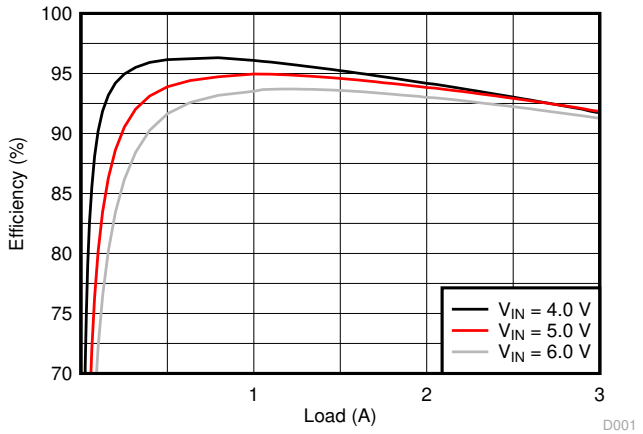
10.2.3 Application Curves

All plots have been taken with a nominal switching frequency of 2.25 MHz when set to PWM mode, unless otherwise noted. The BOM is according to Table 8-1.



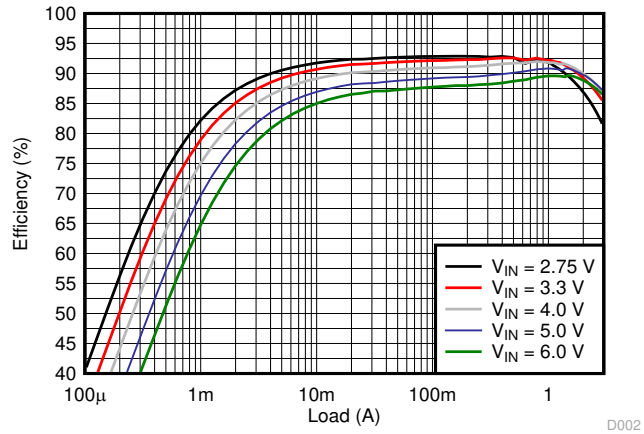
V_{OUT} = 3.3 V PFM T_A = 25°C

Figure 10-2. Efficiency vs Output Current



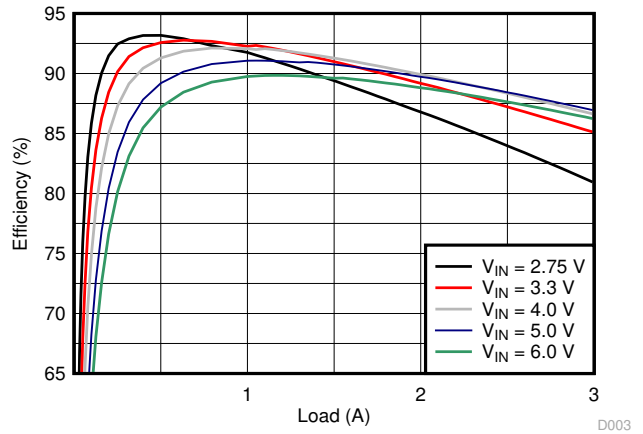
V_{OUT} = 3.3 V PWM T_A = 25°C

Figure 10-3. Efficiency vs Output Current



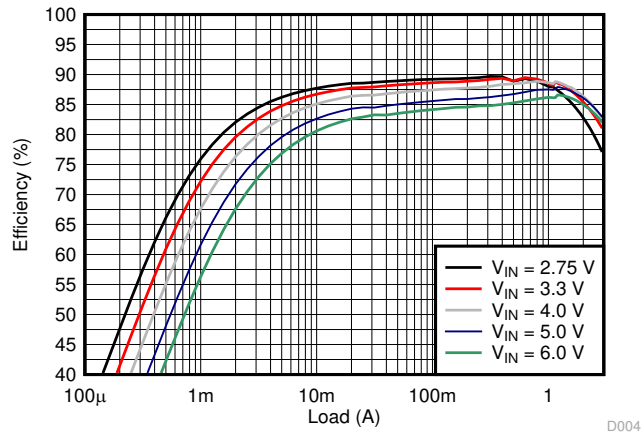
V_{OUT} = 1.8 V PFM T_A = 25°C

Figure 10-4. Efficiency vs Output Current



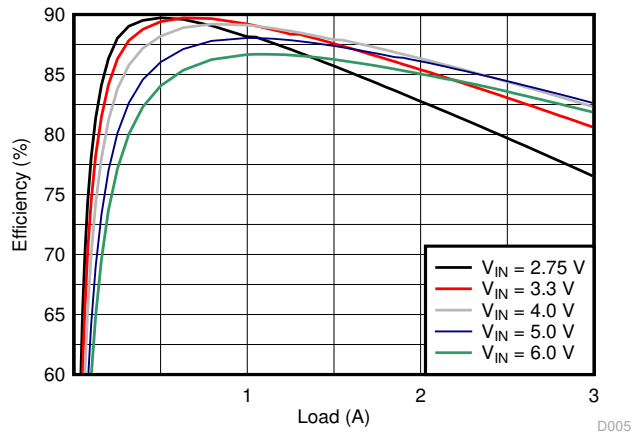
V_{OUT} = 1.8 V PWM T_A = 25°C

Figure 10-5. Efficiency vs Output Current



V_{OUT} = 1.2 V PFM T_A = 25°C

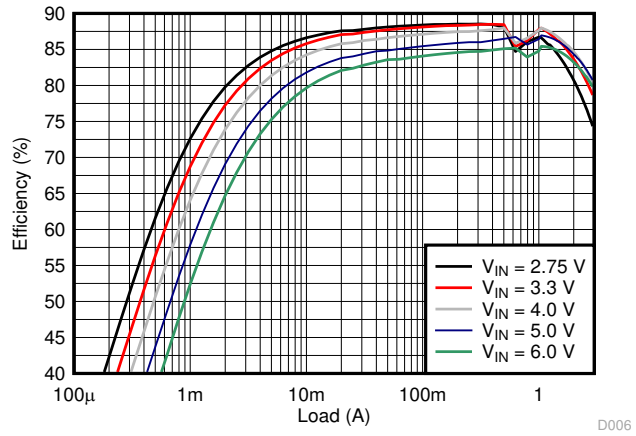
Figure 10-6. Efficiency vs Output Current



V_{OUT} = 1.2 V PWM T_A = 25°C

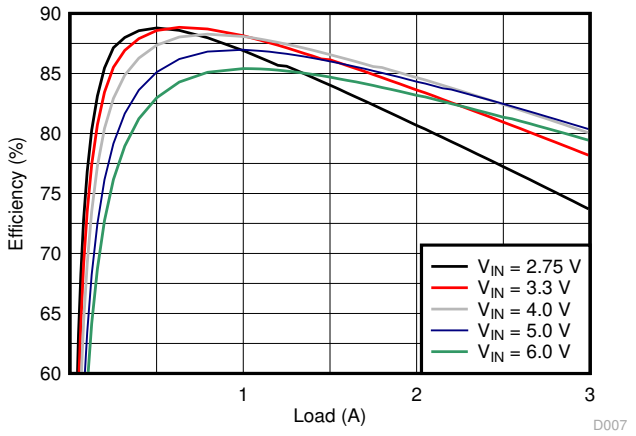
Figure 10-7. Efficiency vs Output Current

10.2.3 Application Curves (continued)



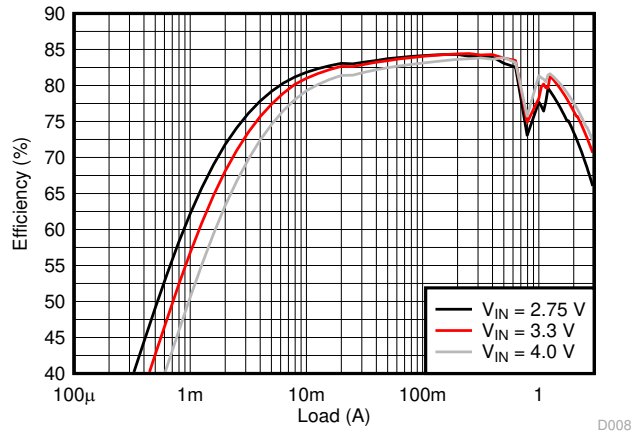
V_{OUT} = 1.0 V PFM T_A = 25°C

Figure 10-8. Efficiency vs Output Current



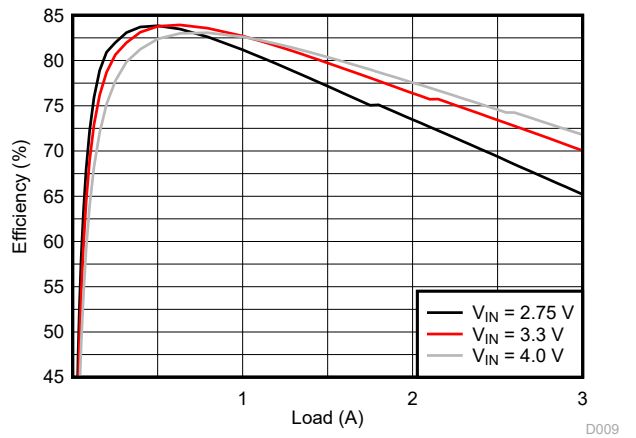
V_{OUT} = 1.0 V PWM T_A = 25°C

Figure 10-9. Efficiency vs Output Current



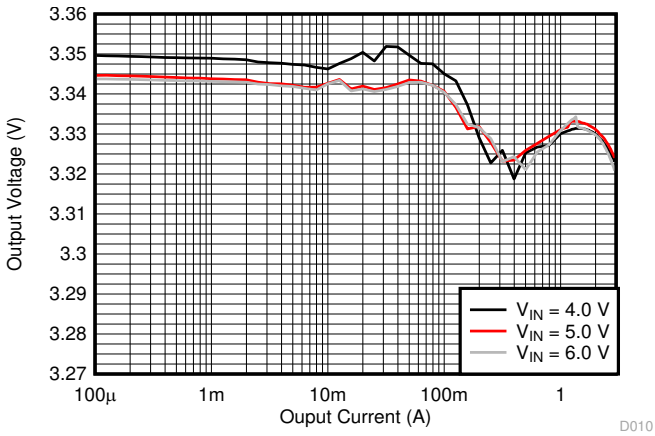
V_{OUT} = 0.6 V PFM T_A = 25°C

Figure 10-10. Efficiency vs Output Current



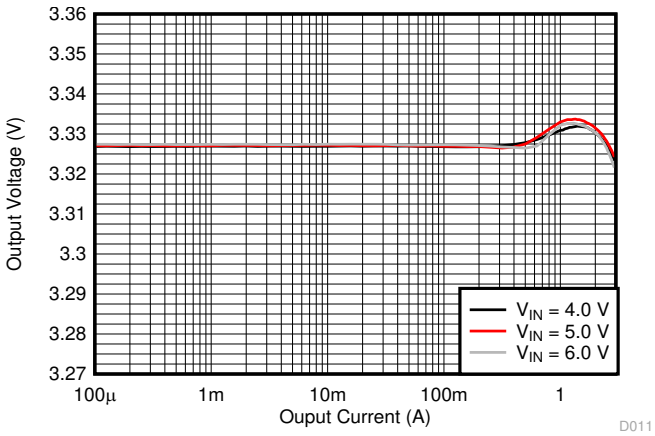
V_{OUT} = 0.6 V PWM T_A = 25°C

Figure 10-11. Efficiency vs Output Current



V_{OUT} = 3.3 V PFM T_A = 25°C

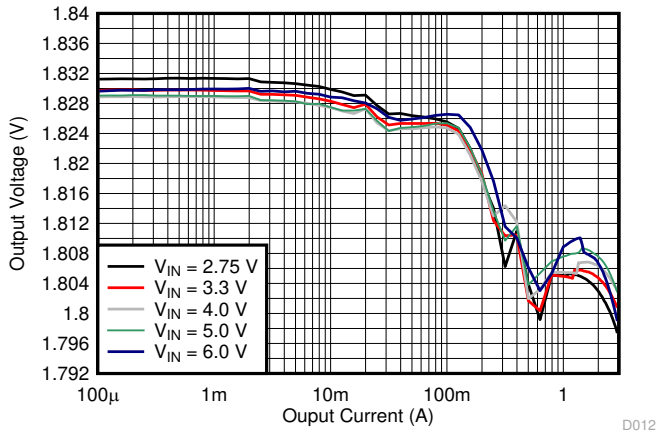
Figure 10-12. Output Voltage vs Output Current



V_{OUT} = 3.3 V PWM T_A = 25°C

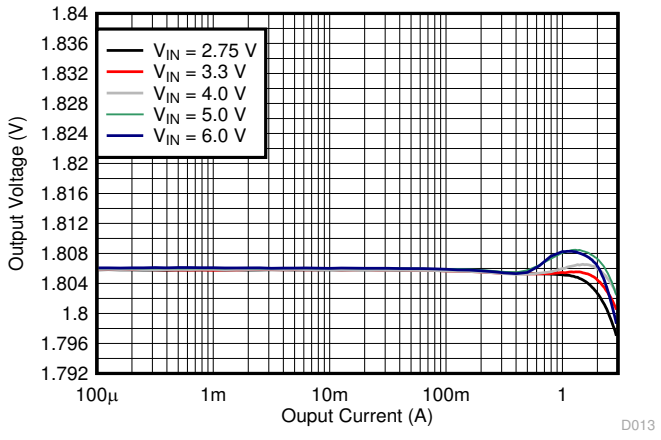
Figure 10-13. Output Voltage vs Output Current

10.2.3 Application Curves (continued)



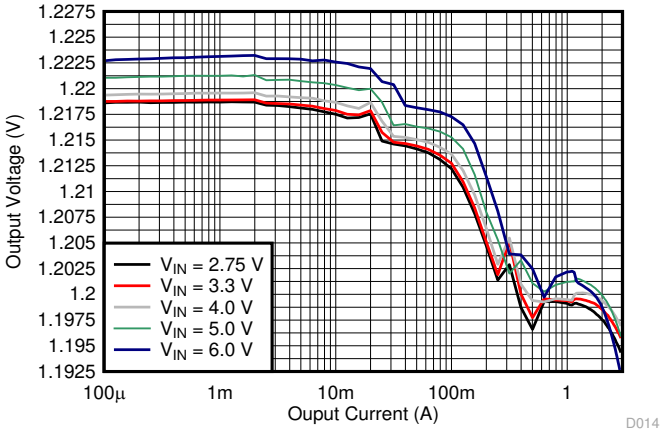
V_{OUT} = 1.8 V PFM T_A = 25°C

Figure 10-14. Output Voltage vs Output Current



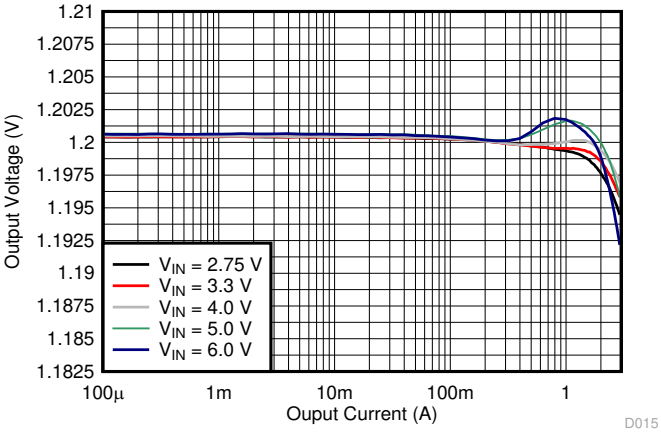
V_{OUT} = 1.8 V PWM T_A = 25°C

Figure 10-15. Output Voltage vs Output Current



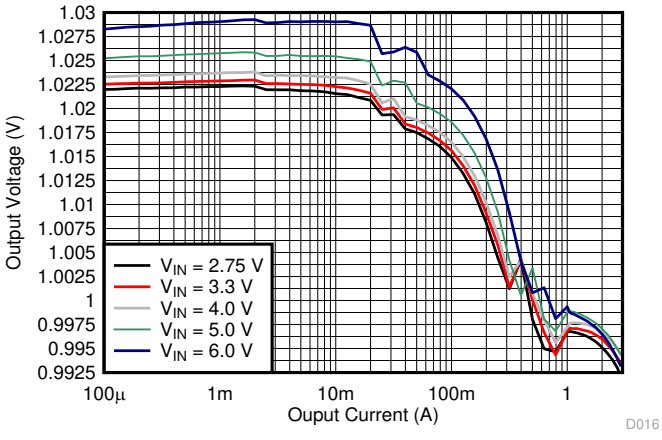
V_{OUT} = 1.2 V PFM T_A = 25°C

Figure 10-16. Output Voltage vs Output Current



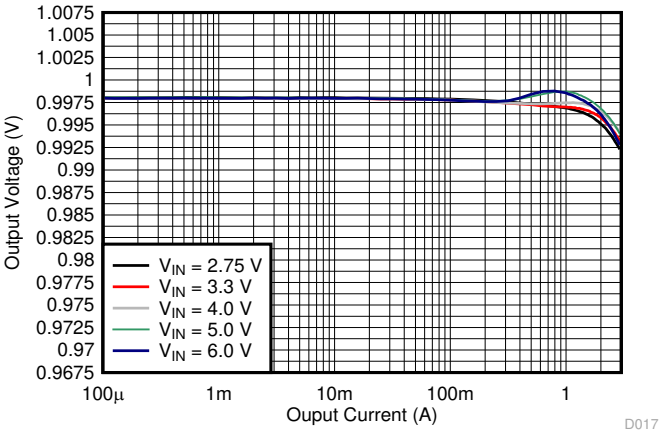
V_{OUT} = 1.2 V PWM T_A = 25°C

Figure 10-17. Output Voltage vs Output Current



V_{OUT} = 1.0 V PFM T_A = 25°C

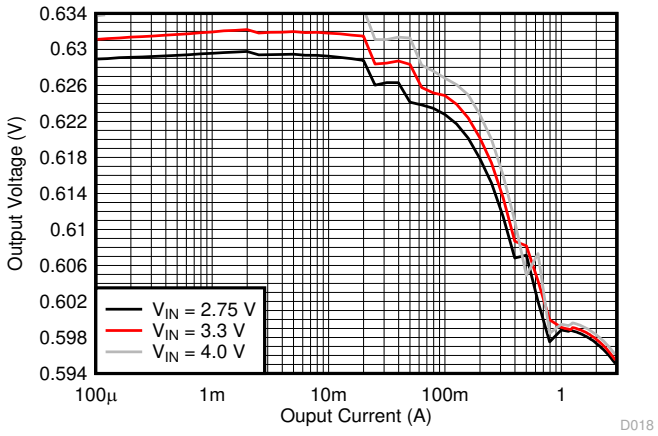
Figure 10-18. Output Voltage vs Output Current



V_{OUT} = 1.0 V PWM T_A = 25°C

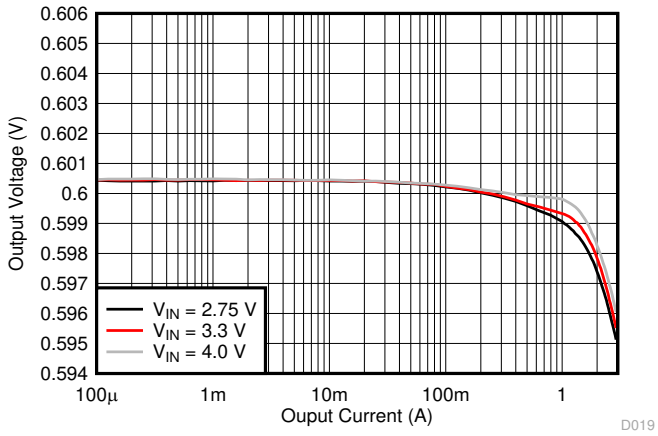
Figure 10-19. Output Voltage vs Output Current

10.2.3 Application Curves (continued)



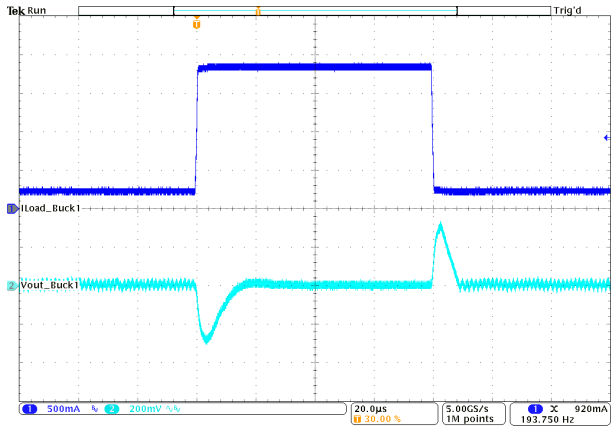
V_{OUT} = 0.6 V PFM T_A = 25°C

Figure 10-20. Output Voltage vs Output Current



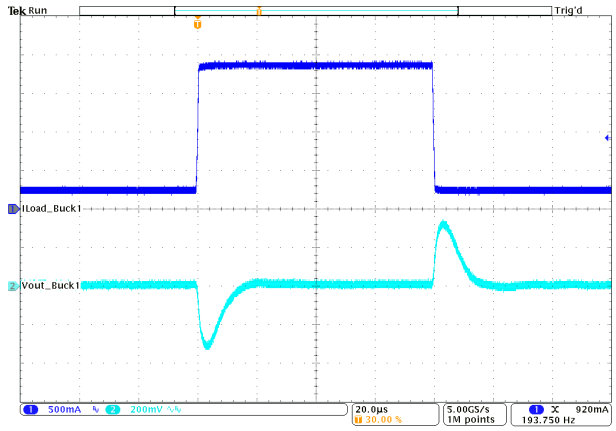
V_{OUT} = 0.6 V PWM T_A = 25°C

Figure 10-21. Output Voltage vs Output Current



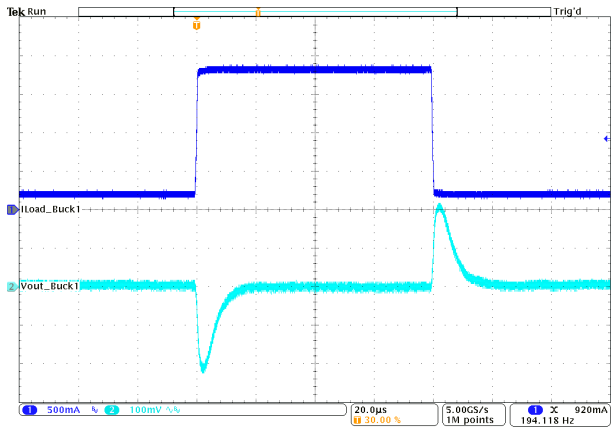
V_{OUT} = 3.3 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

Figure 10-22. Load Transient Response



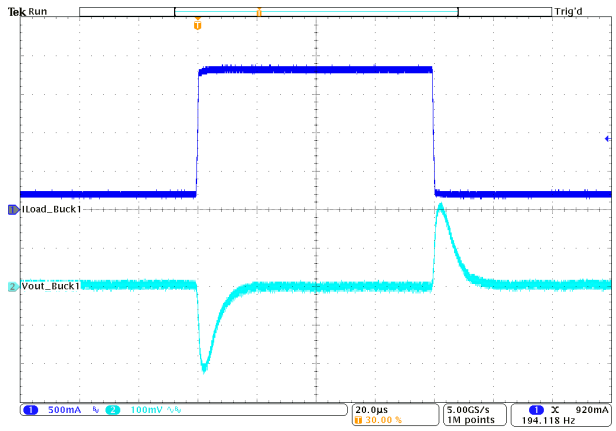
V_{OUT} = 3.3 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

Figure 10-23. Load Transient Response



V_{OUT} = 1.8 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

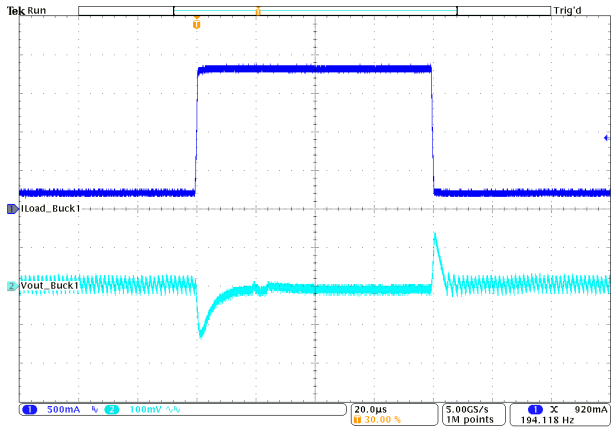
Figure 10-24. Load Transient Response



V_{OUT} = 1.8 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

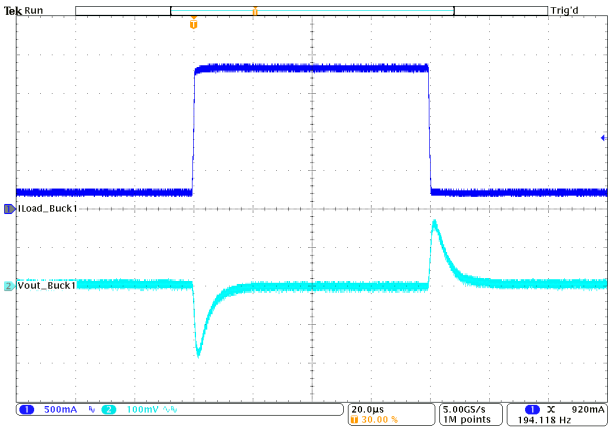
Figure 10-25. Load Transient Response

10.2.3 Application Curves (continued)



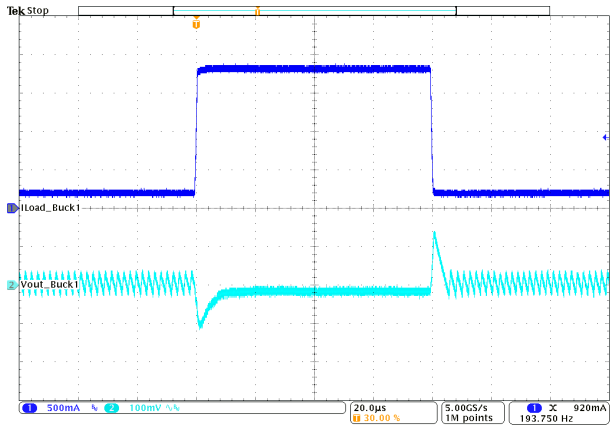
V_{OUT} = 1.2 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

Figure 10-26. Load Transient Response



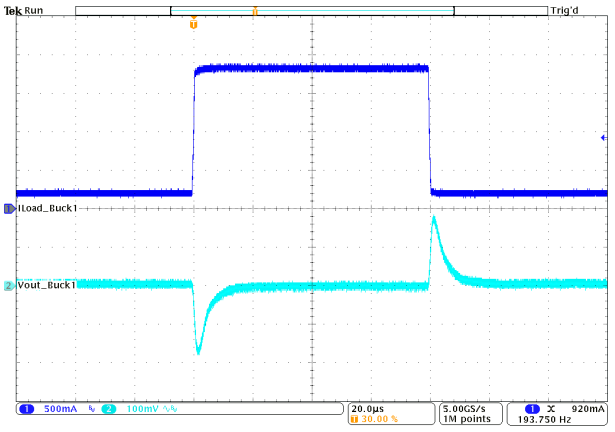
V_{OUT} = 1.2 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

Figure 10-27. Load Transient Response



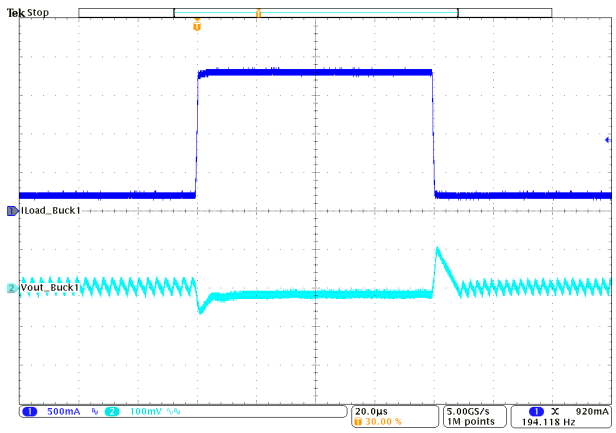
V_{OUT} = 1.0 V PFM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

Figure 10-28. Load Transient Response



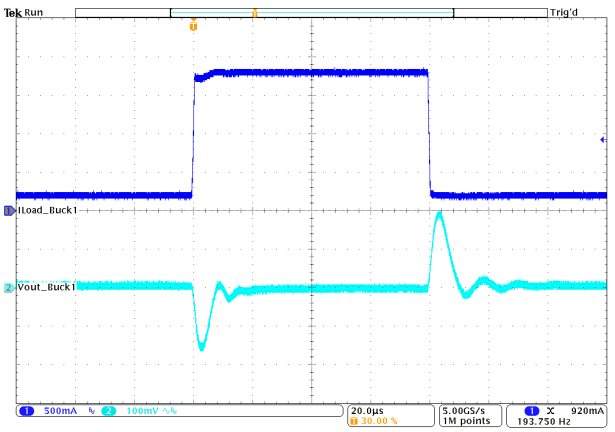
V_{OUT} = 1.0 V PWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

Figure 10-29. Load Transient Response



V_{OUT} = 0.6 V PFM T_A = 25°C
V_{IN} = 3.3 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

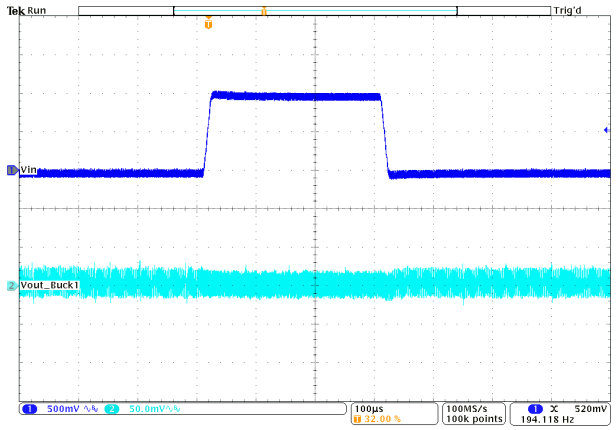
Figure 10-30. Load Transient Response



V_{OUT} = 0.6 V PWM T_A = 25°C
V_{IN} = 3.3 V I_{OUT} = 0.2 A to 1.8 A to 0.2 A

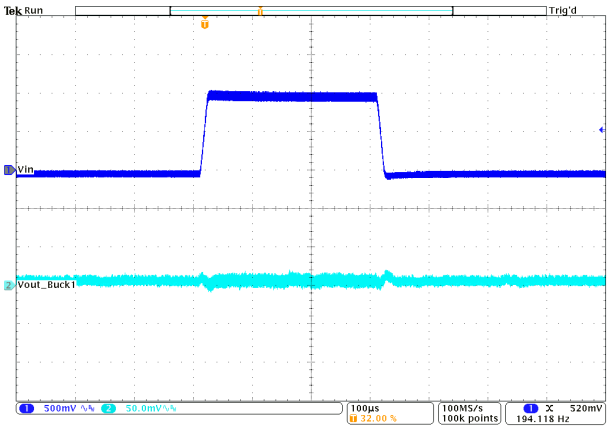
Figure 10-31. Load Transient Response

10.2.3 Application Curves (continued)



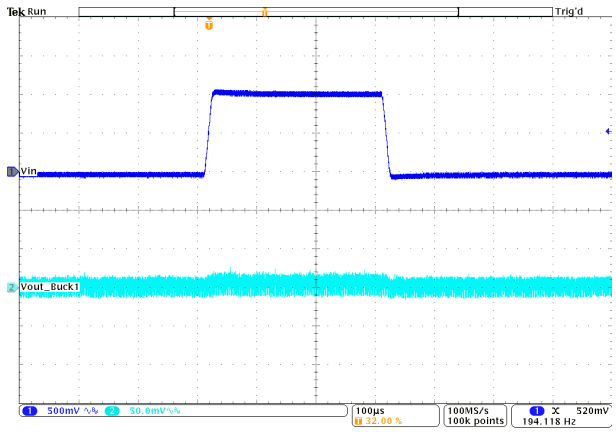
V_{OUT} = 3.3 V PFM T_A = 25°C
I_{OUT} = 0.3 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-32. Line Transient Response



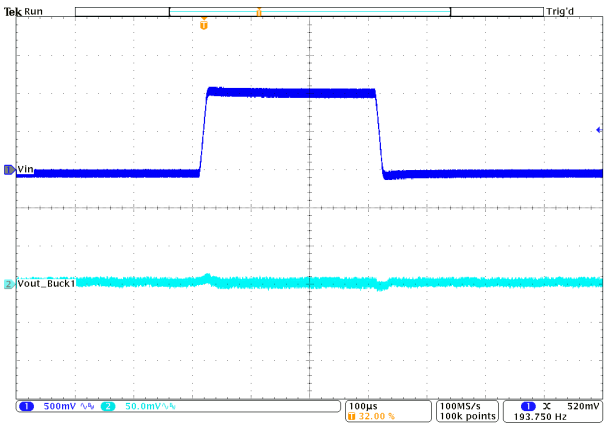
V_{OUT} = 3.3 V PWM T_A = 25°C
I_{OUT} = 3 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-33. Line Transient Response



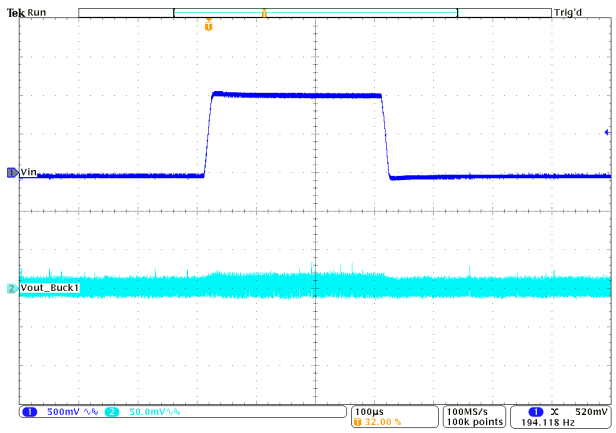
V_{OUT} = 1.8 V PFM T_A = 25°C
I_{OUT} = 0.3 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-34. Line Transient Response



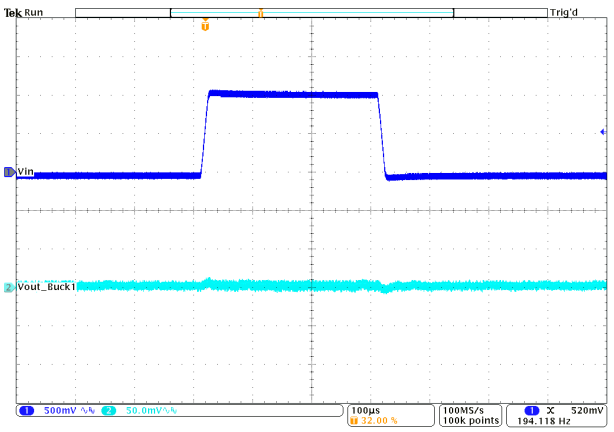
V_{OUT} = 1.8 V PWM T_A = 25°C
I_{OUT} = 3 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-35. Line Transient Response



V_{OUT} = 1.2 V PFM T_A = 25°C
I_{OUT} = 0.3 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

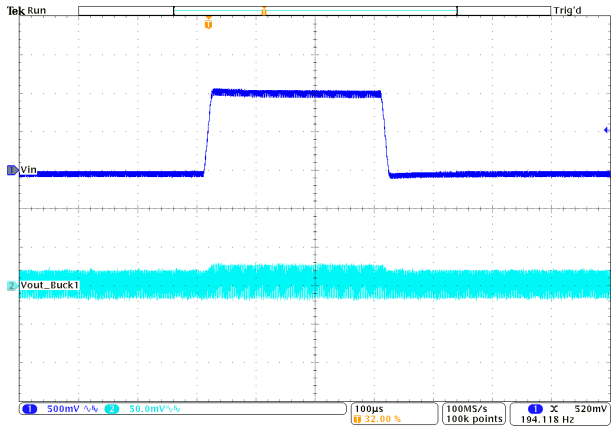
Figure 10-36. Line Transient Response



V_{OUT} = 1.2 V PWM T_A = 25°C
I_{OUT} = 3 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

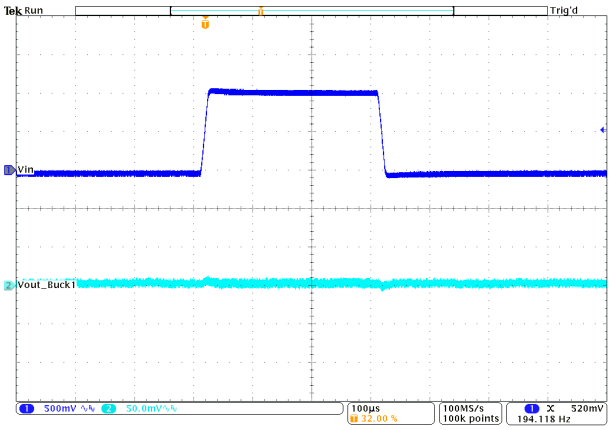
Figure 10-37. Line Transient Response

10.2.3 Application Curves (continued)



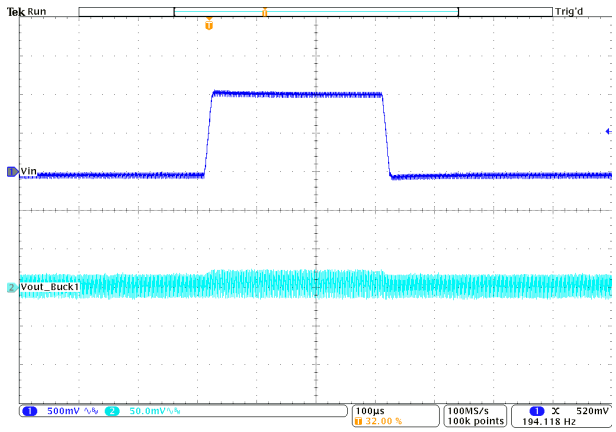
V_{OUT} = 1.0 V PFM T_A = 25°C
I_{OUT} = 0.3 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-38. Line Transient Response



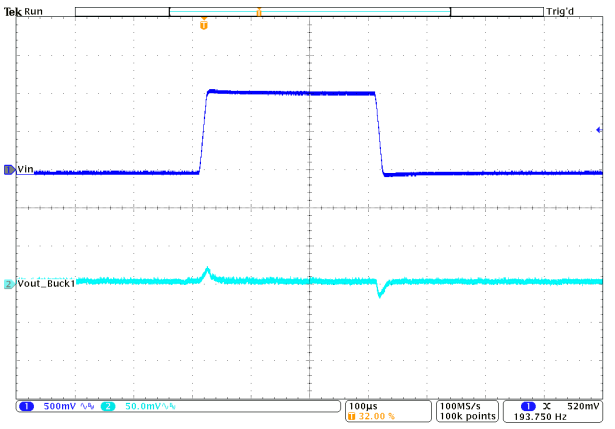
V_{OUT} = 1.0 V PWM T_A = 25°C
I_{OUT} = 3 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-39. Line Transient Response



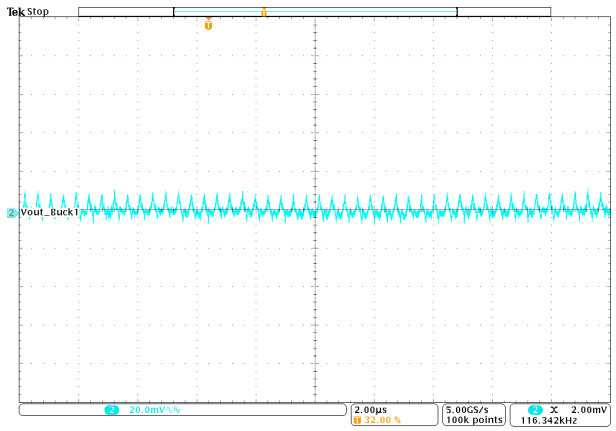
V_{OUT} = 0.6 V PFM T_A = 25°C
I_{OUT} = 0.3 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-40. Line Transient Response



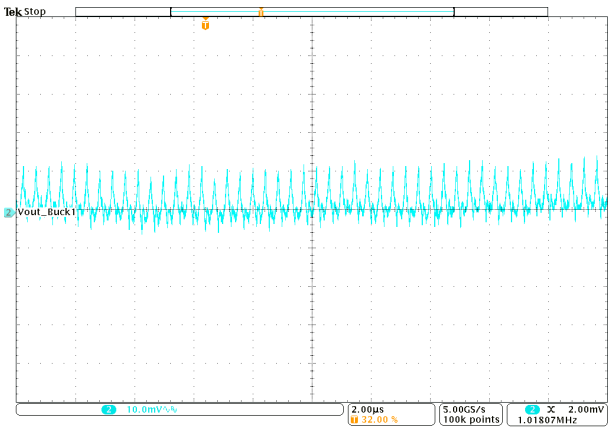
V_{OUT} = 0.6 V PWM T_A = 25°C
I_{OUT} = 3 A V_{IN} = 4.5 V to 5.5 V to 4.5 V

Figure 10-41. Line Transient Response



V_{OUT} = 3.3 V PFM T_A = 25°C
I_{OUT} = 0.3 A V_{IN} = 5.0 V BW = 20 MHz

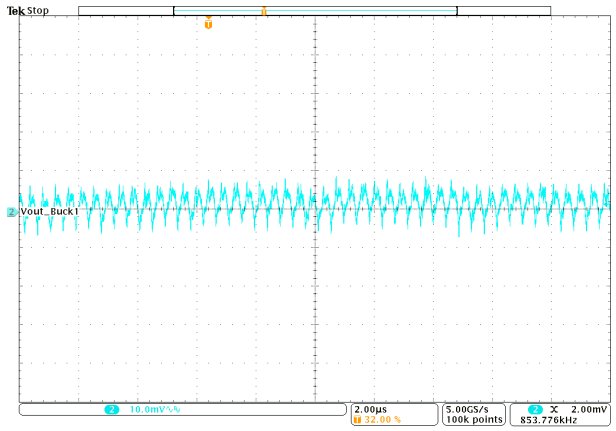
Figure 10-42. Output Voltage Ripple



V_{OUT} = 3.3 V PWM T_A = 25°C
I_{OUT} = 3 A V_{IN} = 5.0 V BW = 20 MHz

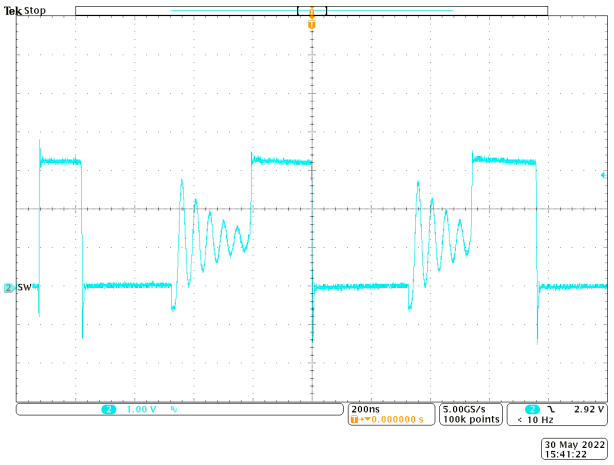
Figure 10-43. Output Voltage Ripple

10.2.3 Application Curves (continued)



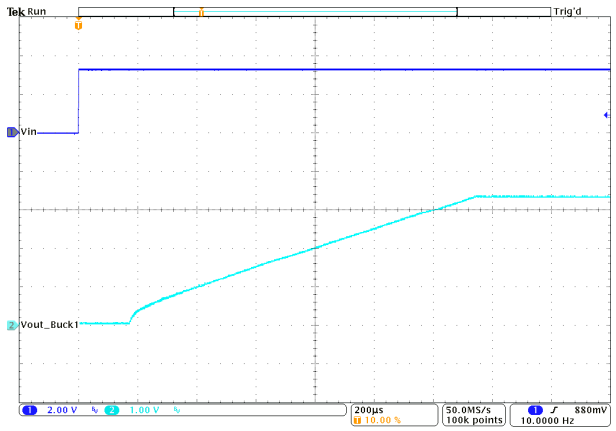
V_{OUT} = 1.8 V PWM T_A = 25°C
I_{OUT} = 3 A V_{IN} = 5.0 V BW = 20 MHz

Figure 10-44. Output Voltage Ripple



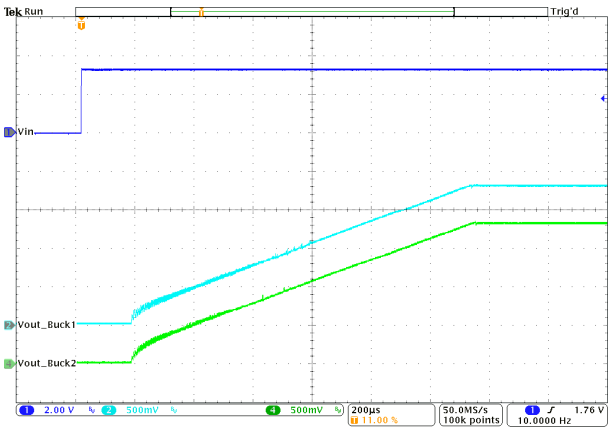
V_{OUT} = 1.2 V T_A = 25°C
I_{OUT} = 0.4 A V_{IN} = 3.3 V

Figure 10-45. Switching Waveform in PFM Mode



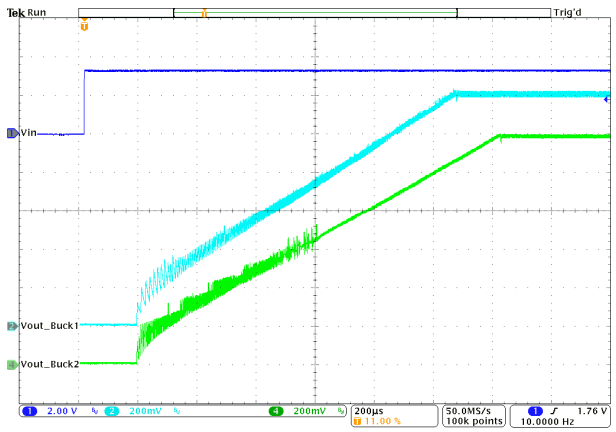
V_{OUT} = 3.3 V PWM T_A = 25°C
I_{OUT} = 3 A V_{IN} = 5.0 V

Figure 10-46. Start-Up Timing



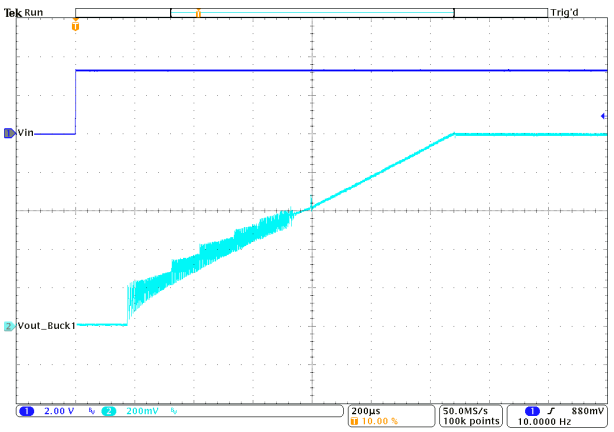
$V_{OUT1/2}$ = 1.8 V PWM T_A = 25°C
I_{OUT1} = 2 A I_{OUT2} = 2 A V_{IN} = 5.0 V

Figure 10-47. Start-Up Timing



$V_{OUT1/2}$ = 1.2 V PWM T_A = 25°C
I_{OUT1} = 1 A I_{OUT2} = 3 A V_{IN} = 5.0 V

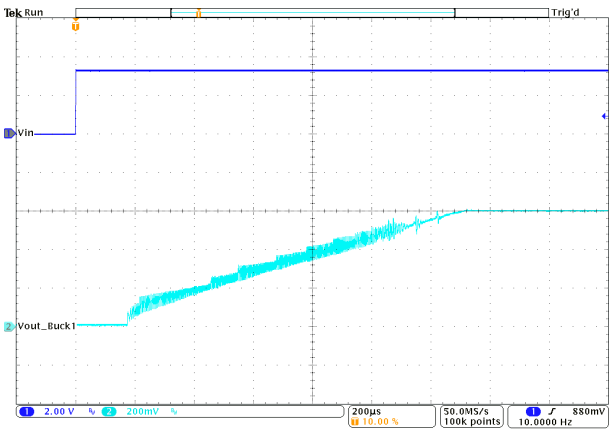
Figure 10-48. Start-Up Timing



V_{OUT} = 1.0 V PWM T_A = 25°C
I_{OUT1} = 3 A V_{IN} = 5.0 V

Figure 10-49. Start-Up Timing

10.2.3 Application Curves (continued)



V_{OUT} = 0.6V PWM T_A = 25°C
I_{OUT1} = 3 A V_{IN} = 5.0 V

Figure 10-50. Start-Up Timing

11 Power Supply Recommendations

The TPS6244x-Q1 device family has no special requirements for its input power supply. The output current of the input power supply needs to be rated according to the supply voltage, output voltage, and output current of the TPS6244x-Q1.

12 Layout

12.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS6244x-Q1 demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like the following:

- Poor regulation (both line and load)
- Stability and accuracy weaknesses
- Increased EMI radiation
- Noise sensitivity

See Figure 12-1 for the recommended layout of the TPS6244x-Q1, which is designed for common external ground connections. The input capacitor should be placed as close as possible between the VIN and GND pin.

Provide low inductive and resistive paths for loops with high di/dt. Therefore, paths conducting the switched load current must be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore, the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops that conduct an alternating current must outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB need to be connected with short wires and not nearby high dv/dt signals (for example, SW). As they carry information about the output voltage, nodes must be connected as close as possible to the actual output voltage (at the output capacitor). The FB resistors, R_1 and R_2, as well as R_3 and R_4 must be kept close to the IC and connect directly to those pins and the system ground plane.

The package uses the pins for power dissipation. Thermal vias on the VIN, GND, and SW pins help to spread the heat into the PCB.

The recommended layout is implemented on the EVM and shown in the *TPS62442EVM-122 User's Guide*.

12.2 Layout Example

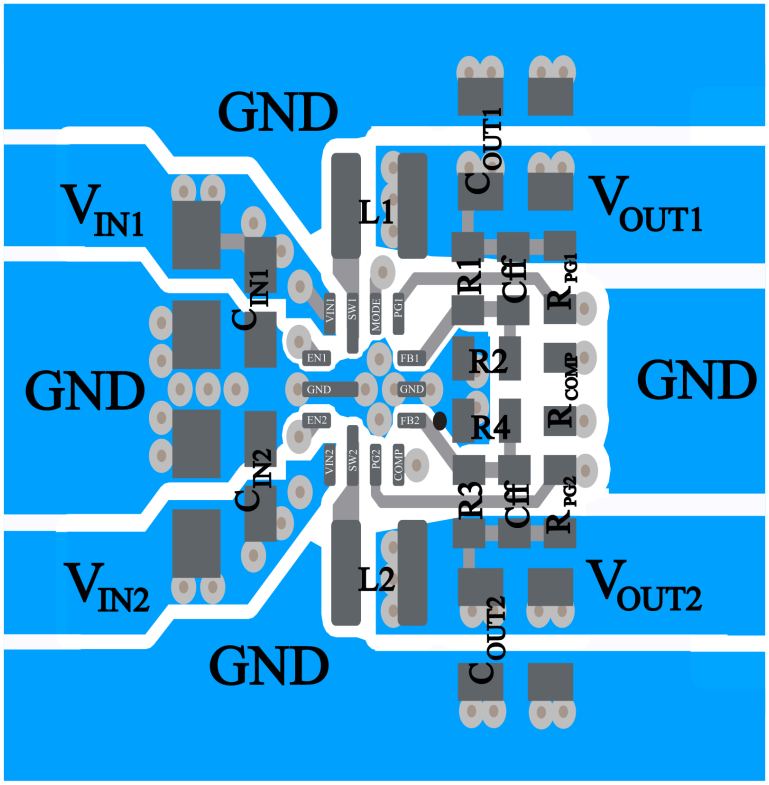


Figure 12-1. Example Layout

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TPS62442EVM-122 User's Guide*

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62441QWRQRRQ1	ACTIVE	VQFN-HR	RQR	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	441QW	Samples
TPS62442QWRQRRQ1	ACTIVE	VQFN-HR	RQR	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	442QW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS62442-Q1 :

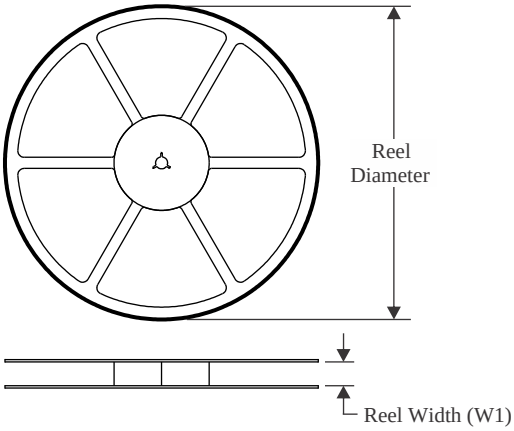
- Catalog : TPS62442

NOTE: Qualified Version Definitions:

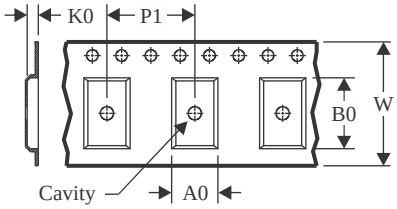
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

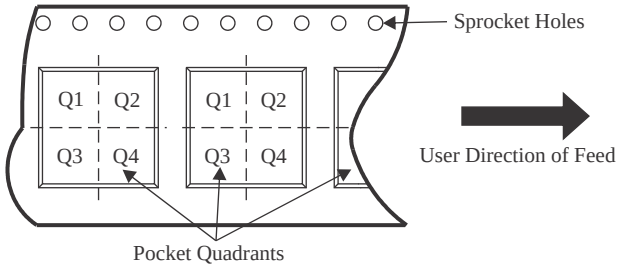


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

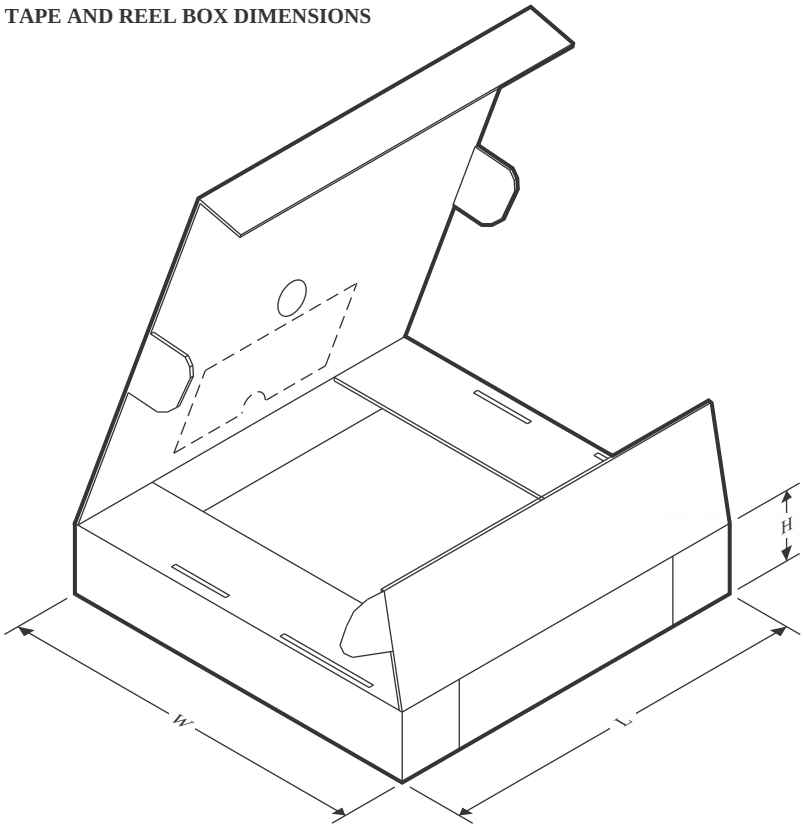
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62441QWRQRRQ1	VQFN-HR	RQR	14	3000	180.0	8.4	2.6	3.0	1.2	4.0	8.0	Q1
TPS62442QWRQRRQ1	VQFN-HR	RQR	14	3000	180.0	8.4	2.6	3.0	1.2	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62441QWRQRRQ1	VQFN-HR	RQR	14	3000	210.0	185.0	35.0
TPS62442QWRQRRQ1	VQFN-HR	RQR	14	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

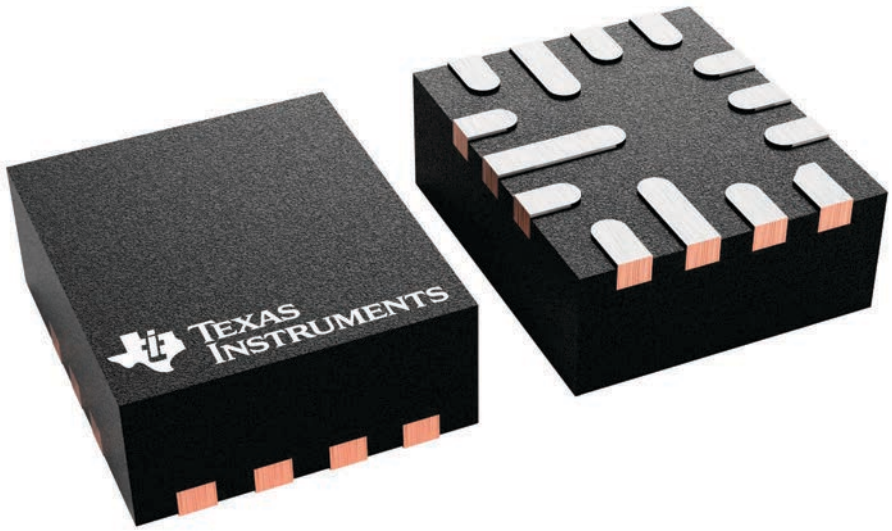
RQR 14

VQFN-HR - 1 mm max height

2.3 x 2.7, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



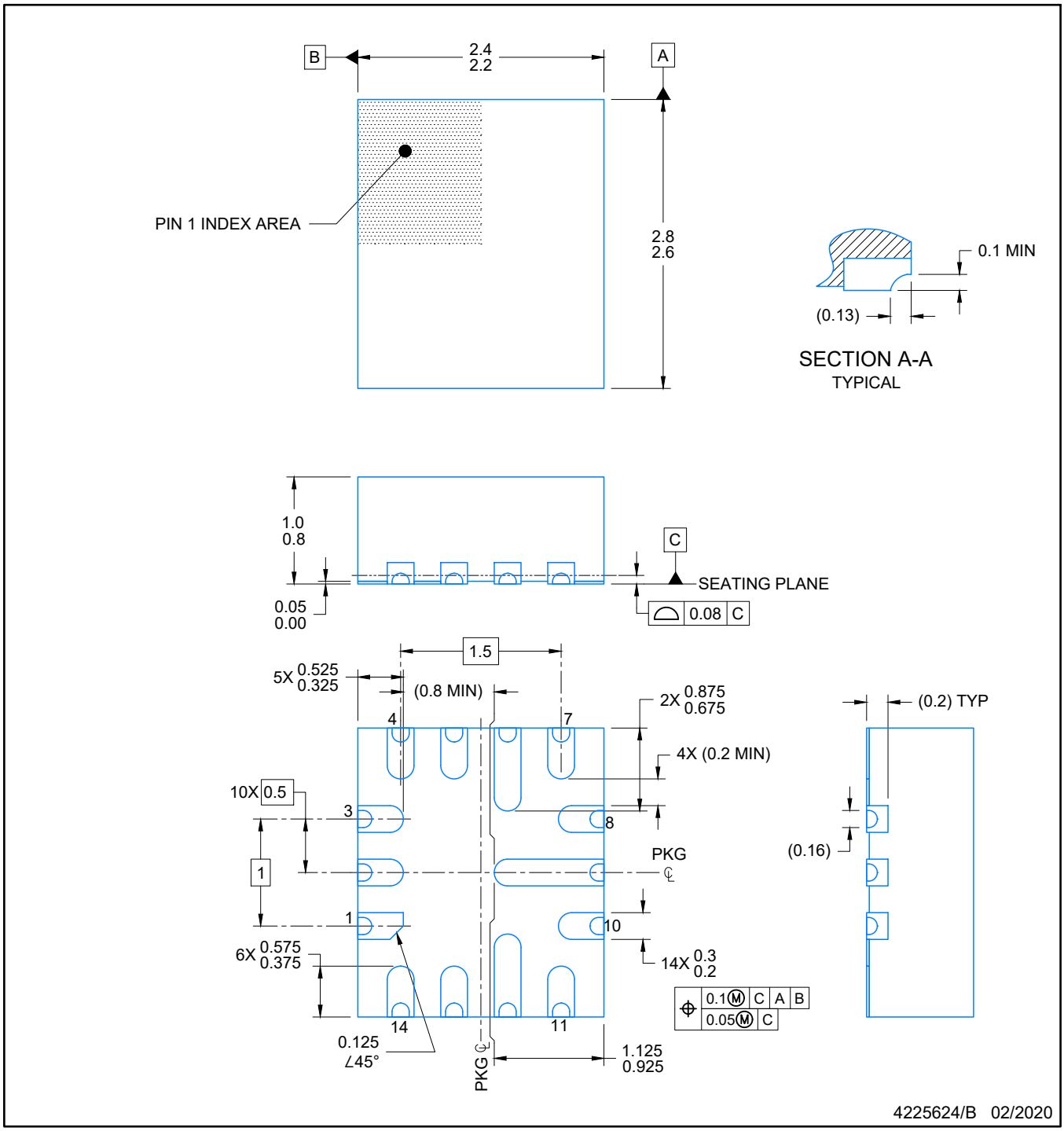
4229224/A

PACKAGE OUTLINE

RQR0014A

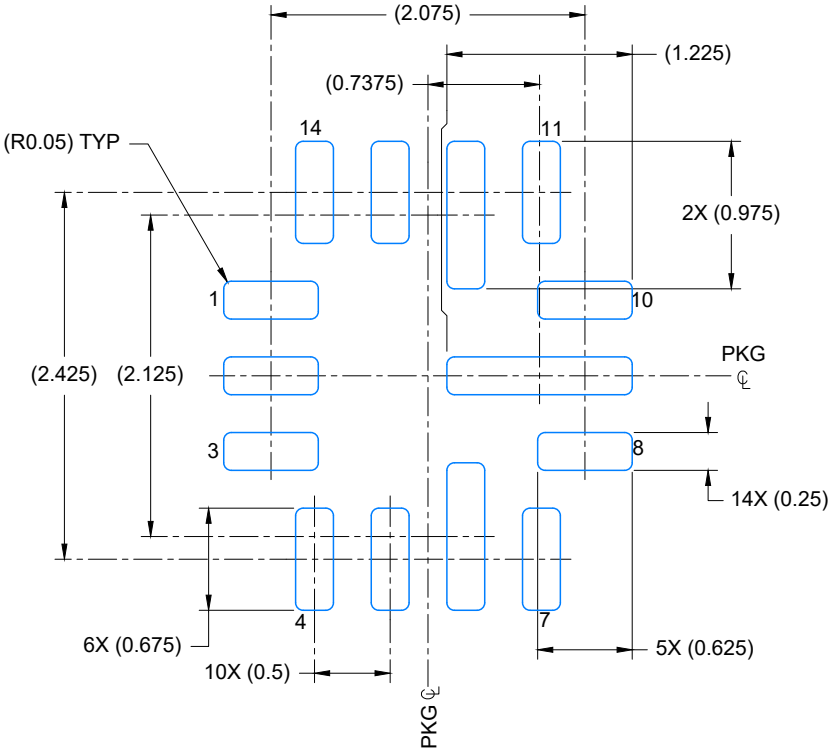
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



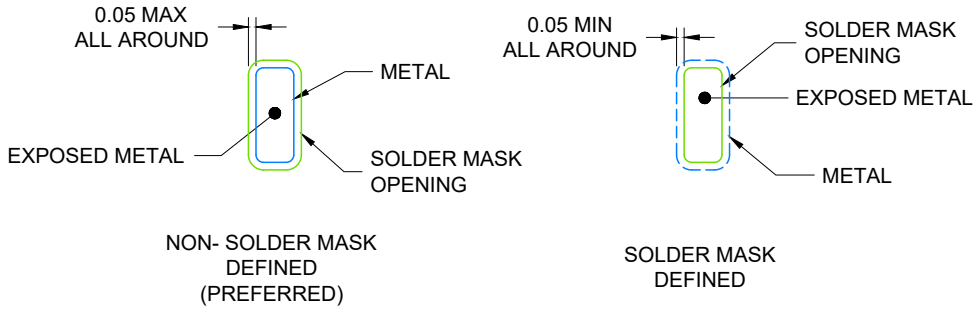
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 20X



SOLDER MASK DETAILS

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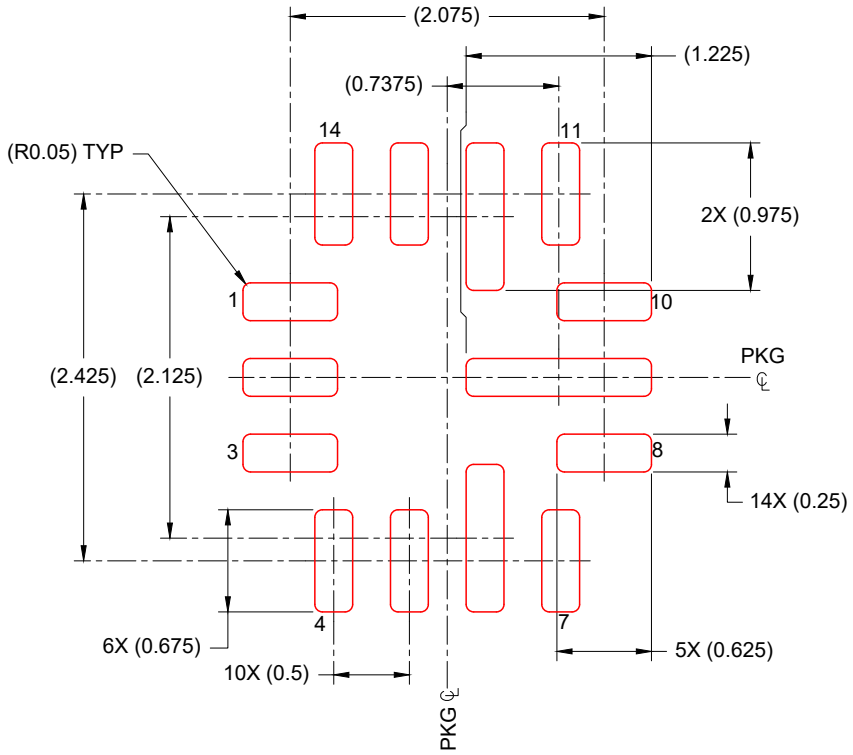
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 18X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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