TXS0206A SD Card Voltage-Translation Transceiver

1 Features

- Level Translator
  - V_{CCA} and V_{CCB} Range of 1.1 V to 3.6 V
  - Fast Propagation Delay (4.4 ns Maximum When Translating Between 1.8 V and 3 V)
- ESD Protection Exceeds JESD 22
  - 2500-V Human-Body Model (A114-B)
  - 250-V Machine Model (A115-A)
  - 1500-V Charged-Device Model (C101)

2 Applications

- Mobile Phones
- Tablet PCs
- Notebooks
- Ultrabook Computers

3 Description

The TXS0206A is a level shifter for interfacing microprocessors with MultiMediaCards (MMCs), secure digital (SD) cards, and Memory Stick™ cards.

The voltage-level translator has two supply voltage pins. V_{CCA} as well as V_{CCB} can be operated over the full range of 1.1 V to 3.6 V. The TXS0206A enables system designers to easily interface applications processors or digital basebands to memory cards and SDIO peripherals operating at a different I/O voltage level.

The TXS0206A is offered in a 20-bump wafer chip scale package (WCSP). This package has dimensions of 1.96 mm × 1.56 mm, with a 0.4-mm ball pitch for effective board-space savings. Memory cards are widely used in mobile phones, PDAs, digital cameras, personal media players, camcorders, set-top boxes, etc. Low static power consumption and small package size make the TXS0206A an ideal choice for these applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
TXS0206A	DSBGA (20)	1.96 mm × 1.56 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Example

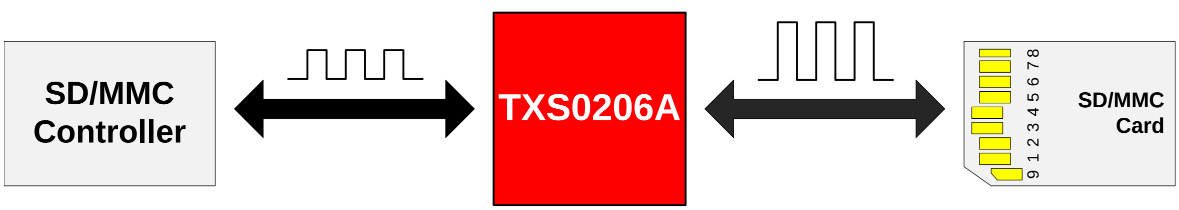


Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 6
6.5 Electrical Characteristics ... 6
6.6 Timing Requirements—V_{CCA} = 1.2 V ± 0.1 V ... 7
6.7 Timing Requirements—V_{CCA} = 1.8 V ± 0.15 V ... 8
6.8 Timing Requirements—V_{CCA} = 3.3 V ± 0.3 V ... 8
6.9 Switching Characteristics—V_{CCA} = 1.2 V ± 0.1 V ... 9
6.10 Switching Characteristics—V_{CCA} = 1.8 V ± 0.15 V ... 10
6.11 Switching Characteristics—V_{CCA} = 3.3 V ± 0.3 V ... 11
6.12 Operating Characteristics —V_{CCA} = 1.2 V ... 12
6.13 Operating Characteristics —V_{CCA} = 1.8 V ... 13
6.14 Operating Characteristics — V_{CCA} = 3.3 V ... 13
6.15 Typical Characteristics ... 14
7 Parameter Measurement Information ... 15
8 Detailed Description ... 16
8.1 Overview ... 16
8.2 Functional Block Diagram ... 16
8.3 Feature Description ... 17
8.4 Device Functional Modes ... 18
9 Application and Implementation ... 19
9.1 Application Information ... 19
9.2 Typical Application ... 19
9.3 System Examples ... 21
10 Power Supply Recommendations ... 22
11 Layout ... 22
11.1 Layout Guidelines ... 22
11.2 Layout Example ... 23
12 Device and Documentation Support ... 24
12.1 Documentation Support ... 24
12.2 Community Resources ... 24
12.3 Trademarks ... 24
12.4 Electrostatic Discharge Caution ... 24
12.5 Glossary ... 24
13 Mechanical, Packaging, and Orderable Information ... 24

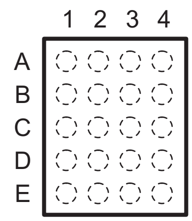
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2012) to Revision B	Page
• Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Deleted the ordering information. See POA at the end of the datasheet	1

5 Pin Configuration and Functions

YFP Package
20–Pin DSBGA
Top View



Pin Assignments

	1	2	3	4
A	DAT2A	V_{CCA}	WP	DAT2B
B	DAT3A	CD	V_{CCB}	DAT3B
C	CMDA	GND	GND	CMDB
D	DAT0A	CLKA	CLKB	DAT0B
E	DAT1A	CLK-f	EN	DAT1B

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	DAT2A	I/O	Data bit 2 connected to host. Referenced to V_{CCA}. Includes a 40-kΩ pullup resistor to V_{CCA}.
A2	V_{CCA}	Pwr	A-port supply voltage. V_{CCA} powers all A-port I/Os and control inputs.
A3	WP	O	Connected to write protect on the mechanical connector. The WP pin has an internal 100-kΩ (± 30%) pullup resistor to V_{CCA}. Leave unconnected if not used.
A4	DAT2B	I/O	Data bit 2 connected to memory card. Referenced to V_{CCB}. Includes a 40-kΩ pullup resistor to V_{CCB}.
B1	DAT3A	I/O	Data bit 3 connected to host. Referenced to V_{CCA}. Includes a 40-kΩ pullup resistor to V_{CCA}.
B2	CD	O	Connected to card detect on the mechanical connector. The CD pin has an internal 100-kΩ (± 30%) pullup resistor to V_{CCA}. Leave unconnected if not used.
B3	V_{CCB}	Pwr	B-port supply voltage. V_{CCB} powers all B-port I/Os.
B4	DAT3B	I/O	Data bit 3 connected to memory card. Referenced to V_{CCB}. Includes a 40-kΩ pullup resistor to V_{CCB}.
C1	CMDA	I/O	Command bit connected to host. Referenced to V_{CCA}. Includes a 40-kΩ pullup resistor to V_{CCA}.
C2	GND	—	Ground
C3	GND	—	Ground
C4	CMDB	I/O	Command bit connected to memory card. Referenced to V_{CCB}. Includes a 40-kΩ pullup resistor to V_{CCB}.
D1	DAT0A	I/O	Data bit 0 connected to host. Referenced to V_{CCA}. Includes a 40-kΩ pullup resistor to V_{CCA}.
D2	CLKA	I	Clock signal connected to host. Referenced to V_{CCA}.
D3	CLKB	O	Clock signal connected to memory card. Referenced to V_{CCB}.
D4	DAT0B	I/O	Data bit 0 connected to memory card. Referenced to V_{CCB}. Includes a 40-kΩ pullup resistor to V_{CCB}.
E1	DAT1A	I/O	Data bit 1 connected to host. Referenced to V_{CCA}. Includes a 40-kΩ pullup resistor to V_{CCA}.
E2	CLK-f	O	Clock feedback to host for resynchronizing data to a processor. Leave unconnected if not used.
E3	EN	I	Enable/disable control. Pull EN low to place all outputs in Hi-Z state. Referenced to V_{CCA}.
E4	DAT1B	I/O	Data bit 1 connected to memory card. Referenced to V_{CCB}. Includes a 40-kΩ pullup resistor to V_{CCB}.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CCA}	Supply voltage, A-Port		–0.5	4.6	V
V_{CCB}	Supply voltage, B-Port		–0.5	4.6	V
V_I	Input voltage	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state	A port	–0.5	4.6	V
		B port	–0.5	4.6	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	
		Machine model (MM)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.1	3.6	V
V_{CCB}	Supply voltage				1.1	3.6	V
V_{IH}	High-level input voltage	A-Port CMD and DATA I/Os	1.1 V to 1.95 V	1.1 V to 1.95 V	V_{CCI} – 0.2	V_{CCI}	V
		B-Port CMD and DATA I/Os	1.95 V to 3.6 V	1.95 V to 3.6 V			
		EN and CLKA	1.1 V to 3.6 V	1.1 V to 3.6 V	V_{CCI} × 0.65	V_{CCI}	
V_{IL}	Low-level input voltage	A-Port CMD and DATA I/Os	1.1 V to 1.95 V	1.1 V to 1.95 V	0	0.15	V
		B-Port CMD and DATA I/Os	1.95 V to 3.6 V	1.95 V to 3.6 V			
		EN and CLKA	1.1 V to 3.6 V	1.1 V to 3.6 V	0	V_{CCI} × 0.35	
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current (CLK-f output)		1.1 V to 3.6 V	1.1 V to 3.6 V		–100	µA
			1.1 V to 1.3 V			–0.5	mA
			1.4 V to 1.6 V			–1	
			1.65 V to 1.95 V			–2	
			2.3 V to 2.7 V			–4	
			3 V to 3.6 V			–8	
I_{OL}	Low-level output current (CLK-f output)		1.1 V to 3.6 V	1.1 V to 3.6 V		100	µA
			1.1 V to 1.3 V			0.5	mA
			1.4 V to 1.6 V			1	
			1.65 V to 1.95 V			2	
			2.3 V to 2.7 V			4	
			3 V to 3.6 V			8	
I_{OH}	High-level output current (CLK output)		1.1 V to 3.6 V	1.1 V to 3.6 V		–100	µA
				1.1 V to 1.3 V		–0.5	mA
				1.4 V to 1.6 V		–1	
				1.65 V to 1.95 V		–2	
				2.3 V to 2.7 V		–4	
				3 V to 3.6 V		–8	
I_{OL}	Low-level output current (CLK output)		1.1 V to 3.6 V	1.1 V to 3.6 V		100	µA
				1.1 V to 1.3 V		0.5	mA
				1.4 V to 1.6 V		1	
				1.65 V to 1.95 V		2	
				2.3 V to 2.7 V		4	
				3 V to 3.6 V		8	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC[(1)]		TXS0206A YFP (DSBGA) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP[(1)]	MAX	UNIT
V_{OH}	A port (CLK-f output)	I_{OH} = –100 µA	1.1 V to 3.6 V	1.65 V to 3.6 V	V_{CCA} × 0.8			V
		I_{OH} = –0.5 mA	1.1 V	1.65 V to 3.6 V	0.8			
		I_{OH} = –1 mA	1.4 V	1.65 V to 3.6 V	1.05			
		I_{OH} = –2 mA	1.65 V	1.65 V to 3.6 V	1.2			
		I_{OH} = –4 mA	2.3 V	1.65 V to 3.6 V	1.75			
		I_{OH} = –8 mA	3 V	1.65 V to 3.6 V	2.3			
	A port (DAT and CMD outputs)	I_{OH} = –20 µA	1.1 V to 3.6 V	1.65 V to 3.6 V	V_{CCA} × 0.8			
V_{OL}	A port (CLK-f output)	I_{OL} = 100 µA	1.1 V to 3.6 V	1.65 V to 3.6 V			V_{CCA} × 0.2	V
		I_{OL} = 0.5 mA	1.1 V	1.65 V to 3.6 V			0.35	
		I_{OL} = 1 mA	1.4 V	1.65 V to 3.6 V			0.35	
		I_{OL} = 2 mA	1.65 V	1.65 V to 3.6 V			0.45	
		I_{OL} = 4 mA	2.3 V	1.65 V to 3.6 V			0.55	
		I_{OL} = 8 mA	3 V	1.65 V to 3.6 V			0.7	
	A port (DAT and CMD outputs)	I_{OL} = 135 µA	1.1 V	1.65 V to 3.6 V			0.4	V
		I_{OL} = 180 µA	1.4 V	1.65 V to 3.6 V			0.4	
		I_{OL} = 220 µA	1.65 V	1.65 V to 3.6 V			0.4	
		I_{OL} = 300 µA	2.3 V	1.65 V to 3.6 V			0.4	
		I_{OL} = 400 µA	3 V	1.65 V to 3.6 V			0.55	
V_{OH}	B port (CLK output)	I_{OH} = –100 µA	1.1 V to 3.6 V	1.65 V to 3.6 V	V_{CCB} × 0.8			V
		I_{OH} = –2 mA	1.1 V to 3.6 V	1.65 V	1.2			
		I_{OH} = –4 mA	1.1 V to 3.6 V	2.3 V	1.75			
		I_{OH} = –8 mA	1.1 V to 3.6 V	3 V	2.3			
	B port (DAT output)	I_{OH} = –20 µA	1.1 V to 3.6 V	1.65 V to 3.6 V	V_{CCB} × 0.8			

(1) All typical values are at T_A = 25°C.

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP(1)	MAX	UNIT
V_{OL}	B port	I_{OL} = 100 µA	1.1 V to 3.6 V	1.65 V to 3.6 V			V_{CCB} × 0.2	V
		I_{OL} = 2 mA	1.1 V to 3.6 V	1.65 V			0.45	
		I_{OL} = 4 mA	1.1 V to 3.6 V	2.3 V			0.55	
		I_{OL} = 8 mA	1.1 V to 3.6 V	3 V			0.7	
	B port (DAT output)	I_{OL} = 135 µA	1.1 V to 3.6 V	1.65 V to 3.6 V			0.4	V
		I_{OL} = 220 µA	1.1 V to 3.6 V	1.65 V			0.4	
		I_{OL} = 300 µA	1.1 V to 3.6 V	2.3 V			0.4	
		I_{OL} = 300 µA	1.1 V to 3.6 V	3 V			0.55	
I_I	Control inputs	$V_I = V_{CCA}$ or GND	1.1 V to 3.6 V	1.65 V to 3.6 V			±1	µA
I_{CCA}	A port	$V_I = V_{CCI}$, I_O = 0	1.1 V to 3.6 V	1.65 V to 3.6 V			7	µA
I_{CCB}	B port	$V_I = V_{CCI}$, I_O = 0	1.1 V to 3.6 V	1.65 V to 3.6 V			11	µA
C_{io}	A port					5.5	6.5	pF
	B port					7	9.5	
C_i	Control inputs	$V_I = V_{CCA}$ or GND				3.5	4.5	pF
	Clock input	$V_I = V_{CCA}$ or GND				3	4	

6.6 Timing Requirements—V_{CCA} = 1.2 V ± 0.1 V

over recommended operating free-air temperature range (unless otherwise noted)

				V_{CC}	MIN	MAX	UNIT
Data rate		Command	Push-pull driving	V_{CCB} = 1.8 V ± 0.15 V		40	Mbps
				V_{CCB} = 3.3 V ± 0.3 V		40	
			Open-drain driving	V_{CCB} = 1.8 V ± 0.15 V		1	
				V_{CCB} = 3.3 V ± 0.3 V		1	
		Clock	Push-pull driving	V_{CCB} = 1.8 V ± 0.15 V		40	MHz
				V_{CCB} = 3.3 V ± 0.3 V		40	
		Data		V_{CCB} = 1.8 V ± 0.15 V		40	Mbps
				V_{CCB} = 3.3 V ± 0.3 V		40	
t_W	Pulse duration	Command	Push-pull driving	V_{CCB} = 1.8 V ± 0.15 V	25		ns
				V_{CCB} = 3.3 V ± 0.3 V	25		
			Open-drain driving	V_{CCB} = 1.8 V ± 0.15 V	1		µs
				V_{CCB} = 3.3 V ± 0.3 V	1		
		Clock	Push-pull driving	V_{CCB} = 1.8 V ± 0.15 V	10		ns
				V_{CCB} = 3.3 V ± 0.3 V	8.3		
		Data		V_{CCB} = 1.8 V ± 0.15 V	25		ns
				V_{CCB} = 3.3 V ± 0.3 V	25		

6.7 Timing Requirements—V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range (unless otherwise noted)

				V_{CC}	MIN	MAX	UNIT
Data rate		Command	Push-pull driving	V_{CCB} = 1.8 V ± 0.15 V		60	Mbps
				V_{CCB} = 3.3 V ± 0.3 V		60	
			Open-drain driving	V_{CCB} = 1.8 V ± 0.15 V		1	
				V_{CCB} = 3.3 V ± 0.3 V		1	
		Clock	Push-pull driving	V_{CCB} = 1.8 V ± 0.15 V		60	MHz
				V_{CCB} = 3.3 V ± 0.3 V		60	
		Data		V_{CCB} = 1.8 V ± 0.15 V		60	Mbps
				V_{CCB} = 3.3 V ± 0.3 V		60	
t_W	Pulse duration	Command	Push-pull driving	V_{CCB} = 1.8 V ± 0.15 V	17		ns
				V_{CCB} = 3.3 V ± 0.3 V	17		
			Open-drain driving	V_{CCB} = 1.8 V ± 0.15 V	1		µs
				V_{CCB} = 3.3 V ± 0.3 V	1		
		Clock	Push-pull driving	V_{CCB} = 1.8 V ± 0.15 V	8.3		ns
				V_{CCB} = 3.3 V ± 0.3 V	8.3		
		Data		V_{CCB} = 1.8 V ± 0.15 V	17		ns
				V_{CCB} = 3.3 V ± 0.3 V	17		

6.8 Timing Requirements—V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

				V_{CC}	MIN	MAX	UNIT
Data rate		Command	Push-pull driving	V_{CCB} = 1.8 V ± 0.15 V		60	Mbps
				V_{CCB} = 3.3 V ± 0.3 V		60	
			Open-drain driving	V_{CCB} = 1.8 V ± 0.15 V		1	
				V_{CCB} = 3.3 V ± 0.3 V		1	
		Clock	Push-pull driving	V_{CCB} = 1.8 V ± 0.15 V		55	MHz
				V_{CCB} = 3.3 V ± 0.3 V		55	
		Data		V_{CCB} = 1.8 V ± 0.15 V		60	Mbps
				V_{CCB} = 3.3 V ± 0.3 V		60	
t_W	Pulse duration	Command	Push-pull driving	V_{CCB} = 1.8 V ± 0.15 V	17		ns
				V_{CCB} = 3.3 V ± 0.3 V	17		
			Open-drain driving	V_{CCB} = 1.8 V ± 0.15 V	1		µs
				V_{CCB} = 3.3 V ± 0.3 V	1		
		Clock	Push-pull driving	V_{CCB} = 1.8 V ± 0.15 V	9		ns
				V_{CCB} = 3.3 V ± 0.3 V	9		
		Data		V_{CCB} = 1.8 V ± 0.15 V	17		ns
				V_{CCB} = 3.3 V ± 0.3 V	17		

6.9 Switching Characteristics—V_{CCA} = 1.2 V ± 0.1 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	CMDA	CMDB	V_{CCB} = 1.8 V ± 0.15 V		5.7	ns
			V_{CCB} = 3.3 V ± 0.3 V		4.4	
	CMDB	CMDA	V_{CCB} = 1.8 V ± 0.15 V		6.7	
			V_{CCB} = 3.3 V ± 0.3 V		5.8	
	CLKA	CLKB	V_{CCB} = 1.8 V ± 0.15 V		6.2	
			V_{CCB} = 3.3 V ± 0.3 V		4.5	
	DATxA	DATxB	V_{CCB} = 1.8 V ± 0.15 V		7.6	
			V_{CCB} = 3.3 V ± 0.3 V		7.5	
	DATxB	DATxA	V_{CCB} = 1.8 V ± 0.15 V		6.3	
			V_{CCB} = 3.3 V ± 0.3 V		4.6	
	CLKA	CLK-f	V_{CCB} = 1.8 V ± 0.15 V		12	
			V_{CCB} = 3.3 V ± 0.3 V		7.9	
t_{en}	EN	B-port	V_{CCB} = 1.8 V ± 0.15 V		1	µs
			V_{CCB} = 3.3 V ± 0.3 V		1	
	EN	A-port	V_{CCB} = 1.8 V ± 0.15 V		1	
			V_{CCB} = 3.3 V ± 0.3 V		1	
t_{dis}	EN	B-port	V_{CCB} = 1.8 V ± 0.15 V		412	ns
			V_{CCB} = 3.3 V ± 0.3 V		363	
	EN	A-port	V_{CCB} = 1.8 V ± 0.15 V		423	
			V_{CCB} = 3.3 V ± 0.3 V		422	
t_{rA}	CMDA rise time		V_{CCB} = 1.8 V ± 0.15 V	3.5	8.4	ns
			V_{CCB} = 3.3 V ± 0.3 V	3.4	8.1	
	CLK-f rise time		V_{CCB} = 1.8 V ± 0.15 V	1	4.7	
			V_{CCB} = 3.3 V ± 0.3 V	1	4.1	
	DATxA rise time		V_{CCB} = 1.8 V ± 0.15 V	3.5	8.4	
			V_{CCB} = 3.3 V ± 0.3 V	3.4	8.1	
t_{rB}	CMDB rise time		V_{CCB} = 1.8 V ± 0.15 V	1.4	6.5	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.6	3.1	
	CLKB rise time		V_{CCB} = 1.8 V ± 0.15 V	0.6	5.9	
			V_{CCB} = 3.3 V ± 0.3 V	0.5	4.3	
	DATxB rise time		V_{CCB} = 1.8 V ± 0.15 V	1.4	10.9	
			V_{CCB} = 3.3 V ± 0.3 V	0.6	5	
t_{fA}	CMDA fall time		V_{CCB} = 1.8 V ± 0.15 V	2.4	5.7	ns
			V_{CCB} = 3.3 V ± 0.3 V	2	5.1	
	CLK-f fall time		V_{CCB} = 1.8 V ± 0.15 V	0.8	2.5	
			V_{CCB} = 3.3 V ± 0.3 V	0.8	3	
	DATxA fall time		V_{CCB} = 1.8 V ± 0.15 V	2.4	5.7	
			V_{CCB} = 3.3 V ± 0.3 V	1.9	5.1	
t_{fB}	CMDB fall time		V_{CCB} = 1.8 V ± 0.15 V	1.2	5.4	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.6	3.6	
	CLKB fall time		V_{CCB} = 1.8 V ± 0.15 V	0.6	6.3	
			V_{CCB} = 3.3 V ± 0.3 V	0.5	4	
	DATxB fall time		V_{CCB} = 1.8 V ± 0.15 V	0.6	6.3	
			V_{CCB} = 3.3 V ± 0.3 V	0.5	3.6	
$t_{SK(O)}$	Channel-to-channel skew		V_{CCB} = 1.8 V ± 0.15 V		1	ns
			V_{CCB} = 3.3 V ± 0.3 V		1	

Switching Characteristics—V_{CCA} = 1.2 V ± 0.1 V (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
Max data rate	Command	Push-pull driving	V_{CCB} = 1.8 V ± 0.15 V		40	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		40	
		Open-drain driving	V_{CCB} = 1.8 V ± 0.15 V		1	
			V_{CCB} = 3.3 V ± 0.3 V		1	
	Clock		V_{CCB} = 1.8 V ± 0.15 V		40	MHz
			V_{CCB} = 3.3 V ± 0.3 V		60	
	Data		V_{CCB} = 1.8 V ± 0.15 V		40	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		40	

6.10 Switching Characteristics—V_{CCA} = 1.8 V ± 0.15 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	CMDA	CMDB	V_{CCB} = 1.8 V ± 0.15 V		4.9	ns
			V_{CCB} = 3.3 V ± 0.3 V		3.3	
	CMDB	CMDA	V_{CCB} = 1.8 V ± 0.15 V		5.6	
			V_{CCB} = 3.3 V ± 0.3 V		3.6	
	CLKA	CLKB	V_{CCB} = 1.8 V ± 0.15 V		5.4	
			V_{CCB} = 3.3 V ± 0.3 V		3.4	
	DATxA	DATxB	V_{CCB} = 1.8 V ± 0.15 V		5	
			V_{CCB} = 3.3 V ± 0.3 V		4.4	
	DATxB	DATxA	V_{CCB} = 1.8 V ± 0.15 V		5.4	
			V_{CCB} = 3.3 V ± 0.3 V		3.5	
	CLKA	CLK-f	V_{CCB} = 1.8 V ± 0.15 V		10.2	
			V_{CCB} = 3.3 V ± 0.3 V		5.7	
t_{en}	EN	B-port	V_{CCB} = 1.8 V ± 0.15 V		1	µs
			V_{CCB} = 3.3 V ± 0.3 V		1	
	EN	A-port	V_{CCB} = 1.8 V ± 0.15 V		1	
			V_{CCB} = 3.3 V ± 0.3 V		1	
t_{dis}	EN	B-port	V_{CCB} = 1.8 V ± 0.15 V		411	ns
			V_{CCB} = 3.3 V ± 0.3 V		411	
	EN	A-port	V_{CCB} = 1.8 V ± 0.15 V		413	
			V_{CCB} = 3.3 V ± 0.3 V		361	
t_{rA}	CMDA rise time		V_{CCB} = 1.8 V ± 0.15 V	2.1	4.5	ns
			V_{CCB} = 3.3 V ± 0.3 V	2.1	4.1	
	CLK-f rise time		V_{CCB} = 1.8 V ± 0.15 V	0.6	2.5	
			V_{CCB} = 3.3 V ± 0.3 V	0.6	2.3	
	DATxA rise time		V_{CCB} = 1.8 V ± 0.15 V	1.8	4.5	
			V_{CCB} = 3.3 V ± 0.3 V	1.8	4.2	
t_{rB}	CMDB rise time		V_{CCB} = 1.8 V ± 0.15 V	1.4	6.6	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.7	3.8	
	CLKB rise time		V_{CCB} = 1.8 V ± 0.15 V	0.5	5.8	
			V_{CCB} = 3.3 V ± 0.3 V	0.5	4.4	
	DATxB rise time		V_{CCB} = 1.8 V ± 0.15 V	1.4	10.8	
			V_{CCB} = 3.3 V ± 0.3 V	0.7	8	

Switching Characteristics—V_{CCA} = 1.8 V ± 0.15 V (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{fA}	CMDA fall time		V_{CCB} = 1.8 V ± 0.15 V	0.4	3.4	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.3	2.9	
	CLK-f fall time		V_{CCB} = 1.8 V ± 0.15 V	0.3	2.8	
			V_{CCB} = 3.3 V ± 0.3 V	0.3	2.8	
	DATxA fall time		V_{CCB} = 1.8 V ± 0.15 V	0.4	3.4	
			V_{CCB} = 3.3 V ± 0.3 V	0.3	2.9	
t_{fB}	CMDB fall time		V_{CCB} = 1.8 V ± 0.15 V	1.1	6.3	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.6	3.7	
	CLKB fall time		V_{CCB} = 1.8 V ± 0.15 V	0.6	8.7	
			V_{CCB} = 3.3 V ± 0.3 V	0.5	4.1	
	DATxB fall time		V_{CCB} = 1.8 V ± 0.15 V	1.2	7	
			V_{CCB} = 3.3 V ± 0.3 V	0.2	4	
$t_{SK(O)}$	Channel-to-channel skew		V_{CCB} = 1.8 V ± 0.15 V		1	ns
			V_{CCB} = 3.3 V ± 0.3 V		1	
Max data rate	Command	Push-pull driving	V_{CCB} = 1.8 V ± 0.15 V		60	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		60	
		Open-drain driving	V_{CCB} = 1.8 V ± 0.15 V		1	
			V_{CCB} = 3.3 V ± 0.3 V		1	
	Clock		V_{CCB} = 1.8 V ± 0.15 V		60	MHz
			V_{CCB} = 3.3 V ± 0.3 V		60	
	Data		V_{CCB} = 1.8 V ± 0.15 V		60	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		60	

6.11 Switching Characteristics—V_{CCA} = 3.3 V ± 0.3 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	CMDA	CMDB	V_{CCB} = 1.8 V ± 0.15 V		5.3	ns
			V_{CCB} = 3.3 V ± 0.3 V		3.2	
	CMDB	CMDA	V_{CCB} = 1.8 V ± 0.15 V		5.1	
			V_{CCB} = 3.3 V ± 0.3 V		3	
	CLKA	CLKB	V_{CCB} = 1.8 V ± 0.15 V		4.8	
			V_{CCB} = 3.3 V ± 0.3 V		3.1	
	DATxA	DATxB	V_{CCB} = 1.8 V ± 0.15 V		5.1	
			V_{CCB} = 3.3 V ± 0.3 V		3.2	
	DATxB	DATxA	V_{CCB} = 1.8 V ± 0.15 V		9.6	
			V_{CCB} = 3.3 V ± 0.3 V		5.1	
	CLKA	CLK-f	V_{CCB} = 1.8 V ± 0.15 V		6.8	
			V_{CCB} = 3.3 V ± 0.3 V		4.2	
t_{en}	EN	B-port	V_{CCB} = 1.8 V ± 0.15 V		1	µs
			V_{CCB} = 3.3 V ± 0.3 V		1	
	EN	A-port	V_{CCB} = 1.8 V ± 0.15 V		1	
			V_{CCB} = 3.3 V ± 0.3 V		1	
t_{dis}	EN	B-port	V_{CCB} = 1.8 V ± 0.15 V		410	ns
			V_{CCB} = 3.3 V ± 0.3 V		364	
	EN	A-port	V_{CCB} = 1.8 V ± 0.15 V		396	
			V_{CCB} = 3.3 V ± 0.3 V		398	

Switching Characteristics—V_{CCA} = 3.3 V ± 0.3 V (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{rA}	CMDA rise time		V_{CCB} = 1.8 V ± 0.15 V	1.4	4.2	ns
			V_{CCB} = 3.3 V ± 0.3 V	1.4	4.2	
	CLK-f rise time		V_{CCB} = 1.8 V ± 0.15 V	0.5	1.5	
			V_{CCB} = 3.3 V ± 0.3 V	0.5	1.4	
	DATxA rise time		V_{CCB} = 1.8 V ± 0.15 V	1.4	3.4	
			V_{CCB} = 3.3 V ± 0.3 V	1.3	3	
t_{rB}	CMDB rise time		V_{CCB} = 1.8 V ± 0.15 V	1.4	6.4	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.9	4	
	CLKB rise time		V_{CCB} = 1.8 V ± 0.15 V	0.6	5.9	
			V_{CCB} = 3.3 V ± 0.3 V	0.5	4.4	
	DATxB rise time		V_{CCB} = 1.8 V ± 0.15 V	1.4	14	
			V_{CCB} = 3.3 V ± 0.3 V	0.9	14	
t_{fA}	CMDA fall time		V_{CCB} = 1.8 V ± 0.15 V	0.8	2.3	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.8	2.3	
	CLK-f fall time		V_{CCB} = 1.8 V ± 0.15 V	0.4	1.3	
			V_{CCB} = 3.3 V ± 0.3 V	0.4	1.3	
	DATxA fall time		V_{CCB} = 1.8 V ± 0.15 V	0.8	2.2	
			V_{CCB} = 3.3 V ± 0.3 V	0.7	2	
t_{fB}	CMDB fall time		V_{CCB} = 1.8 V ± 0.15 V	0.8	6.2	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.8	5	
	CLKB fall time		V_{CCB} = 1.8 V ± 0.15 V	0.6	7.8	
			V_{CCB} = 3.3 V ± 0.3 V	0.5	4.3	
	DATxB fall time		V_{CCB} = 1.8 V ± 0.15 V	0.7	6.8	
			V_{CCB} = 3.3 V ± 0.3 V	0.6	5	
$t_{SK(O)}$	Channel-to-channel skew		V_{CCB} = 1.8 V ± 0.15 V		1	ns
			V_{CCB} = 3.3 V ± 0.3 V		1	
Max data rate	Command	Push-pull driving	V_{CCB} = 1.8 V ± 0.15 V		60	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		60	
		Open-drain driving	V_{CCB} = 1.8 V ± 0.15 V		1	
			V_{CCB} = 3.3 V ± 0.3 V		1	
	Clock		V_{CCB} = 1.8 V ± 0.15 V		55	MHz
			V_{CCB} = 3.3 V ± 0.3 V		55	
	Data		V_{CCB} = 1.8 V ± 0.15 V		60	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		60	

6.12 Operating Characteristics —V_{CCA} = 1.2 V

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCB} TYP		UNIT
				1.8 V	3.3 V	
C_{pdA} (1)	A-port input, B-port output	CLK Enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	15.1	15	pF
		DATA Enabled		9.26	9.19	
	B-port input, A-port output	DATA Enabled		12.4	11.9	
	A-port input, B-port output	CLK Disabled		0.1	0.1	
		DATA Disabled		1.3	1.3	
	B-port input, A-port output	DATA Disabled		0.1	0.1	

(1) Power dissipation capacitance per transceiver.

Operating Characteristics —V_{CCA} = 1.2 V (continued)

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCB} TYP 1.8 V	V_{CCB} TYP 3.3 V	UNIT
C_{pdB} (1)	A-port input, B-port output	DATA Enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	26.7	30.3	pF
	B-port input, A-port output	CLK Enabled		25.6	27	
		DATA Enabled		16.38	19.91	
	A-port input, B-port output	DATA Disabled		0.1	0.1	
	B-port input, A-port output	CLK Disabled		0.1	0.1	
		DATA Disabled		1.1	0.8	

6.13 Operating Characteristics —V_{CCA} = 1.8 V

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCB} TYP 1.8 V	V_{CCB} TYP 3.3 V	UNIT
C_{pdA} (1)	A-port input, B-port output	CLK Enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	17.5	17.1	pF
		DATA Enabled		9.96	9.82	
	B-port input, A-port output	DATA Enabled		15.6	14	
	A-port input, B-port output	CLK Disabled		0.1	0.1	
		DATA Disabled		1.3	1.3	
	B-port input, A-port output	DATA Disabled		0.1	0.1	
C_{pdB} (1)	A-port input, B-port output	DATA Enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	26	28.5	pF
	B-port input, A-port output	CLK Enabled		25.8	27	
		DATA Enabled		16.69	19.6	
	A-port input, B-port output	DATA Disabled		0.1	0.1	
	B-port input, A-port output	CLK Disabled		0.1	0.1	
		DATA Disabled		1.1	0.8	

(1) Power dissipation capacitance per transceiver.

6.14 Operating Characteristics — V_{CCA} = 3.3 V

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCB} TYP 1.8 V	V_{CCB} TYP 3.3 V	UNIT
C_{pdA} (1)	A-port input, B-port output	CLK Enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	17.5	17.1	pF
		DATA Enabled		12.50	13.29	
	B-port input, A-port output	DATA Enabled		15.6	14	
	A-port input, B-port output	CLK Disabled		0.1	0.1	
		DATA Disabled		1.3	1.3	
	B-port input, A-port output	DATA Disabled		0.1	0.1	

(1) Power dissipation capacitance per transceiver.

Operating Characteristics — V_{CCA} = 3.3 V (continued)

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCB} TYP		UNIT
				1.8 V	3.3 V	
C_{pdB} (1)	A-port input, B-port output	DATA Enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	26	28.5	pF
	B-port input, A-port output	CLK Enabled		25.8	27	
		DATA Enabled		16.67	19.92	
	A-port input, B-port output	DATA Disabled		0.1	0.1	
	B-port input, A-port output	CLK Disabled		0.1	0.1	
		DATA Disabled		1.1	0.8	

6.15 Typical Characteristics

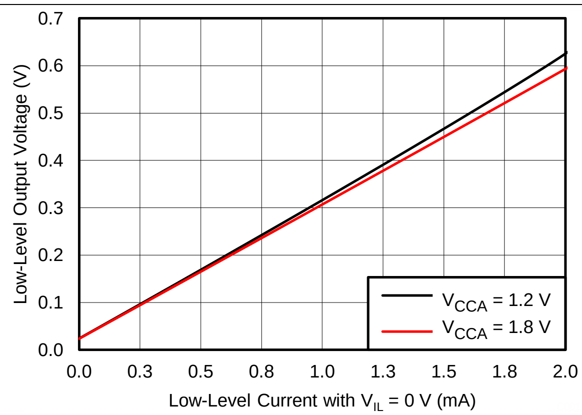


Figure 1. Low-Level Output Voltage (VOL(DATxB)) vs Low-Level Current (IOL(DATxA))

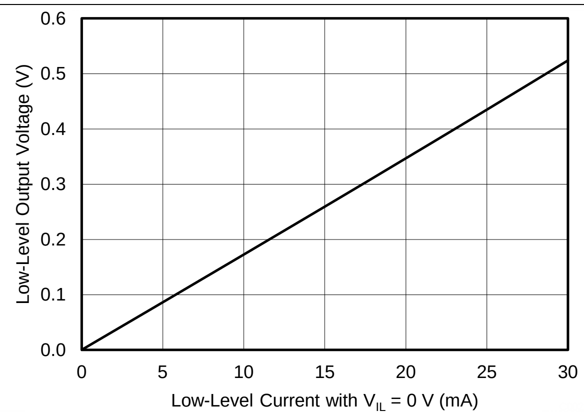
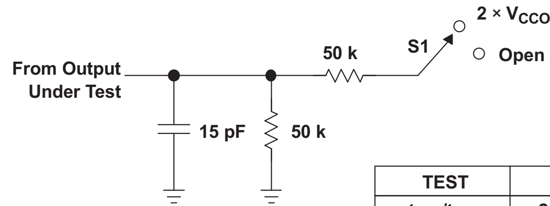


Figure 2. Low-Level Output Voltage (CLKB) vs Low-Level Current (CLKA)

7 Parameter Measurement Information

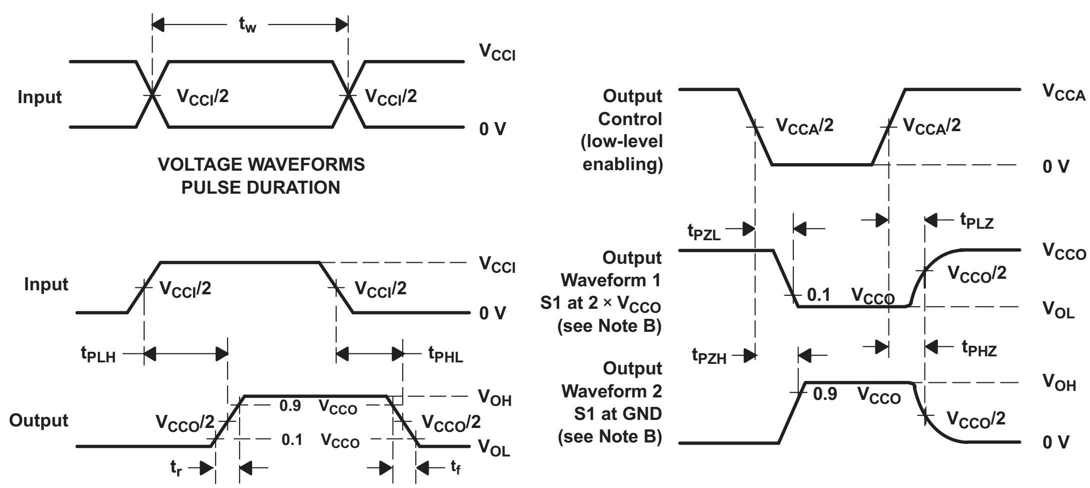
DATA RATE, PULSE DURATION, PROPAGATION DELAY, OUTPUT RISE AND FALL TIME MEASUREMENT USING A PUSH-PULL DRIVER

DATA RATE, PULSE DURATION, PROPAGATION DELAY, OUTPUT RISE AND FALL TIME MEASUREMENT USING AN OPEN-DRAIN DRIVER



LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT

TEST	S1
t_{PZL}/t_{PLZ}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z_O = 50 W, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.
J. All parameters and waveforms are not applicable to all devices.

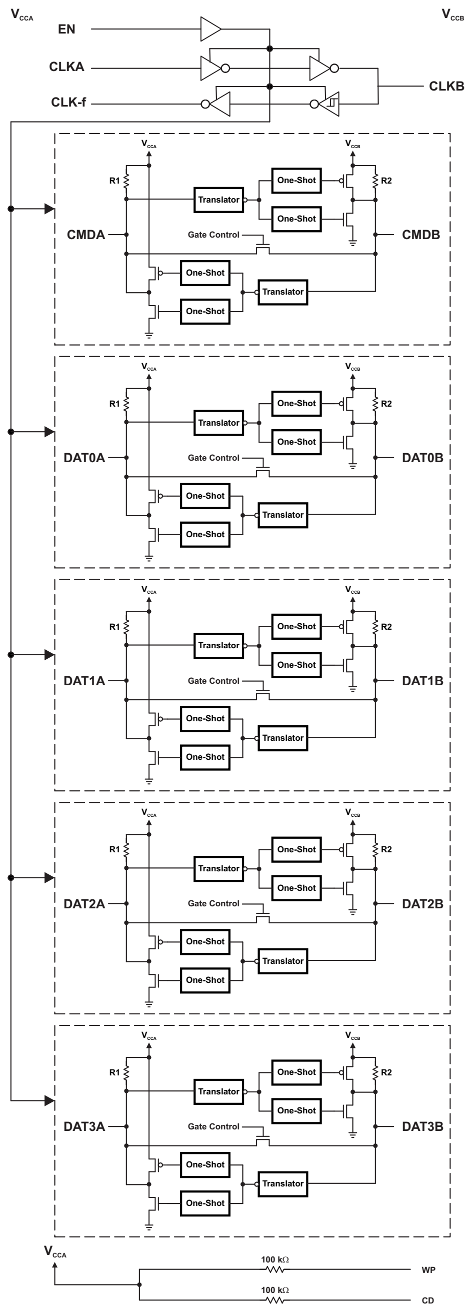
Figure 3. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The TXS0206A is a complete application-specific voltage-translator designed to bridge the digital switching compatibility gap and interface logic threshold levels between a micrprocessor with MMC, SD, and Memory Stick™ cards. It is intended to be used in a point-to-point topology when interfacing these devices that may or may not be operating at different interface voltages.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Architecture

The CLKA, CLKB, and CLK-f subsystem interfaces consist of a fully-buffered voltage translator design that has its output transistors to source and sink current optimized for drive strength. CLKA is a CMOS input and therefore must not be left floating.

The SDIO lines comprise a semi-buffered auto-direction-sensing based translator architecture (see Figure 4) that does not require a direction-control signal to control the direction of data flow of the A to B ports (or from B to A ports).

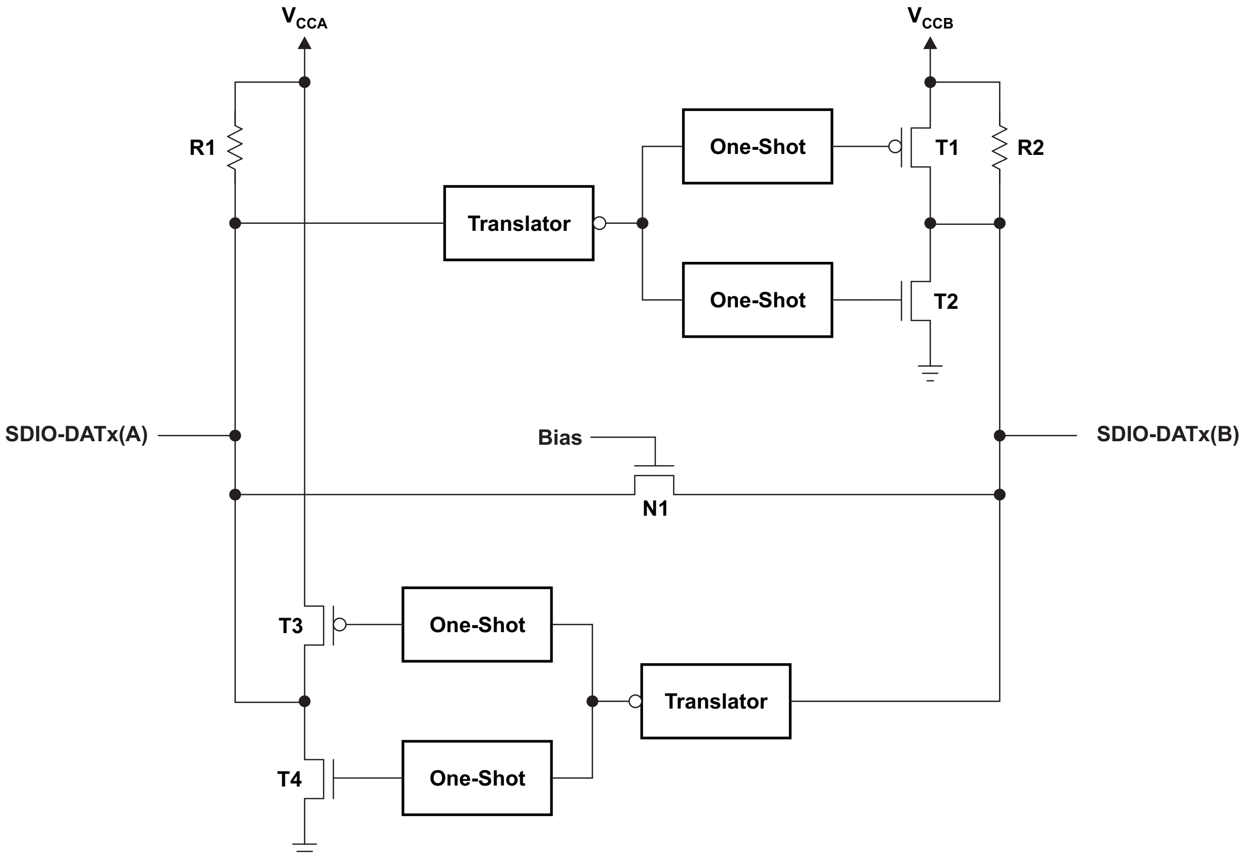

Figure 4. Architecture of an SDIO Switch-Type Cell

Each of these bidirectional SDIO channels independently determines the direction of data flow without a direction-control signal. Each I/O pin can be automatically reconfigured as either an input or an output, which is how this auto-direction feature is realized.

The following two key circuits are employed to facilitate the "switch-type" voltage translation function:

1. Integrated pullup resistors to provide dc-bias and drive capabilities
2. An N-channel pass-gate transistor topology (with a high R_{ON} of approximately 300 Ω) that ties the A-port to the B-port
3. Output one-shot (O.S.) edge-rate accelerator circuitry to detect and accelerate rising edges on the A or B ports

For bidirectional voltage translation, pullup resistors are included on the device for dc current sourcing capability. The V_{GATE} gate bias of the N-channel pass transistor is set at a level that optimizes the switch characteristics for maximum data rate as well as minimal static supply leakage. Data can flow in either direction without guidance from a control signal.

Feature Description (continued)

The edge-rate acceleration circuitry speeds up the output slew rate by monitoring the input edge for transitions, helping maintain the data rate through the device.

During a low-to-high signal rising-edge, the O.S. circuits turn on the PMOS transistors (T_1, T_3) and its associated driver output resistance of the driver is decreased to approximately 50 Ω to 70 Ω during this acceleration phase to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first. This edge-rate acceleration provides high ac drive by bypassing the internal pullup resistors during the low-to-high transition to speed up the rising-edge signal.

During a high-to-low signal falling-edge, the O.S. circuits turn on the NMOS transistors (T_2, T_4) and its associated driver output resistance of the driver is decreased to approximately 50 Ω to 70 Ω during this acceleration phase to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first.

To minimize dynamic I_{CC} and the possibility of signal contention, the user should wait for the O.S. circuit to turn-off before applying a signal in the opposite direction. The worst-case duration is equal to the minimum pulse-width number provided in the *Timing Requirements—V_{CCA} = 1.2 V ± 0.1 V* section of this data sheet.

Once the O.S. is triggered and switched off, both the A and B ports must go to the same state (i.e. both High or both Low) for the one-shot to trigger again. In a DC state, the output drivers maintain a Low state through the pass transistor. The output drivers maintain a High through the "smart pullup resistors" that dynamically change value based on whether a Low or a High is being passed through the SDIO lines, as follows:

- R_1 and R_2 values are a nominal 40 kΩ when the output is driving a low
- R_1 and R_2 values are a nominal 4 kΩ when the output is driving a high
- R_1 and R_2 values are a nominal 40 kΩ when the device is disabled via the EN pin or by pulling the either V_{CCA} or V_{CCB} to 0 V.
- The threshold at which the resistance changes is approximately $V_{CCx}/2$

The reason for using these "smart" pullup resistors is to allow the TXS0206 to realize a lower static power consumption (when the I/Os are low), support lower V_{OL} values for the same size pass-gate transistor, and improved simultaneous switching performance.

8.4 Device Functional Modes

Table 1 lists the functional modes of the TXS0206A.

Table 1. Function Table

EN	TRANSLATOR I/Os
L	Disabled, pulled to V_{CCA}, V_{CCB} through 40 kΩ
H	Active

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Systems engineers working with SD and MMC memory cards face a dilemma. These cards operate at a higher voltage node than the latest multimedia application processors, which have moved to smaller process technology nodes that support a maximum I/O interface voltage of 1.2 V. The problem is bridging the gap between these two voltage nodes while maintaining digital switching compatibility. The TXS0206A was designed specifically to address this. It is an auto direction sensing voltage level shifter that can interface with high speed SD and MMC cards because it supports a clock frequency of up to 60 MHz and each data channel supports up to 60 Mbps.

9.2 Typical Application

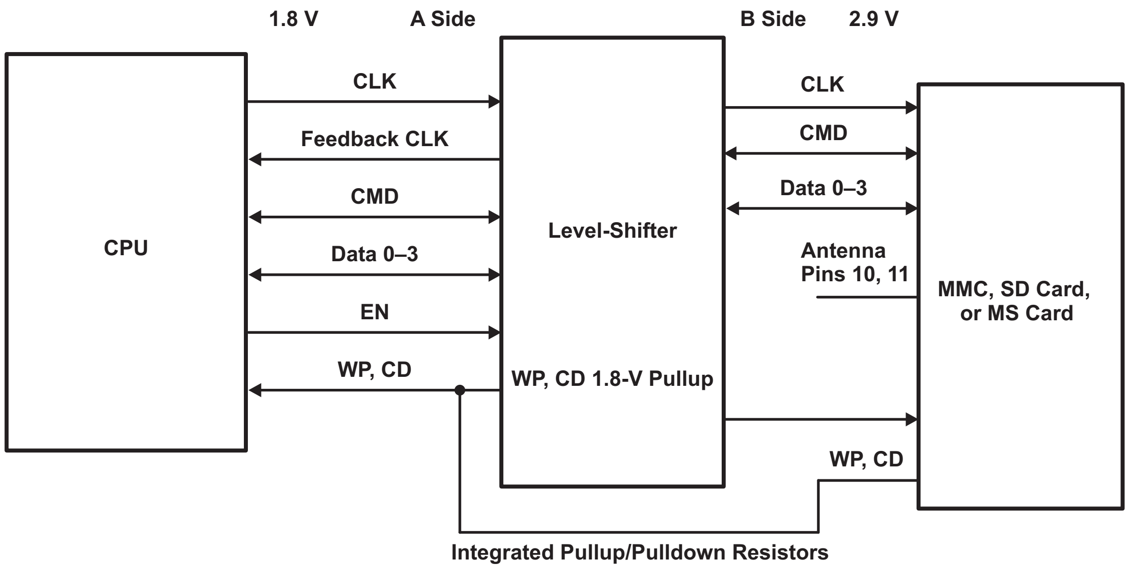

Figure 5. Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2

Table 2. Design Parameters

PARAMETERS	VALUES
Input voltage	1.1 V to 3.6 V
Output voltage	1.1 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the microprocessor that is driving the TXS0206A to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range

– Use the supply voltage of the memory card that the TXS0206A is driving to determine the output voltage range.

9.2.2.1 External Pulldown Resistors

When using the TXS0206A device with MMCs, SD, and Memory Stick™ to ensure that a valid receiver input voltage high (V_{IH}) is achieved, the value of any pulldown resistors (external or internal to a memory card) must not be smaller than a 10-kΩ value. The impact of adding too heavy (less than 10-kΩ value) a pulldown resistor to the data and command lines of the TXS0206A device and the resulting 4-kΩ pullup / 10-kΩ pulldown voltage divider network has a direct impact on the V_{IH} of the signal being sent into the memory card and its associated logic.

The resulting V_{IH} voltage for the 10-kΩ pulldown resistor value would be:

$V_{CC} \times 10\ k\Omega / (10\ k\Omega + 4\ k\Omega) = 0.714 \times V_{CC}$

This is marginally above a valid input high voltage for a 1.8-V signal (i.e., $0.65 \times V_{CC}$).

The resulting V_{IH} voltage for 20-kΩ pulldown resistor value would be:

$V_{CC} \times 20\ k\Omega / (20\ k\Omega + 4\ k\Omega) = 0.833 \times V_{CC}$

Which is above the valid input high voltage for a 1.8-V signal of $0.65 \times V_{CC}$.

9.2.3 Application Curves

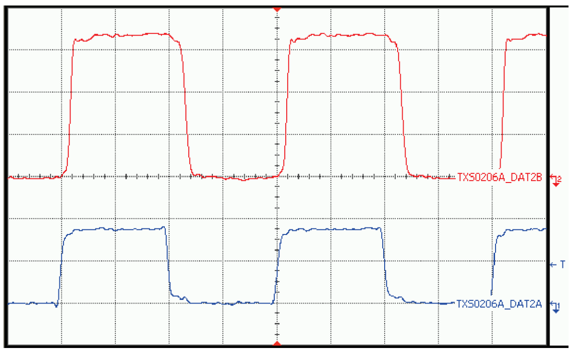

Figure 6. 1.8 V to 3.3 V Translation at 25 MHz

9.3 System Examples

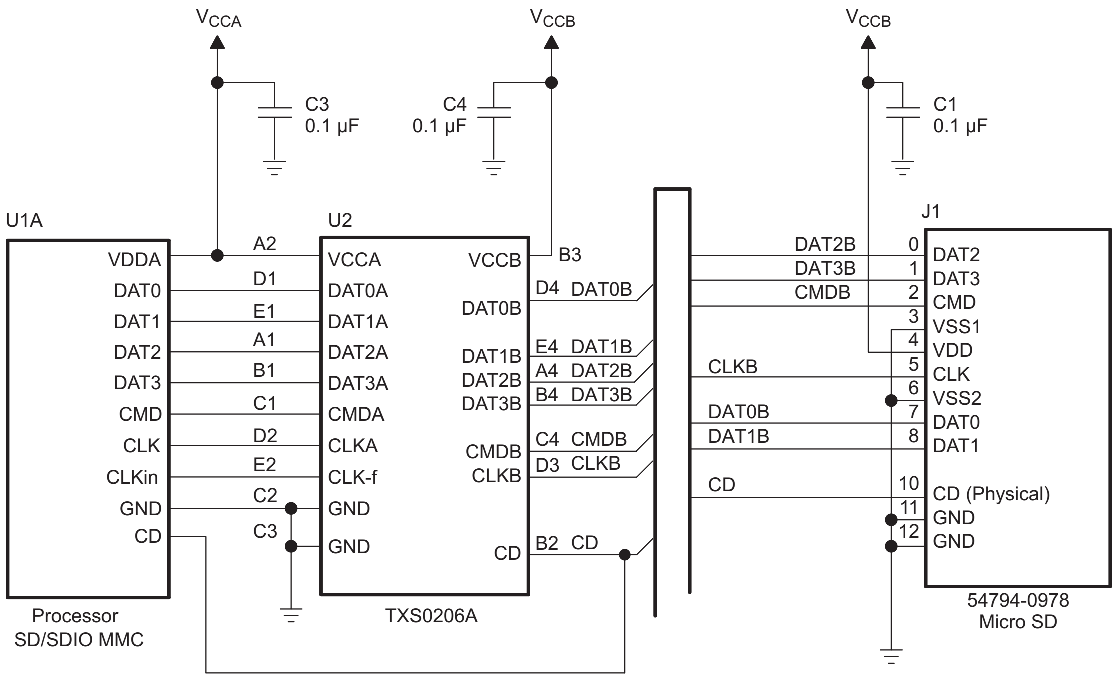

Figure 7. Interfacing With SD/SDIO Card

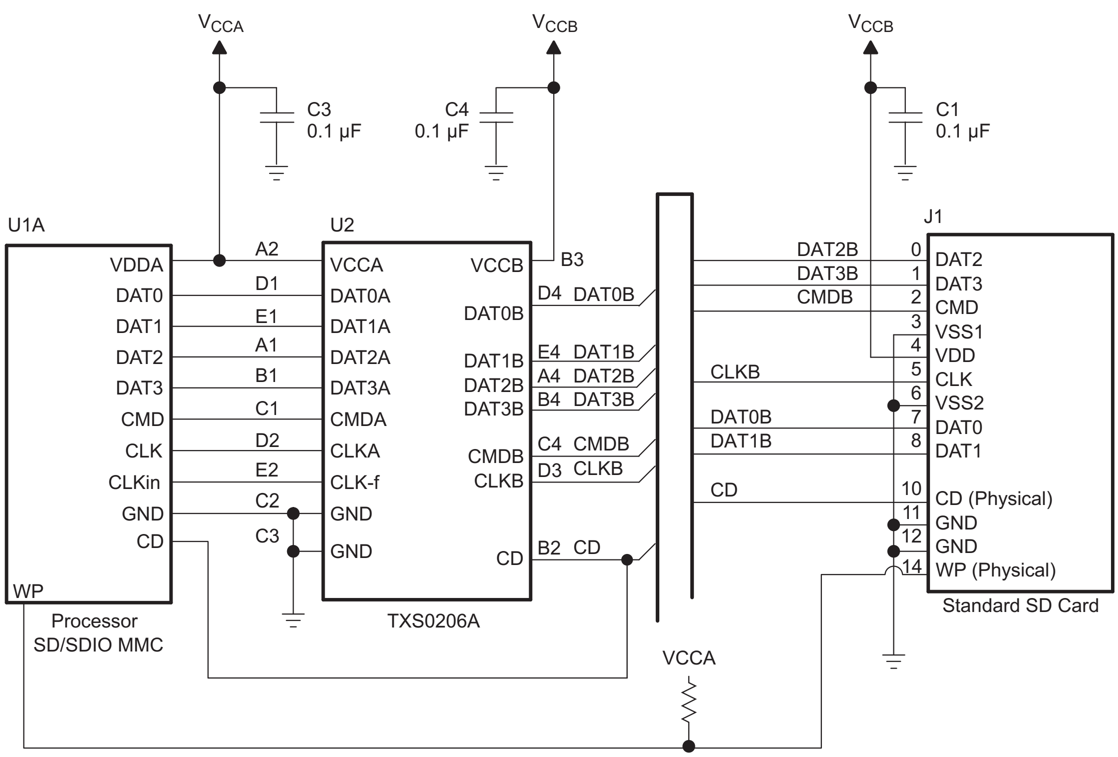

Figure 8. Interfacing With Seperate WP and CD Pin

System Examples (continued)

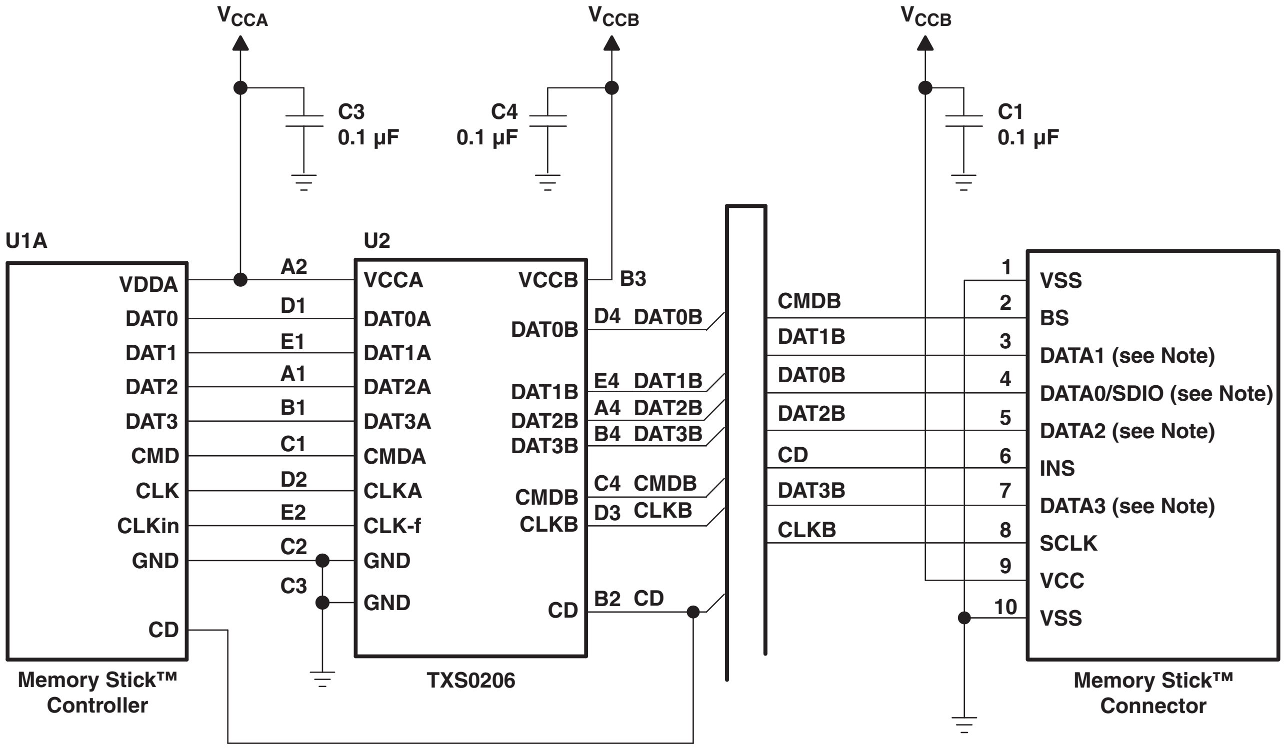

Figure 9. Interfacing With Memory Stick™ Card

10 Power Supply Recommendations

The TXS0206A does not require power sequencing between V_{CCA} and V_{CCB} during power-up so the power-supply rails can be ramped in any order.

The EN pin is referenced to V_{CCA} and when configured to low, will place all outputs into a high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the EN pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver controlling the EN pin.

Finally, the EN pin may be shorted to V_{CCA} if the application does not require use of the high-impedance state at any time.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, TI recommends following common printed-circuit board layout guidelines.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 30 ns, ensuring that any reflection encounters low impedance at the source driver
- With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail, so it is recommended that this lumped-load capacitance be considered and kept below 50 pF to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

11.2 Layout Example

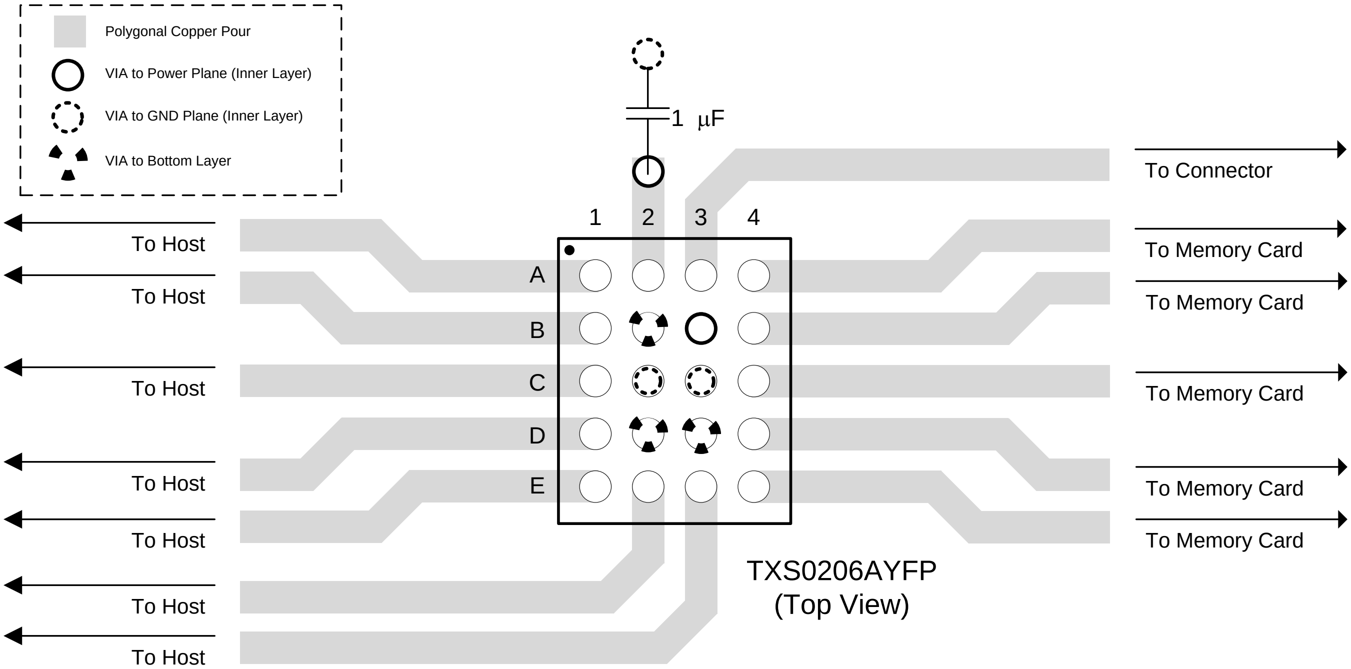

Figure 10. TXS0206A Example Layout (Top Layer)

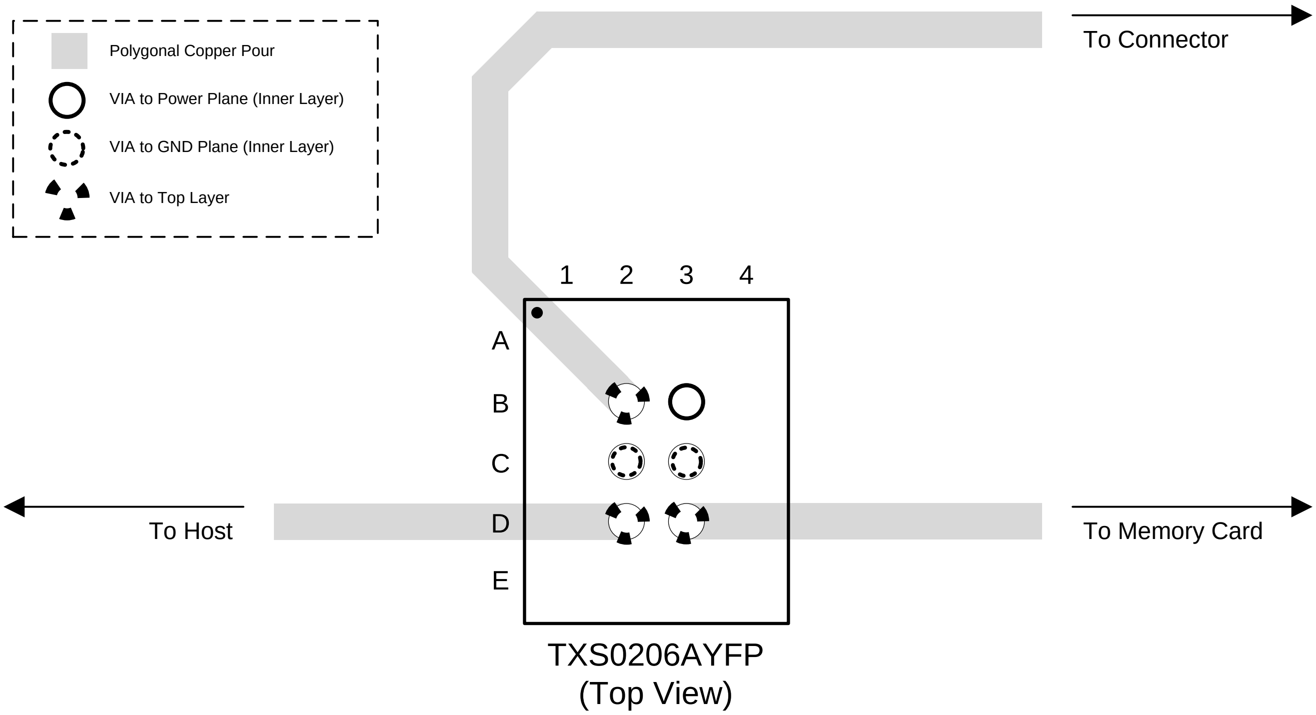

Figure 11. TXS0206A Example Layout (Bottom Layer)

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Introduction to Logic*, SLVA700.
- *TXS0206A Evaluation Module*, SCEU008.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXS0206AYFPR	ACTIVE	DSBGA	YFP	20	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TXS0206A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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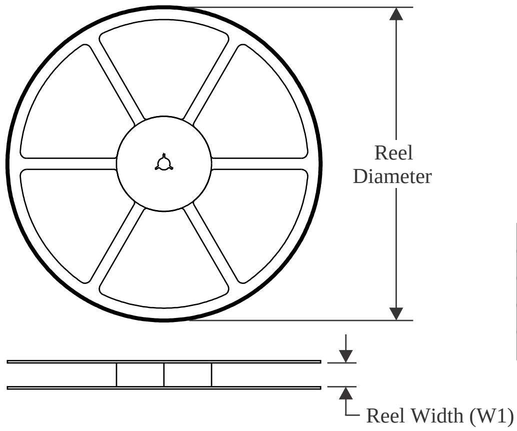
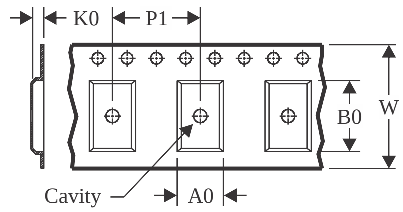
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

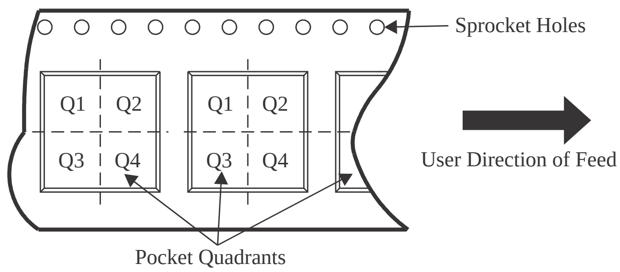


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

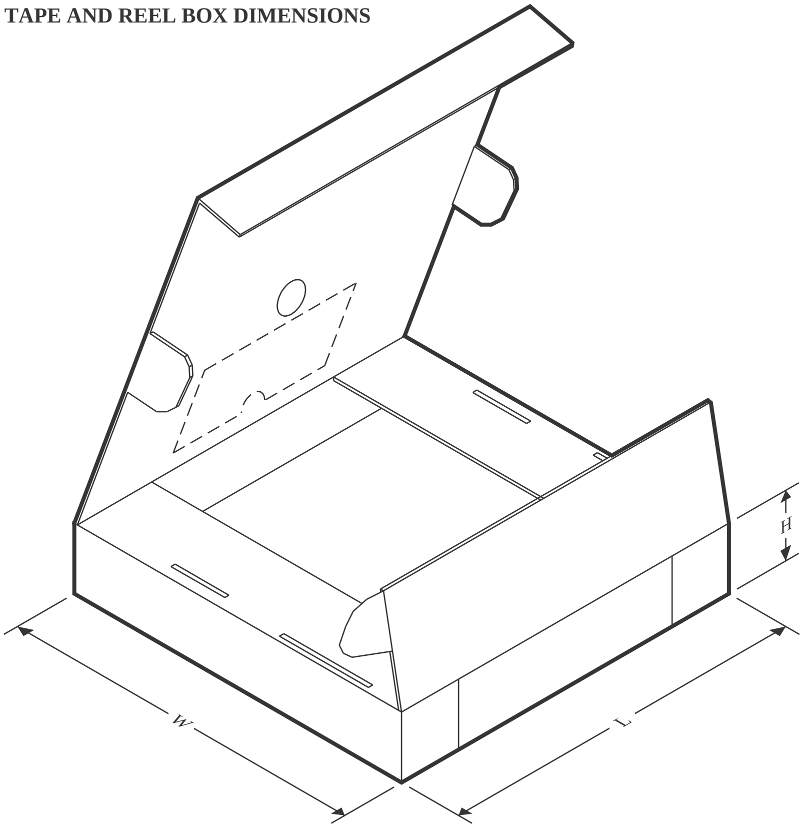
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

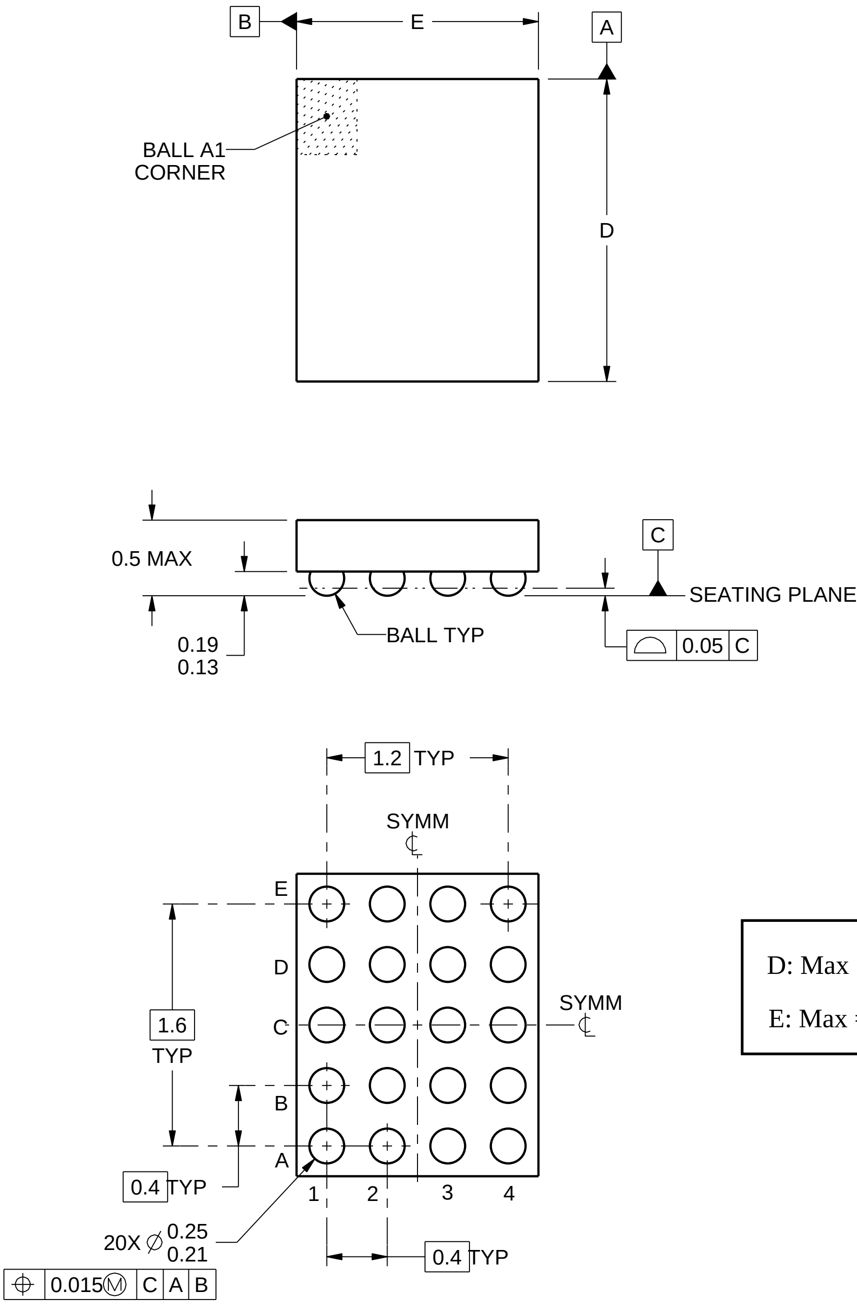
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0206AYFPR	DSBGA	YFP	20	3000	180.0	8.4	1.66	2.06	0.56	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0206AYFPR	DSBGA	YFP	20	3000	182.0	182.0	20.0



D: Max = 1.988 mm, Min =1.928 mm

E: Max = 1.588 mm, Min =1.527 mm

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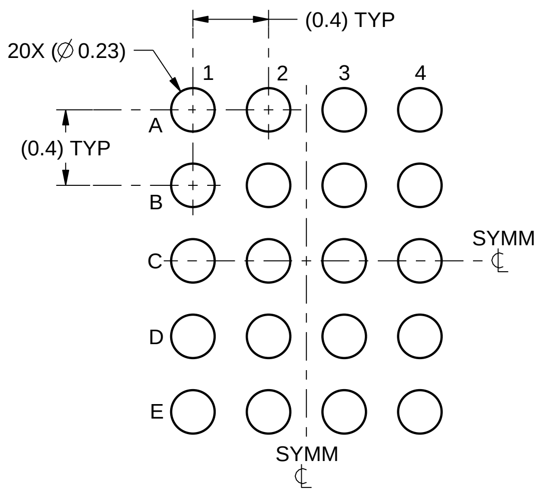
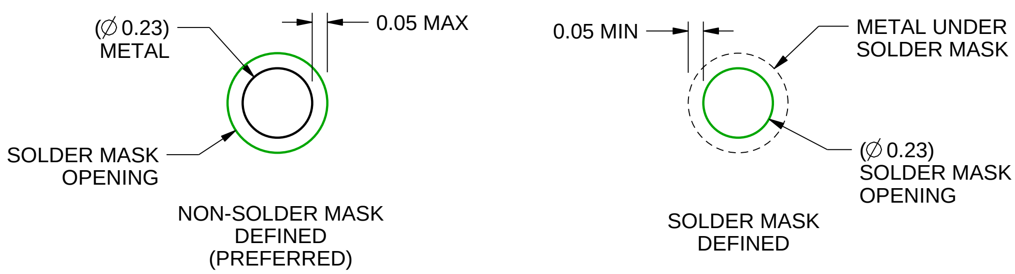
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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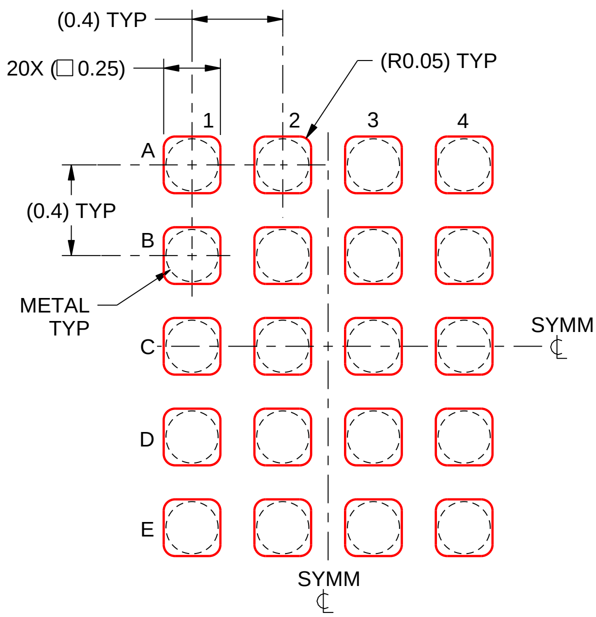
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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