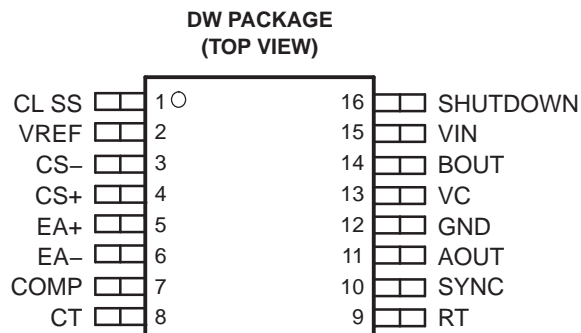


IMPROVED CURRENT MODE PWM CONTROLLER

 Check for Samples: [UC2856Q](#)

FEATURES

- Pin-for-Pin Compatible With the UC2846
- 65-ns Typical Delay From Shutdown to Outputs and 50-ns Typical Delay From Sync to Outputs
- Improved Current Sense Amplifier With Reduced Noise Sensitivity
- Differential Current Sense With 3-V Common Mode Range
- Trimmed Oscillator Discharge Current for Accurate Deadband Control
- Accurate 1-V Shutdown Threshold
- High Current Dual Totem Pole Outputs (1.5-A peak)
- TTL Compatible Oscillator SYNC Pin Thresholds
- 4-kV ESD Protection



P0008-01

DESCRIPTION

The UC2856 is a high performance version of the popular UC2846 series of current mode controllers, and is intended for both design upgrades and new applications where speed and accuracy are important. All input to output delays have been minimized, and the current sense output is slew rate limited to reduce noise sensitivity. Fast 1.5-A peak output stages have been added to allow rapid switching of power FETs.

A low impedance TTL compatible sync output has been implemented with a 3-state function when used as a sync input.

Internal chip grounding has been improved to minimize internal *noise* caused when driving large capacitive loads. This, in conjunction with the improved differential current sense amplifier, results in enhanced noise immunity.

Other features include a trimmed oscillator current (8%) for accurate frequency and dead time control; a 1 V, 5% shutdown threshold; and 4 kV minimum ESD protection on all pins.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOP-DW	Tape and reel	UC2856QDWR	UC2856Q

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UC2856Q

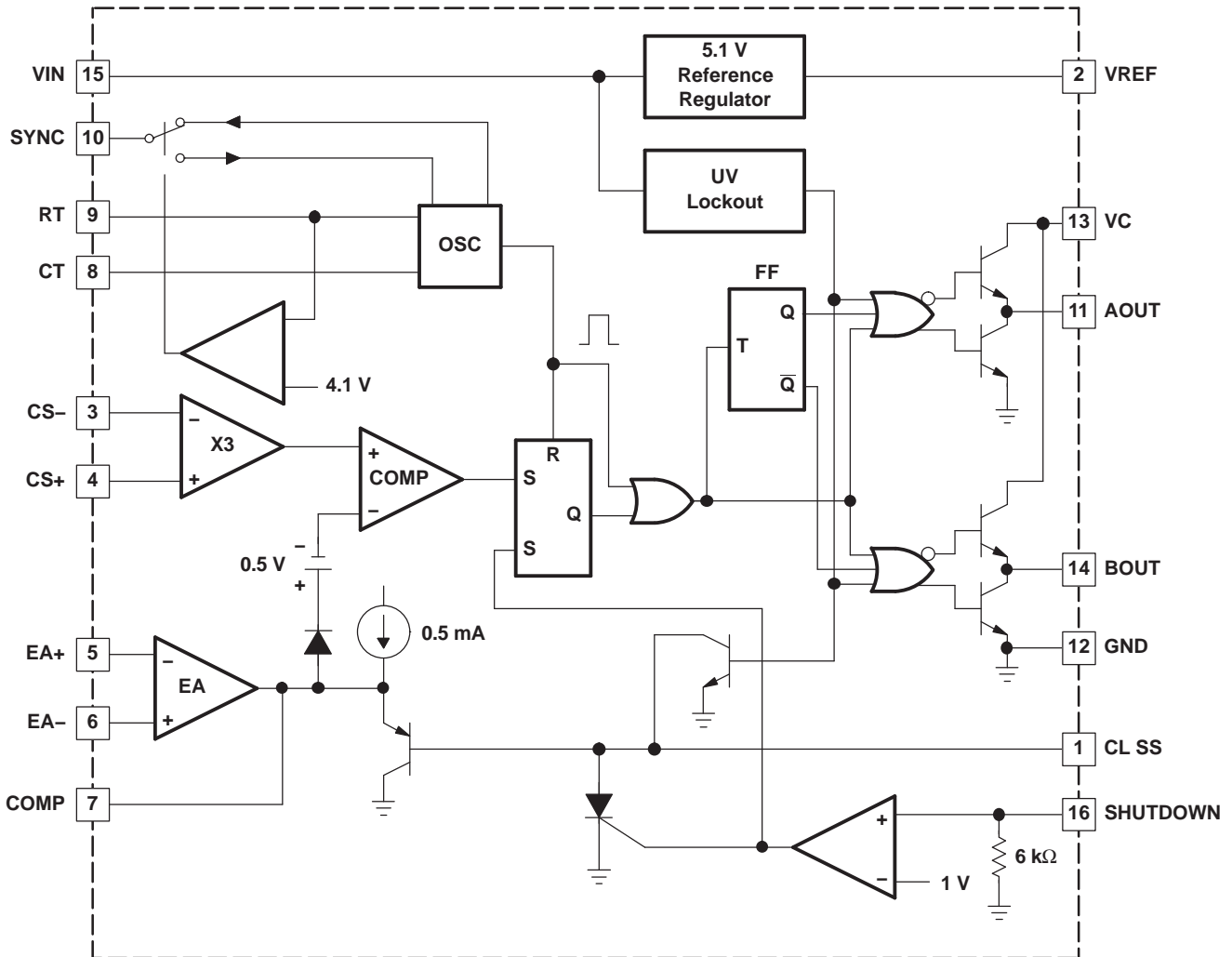
SGLS265A –NOVEMBER 2004–REVISED MAY 2011

www.ti.com



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

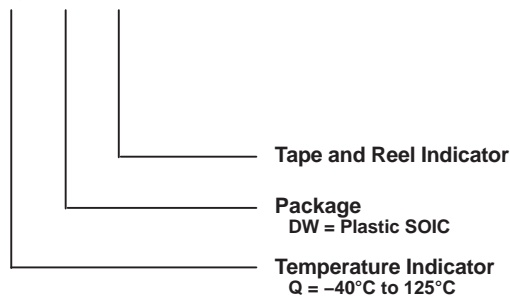
BLOCK DIAGRAM



B0010-01

ORDERING INFORMATION

UC 285 6 Q DW R



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		UNIT
Supply voltage		40 V
Collector supply voltage		40 V
I _O	Output current (sink or source)	DC
		Pulse (0.5 ms)
		0.5 A
		2 A
Error amplifier input voltage		-0.3 V to VIN
Shutdown input voltage		-0.3 V to 10 V
Current sense input voltage		-0.3 V to 3 V
SYNC output current		±10 mA
Error amplifier output current		-5 mA
Soft start sink current		50 mA
Oscillator charging current		5 mA
Power dissipation	T _A = 25°C	1 W
	T _C = 25°C	2 W
T _J	Operating junction temperature range	-55°C to 150°C
T _{stg}	Storage temperature range	-65°C to 150°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Unless otherwise indicated, voltages are reference to ground and currents are positive into and negative out of the specified terminals.

ELECTRICAL CHARACTERISTICS

T_A = -40°C to 125°C, VIN = 15 V, RT = 10 kΩ, CT = 1 nF, and T_A = T_J (unless otherwise stated)⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE SECTION					
Output voltage	I _O = 1 mA, T _J = 25°C	5.05	5.1	5.15	V
Line regulation voltage	VIN = 8 V to 40 V			20	mV
Load regulation voltage	I _O = -1 mA to -10 mA			15	mV
Total output variation	Line, Load, and Temperature	5		5.2	V
Output noise voltage	f = 10 Hz to 10 kHz, T _J = 25°C		50		μV
Long term stability	1000 hours, ⁽²⁾ T _J = 25°C		5	25	mV
Short circuit current	VREF = 0 V	-25	-45	-65	mA
OSCILLATOR SECTION					
Initial accuracy	T _J = 25°C	180	200	220	kHz
	T _J = Full range	170		230	
Voltage stability	VIN = 8 V to 40 V			2%	
Discharge current	VCT = 2 V, T _J = 25°C	7.5	8	8.8	mA
	VCT = 2 V	6.7	8	8.8	
Sync output high level voltage	I _O = -1 mA	2.4	3.6		V
Sync output low level voltage	I _O = 1 mA		0.2	0.4	V
Sync input high level voltage	CT = 0 V, RT = VREF	2	1.5		V
Sync input low level voltage	CT = 0 V, RT = VREF		1.5	0.8	V
Sync input current	CT = 0 V, RT = VREF, V _{SYNC} = 5 V		1	10	μA
Sync delay to outputs	CT = 0 V RT = VREF, V _{SYNC} = 0.8 V to 2 V		50	100	ns

- (1) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.
- (2) This parameter, although specified over the recommended operating conditions, is not 100% tested in production.

ELECTRICAL CHARACTERISTICS (continued)
 $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 15\text{ V}$, $R_T = 10\text{ k}\Omega$, $C_T = 1\text{ nF}$, and $T_A = T_J$ (unless otherwise stated)⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER SECTION					
Input offset voltage	$V_{CM} = 2\text{ V}$			5	mV
Input bias current				-1	μA
Input offset current				500	nA
Common mode range	$V_{IN} = 8\text{ V}$ to 40 V	0		$V_{IN}-2$	V
Open loop gain	$V_O = 1.2\text{ V}$ to 3 V	80	100		dB
Unity gain bandwidth	$T_J = 25^{\circ}\text{C}$	1	1.5		MHz
CMRR	$V_{CM} = 0\text{ V}$ to 38 V , $V_{IN} = 40\text{ V}$	75	100		dB
PSRR	$V_{IN} = 8\text{ V}$ to 40 V	80	100		dB
Output sink current	$V_{ID} = -15\text{ mV}$, $V_{COMP} = 1.2\text{ V}$	5	10		mA
Output source current	$V_{ID} = 15\text{ mV}$, $V_{COMP} = 2.5\text{ V}$	-0.4	-0.5		mA
High-level output voltage	$V_{ID} = 50\text{ mV}$, $R_L(\text{COMP}) = 15\text{ k}\Omega$	4.3	4.6	4.9	V
Low-level output voltage	$V_{ID} = -50\text{ mV}$, $R_L(\text{COMP}) = 15\text{ k}\Omega$		0.7	1	V
CURRENT SENSE AMPLIFIER SECTION					
Amplifier gain	$V_{CS-} = 0\text{ V}$, CL SS Open ⁽³⁾ ⁽⁴⁾	2.5	2.75	3	V/V
Maximum differential input signal ($V_{CS+} - V_{CS-}$)	CL SS Open 3, $R_L(\text{COMP}) = 15\text{ k}\Omega$	1.1	1.2		V
Input offset voltage	$V_{CL\text{ SS}} = 0.5\text{ V}$, COMP open ⁽³⁾		5	35	mV
CMRR	$V_{CM} = 0\text{ V}$ to 3 V	60			dB
PSRR	$V_{IN} = 8\text{ V}$ to 40 V	60			dB
Input bias current	$V_{CL\text{ SS}} = 0.5\text{ V}$, COMP open ⁽³⁾			-1	μA
Input offset current	$V_{CL\text{ SS}} = 0.5\text{ V}$, COMP open ⁽³⁾			1	mA
Input common mode range		0		3	V
Delay to outputs	$V_{EA+} = V_{REF}$, $EA- = 0\text{ V}$, $CS+ - CS- = 0\text{ V}$ to 1.5 V		120	250	ns
CURRENT LIMIT ADJUST SECTION					
Current limit offset	$V_{CS-} = 0\text{ V}$, $V_{CS+} = 0\text{ V}$, COMP Open ⁽³⁾	0.4	0.5	0.6	V
Input bias current	$V_{EA+} = V_{REF}$, $V_{EA-} = 0\text{ V}$		-10	-30	μA
SHUTDOWN TERMINAL SECTION					
Threshold voltage		0.95	1.00	1.05	V
Input voltage range		0		5	V
Minimum latching current ($I_{CL\text{ SS}}$)		⁽⁵⁾ 3	1.5		mA
Maximum non-latching current ($I_{CL\text{ SS}}$)			⁽⁶⁾ 1.5	0.8	mA
Delay to outputs	$V_{SHUTDOWN} = 0\text{ V}$ to 1.3 V		65	110	ns
OUTPUT SECTION					
Collector-emitter voltage		40			V
Off-state bias current	$V_C = 40\text{ V}$			250	μA
Output low level voltage	$I_{OUT} = 20\text{ mA}$		0.1	0.5	V
	$I_{OUT} = 200\text{ mA}$		0.5	2.6	
Output high level voltage	$I_{OUT} = -20\text{ mA}$	12.5	13.2		V
	$I_{OUT} = -200\text{ mA}$	12	13.1		
Rise time	$C_1 = 1\text{ nF}$		40	80	ns
Fall time	$C_1 = 1\text{ nF}$		40	80	ns
UVLO low saturation	$V_{IN} = 0\text{ V}$, $I_{OUT} = 20\text{ mA}$		0.8	1.5	V

(3) Parameter measured at trip point of latch with $V_{EA+} = V_{REF}$, $V_{EA-} = 0\text{ V}$.

$$G = \frac{\Delta V_{COMP}}{\Delta V_{CS+}}; \Delta V_{CS-} = 0\text{ V } 1\text{ V.}$$

(4) Amplifier gain defined as:

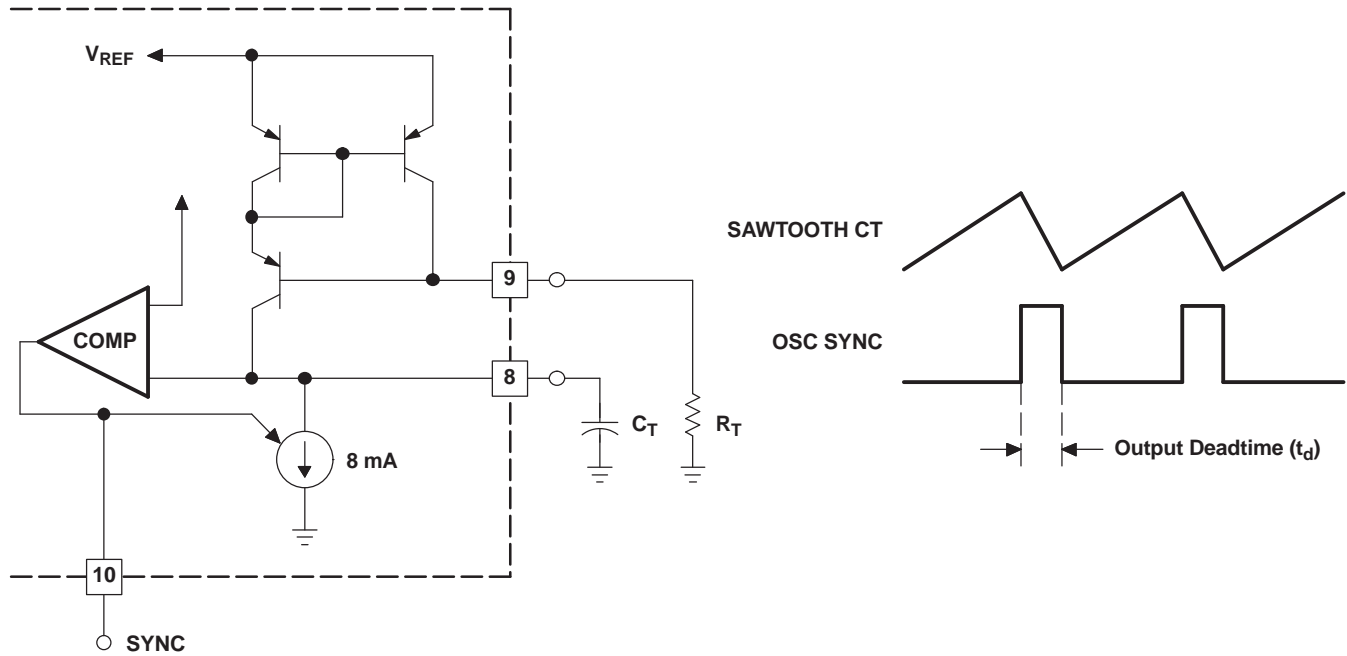
(5) Current into CL SS assured to latch circuit into shutdown state.

(6) Current into CL SS assured not to latch circuit into shutdown state.

ELECTRICAL CHARACTERISTICS (continued)
 $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 15\text{ V}$, $R_T = 10\text{ k}\Omega$, $C_T = 1\text{ nF}$, and $T_A = T_J$ (unless otherwise stated)⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM SECTION					
Maximum duty cycle		45%	47%	50%	
Minimum duty cycle				0%	
UNDERVOLTAGE LOCKOUT SECTION					
Startup threshold			7.7	8	
Threshold hysteresis			0.7		
TOTAL STANDBY CURRENT					
Supply current			18	23	mA

APPLICATION AND OPERATION INFORMATION

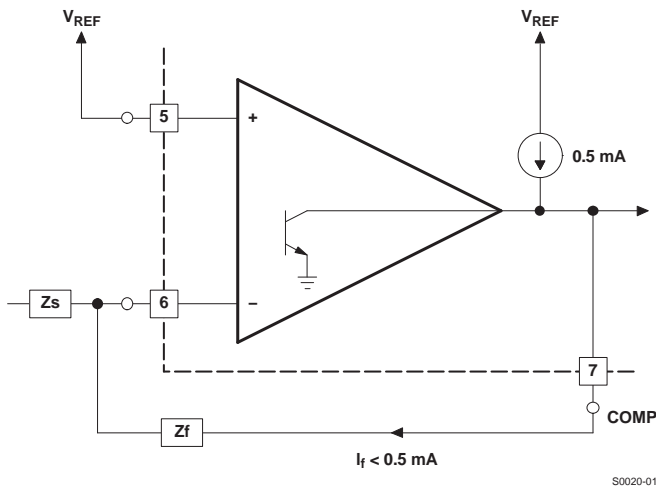


NOTE: Output deadtime is determined by the size of the external capacitor, C_T , according to the formula: $T_d = \frac{2C_T}{8 \text{ mA} - \frac{3.6}{R_T}}$
 For large values of R_T : $T_d = 250 C_T$
 Oscillator frequency is approximated by the formula: $f_T = \frac{2}{R_T \times C_T}$

S0019-01

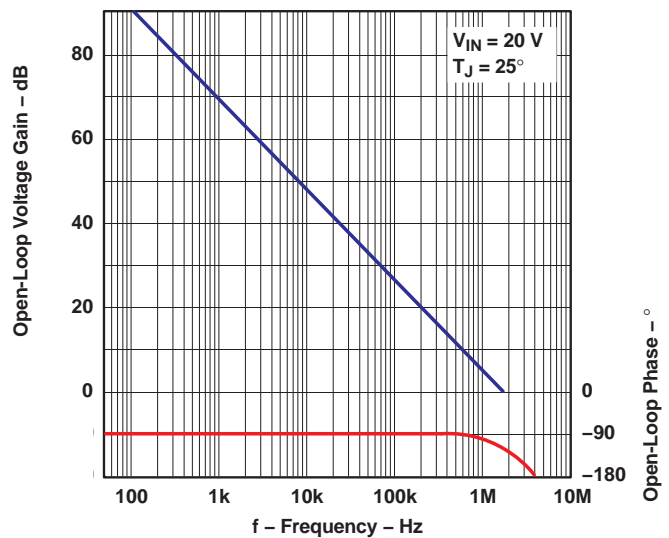
Figure 1. Oscillator Circuit

NOTE: Error Amplifier can source up to 0.5 mA.



S0020-01

Figure 2. Error Amplifier Output Configuration



G001

Figure 3. Error Amplifier Gain and Phase vs Frequency

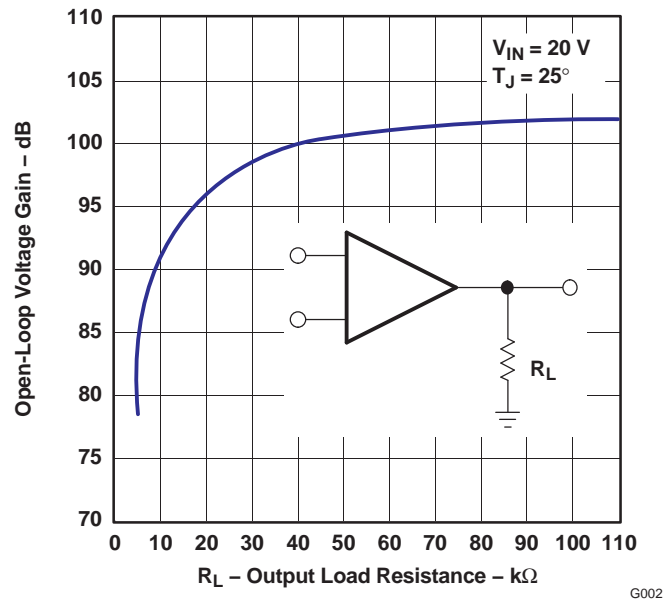
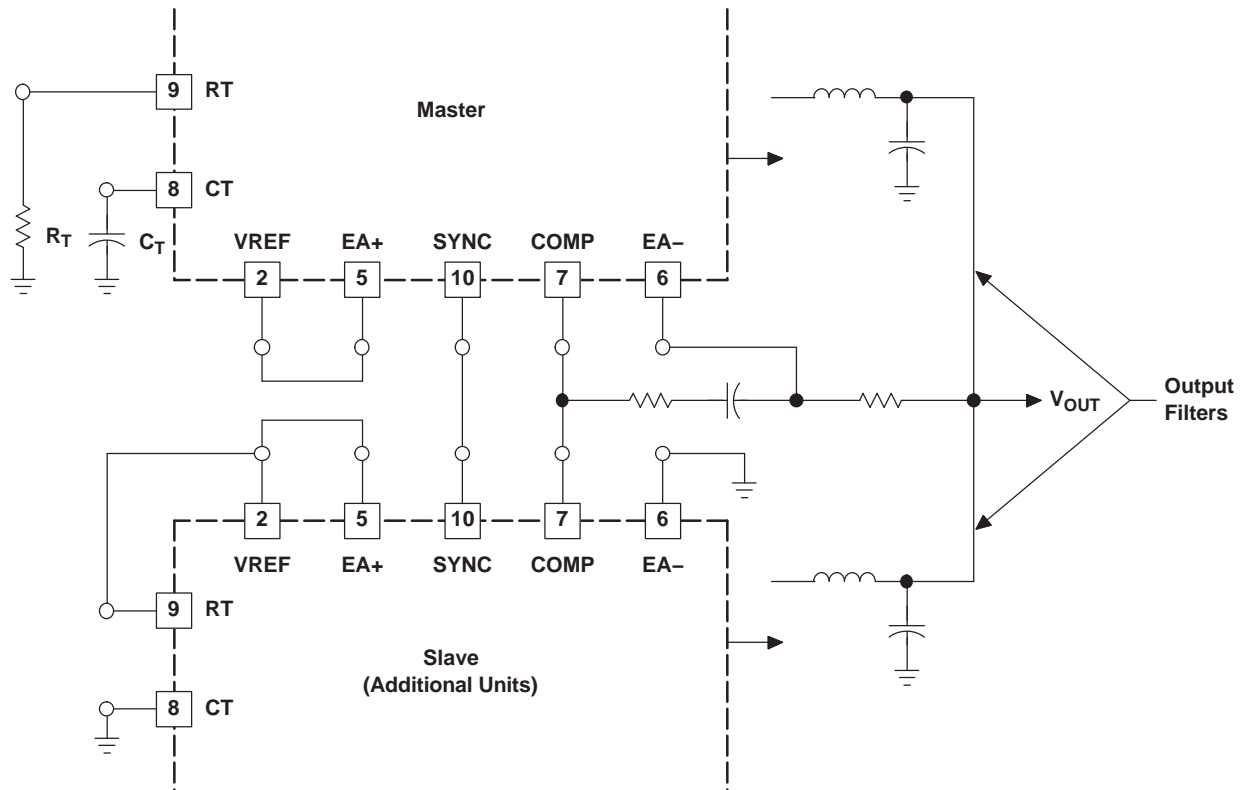


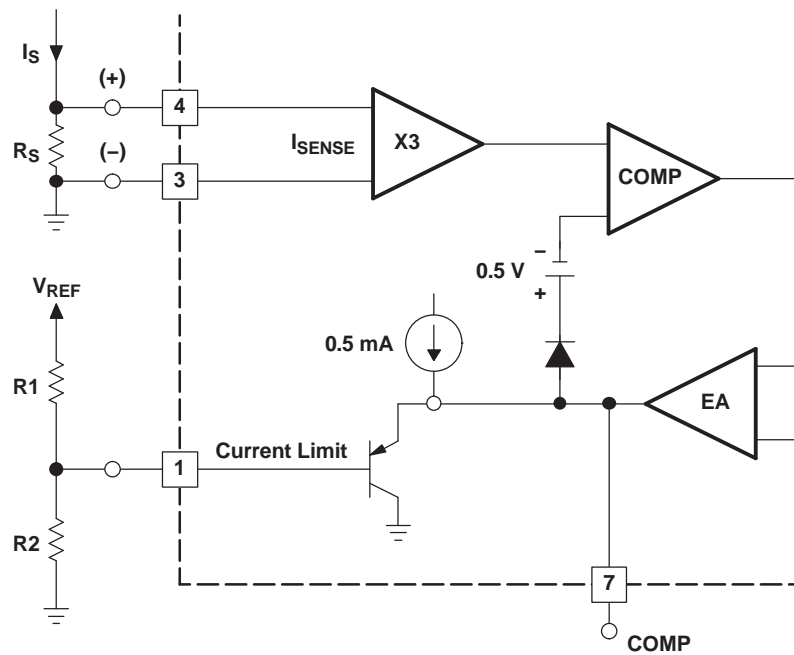
Figure 4. Error Amplifier Open-Loop DC Gain vs Load Resistance



NOTE: Slaving allows parallel operation of two or more units with equal current sharing.

Figure 5. Parallel Operation

S0021-01

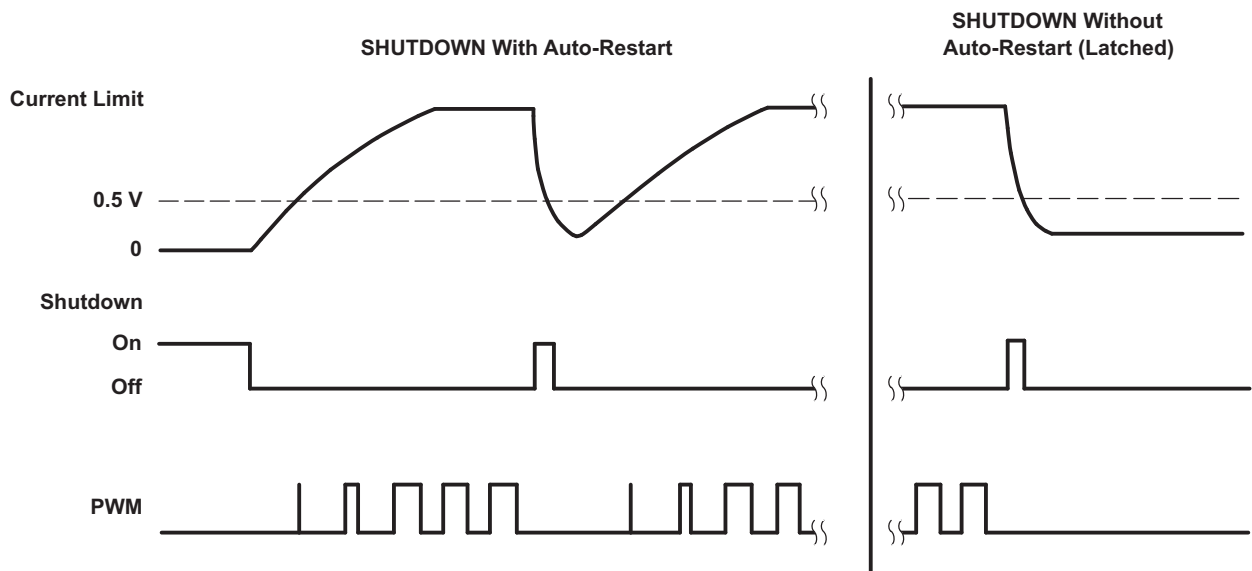
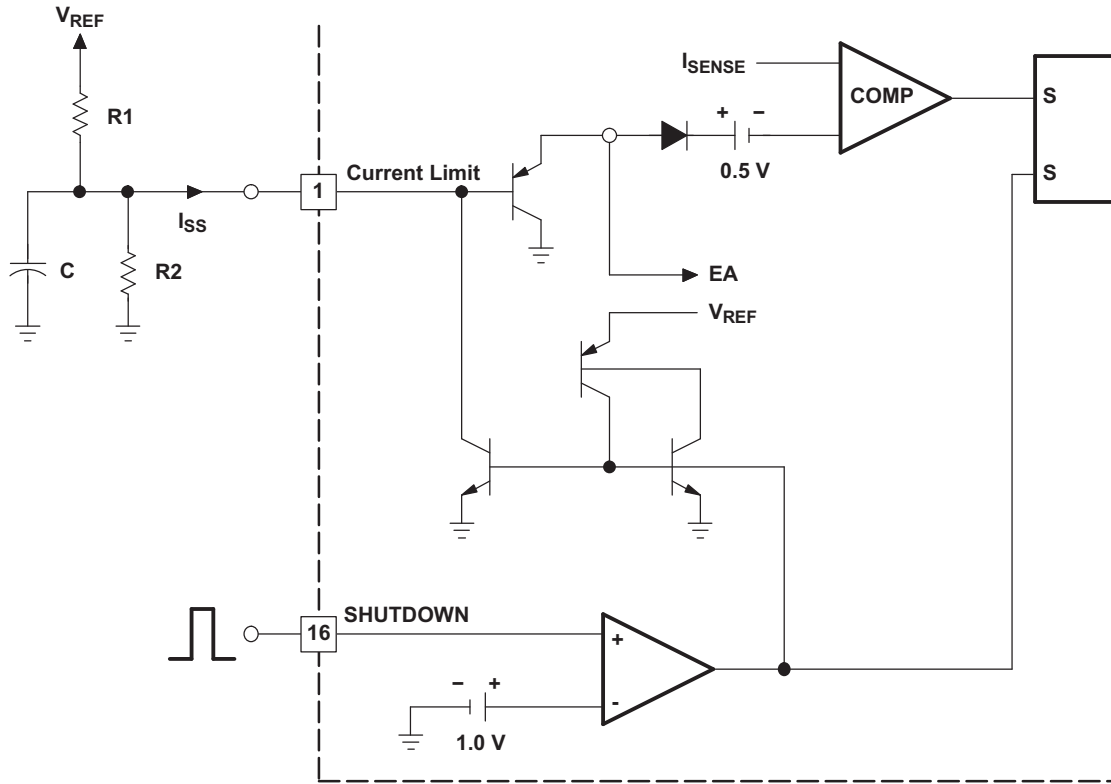


S0022-01

$$I_S = \frac{\left(R_2 \times \frac{V_{REF}}{R_1 + R_2} \right) - 0.5}{3R_S}$$

NOTE: Peak current (I_S) is determined by the formula:

Figure 6. Pulse by Pulse Current Limiting



S0023-01

NOTE: If $V_{REF} / R1 < 0.8 \text{ mA}$, the shutdown latch commutates when $I_{SS} = 0.8 \text{ mA}$ and a restart cycle will be initiated. If $V_{REF} / R1 > 3 \text{ mA}$, the device will latch off until power is recycled.

Figure 7. Shutdown

REVISION HISTORY

Changes from Original (November 2004) to Revision A	Page
• Changed the polarity of the comparator connected to pin 16 in Figure 7	9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2856QDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UC2856Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2856QDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2856QDWR	SOIC	DW	16	2000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A



DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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