UCC5710x-Q1 High-Speed, Low-Side Gate Drivers With DESAT Protection For Automotive Applications

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified
  - Device temperature grade 1
- Typical 3A sink 3A source output currents
- DESAT protection with programmable delay
- Soft turn-off when fault happens
- Absolute maximum VDD voltage: 30V
- Input and enable pins capable of withstanding up to –5V
- Tight UVLO thresholds for bias flexibility
- Typical 26ns propagation delay
- Self-protect driver with thermal shutdown function
- Wide bias voltage range
- Available in 5mm × 4mm SOIC-8 package
- Operating junction temperature range of –40°C to 150°C

2 Applications

- HEV/EV PTC heaters
- Traction inverters
- Residential EV chargers
- Motor drives
- HVAC compressors

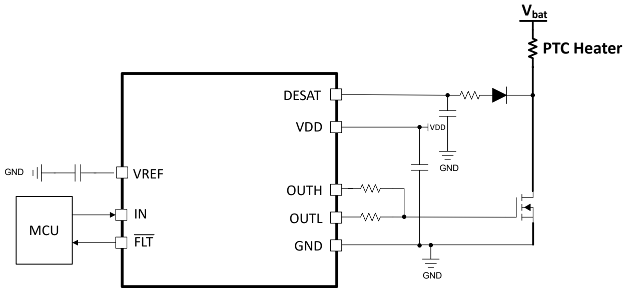
3 Description

The UCC5710x-Q1 is a single channel, high-performance low-side IGBT/SiC gate driver for high power automotive applications such as PTC heaters, traction inverter active discharge circuit, and other auxiliary subsystems. It offers protection features including Under-voltage-lock-out (UVLO), Desaturation protection (DESAT), FAULT report, and thermal shutdown protection. The UCC5710x-Q1 has a typical peak drive strength of 3A and it can handle –5V on its inputs, which improves robustness in systems with moderate ground bouncing. The inputs are independent of supply voltage and can be connected to most controller outputs for maximum control flexibility. Depending on the different pin configuration, the wide voltage range of the bias supply provided in the UCC5710xB-Q1 accommodates bipolar voltage. Also, seperate high and low driver outputs (UCC5710xC-Q1) and an enable function (UCC5710xW-Q1) are provided. An accurate 5V output is available with the UCC5710xB-Q1 and UCC5710xC-Q1.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]	BODY SIZE (NOM)
UCC5710xB-Q1	D (SOIC 8)	4.9mm × 6.0mm	4.90mm × 3.91mm
UCC5710xC-Q1	D (SOIC 8)	4.9mm × 6.0mm	4.90mm × 3.91mm
UCC5710xW-Q1	D (SOIC 8)	4.9mm × 6.0mm	4.90mm × 3.91mm

(1) For all available packages, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application Diagram

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4 Pin Configuration and Functions

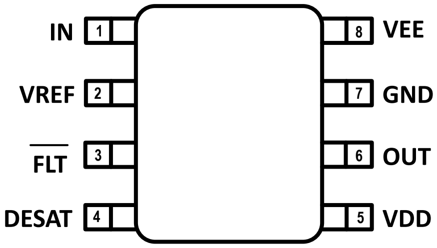


Figure 4-1. UCC5710xB-Q1 D Package SOIC-8 Top View

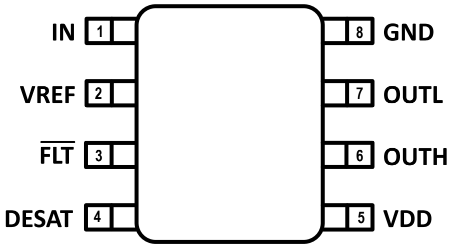


Figure 4-2. UCC5710xC-Q1 D Package SOIC-8 Top View

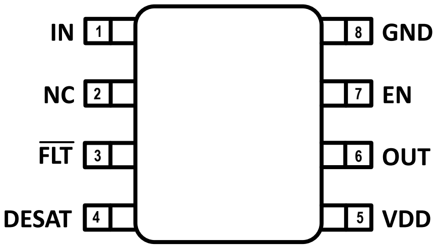


Figure 4-3. UCC5710xW-Q1 D Package SOIC-8 Top View

Table 4-1. Pin Functions

PIN				TYPE[1]	DESCRIPTION
NAME	UCC5710xB-Q1	UCC5710xC-Q1	UCC5710xW-Q1		
IN	1	1	1	I	Non-inverting PWM input
VREF	2	2	NA	O	5V Reference generated within the driver
NC	NA	NA	2		Not Connected
FLTb	3	3	3	O	Active low fault reporting
DESAT	4	4	4	I	Input for detecting the desatuation fault
VDD	5	5	5	P	Driver bias supply
OUT	6	NA	6	O	Output of the driver
OUTH	NA	6	NA	O	Driver high output
EN	NA	NA	6	I	Enable or disable control pin.
OUTL	NA	7	NA	O	Driver low output
GND	7	8	8	G	Driver ground
VEE	8	NA	NA	P	Driver negtive bias supply with respect to GND

(1) I/O = Digital input/output, IA = Analog input, AO= Analog output, P = Power connection

5 Specifications

5.1 Absolute Maximum Ratings

All the voltages are with respect to GND. Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD-GND	Positive power supply	–0.3	30	V
VDD-VEE	Differential Power Supply	-0.3	30	V
VEE-GND	Negative Power Supply	-18	0.3	V
OUT	Output signal DC voltage	GND/VEE–0.3	VDD+0.3	V
	Output signal transient voltage for 200-ns	GND/VEE–2	VDD+3	V
V_{DESAT}	Desat voltage	–0.3	VDD+0.3	V
V_{IN}	IN signal DC voltage	–5	30	V
V_{EN}	EN signal DC voltage (W Version)	–5	30	V
$I_{\overline{FLT}}$	$\overline{FLT}$ current sink		20	mA
$V_{\overline{FLT}}$	External pull-up	-0.3	VDD+0.3	V
T_J	Junction temperature	–40	150	℃
T_{stg}	Storage temperature	–65	150	℃

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Thermal Information

THERMAL METRIC(1)	THERMAL METRIC(1)	UCC5710X-Q1	UNIT
		D	
		8PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	132.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	75.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Recommended Operating Conditions

All voltages are with reference to GND. Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD-GND	Positive Power Supply (8V UVLO Option)	8.5		26	V
VDD-GND	Positive Power Supply (12.5V UVLO Option)	14.5		26	V

5.4 Recommended Operating Conditions (continued)

All voltages are with reference to GND. Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD-VEE	Differential Power Supply			26	V
VEE-GND	Negative Power Supply	-15		0	V
V_{OUT}	Output Voltage	GND/VEE		VDD	V
V_{IN}	IN signal DC voltage	-2		26	V
V_{EN}	EN signal DC voltage (W Version)	-2		26	V
T_J	Junction temperature	–40		150	℃

5.5 Electrical Characteristics

VDD = 15 V, VEE = 0 V, 1-µF capacitor from VDD to GND, 1-µF capacitor from VEE to GND, TJ = –40°C to +150°C, CL = 0 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VDDQ}	VDD quiescent supply current	V_{IN} = 3.3V, EN = 5V, VDD = 6.5V			1.4	mA
I_{VDD}	VDD static supply current	V_{IN} = 3.3 V, EN = 5V		1.1	1.5	mA
I_{VDD}	VDD static supply current	V_{IN} = 0 V, EN = 5V		0.8	1.2	mA
I_{VEEQ}	VEE static supply current	V_{IN} = 0 V, EN = 5V, VEE = -10V			1.1	mA
I_{VDDO}	VDD dynamic operating current	f_{SW} = 1 MHz, EN = 5V, VDD=15 V, C_L=1.8nF			35	mA
I_{DIS}	VDD disable current	V_{IN} = 3.3 V, EN = 0 V		0.8	1.1	mA
VDD UNDERVOLTAGE THRESHOLDS AND DELAY						
V_{VDD_ON}	VDD UVLO Rising Threshold	8-V UVLO Option	7.6	8	8.4	V
V_{VDD_OFF}	VDD UVLO Falling Threshold	8-V UVLO Option	6.65	7	7.35	V
V_{VDD_HYS}	VDD UVLO Threshold Hysteresis	8-V UVLO Option		1		V
$t_{UVLO2FLT}$	Propagation delay from UVLO shutdown to $\overline{FLT}$			8.4		us
V_{VDD_ON}	VDD UVLO Rising Threshold	12.5-V UVLO Option	12.8	13.5	14.2	V
V_{VDD_OFF}	VDD UVLO Falling Threshold	12.5-V UVLO Option	11.8	12.5	13.2	V
V_{VDD_HYS}	VDD UVLO Threshold Hysteresis	12.5-V UVLO Option		1.0		V
VREF						
V_{REF}	Voltage Reference	I_{REF}=10mA		5		V
I_{REF}	Reference output current				20	mA
IN, EN						
V_{INH}	Input High Threshold Voltage		1.8	2.2	2.6	V
V_{INL}	Input Low Threshold Voltage		0.8	1.2	1.6	V
V_{IN_HYS}	Input-threshold Hysteresis			1.0		V
R_{IND}	IN Pin Pull Down Resistance	IN=EN= 3.3V		120		kΩ
V_{ENH}	Enable High Threshold Voltage		1.8	2.2	2.6	V
V_{ENL}	Enable Low Threshold Voltage		0.8	1.2	1.6	V
V_{EN_HYS}	Enable Threshold Hysteresis			1		V
R_{ENU}	EN Pin Pull Up Resistance	EN = 0V		400		kΩ
$V_{\overline{FLT}th}$	$\overline{FLT}$ threshold voltage	$I_{\overline{FLT}\text{-sink}}$ = 15mA		0.43	1	V
DESAT DETECTION						
I_{CHG}	Blanking capacitor charge current	V_{DESAT} = 3.25V	200	250	316	µA
I_{DCHG}	DESAT pin discharge current	V_{DESAT} = 8V		-20		mA

5.5 Electrical Characteristics (continued)

VDD = 15 V, VEE = 0 V, 1-μF capacitor from VDD to GND, 1-μF capacitor from VEE to GND, TJ = –40°C to +150°C, CL = 0 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DESATTH}$	DESAT Detection Threshold		6.0	6.5	7.0	V
V_{DESLO}	DESAT voltage when OUT=L, referenced to GND				100	mV
$t_{DESLEB1}$ (1)	Leading edge blanking time			150		ns
t_{DESFIL} (1)	DESAT deglitch filter			100	150	ns
$t_{DES2OUT}$ (1)	DESAT propagation delay to 90% of OUT	V_{DESAT}>$V_{DESATTH}$		140	250	ns
$t_{DES2FLT}$ (1)	DESAT propagation delay to $\overline{FLT}$ low	$V_{DESATTH}$ to 90% of $\overline{FLT}$		135	250	ns
SOFT TURN OFF						
R_{STO}	Internal Soft turn-off Pulldown Resistance	DESAT triggered, V_{OUT}=5V		35		Ω
OVERTEMPERATURE PROTECTION						
T_{SD} (1)	Overtemperature threshold			180		C
T_{HYS} (1)	Overtemperature protection hysteresis			30		C
$t_{OTP2FLT}$ (1)	Propagation delay from overtemperature shutdown to $\overline{FLT}$	Over temperature shutdow to 90% of $\overline{FLT}$		8		us
OUTPUT DRIVER STAGE						
I_{SRCPK} (1)	Peak Output Source Current	C_{VDD} = 10 μF, C_L = 0.1 μF, f = 1 kHz		-3		A
I_{SNKPK} (1)	Peak Output Sink Current	C_{VDD} = 10 μF, C_L = 0.1 μF, f = 1 kHz		3		A
R_{OH}	Pull up resistance	I_{OUT} = –500mA		5		Ω
R_{OL}	Pull down resistance	I_{OUT} = 500mA		1		Ω

(1) Parameters are not tested in production.

5.6 Switching Characteristics

VDD = 15 V, VEE = 0 V, 1-μF capacitor from VDD to GND, 1-μF capacitor from VEE to GND, TJ = –40°C to +150°C, CL = 0 pF, unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RA}, t_{RB}	Output Rise Time	C_L=1.8nF, 10% to 90%, Vin = 0 to 3.3V		8	18	ns
t_{FA}, t_{FB}	Output Fall Time	C_L=1.8nF, 90% to 10%, Vin = 0 to 3.3V		14	32	ns
t_{D2}	Propagation Delay – Input falling to output falling	C_L=1.8nF, from 1V falling on Vin to 90% of output fall, Vin=0 - 3.3V, Fsw=500kHz, 50% duty cycle		28	50	ns
t_{D1}	Propagation Delay – Input rising to output rising	C_L=1.8nF, from 2V rising on Vin to 10% of output rise, Vin=0 - 3.3V, Fsw=500kHz, 50% duty cycle		26	50	ns
t_{PD_EN}	EN Response Delay (W Version)	C_L=1.8nF, from 2V rising on EN to 10% of output rise, EN=0 - 3.3V, Fsw=500kHz, 50% duty cycle		26	40	ns
t_{PD_DIS}	DIS Response Delay (W Version)	C_L=1.8nF, from 1V falling on EN to 90% of output fall, EN=0 - 3.3V, Fsw=500kHz, 50% duty cycle		27	45	ns
t_{PWmin}	Minimum Input Pulse Width That Passes to Output	C_L=1.8nF, Vin=0 - 3.3V, Fsw=500kHz, Vo >2V		9	15	ns
t_{PWD}	Pulse Width Distortion	Input Pulse Width = 100ns, 500kHz t_{D2} – t_{D1},C_L=1.8nF	-10		10	ns

(1) Switching parameters are not tested in production.

5.7 Timing Diagrams

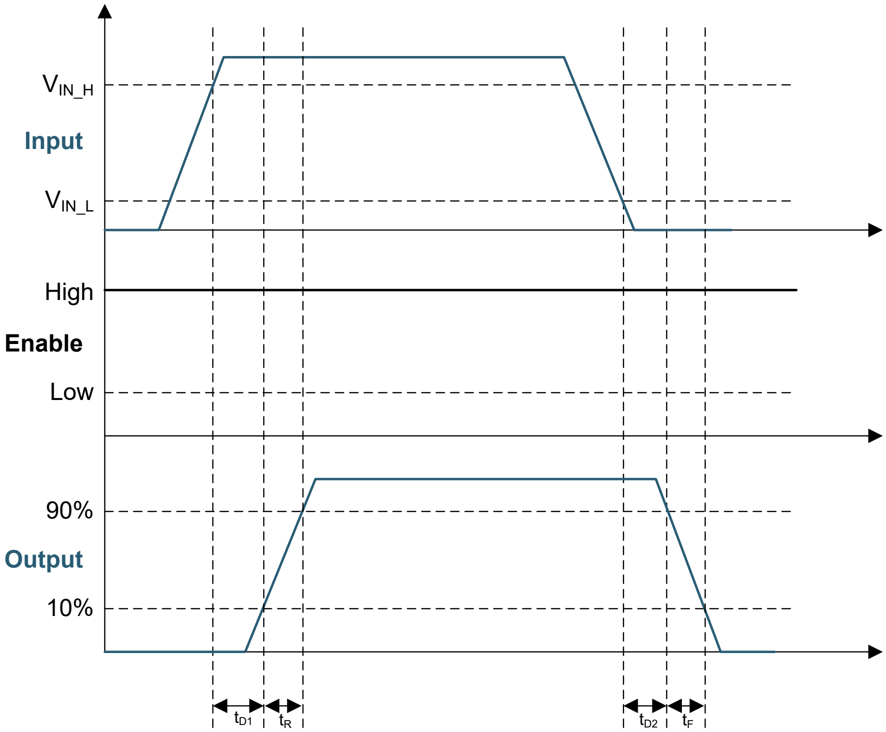


Figure 5-1. Single Input Version, IN = PWM

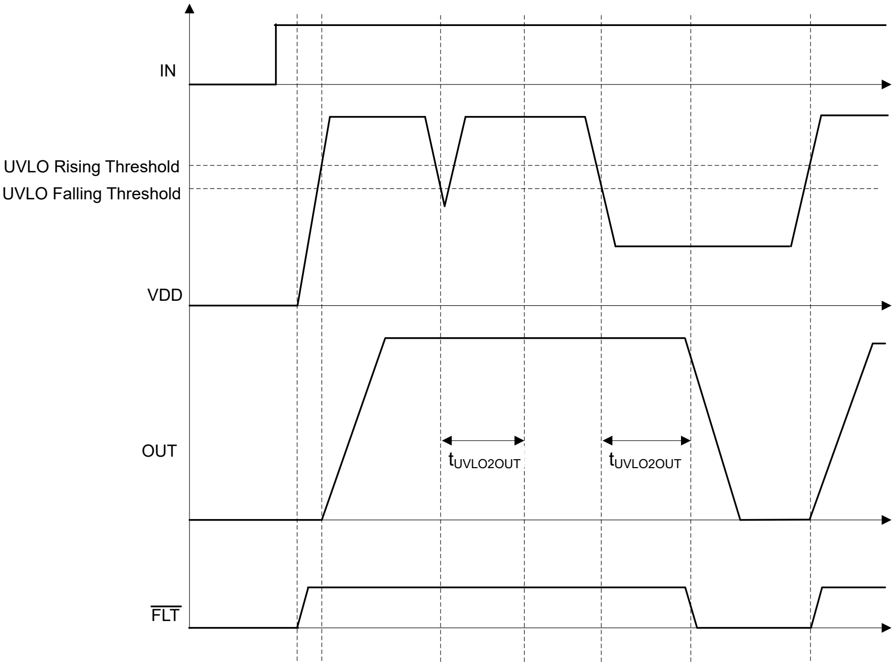


Figure 5-2. UVLO Protection Timing Diagram

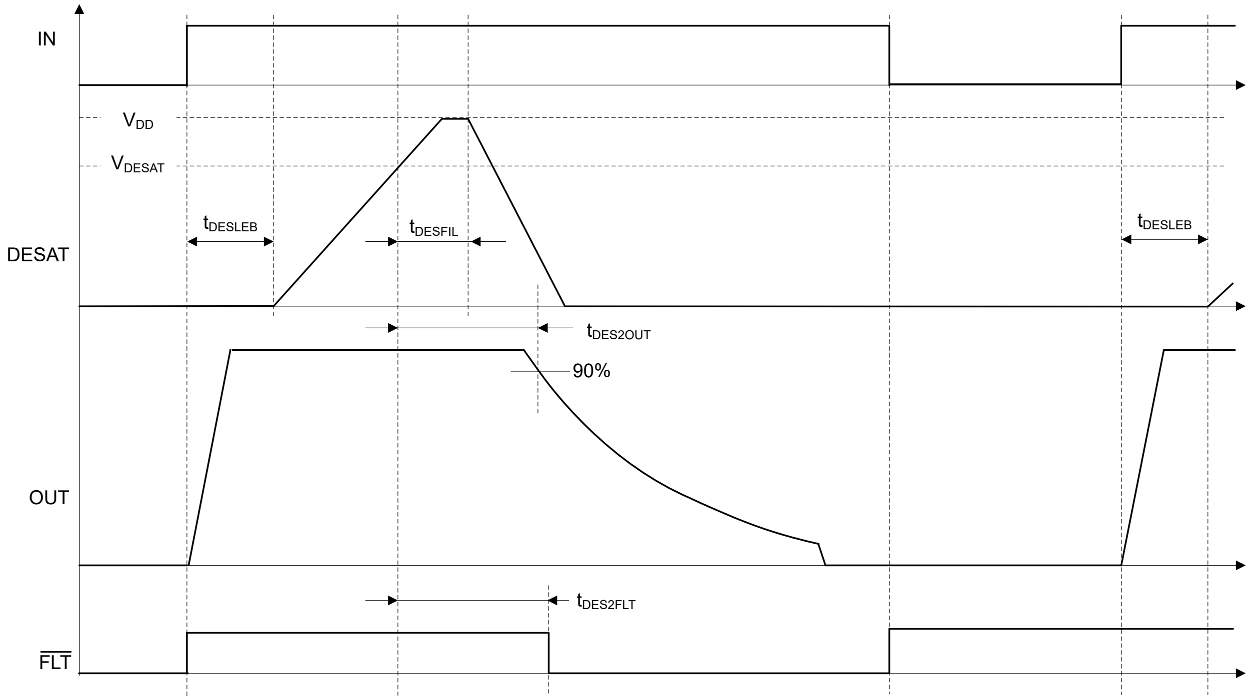


Figure 5-3. DESAT Protection Timing Diagram

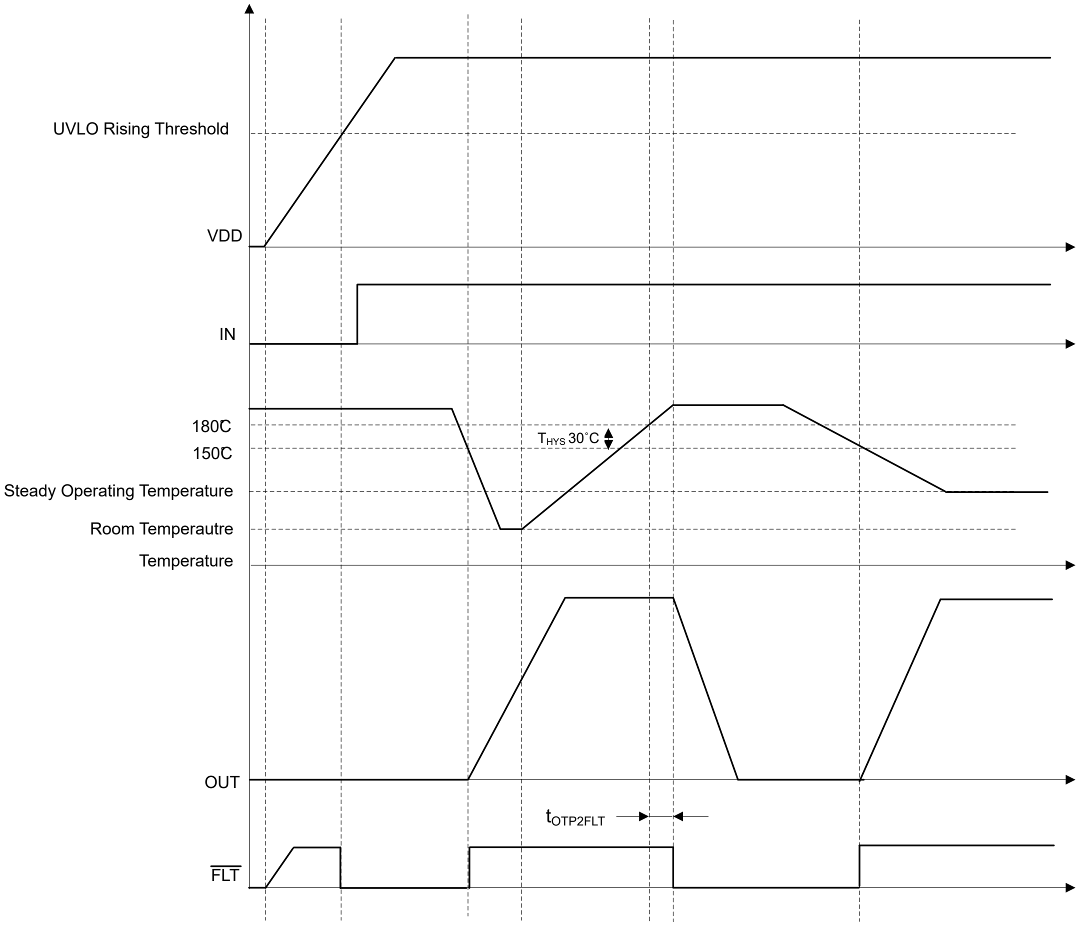
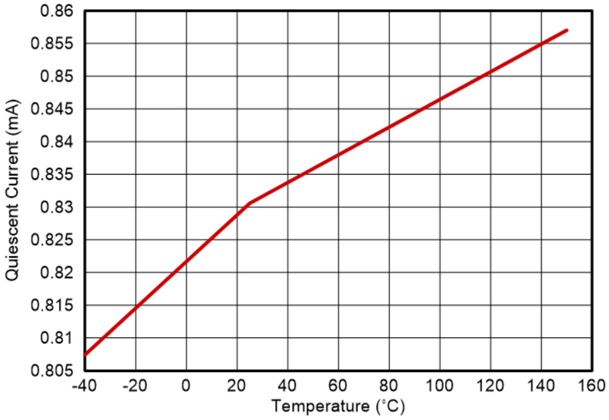


Figure 5-4. Thermal Shutdown Protection Timing Diagram

5.8 Typical Characteristics

Unless otherwise specified, VDD=15V, VEE=0V, IN=3.3V, EN=5V, T_J = 25 °C, No load



V_{DD} = 6.5V

Figure 5-5. Quiescent Current

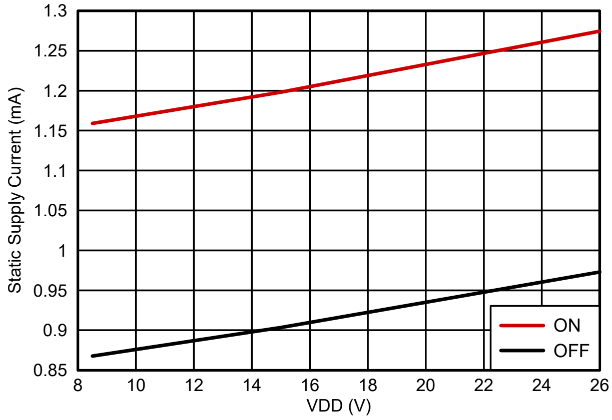


Figure 5-6. Operating Static Supply Current

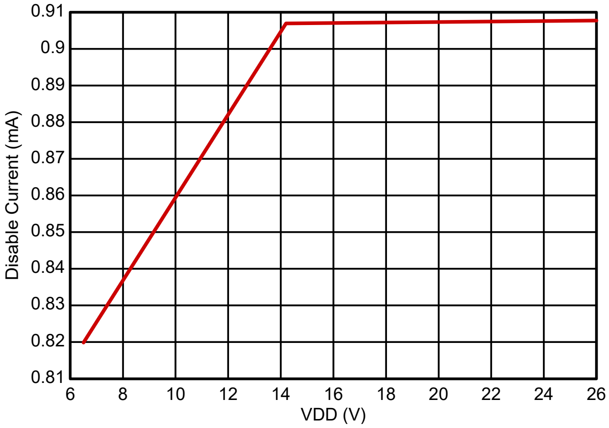
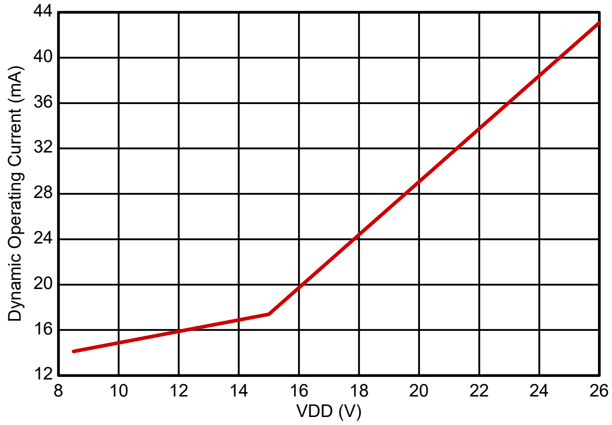


Figure 5-7. Disable Current



C_{LOAD} = 1.8 nF

Figure 5-8. Operating Supply Current

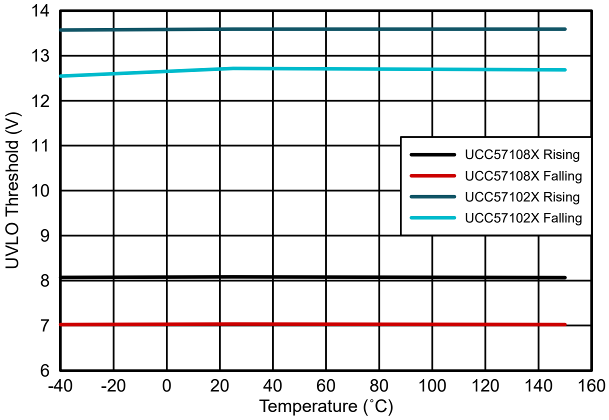


Figure 5-9. UVLO Threshold

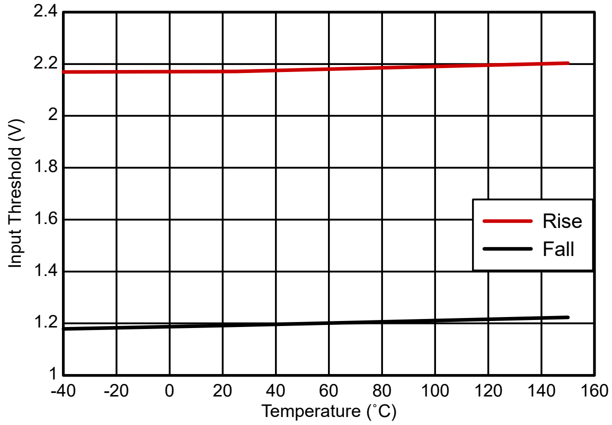


Figure 5-10. Input Threshold

5.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=15V, VEE=0V, IN=3.3V, EN=5V, T_J = 25 °C, No load

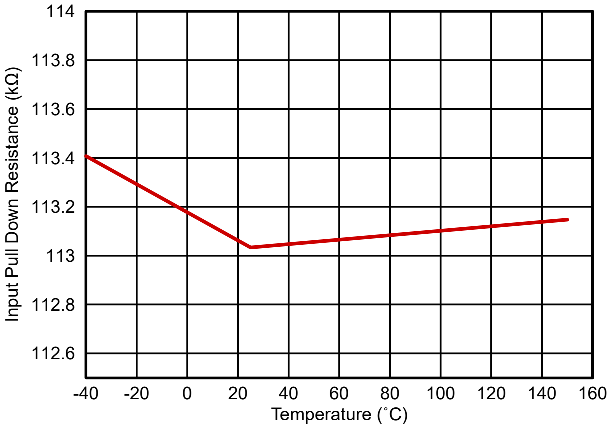


Figure 5-11. Input Pulldown Resistance

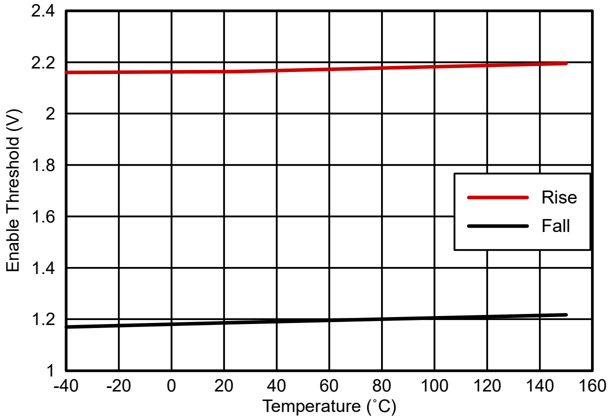


Figure 5-12. Enable Threshold

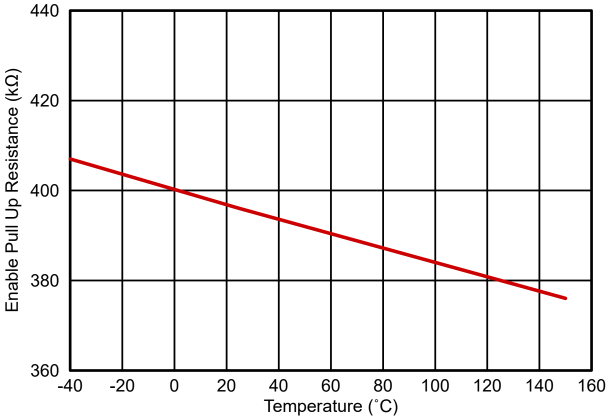


Figure 5-13. Enable Up Resistance

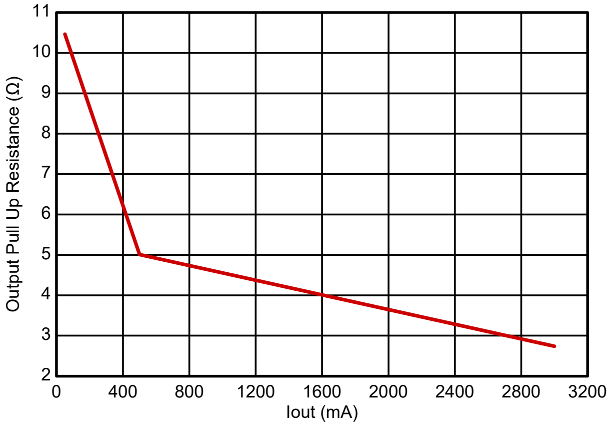


Figure 5-14. Output Pullup Resistance vs VDD

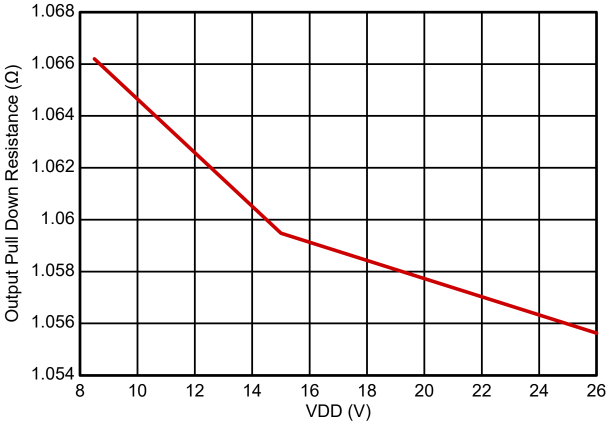
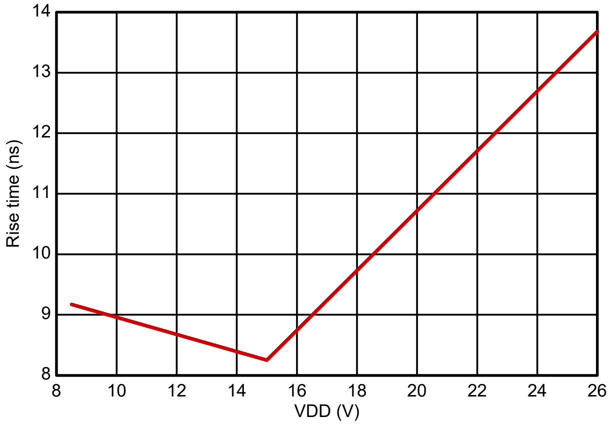


Figure 5-15. Output Pulldown Resistance

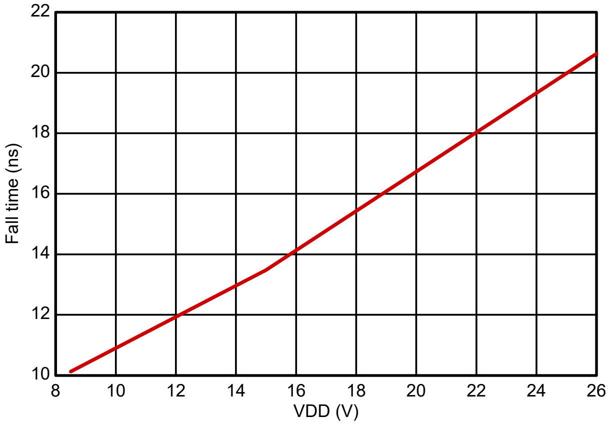


C_{LOAD} = 1.8 nF

Figure 5-16. Output Rise Time

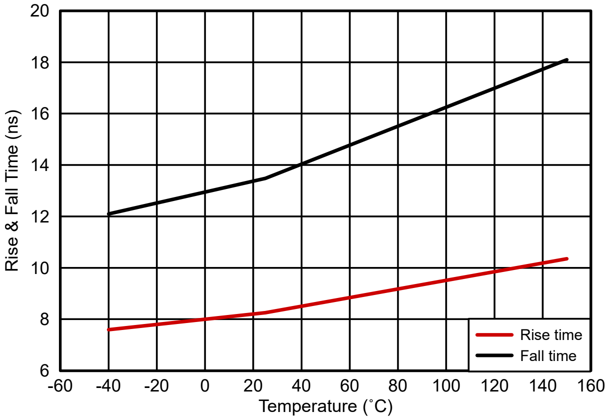
5.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=15V, VEE=0V, IN=3.3V, EN=5V, T_J = 25 °C, No load



C_{LOAD} = 1.8 nF

Figure 5-17. Output Fall Time

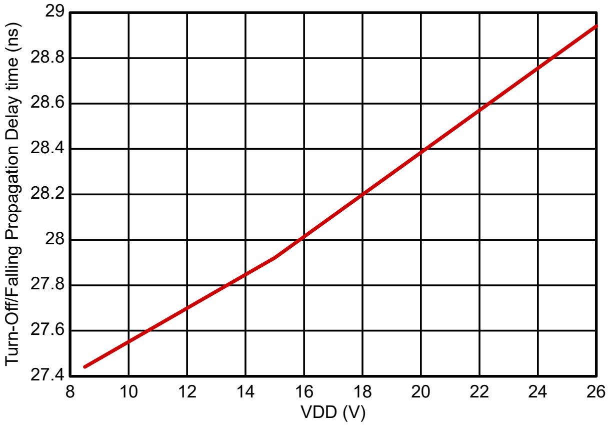


C_{LOAD} = 1.8 nF

Figure 5-18. Output Rise and Fall Time

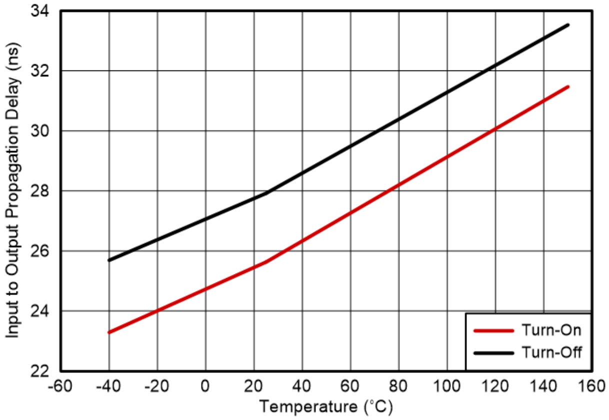
C_{LOAD} = 1.8 nF

Figure 5-19. Input to Output Rising (Turnon) Propagation Delay



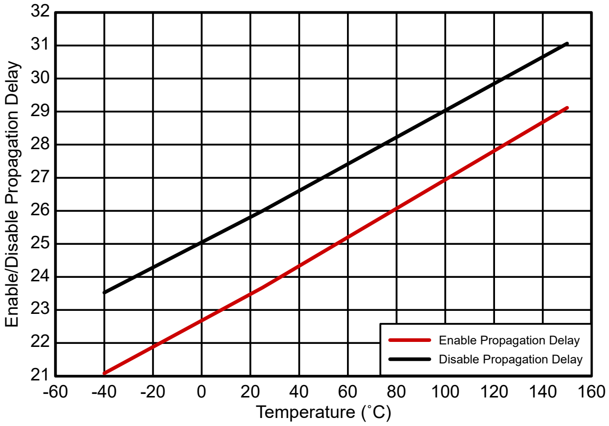
C_{LOAD} = 1.8 nF

Figure 5-20. Input to Output Falling (Turnoff) Propagation Delay



C_{LOAD} = 1.8 nF

Figure 5-21. Input Propagation Delay



C_{LOAD} = 1.8 nF

Figure 5-22. Enable Propagation Delay

5.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=15V, VEE=0V, IN=3.3V, EN=5V, T_J = 25 °C, No load

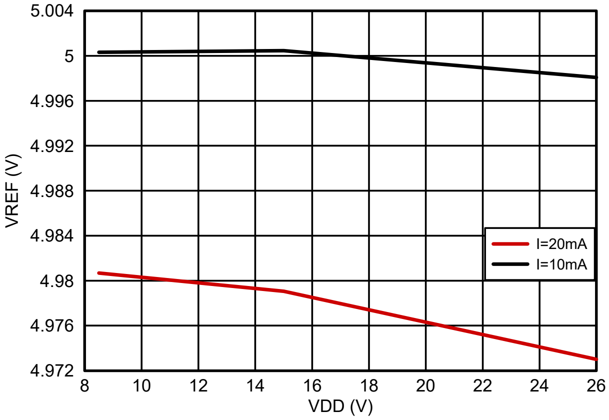


Figure 5-23. Vref Voltage vs VDD

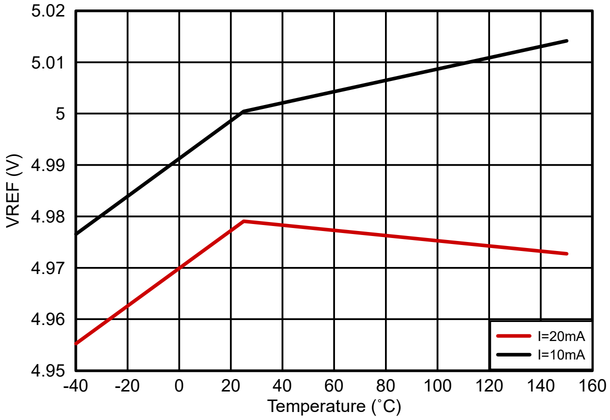


Figure 5-24. Vref Voltage vs Temperature

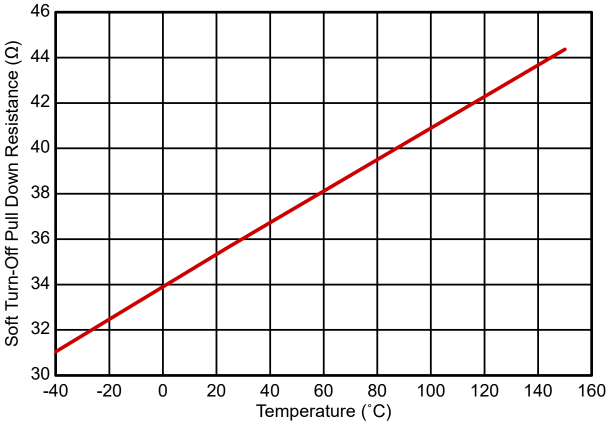


Figure 5-25. Soft Turn Off Pulldown Resistance vs VDD

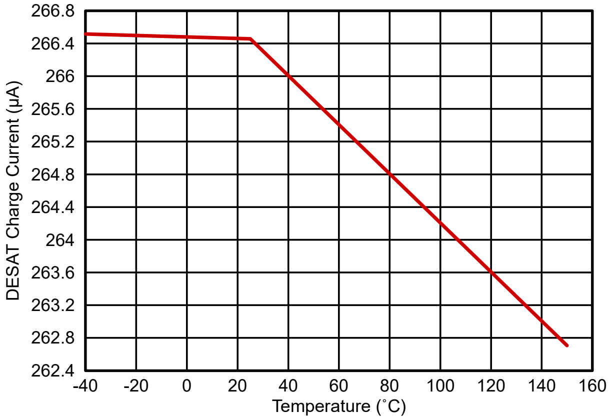


Figure 5-26. DESAT Charge Current vs Temperature

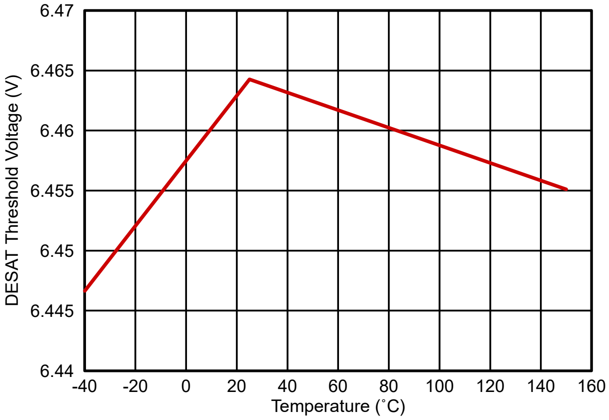
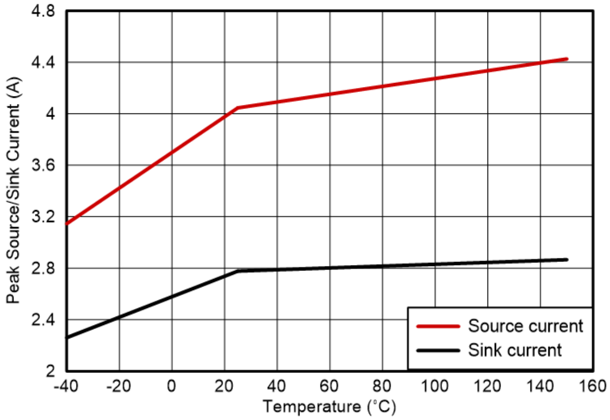


Figure 5-27. DESAT Threshold vs Temperature

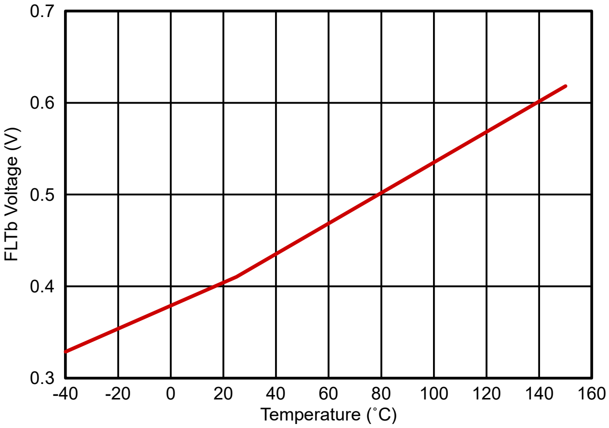


C_{LOAD} = 100 nF

Figure 5-28. Peak Source and Sink Current

5.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=15V, VEE=0V, IN=3.3V, EN=5V, T_J = 25 °C, No load



I_{FLTb_sink} = 15mA

Figure 5-29. FLTb vs Temperature

6 Detailed Description

6.1 Overview

The UCC5710x-Q1 device is a single-channel, high-speed, gate driver capable of effectively driving MOSFET, SiC MOSFET, and IGBT power switches with 3-A source and 3-A sink (symmetrical drive) peak current. The driver has a good transient handling capability on its output due to reverse currents, as well as rail-to-rail drive capability and small propagation delay, typically 26ns. The device has the state-of-art DESAT detection time and fault reporting function to the low voltage side DSP/MCU. Soft turn off is triggered when the DESAT fault is detected, minimizing the short circuit energy while reducing the overshoot voltage on the switch.

The input threshold of the UCC5710x-Q1 is compatible to TTL low-voltage logic, which is fixed and independent of VDD supply voltage. The driver can also work with CMOS based controllers as long as the threshold requirement is met. The 1-V typical hysteresis offers excellent noise immunity.

In the UCC5710xW-Q1, the driver has an EN pin with fixed TTL compatible threshold. EN is internally pulled up. Pulling EN low disables the driver, while leaving EN open provides normal operation. The UCC5710xB-Q1 and UCC5710xC-Q1 offer an additional 5V output (VREF) that source up to 20mA function.

6.2 Functional Block Diagram

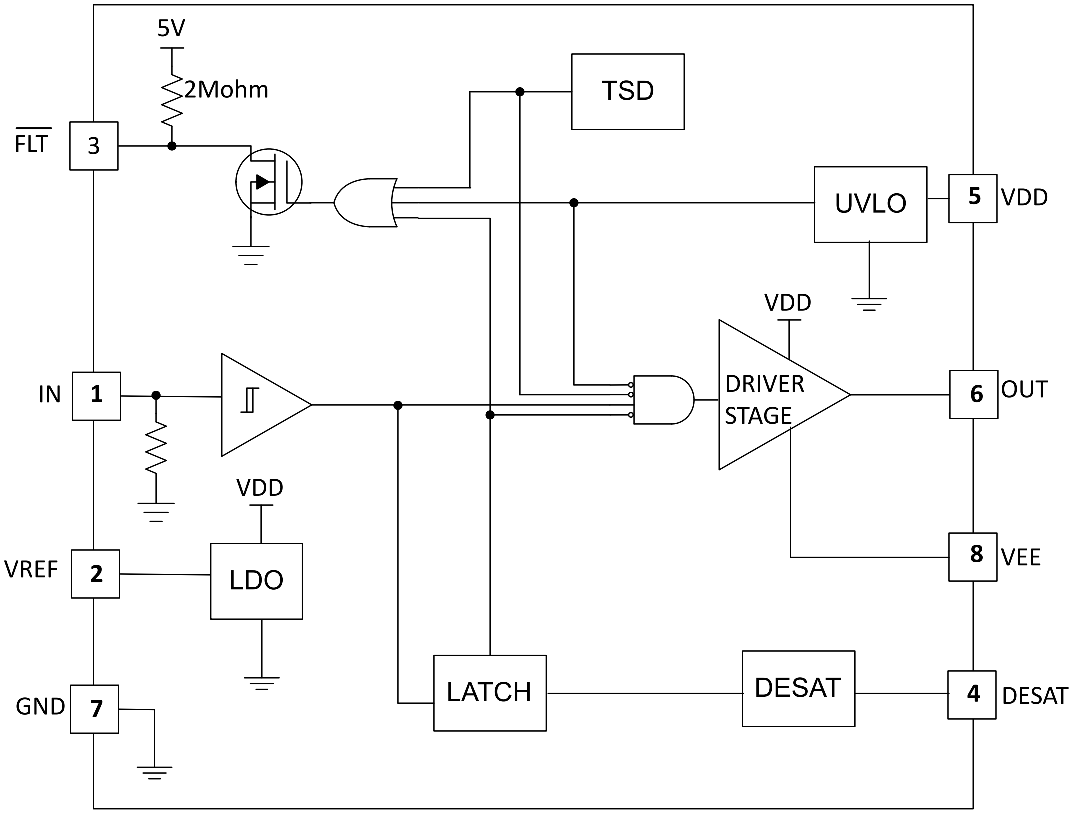


Figure 6-1. UCC5710xB-Q1 Simplified Functional Block Diagram

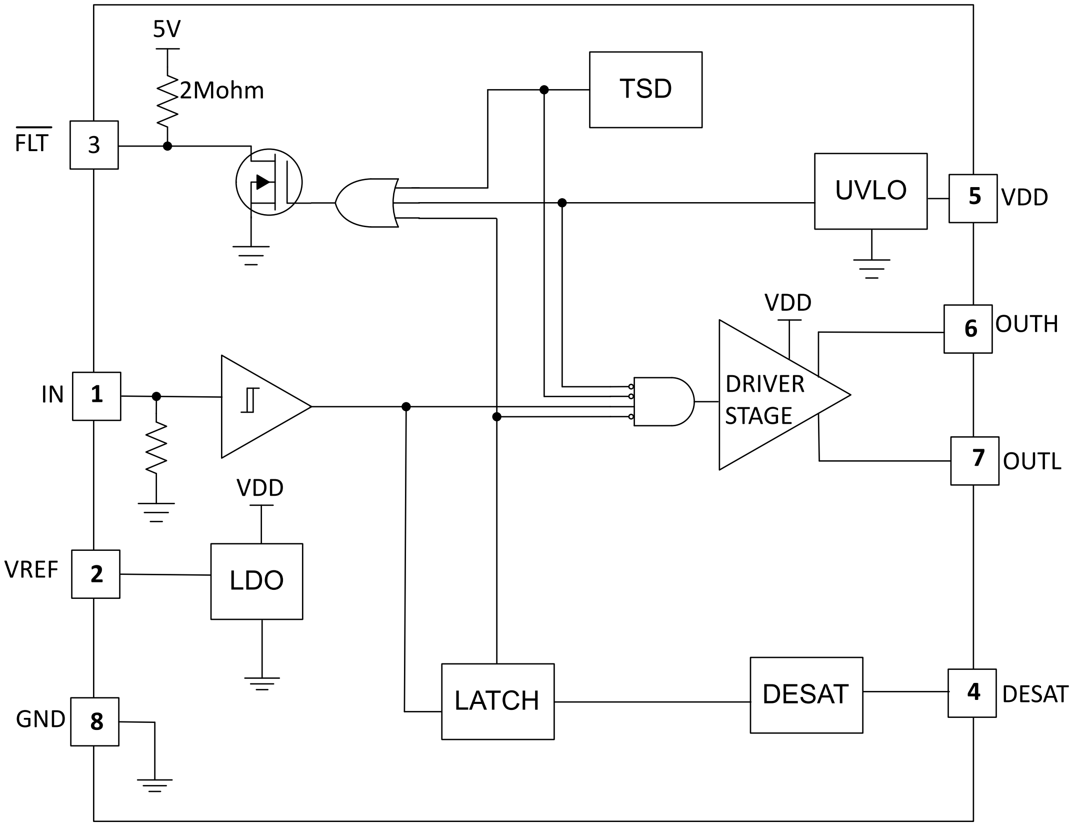


Figure 6-2. UCC5710xC-Q1 Simplified Functional Block Diagram

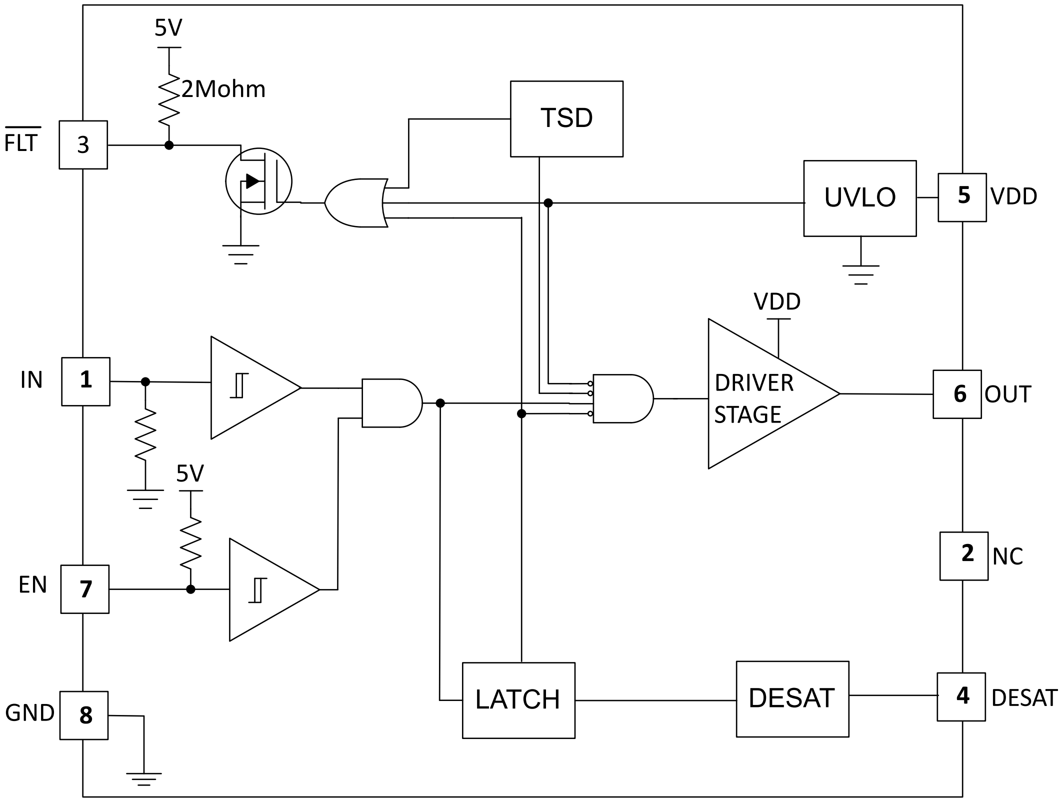


Figure 6-3. UCC5710xW-Q1 Simplified Functional Block Diagram

6.3 Feature Description

6.3.1 Input Stage

The inputs of the UCC5710x-Q1 devices are compatible with TTL based threshold logic and the inputs are independent of the VDD supply voltage. With typical high threshold of 2.2 V and typical low threshold of 1.2 V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3-V or 5-V logic. Wider hysteresis (typically 1 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. This device also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The very low input capacitance, typically less than 8 pF, on these pins reduces loading and increases switching speed.

The device features an important protection function wherein, whenever the input pin is in a floating condition, the output is held in the low state. This is achieved with internal pullup or pulldown resistors on the input pins as shown in the simplified functional block diagrams. In some applications, due to difference in bias supply sequencing, different ICs power-up at different times. This may cause output of the controller to be in tri-state. This output of the controller is connected to the input of the driver IC. If the driver IC does not have a pulldown resistor then the output of the driver may go high erroneously and damage the switching power device.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located on a separate daughter board or PCB layout has long input connection traces:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. Because the device features just one GND pin which may be referenced to the power ground, this may interfere with the differential voltage between input pins and GND and trigger an unintended change of output state. Because of a fast 26-ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses risk of damage.
- 1-V Input threshold hysteresis boosts noise immunity compared to most other industry standard drivers.

An external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This also limits the rise or fall times to the power device which reduces EMI. The external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

Finally, because of the unique input structure that allows negative voltage capability on the input and enable pins, caution must be used in the following applications:

- Input or enable pins are switched to amplitude > 15 V.
- Input or enable pins are switched at dV/dt > 2 V/ns.

If both of these conditions occur, add a series 150-Ω resistor for the pin(s) being switched to limit the current through the input structure.

6.3.2 Enable Function

The enable (EN) pin of the UCC5710xW-Q1 device also has TTL compatible input thresholds with wide hysteresis. The typical turnon threshold is 2.2V and the typical turnoff threshold is 1.2V with typical hysteresis of 1V. The enable (EN) pin of the UCC5710xW-Q1 has an internal pullup resistor to an internal reference voltage. Thus, leaving the enable pin floating turns on the driver and allows it to send output signals properly. If desired, the enable pin can also be driven by low-voltage logic to enable and disable the driver. There is minimum delay from the enable block to the output for fast system response time. Similar to the input pins, the enable pin can also handle significant negative voltage and therefore provides system robustness. The enable pin can withstand a wide range of slew rates such as 1V/ns to 1V/ms. The enable signal is independent of VDD voltage and stable across the full operating temperature range.

6.3.3 Driver Stage

The device has a ±3-A peak drive strength and is suitable for driving IGBT/SiC. The driver features an important safety function wherein, when the input pins are in a floating condition, the output is held in the LOW state.

The driver has rail-to-rail output by implementing an NMOS pull-up with intrinsic bootstrap gate drive. Under DC conditions, a PMOS is used to keep OUT tied to VDD as shown in the following figure. The low pullup impedance of the NMOS results in strong drive strength during the turn-on transient, which shortens the charging time of the input capacitance of the power semiconductor and reduces the turn on switching loss.

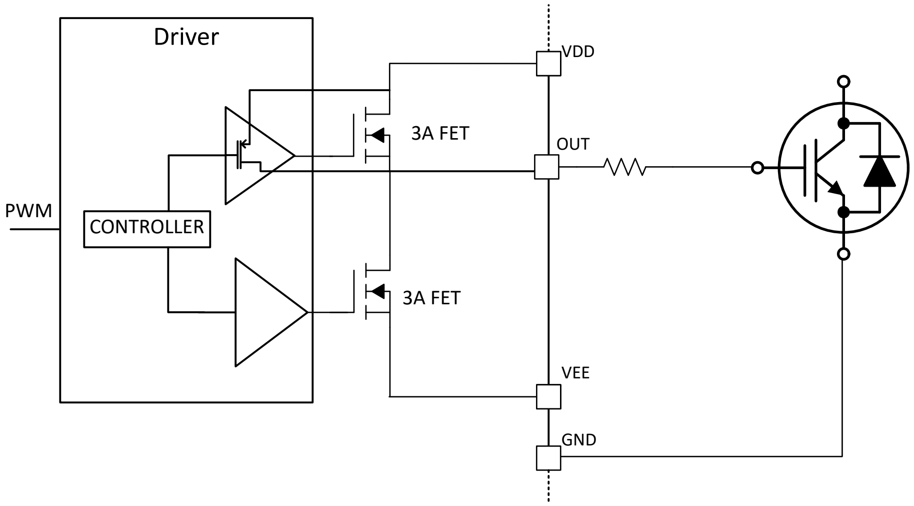


Figure 6-4. Gate Driver Output Stage

6.3.4 Desaturation (DESAT) Protection

The UCC5710x-Q1 implements a fast overcurrent and short circuit protection feature to protect the MOSFET/IGBT from catastrophic breakdown during a fault. The DESAT pin has a typical 6.5 V threshold with respect to GND, the source or emitter of the power semiconductor. When the input is in a floating condition or the output is held in the LOW state, the DESAT pin is pulled down by an internal MOSFET and held in the LOW state, which prevents the overcurrent and short circuit fault from false triggering. The internal current source of the DESAT pin is activated only during the driver ON state, which means the overcurrent and short circuit protection feature only works when the power semiconductor is in the ON state. The internal pulldown MOSFET helps to discharge the voltage of the DESAT pin when the power semiconductor is turned off. The device features a 150-ns internal leading edge blanking time after OUT switches to the HIGH state. The UCC5710x-Q1 internal current source is activated to charge the external blanking capacitor after the internal leading edge blanking time. The typical value of the internal current source is 250 μA. More details about the DESAT circuit design can be found in Applications and Benefits of UCC5710x-Q1.

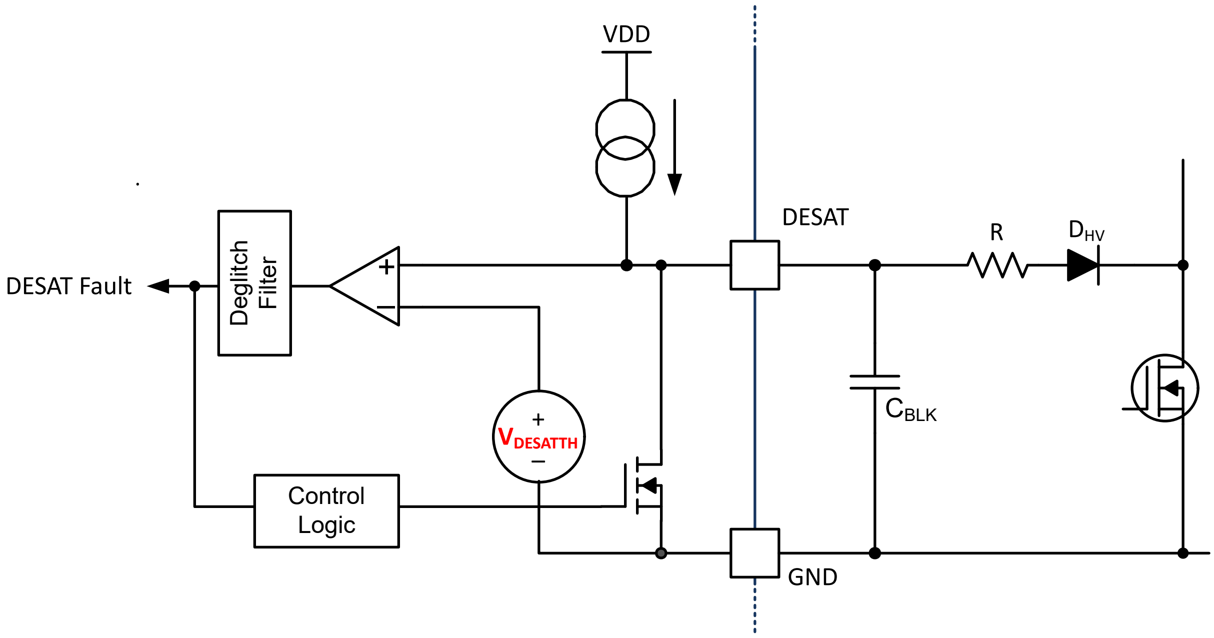


Figure 6-5. DESAT Protection

6.3.5 Fault ($\overline{FLT}$)

The $\overline{FLT}$ pin of the UCC5710x-Q1 can report a fault signal to the DSP/MCU when a fault is detected through the DESAT pin, internal TSD, or the UVLO. The $\overline{FLT}$ pin is pulled down to GND after the fault is detected and is held low until the fault is cleared. It can be pull up to external voltage rail up to VDD level with the considersion that the maximum sink current on the $\overline{FLT}$ is 20mA. Also a 100pF capacitor between $\overline{FLT}$ and GND is recommened.

6.3.6 VREF

The UCC5710x-Q1 devices provides the 5V bias intergrated in to the gate driver. This output is capable of sourcing up to 20mA. for voltage sensing modulators, current-sensing modulators or other external comparator interface. A 100nF bypass capacitor is required on the VREF pin even it is bias any external functions. The detail performance for VREF pin can be found in the Typical Characteristics.

6.3.7 Thermal Shutdown

The UCC5710x-Q1 devices provides the thermal shutdown function that can protect the driver when the internal temperature goes above threshold. When the it excess the overtemperature threshold, the $\overline{FLT}$ will be pulled low after the 8us propagation delay. The device will active again once the temperature falls below the threshold. More information can be found in the Section 5.7.

6.4 Device Functional Modes

The UCC5710x-Q1 devices operate in normal mode and UVLO mode (see Section 7.2.2.1 for information on UVLO operation). In normal mode, the output state is dependent on the states of the device and the input pins.

The UCC5710xW-Q1 features a single, noninverting input, but also contains enable and disable functionality through the EN pin. Setting the EN pin to logic HIGH enables the noninverting input to output on the IN pin.

Table 6-1. UCC5710xB-Q1 Truth Table

IN	DESAT	INTERNAL TSD	$\overline{FLT}$	OUT
H	L	L	Open drain	H
L	L	L	Open drain	L
H	H	L	L	L

Table 6-1. UCC5710xB-Q1 Truth Table (continued)

IN	DESAT	INTERNAL TSD	$\overline{\text{FLT}}$	OUT
X	X	H	L	L

Table 6-2. UCC5710xC-Q1 Truth Table

IN	DESAT	INTERNAL TSD	$\overline{\text{FLT}}$	OUTH	OUTL
H	L	L	Open drain	H	High-impedance
L	L	L	Open drain	High-impedance	L
H	H	L	L	High-impedance	L
X	X	H	L	High-impedance	L

Table 6-3. UCC5710xW-Q1 Truth Table

IN	EN	DESAT	INTERNAL TSD	$\overline{\text{FLT}}$	OUT
L	H	L	L	Open drain	L
H	H	L	L	Open drain	H
X	L	X	X	X	L
H	H	H	L	L	L
X	H	X	H	L	L

7 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. To enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation is often encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. Level-shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar (or P- N-channel MOSFET) transistors in a totem-pole arrangement, being emitter follower configurations, prove inadequate for this because they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive, and UVLO functions. Gate drivers also find other needs such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The UCC5710x-Q1 is very flexible in this role with a strong drive current capability and wide recommended supply voltage range of UVLO to 26 V. This allows the driver to be used in 5-V bias logic level very high frequency MOSFET applications, 12-V MOSFET applications, 20-V and -5-V (relative to source) SiC FET applications, 15-V and -8-V (relative to emitter) IGBT applications and many others.

These requirements, coupled with the need for low propagation delays and availability in compact, and low-inductance packages with good thermal capability, make gate driver devices such as the UCC5710x-Q1 extremely important components in switching power combining benefits of high-performance, low cost, low component count, board space reduction and simplified system design.

7.2 Typical Application

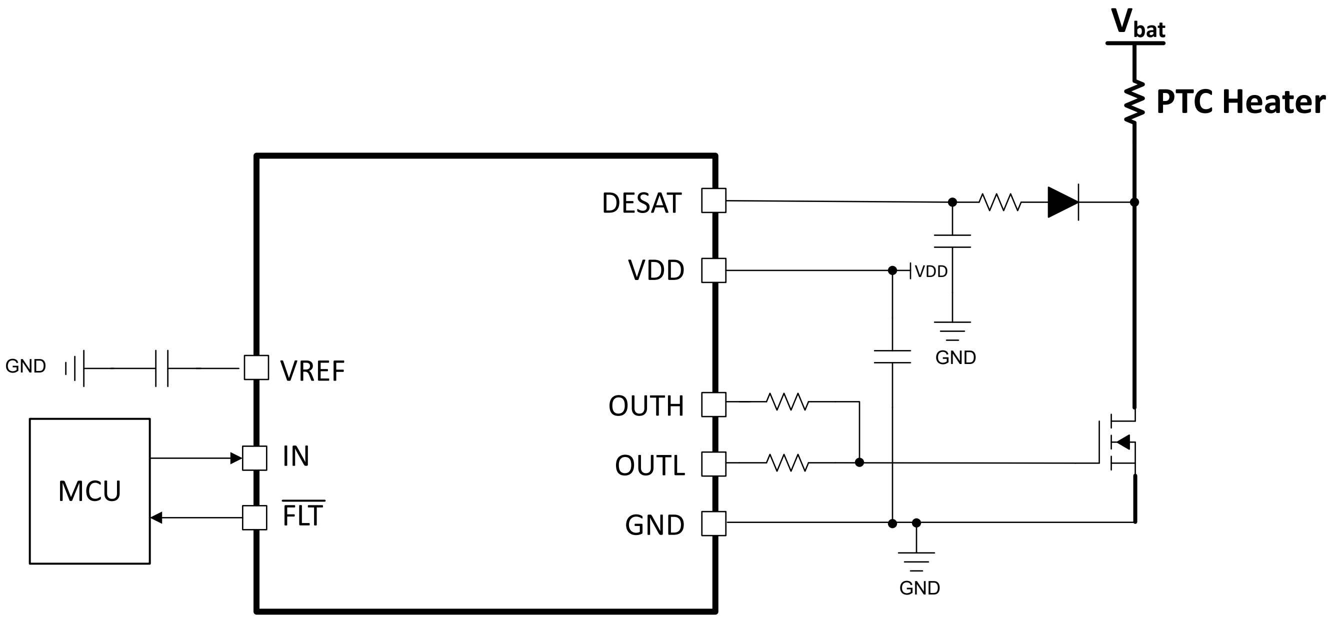


Figure 7-1. UCC57108C-Q1 Used in a PTC Heater Application

7.2.1 Design Requirements

When selecting the gate driver device for an end application, some design considerations must be evaluated in order to make the most appropriate selection. Following are some of the design parameters that should be used when selecting the gate driver device for an end application: input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type. Example design parameters and requirements are listed in Table 7-1.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input to output logic	Noninverting
Input threshold type	TTL
Bias supply voltage levels	+18 V
Negative output low voltage	N/A
dV_{DS}/dt(1)	100 V/ns
Enable function	Yes
Disable function	N/A
Propagation delay	<30 ns
Power dissipation	<1 W
Package type	SON-8 or SOIC-8

(1) dV_{DS}/dt is a typical requirement for a given design. This value can be used to find the peak source/sink currents needed as shown in .

7.2.2 Detailed Design Procedure

7.2.2.1 VDD Undervoltage Lockout

The UCC57108-Q1 device offers an undervoltage lockout threshold of 8 V and the UCC57102-Q1 provides an undervoltage lockout threshold of 12V. The device's hysteresis range helps to avoid any chattering due to the presence of noise on the bias supply. 1V of typical UVLO hysteresis is expected. There is no significant driver output turnon delay due to the UVLO feature, and 4 µs of UVLO delay is expected. The UVLO turn-off delay is also minimized as much as possible. The UVLO delay is designed to minimize chattering that may occur due to very fast transients that may appear on VDD. When the bias supply is below UVLO thresholds, the outputs are held actively low irrespective of the state of the input pins and enable pin. The device accepts a wide range of slew rates on its VDD pin, and VDD noise within the hysteresis range does not affect the output state of the driver (neither ON nor OFF).

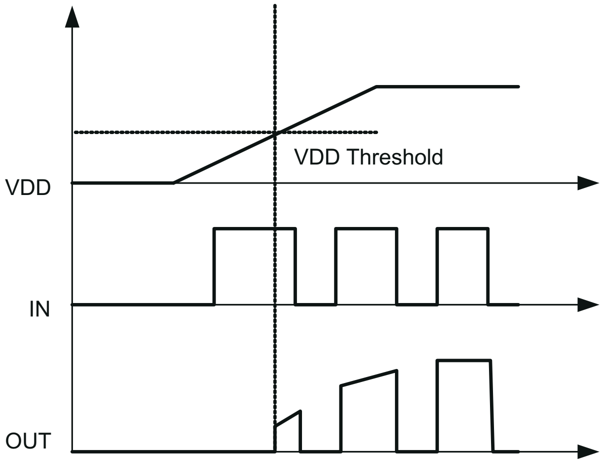


Figure 7-2. Power Up

7.2.2.2 Drive Current and Power Dissipation

The UCC5710x-Q1 driver is capable of delivering 3-A of current to a MOSFET gate for a period of several-hundred nanoseconds at VDD = 12V. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground which repeats at the operating frequency of the power device. The power dissipated in the gate driver device package depends on the following factors:

- Gate charge required of the power MOSFET (usually a function of the drive voltage V_{GS}, which is very close to input bias supply voltage V_{DD} due to low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

Because UCC5710x-Q1 features low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver can be safely assumed to be negligible.

When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The following equation provides an example of the energy that must transfer from the bias supply to charge the capacitor.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \tag{1}$$

where

- C_{LOAD} is the load capacitor
- $V_{DD}{}^2$ is the bias voltage feeding the driver

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss shown as below.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} \tag{2}$$

where

- f_{SW} is the switching frequency

With V_{DD} = 12 V, C_{LOAD} = 10 nF and f_{SW} = 300 kHz the power loss is calculated with Equation 3.

$$P_G = 10\,\text{nF} \times 12\,\text{V}^2 \times 300\,\text{kHz} = 0.432\,\text{W} \tag{3}$$

The switching load presented by a power MOSFET is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, the power that must be dissipated when charging a capacitor is determined which by using the equivalence $Q_g = C_{LOAD} V_{DD}$ to provide Equation 4 for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \tag{4}$$

Assuming that the UCC5710x-Q1 device is driving power MOSFET with 60 nC of gate charge (Q_g = 60 nC at V_{DD} = 12 V) on each output, the gate charge related power loss is calculated with Equation 5.

$$P_G = 2 \text{x} 60\,\text{nC} \times 12\,\text{V} \times 300\,\text{kHz} = 0.432\,\text{W} \tag{5}$$

This power PG is dissipated in the resistive elements of the circuit when the MOSFET turns on or turns off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows (see):

$$P_{SW} = 0.5 \times Q_G \times VDD \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right) \tag{6}$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pullup structure) = 1.5 x R_{OL}

In addition to the above gate-charge related power dissipation, additional dissipation in the driver is related to the power associated with the quiescent bias current consumed by the device to bias all internal circuits such as input stage (with pullup and pulldown resistors), enable, and UVLO sections. As shown in Operating Supply Current vs Temperature (Outputs Switching), the quiescent current is less than 0.6 mA even in the highest case. The quiescent power dissipation is calculated easily with Equation 7.

$$P_Q = I_{DD} V_{DD} \tag{7}$$

Assuming , I_{DD} = 6 mA, the power loss is:

$$P_Q = 0.6\ \text{mA} \times 12\,\text{V} = 7.2\,\text{mW} \tag{8}$$

Clearly, this power loss is insignificant compared to gate charge related power dissipation calculated earlier.

With a 12-V supply, the bias current is estimated as follows, with an additional 0.6-mA overhead for the quiescent consumption:

$$I_{DD} \sim \frac{P_G}{V_{DD}} = \frac{0.432\ \text{W}}{12\ \text{V}} = 0.036\ \text{A} \tag{9}$$

7.2.3 Application Curves

The figures below show the typical switching characteristics of the UCC57108-Q1 device with a 1nF capacitor load.

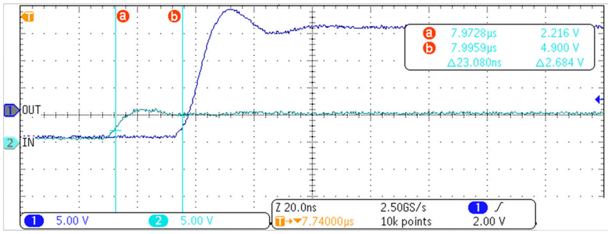


Figure 7-3. UCC57108-Q1 Rising (Turn-On) Propagation Delay

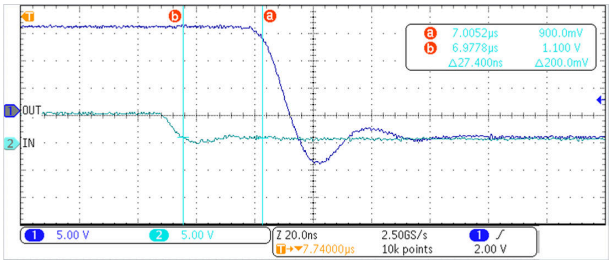


Figure 7-4. UCC57108-Q1 Falling (Turn-Off) Propagation Delay

8 Power Supply Recommendations

The bias supply voltage range for which the UCC5710x-Q1 devices are recommended to operate is from UVLO to 26 V. The lower end of this range is governed by the internal UVLO protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the $V_{(ON)}$ supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 26-V recommended maximum voltage rating of the VDD pin of the device. The absolute maximum voltage for the VDD pin is 30 V.

The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and the device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification. Therefore, ensuring that, while operating at or near the UVLO range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown.

During system shutdown, device operation continues until the VDD pin voltage has dropped below the VDD UVLO falling threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up, the device does not begin operation until the VDD pin voltage has exceeded the VDD UVLO rising threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUT pin is also supplied through the same VDD pin is important. As a result, every time a current is sourced out of the output pin (OUT), a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that local bypass capacitors are provided between the VDD and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low-ESR, ceramic surface-mount capacitor is needed. TI recommends having two capacitors; a 100-nF ceramic surface-mount capacitor placed less than 1mm from the VDD pin of the device and another ceramic surface-mount capacitor of a few microfarads added in parallel.

The UCC5710x-Q1 is a high current gate driver. If the gate driver is placed far from a switching power device such as a MOSFET then that may create a large inductive loop. A large inductive loop may cause excessive ringing on any and all pins of the gate driver. This may result in stress exceeding device recommended ratings. Therefore, it is recommended to place the gate driver as close to the switching power device as possible. It is also advisable to use an external gate resistor to damp any ringing due to high switching currents and board parasitic elements.

9 Layout

9.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. The UCC5710x-Q1 gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of a power switch to facilitate voltage transitions very quickly. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are recommended when designing with these high-speed drivers.

- Place the driver device as close as possible to power device to minimize the length of high-current traces between the driver output pins and the gate of the power switch device.
- Place the bypass capacitors between the VDD pin and the GND pin and as close to the driver pins as possible to minimize the trace length for improved noise filtering. TI recommends having two capacitors; a 100-nF ceramic surface-mount capacitor placed less than 1mm from the VDD pin of the device and another ceramic surface-mount capacitor of a few microfarads added in parallel. These capacitors support high peak current being drawn from VDD during turnon of the power switch. The use of low inductance surface-mount components such as chip capacitors is highly recommended.
- The turnon and turn-off current loop paths (driver device, power switch, and VDD bypass capacitor) should be minimized as much as possible in order to keep stray inductance to a minimum. High di/dt is established in these loops at two instances – during turnon and turn-off transients, which induces significant voltage transients on the output pins of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces of a current loop, taking advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- To minimize switch node transients and ringing, adding some gate resistance and/or snubbers on the power devices may be necessary. These measures may also reduce EMI.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as the source of the power switch, the ground of the PWM controller, and so forth, at a single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at the OUT pin may corrupt the input signals during transitions. The ground plane must not be a conduction path for any current loop. Instead the ground plane should be connected to the star-point with one trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

9.2 Layout Example

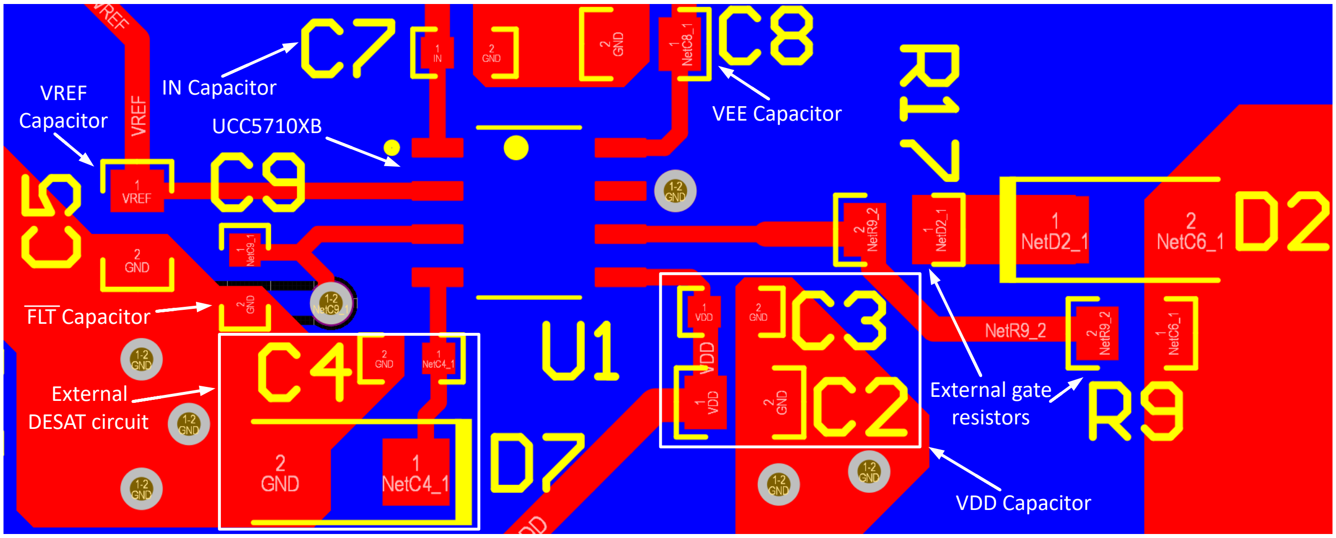


Figure 9-1. Layout Example: UCC5710xB-Q1

10 Device and Documentation Support

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2024) to Revision E (October 2024)	Page
• Changed UCC57102B-Q1 and UCC5710xC-Q1 from Advance Information to Production Data	1

Changes from Revision C (June 2024) to Revision D (September 2024)	Page
• Changed UCC5710xW-Q1 from Advance Information to Production Data	1

Changes from Revision B (June 2024) to Revision C (June 2024)	Page
• Changed UCC57108B-Q1 from Advance Information to Production Data	1
• Changed UCC5710xC-Q1 and UCC5710xW-Q1 from Product Preview to Advance Information	1

Changes from Revision A (March 2024) to Revision B (June 2024)	Page
• Added UCC57102-Q1 for Public Advance Information Release	1

Changes from Revision * (December 2023) to Revision A (March 2024)	Page
• UCC57108B-Q1 Public Advance Information Release	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PUCC57102BQDRQ1	ACTIVE	SOIC	D	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PUCC57102CQDRQ1	ACTIVE	SOIC	D	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
UCC57102WQDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 125	U102WQ	Samples
UCC57108BQDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 125	U108BQ	Samples
UCC57108WQDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 125	U108WQ	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC57102-Q1, UCC57108-Q1 :

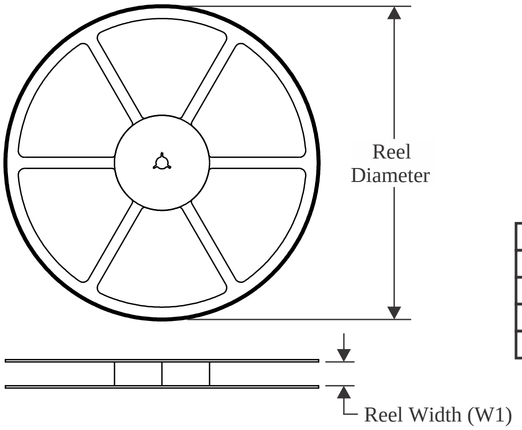
- Catalog : UCC57102, UCC57108

NOTE: Qualified Version Definitions:

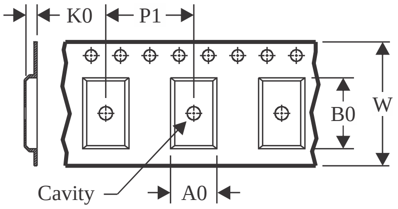
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

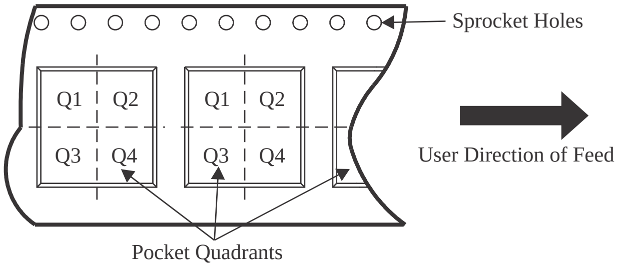


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

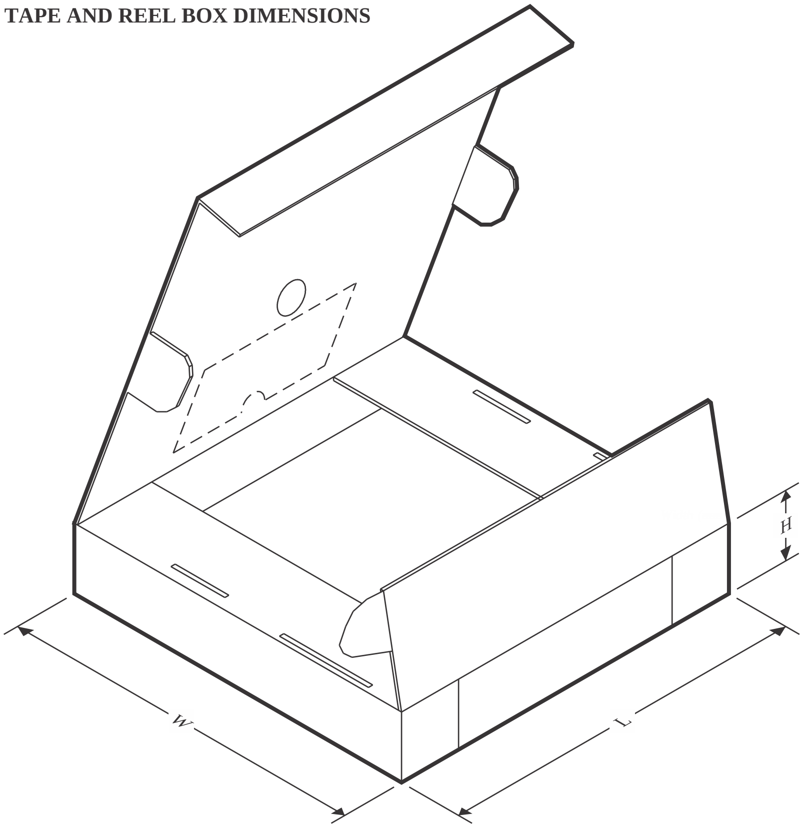
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

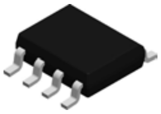
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC57108BQDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

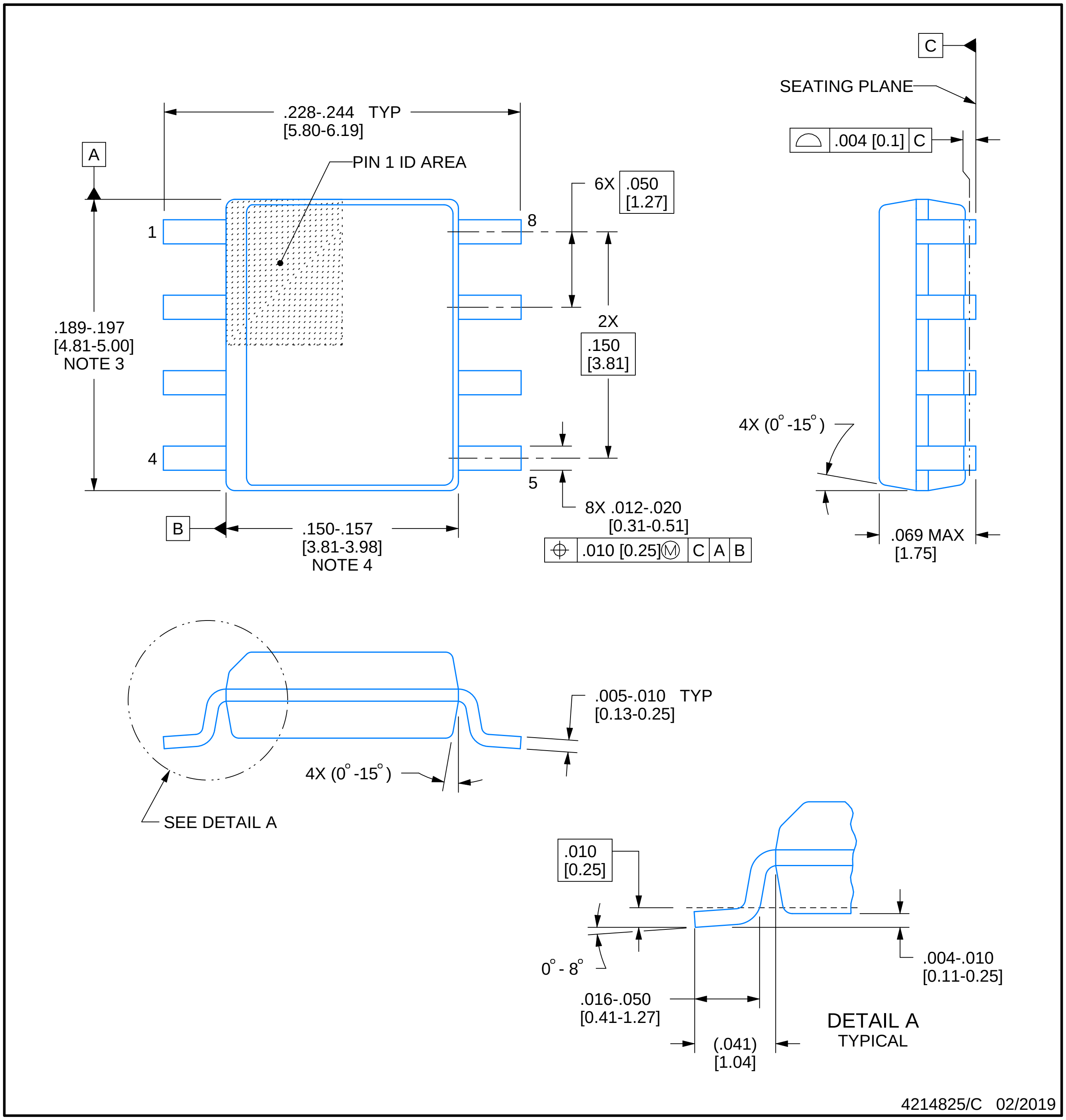
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC57108BQDRQ1	SOIC	D	8	3000	353.0	353.0	32.0



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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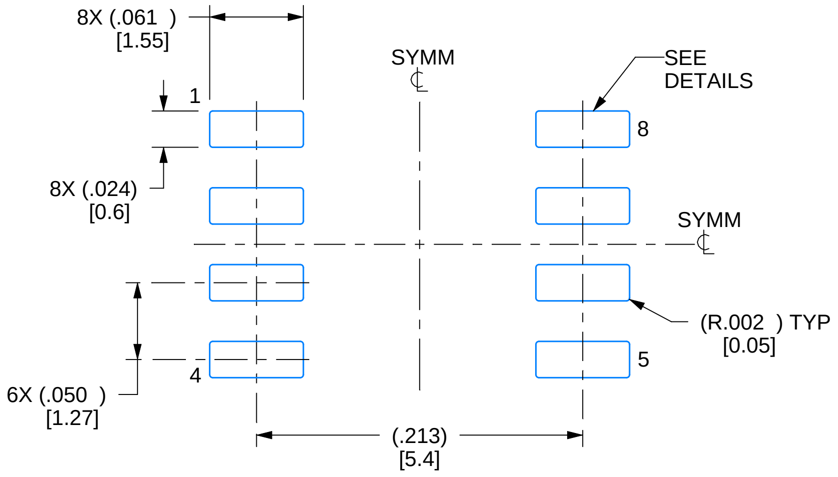
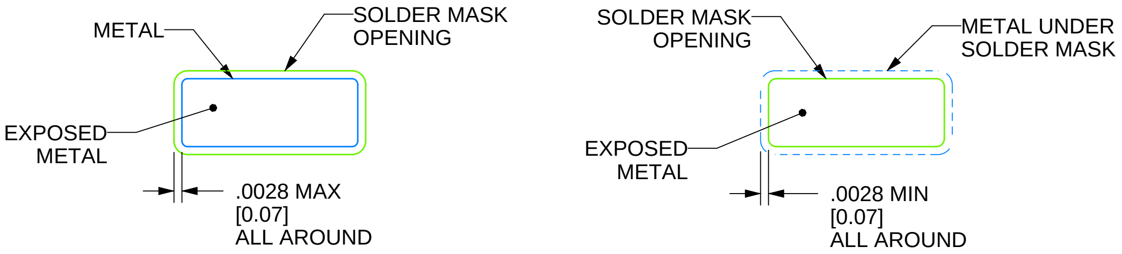
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



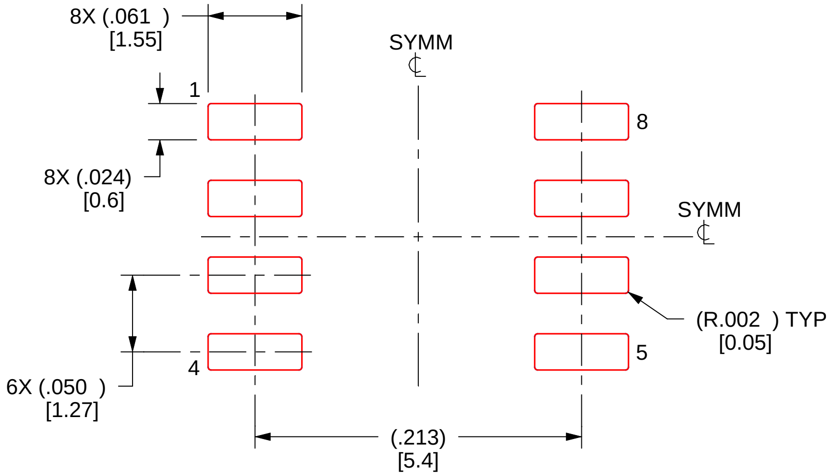
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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