UCG28826 Self-biased High Frequency QR Flyback Converter with Integrated GaN

1 Features

- Integrated 700V GaN with 170mΩ $R_{ds(on)}$
- Dynamic QR/DCM/CCM modes of operation
- Support up to 500kHz switching frequency
- Enable low BoM cost by integration
  - Remove auxiliary winding with self bias
  - Integrated input/output voltage sensing
  - Integrated current sense
  - Integrated HV startup
  - Integrated X-cap discharge
- High efficiency and low EMI performance
  - Ultra-low standby power: <30mW
  - Frequency foldback and burst mode
  - Valley locking
  - Frequency dithering
  - Switching slew rate control
- Comprehensive protection features
  - Over Temperature Protection
  - Over Voltage Protection
  - Short Circuit Protection
  - Cycle-by-cycle current limit
  - Two-Level Over Power Protection with LPS
  - Brown-in/out Protection
  - Open feedback protection
- Flexible configurability via external resistors
  - X-cap discharge and CCM mode disable
  - Selectable switching slew rate
  - Multiple clamping frequency settings
  - Fault latch or auto-restart
  - Max/min peak current ratio
  - Dithering amplitude

2 Applications

- USB-PD Adapter for portable electronics
- USB wall outlets and docking stations
- Industrial DIN Rail power supplies
- Server Aux Power Supplies

3 Description

UCG28826 is a high frequency, quasi-resonant flyback converter with built-in 170mΩ GaN high electron mobility transistor (HEMT) to convert AC to DC for up to 65W power converters. It is best suited for high power density applications such as cell phone fast chargers and laptop adapters. The key feature of this device is the self-bias and auxless sensing scheme which completely eliminates the need of the auxiliary winding and simplifies the system design with higher efficiency.

This device also features intelligent mode transition (CCM/QR/DCM) to enable high efficiency across wide power range and <30mW standby power consumption. In addition, UCG28826 includes a full list of protections such as brown-in/out protection, SCP, OVP, OLP, OFB and OTP. The cycle-by-cycle current limit ensures fast response to the fault conditions to safeguard the system and improve the reliability. The Input feedforward and output voltage based OLP correction are implemented to meet LPS requirements. Furthermore, the UCG28826 has dedicated configuration pins to offer more flexibility. Only resistors are needed to tune certain parameters for each system, enabling a platform design with a single device.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
UCG28826	REZ (QFN-12)	5mm x 5mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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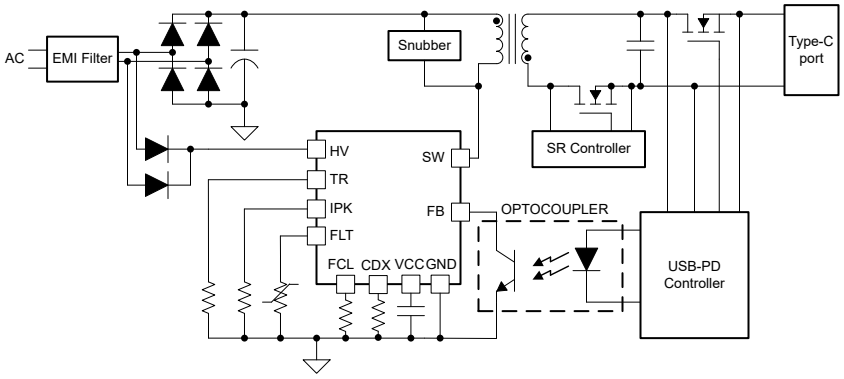

Simplified schematic of AC/DC Flyback Converter using UCG28826

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4 Pin Configuration and Functions

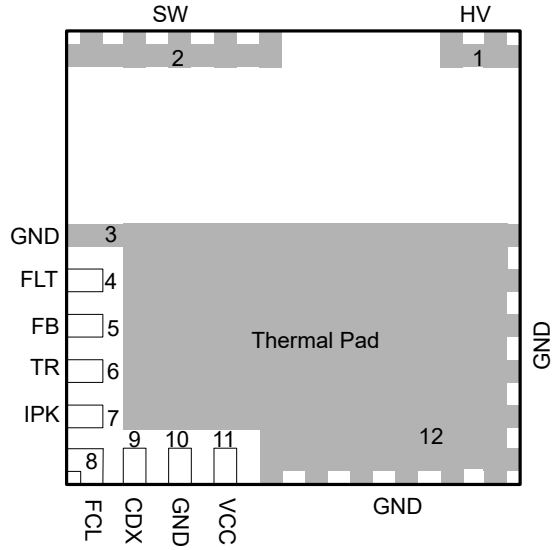

Figure 4-1. UCG28826 5 x 5mm Package, 12-Pin QFN, (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
HV	1	P	HV startup, AC line input presence detection and X-cap discharge
SW	2	P	Drain pin of integrated high-voltage GaN HEMT. This is also the sensing pin for valley switching and protections.
GND	3,10	G	Signal ground. Internally connected to power ground.
FLT	4	O	Fault pin for external overtemperature protection. Connect an NTC from this pin to GND.
FB	5	I	Feedback signal. Connect this pin to the collector of an optocoupler.
TR	6	I	Turns ratio setting. A resistor from this pin to GND sets the transformer turns ratio Np/Ns.
IPK	7	I	Peak current and frequency dither setting pin. A resistor from this pin to GND sets the maximum/minimum primary-side peak current and dithering depth.
FCL	8	I	Switching frequency clamp and fault behavior setting.
CDX	9	I	Multi-function pin to enable/disable CCM mode, gate drive current setting and X-cap discharge enable/disable.
VCC	11	P	IC bias supply. Connect an external capacitor (at least 10V rated) from this pin to GND. The capacitor value should be between 10uF to 47uF. The capacitor value is determined by the hold up time for missing input line cycles.
GND	12	G	Power ground. Connect to negative terminal of input bulk capacitor.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{HV}	GaN HEMT drain-source voltage, surge condition			800	V
$V_{SW(tr)(surge)}$	GaN power HEMT transient drain-source voltage, surge condition(2)			800	V
$V_{SW(surge)}$	GaN power HEMT drain-source voltage, surge condition, FET off(2)			750	V
V_{SW}	GaN power HEMT drain-source voltage, FET off			700	V
I_{DS}	GaN power HEMT continuous current, FET on		Internally limited		A
	Pin voltage	FLT, TR, IPK, FCL, CDX, FB	–0.3	5.5	V
		VCC	–0.3	6.2	
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) See GaN HEMT Switching Capability for more information on the GaN power FET switching capability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (all pins except HV and SW pins) (1)	±2000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (HV and SW pins) (1)	±1000	
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I_{SW}	SW pin current, continuous			4.5	A
V_{VCC}	VCC supply, self-regulating	5.2		6	V
C_{VCC}	Capacitance on VCC pin	10		47	µF
C_{X2}	X2 capacitance			1	µF
L_{MAG}	Primary magnetising inductance			380	µH
L_{LK}	Primary winding leakage inductance			3	%
C_{SW}	SW pin capacitance (GaN HEMT excluded)			300	pF
C_{HV}	HV pin parasitic capacitance		50	100	pF
T_A	Ambient temperature	–40		105	°C
T_J	Junction temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		UCG28826 REZ (QFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
Y_{JB}	Junction-to-board characterization parameter	7.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS SUPPLY						
$V_{VCCSHORT}$	Threshold for reduced VCC startup current			0.9		V
I_{HVLO}	Reduced HV startup current	Before VCC reaches $V_{VCCSHORT}$		1		mA
I_{HVHI}	Full HV startup current	After VCC exceeds $V_{VCCSHORT}$		4		mA
V_{VCCOFF}	VCC under voltage lock out threshold			5.1		V
V_{VCC_REG}	VCC regulation voltage and start-up threshold			5.8		V
V_{VCC_CHG}	VCC charging trigger threshold	Trigger VCC charging to V_{VCC_REG}		5.6		V
I_{VCC}	Operating supply current	No switching		700		µA
$I_{VCCSLEEP}$	Supply current in burst mode	No switching		250		µA
$I_{VCCFAULT}$	Supply current when a protection is triggered			250		µA
GAN POWER TRANSISTOR						
R_{DSON}	Drain-source on-resistance	T_J = 25 °C		170		mΩ
C_{OSS}	Output capacitance	V_{SW} = 400V		40		pF
GAN GATE DRIVER						
	Turn-on dV/dt	For SW node, V_{DS} = 325V, Option 1		7		V/ns
	Turn-on dV/dt	For SW node, V_{DS} = 325V, Option 2		5		V/ns
	Turn-on dV/dt	For SW node, V_{DS} = 325V, Option 3		3		V/ns
PEAK CURRENT CONTROL						
I_{PKMAX}	Maximum peak current	Option 1		2.8		A
		Option 2		3.1		
		Option 3		3.5		
I_{PKMAX}/ I_{PKMIN}	Max. to min. peak current ratio	Option 1		4		
		Option 2		3		
T_{SS}	Soft start time			4		ms
FEEDBACK CONTROL						
R_{FB}	FB pull-up resistor			60		kΩ
V_{FBOPEN}	Open FB Pin voltage	See Table 6-5				
	Mode transition thresholds					
V_{BST_OFF}	Burst-off threshold	Turn-off switching		250		mV

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BST_ON}	Burst-on threshold	Resume burst switching		300		mV
V_{BST_EX}	Burst mode exit threshold	Exit to frequency foldback		500		mV
$f_{MIN,CLAMP}$	Minimum frequency clamp	During normal operation		25		kHz
		During soft start		10		
T_{SWMAX}	Maximum time period			40		µs
T_{ONMAX}	Maximum on time			17		µs
$f_{MAX,CLAMP}$	Frequency clamp	Option 1		140		kHz
		Option 2		200		
		Option 3		250		
		Option 4		500		
T_{DDCM}	DCM ring fixed timer	From last seen DCM ring valley		3.75		µs
EMI DITHERING						
$f_{carrier}$	Carrier frequency			390		Hz
$I_{Dither,max}$	Carrier amplitude	% of instantaneous peak currents, Option 1		±6.25		%
		% of instantaneous peak currents, Option 2		±12.5		
PROTECTIONS						
V_{TH_BI}	Brown-in threshold			112		V
V_{TH_BO}	Brownout threshold			98		V
T_{DBO}	Brown-out delay time			60		ms
I_{FLT}	FLT pin source current			75		µA
V_{TH_OTP}	FLT threshold voltage	Triggers external overtemperature fault		0.6		V
	I_{FLT} on time			260		µs
	I_{FLT} time period			10		ms
	Number of external TSD cycles	Before fault is triggered		3		
R_{SW}	SW pin impedance			9.5		MΩ
V_{OVP}	OVP detection threshold	V_{OUT} threshold		25		V
	Internal overtemperature protection shut down threshold	Temperature increasing		150		°C
	Internal overtemperature protection hysteresis	Temperature reducing		10		°C
T_{RETRY}	Auto-retry time			1		s
P_{OPPH}	Over power protection threshold	Triggers after 80ms		140		W
P_{OPPL}	Over power protection threshold	Triggers after 4.2s		90		W
I_{LPS}	LPS fault output current threshold	Input referred, triggers after 4.2s		7		A
I_{SCP}	Short Circuit Protection	Primary current threshold		4.5		A
	Short Circuit Protection	No of cycles		3		
t_{SCP}	Short-circuit response time			140		ns
X CAP DISCHARGE						
I_{ACDET}	Line removal detection current	Current sink from HV pin		2		mA
I_{XDIS}	X-cap discharge Current			5		mA
T_{XDIS}	X-cap discharge Time	C_{XCAP} = 1µF			1	s

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6 Detailed Description

6.1 Overview

The UCG28826 is a high frequency, quasi-resonant (QR) AC/DC flyback converter with integrated 700V primary-side GaN high electron mobility transistor (HEMT)(hereinafter referred to as GaN HEMT) suitable for use in power supplies up to 65W. This device gives benefit of GaN integration to achieve high power density designs with high switching frequency up to 500kHz.

The UCG28826 features industry's first auxless flyback architecture with self-bias to give a compact and low cost power supply design without the need for an auxiliary winding in the transformer. The self bias feature reduces losses to improve efficiency in wide output voltage applications like USB-PD chargers by eliminating the need for a low dropout regulator (LDO) and its associated losses to generate the device bias.

The UCG28826 supports continuous conduction mode (CCM) operation for upto 4msec for transient output power conditions of min. 130W (two times the 65W nominal output power) in low-line input conditions without the need for a transformer designed for such transient load conditions, saving space and cost. This device also includes frequency foldback and burst modes for higher efficiency operation during light load and no-load conditions, respectively. The X-cap discharge circuit discharges the X-capacitor in the input EMI filter to 0V within less than 1s to prevent the user from an electric shock at the time of unplugging the power supply from the wall socket.

The UCG28826 overcomes the system design limitations of integrated converters by offering resistor programmable options to the user for maximum flexibility to optimize performance at the desired operating point. The device also includes many built-in protections such as output over-voltage protection (OVP), short-circuit protection (SCP), two-level over power protection (OPPH and OPPL) and over-temperature protections (OTP) with auto-restart and latch response for a robust power supply design preventing any damage during such fault conditions.

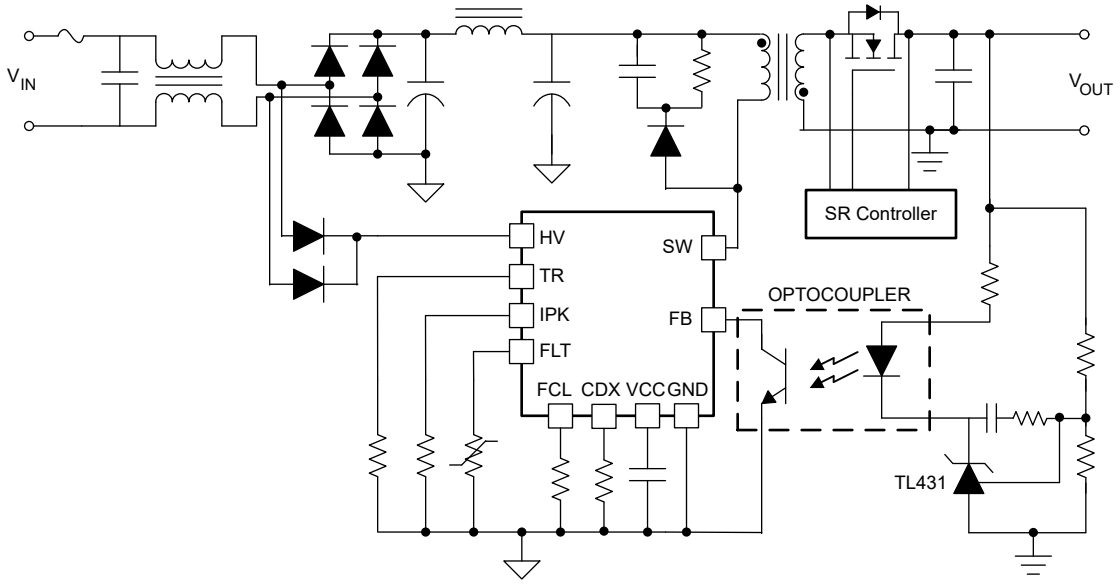

Figure 6-1. AC/DC Flyback Converter Schematic using UCG28826

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6.2 Functional Block Diagram

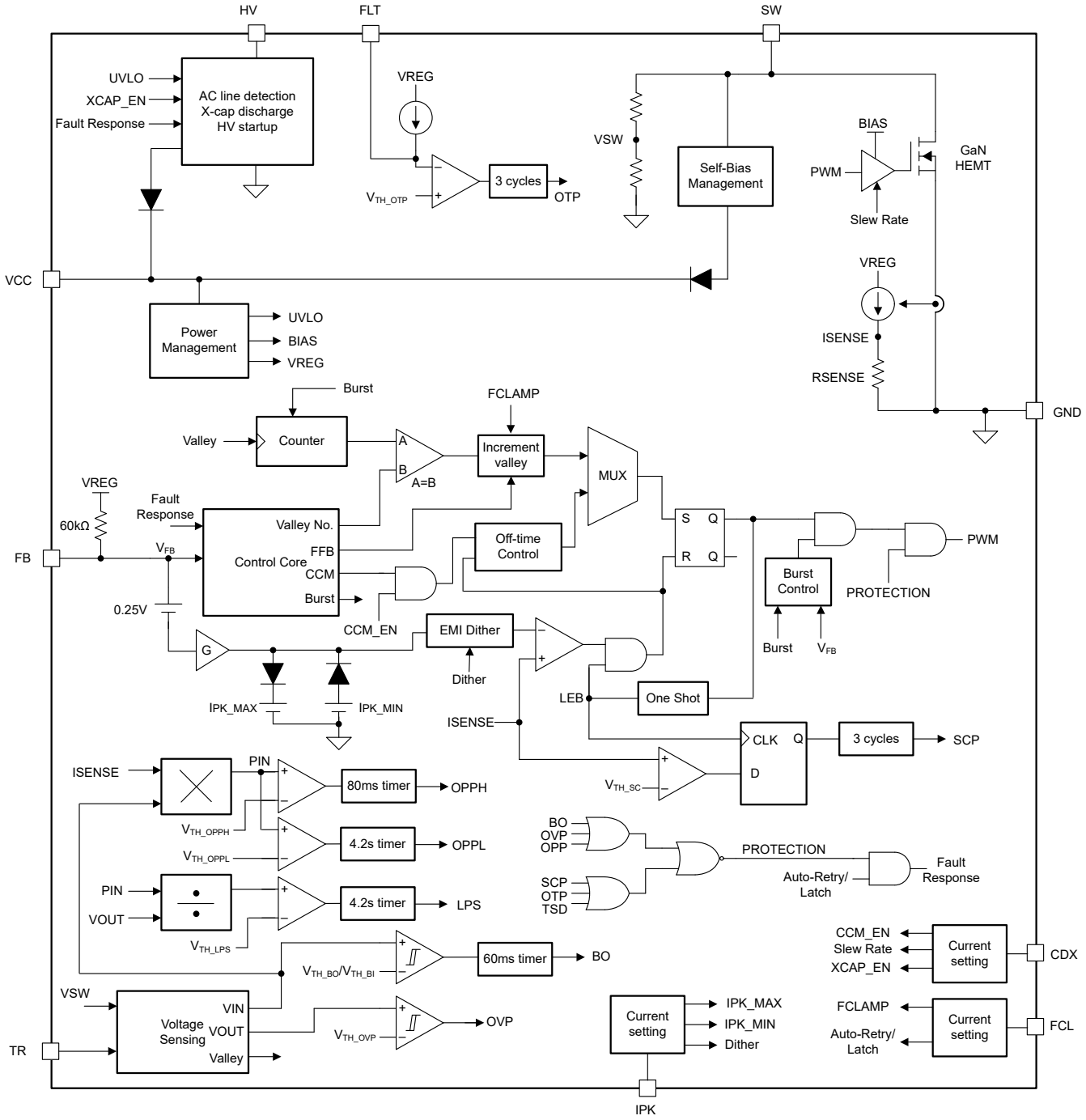

Figure 6-2. Functional Block Diagram

6.3 Detailed Pin Descriptions

The UCG28826 is a QR flyback converter with integrated 700V GaN HEMT with self bias and auxless sensing. It includes HV, SW and GND pins for interface with the flyback power stage components. In addition to this, the device has bias supply and a feedback pin for secondary side regulation. There are several programmable setting pins for user to configure the device for their power supply design. These programming pins require a resistor to ground and offer the flexibility to optimize various parameters during power stage design enabling a platform design with a single device.

6.3.1 HV - High Voltage Input

The high voltage (HV) pin should be connected to the two ends of the X-capacitor at the line input, through two diodes as shown in Figure 6-1. This pin charges the bias supply (VCC) capacitor at startup. The HV pin also discharges the X-capacitor when the input line voltage is removed.

6.3.2 SW - Switch Node

The SW pin should be connected to the switch node on the primary side of the flyback converter. This is the drain of the integrated 700V GaN HEMT. This is also the sensing pin for valley switching and OVP, OPP and LPS protections. The maximum total switch node capacitance at this pin should be minimized to keep the switching losses low. The capacitance seen at the SW pin includes the transformer parasitic capacitance, GaN HEMT drain-source capacitance, reflected capacitance from secondary side and any additional capacitance which may be added to slow down the switch node turn-on and turn-off slew rates.

6.3.3 GND – Ground Return

The GND pin is the external return pin, and provides a reference point for the internal circuitry and the gate drive of the device. This is the return pin for the power stage and should be connected to the negative terminal of the input bulk capacitor(s).

6.3.4 FLT - External Overtemperature Fault

Connect a negative thermal coefficient (NTC) resistor from this pin to GND for monitoring the temperature of a critical point on the power supply external to the device, and trigger overtemperature protection to avoid damage to components. The device sources 75µA current into the NTC. As the NTC resistance reduces with increase in sensed temperature, the external over-temperature fault is triggered when the voltage on FLT pin reduces to less than 0.6V. See Section 6.4.10.5 for details of overtemperature protection.

6.3.5 FB – Feedback

Connect the feedback (FB) pin to the collector of the optocoupler for secondary side regulation. This pin has an internal 60kΩ pull up for optocoupler bias. The instantaneous voltage on this pin determines the switching frequency, peak current and mode of operation (burst, foldback, valley switching or CCM) as per the control law in Figure 6-4 to deliver the required output power. Connect a 100pF or 220pF capacitor from this pin to ground for high frequency noise filtering.

6.3.6 TR - Turns Ratio

Set the transformer turns ratio information with a resistor from this pin to GND as per values in Table 6-1. This turns ratio information is used for output voltage sensing. The resistor need to be 1% accurate.

Table 6-1. Turns Ratio Setting Resistor Values

TR Pin Resistor (kΩ)	Turns Ratio
0	7.875
5.23	6
6.34	6.125
7.68	6.25
9.31	6.375
11.3	6.5
13.7	6.625
16.9	6.75
20.5	6.875
25.5	7
31.6	7.125
39.2	7.25
51.1	7.375
66.5	7.5
84.5	7.625
113	7.75
174	7.875

6.3.7 IPK - Peak Current and Dithering

This pin offers settings for peak current thresholds and dithering. Connect a resistor from this pin to GND as per values in Table 6-2 to select the preferred option for the following specifications:

- Maximum peak current
- Ratio of maximum to minimum peak current
- EMI dithering depth

Table 6-2. IPK Pin Programming Resistor Values

IPK Pin Resistor (kΩ)	Maximum Peak Current (A)	$I_{PK,MAX}/I_{PK,MIN}$	EMI Dithering Depth (%)
0	3.1	4	6.25
5.23	2.8	4	12.5
6.34	3.1	4	12.5
7.68	3.5	4	12.5
9.31	2.8	3	12.5
11.5	3.1	3	12.5
14.3	3.5	3	12.5
17.8	2.8	4	6.25
22.6	3.1	4	6.25
28.7	3.5	4	6.25
36.5	2.8	3	6.25
51.1	3.1	3	6.25
75	3.5	3	6.25

6.3.8 FCL - Frequency clamp and fault response

Use the FCL pin to select the maximum switching frequency clamp value and fault response behavior. Table 6-3 lists the resistor values to be used for the given operating conditions. The resistor needs to be 1% accurate.

Table 6-3. FCL Pin Programming Resistor Values

FCL Pin Resistor (kΩ)	Frequency Clamp (kHz)	Fault Response
0	140	EXTOTP and OVP Latched, rest Auto retry
5.23	140	All latched
6.34	200	All latched
7.68	250	All latched
9.31	500	All latched
28.7	140	EXTOTP fault and OVP Latched, rest Auto retry
36.5	200	EXTOTP fault and OVP Latched, rest Auto retry
51.1	250	EXTOTP fault and OVP Latched, rest Auto retry
75	500	EXTOTP fault and OVP Latched, rest Auto retry

6.3.9 CDX - CCM, drive strength and X-cap discharge

Use the CDX pin to enable/disable CCM mode and X-cap discharge and select the SW node slew rate when turning on the GaN HEMT. Refer to Table 8-4 for values of resistors to connect from this pin to GND for the given operating points. The resistor needs to be 1% accurate.

Table 6-4. CDX Pin Programming Resistor Values

CDX Pin Resistor (kΩ)	CCM	SW node turn-on slew rate	X-cap discharge
5.23	Disabled	7V/ns	Enabled
6.34	Disabled	5V/ns	Enabled
7.68	Disabled	3V/ns	Enabled
9.31	Disabled	7V/ns	Disabled
11.5	Disabled	5V/ns	Disabled
14.3	Disabled	3V/ns	Disabled
17.8	Enabled	7V/ns	Enabled
22.6	Enabled	5V/ns	Enabled
28.7	Enabled	3V/ns	Enabled
36.5	Enabled	7V/ns	Disabled
51.1	Enabled	5V/ns	Disabled
75	Enabled	3V/ns	Disabled

6.3.10 VCC - Input Bias

The VCC pin provides the bias to the device, powering the internal references, gate driver, regulators, control circuits and protection features. Use a minimum of 10µF capacitance from this pin to GND for maintaining VCC voltage regulation with self-bias feature. Use of an additional 10nF ceramic capacitor in parallel is recommended for low ESR and minimum over/undershoot on this pin. Use 30µF capacitance at this pin for holdup without reset in the event of two missing line cycles at the input.

6.4 Feature Description

6.4.1 Self Bias and Auxless Sensing

The UCG28826 includes self bias and auxless sensing to eliminate the transformer auxiliary winding. This makes the system design simpler, smaller and cheaper by reducing the auxiliary winding and the associated components.

The self bias feature is especially useful in application like USB-PD chargers with wide output voltage range. Typically in such designs, the aux winding generates device supply voltage (VCC) greater than its UVLO threshold at the minimum V_{OUT} which is 3.3V. In such case, the voltage on aux winding increases six times when V_{OUT} = 20V which needs an internal/external power conversion stage to reduce to VCC range, increasing external components and reducing efficiency. The UCG28826's self bias eliminates the need for such additional power conversion stage at the VCC pin thus reducing the number of components and recovering their power losses. The self bias circuit is designed to keep VCC higher than its UVLO threshold throughout the range of operation of the device, given the components around the device are used within the datasheet recommended range. Auxless sensing circuits are connected to the SW pin. The device senses the voltage on SW for valley sensing and various protections.

6.4.2 Control Law

The UCG28826 is a peak current mode control QR flyback converter. The converter starts by turning on the primary-side integrated GaN HEMT. The current in the transformer primary side winding I_{PRI} increases with a slope dependent on V_{IN} and primary magnetizing inductance L_M and equals V_{IN}/L_M. Once I_{PRI} reaches the peak value $I_{PK,PRI}$, the GaN HEMT turns off. By flyback action, the secondary winding voltage increases and turns on the synchronous rectifier (SR) FET body diode to clamp to output voltage V_{OUT}. During this time, the secondary winding current reduces from secondary peak current $I_{PK,SEC}$with a slope V_{OUT}/L_S, where $L_S$is the secondary winding inductance. The switch node voltage is equal to the sum of V_{IN} and primary to secondary turns ratio N times V_{OUT}, called the plateau voltage. Once the secondary current reduces to zero, L_M and total switch node capacitance C_{SW} begin to resonate to cause magnetizing ring. The UCG28826 turns on the primary GaN HEMT at a valley in this magnetizing ring to reduce the turn-on switching losses.

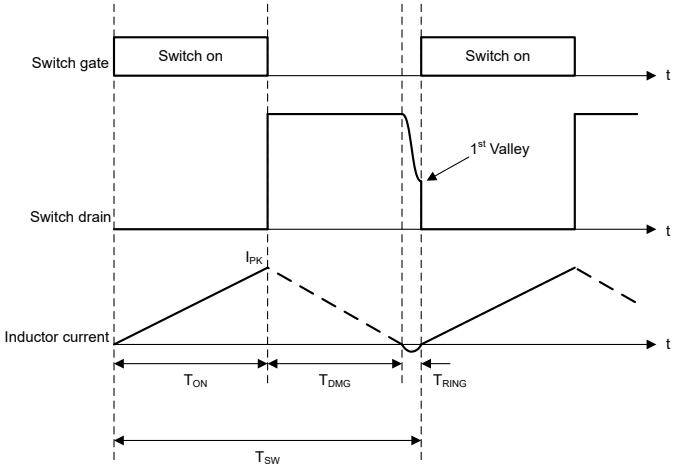

Figure 6-3. Flyback converter waveforms

Hence, in UCG28826, in every cycle, the primary GaN HEMT turns off after reaching the peak current threshold and turns on next at a target valley in magnetizing ring during discontinuous mode (DCM) operation. The instantaneous primary peak current and target valley is determined by the feedback (FB) pin voltage as per the control law of Figure 6-4. Connect the FB pin to the optocoupler collector. The negative feedback loop sets FB pin voltage to the required value to support a certain V_{OUT} and P_{OUT} on the output. The device can operate in one of the four modes of operation: burst, frequency foldback, valley switching or continuous conduction mode, as described later.

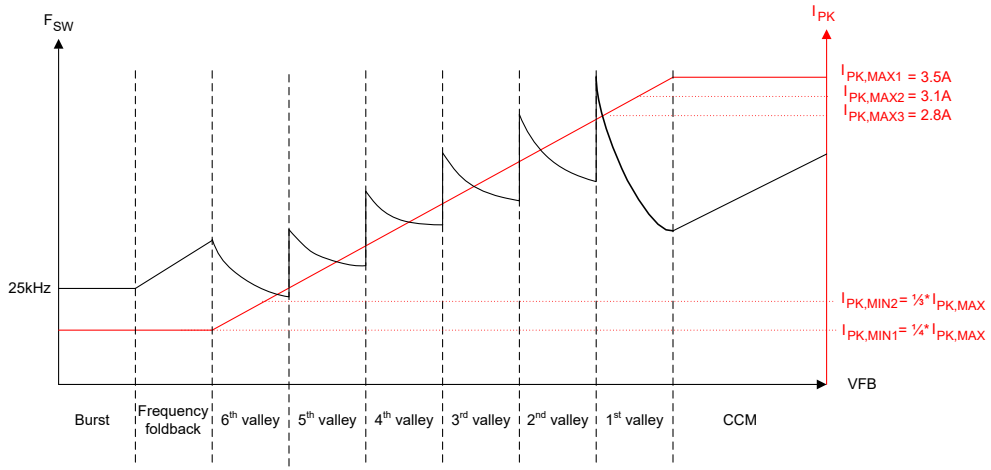

Figure 6-4. UCG28826 Control Law

In the control law shown in Figure 6-4, the UCG28826 offers flexibility to select a max peak current $I_{PK,MAX}$ to optimize for the switching frequency at rated load and transformer size. For each $I_{PK,MAX}$ setting, a scaling ratio of 1/3rd or 1/4th is available for the minimum peak current $I_{PK,MIN}$. This $I_{PK,MIN}$ value determines the switching frequency and losses in light load conditions when the flyback converter is operating in frequency foldback or burst modes. For all values of $I_{PK,MAX}$ and $I_{PK,MIN}$, the slope of control law peak current vs feedback voltage remains the same, as per Equation 1. Table 6-5 shows the threshold voltages for transition between different modes and between valleys for different peak current settings of Table 6-2.

Table 6-5. FB Pin Voltage Thresholds for Various Peak Current Settings

	PARAMETER	TEST CONDITIONS	$I_{PK,MAX}$=2.8A	$I_{PK,MAX}$=3.1A	$I_{PK,MAX}$=3.5A	UNIT
V_{FBOPEN}	Open FB pin voltage		3.3	3.45	3.65	V
$V_{THCCMto1}$	CCM to 1st valley threshold	VFB decreasing	2.18	2.4	2.65	
V_{TH12}	1st to 2nd valley threshold		1.09	1.19	1.31	
V_{TH23}	2nd to 3rd valley threshold		0.97	1.05	1.16	
V_{TH34}	3rd to 4th valley threshold		0.91	0.98	1.08	
V_{TH45}	4th to 5th valley threshold		0.85	0.92	1.0	
V_{TH56}	5th to 6th valley threshold		0.79	0.85	0.93	
V_{TH65}	6th to 5th valley threshold	VFB increasing	1.16	1.25	1.38	
V_{TH54}	5th to 4th valley threshold		1.22	1.32	1.46	
V_{TH43}	4th to 3rd valley threshold		1.28	1.39	1.53	
V_{TH32}	3rd to 2nd valley threshold		1.34	1.45	1.61	
V_{TH21}	2nd to 1st valley threshold		1.46	1.59	1.76	
$V_{TH1toCCM}$	1st valley to CCM threshold		2.18	2.4	2.65	
V_{THFF}	6th valley to frequency foldback threshold	$I_{PK,MIN}$=1/4 x $I_{PK,MAX}$	0.73	0.78	0.85	
		$I_{PK,MIN}$=1/3 x $I_{PK,MAX}$	0.89	0.96	1.05	

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6.4.2.1 Valley Switching

The UCG28826 is designed to operate with soft switching and primary FET turn-on at a valley to reduce switching losses. The converter operates in valley switching except during peak load transients during which control can transition to CCM mode (if enabled using CDX pin). During valley switching mode, the target valley and peak current threshold are governed by the control law of Figure 6-4 and Equation 1:

$$I_{PK} = 1.45\ x\ (V_{FB} - 0.25) \quad (1)$$

During valley switching, with increasing output power, the peak current threshold continues to increase linearly as per above equation. The switching frequency also varies based on I_{PK} and valley targets corresponding to the instantaneous FB pin voltage. When output power is increasing from light loads to rated power, the control transitions from 6th valley till 1st valley with corresponding linear increase in I_{PK} threshold. As output power continues to increase further to take FB voltage to the edge of 1st valley operation, the converter transitions into CCM mode operation with I_{PK} clamped to its max. value $I_{PK,MAX}$ and increase in switching frequency F_{SW} with further increase in output load. This clamp on $I_{PK,MAX}$ limits the transformer size in a high density power supply design. See Section 6.4.2.4 for details of CCM mode of operation. If output power reduces while operating in 6th valley, the control transitions to frequency foldback mode to operate at higher valleys and lower frequency to reduce switching losses further.

The FB pin voltage thresholds for valley transitions include a hysteresis and vary depending on increasing or decreasing P_{OUT} to enable valley locking and prevent any audible noise due to hopping between valleys. Refer to the Electrical Characteristics table for FB pin voltage thresholds which determine the mode of operation for UCG28826. For zero optocoupler collector current with large P_{OUT}, the FB pin is pulled up to V_{FBOPEN} through a 60kΩ resistor.

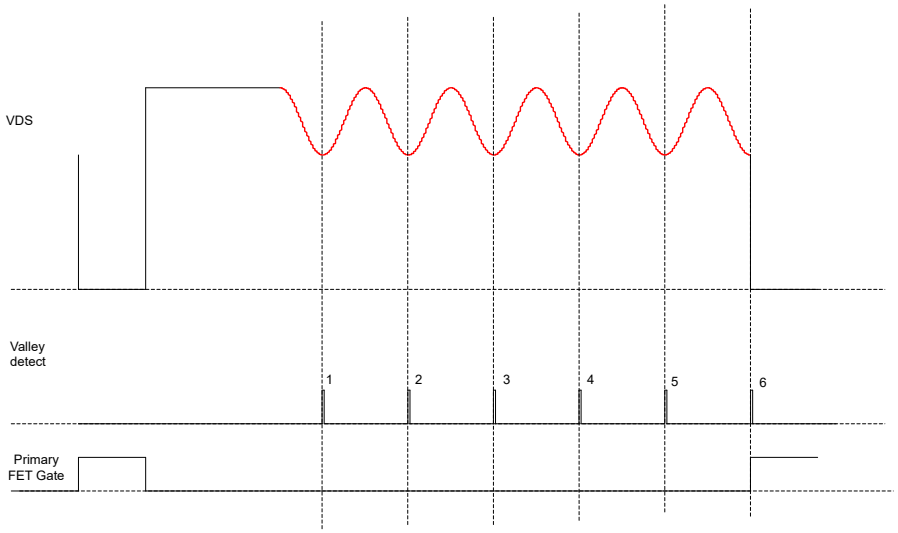

Figure 6-5. Valley counter with continuous valley occurrence

Typically, the control counts the valleys and turns on the primary GaN HEMT once the target valley is reached, shown in Figure 6-5. For the case when SW node waveform is damped so the valleys disappear before reaching the target valley, a DCM ring fixed timer of 3.75µs starts to continue counting valleys and turn on the primary GaN HEMT once the valley target is reached, shown in Figure 6-6. During startup (soft start) when V_{OUT} is small, if the valleys don't appear, the controller turns on the primary GaN HEMT after 100µs from last turn on, to switch at 10kHz (min. frequency clamp during soft start) for initial few cycles to avoid latch up condition.

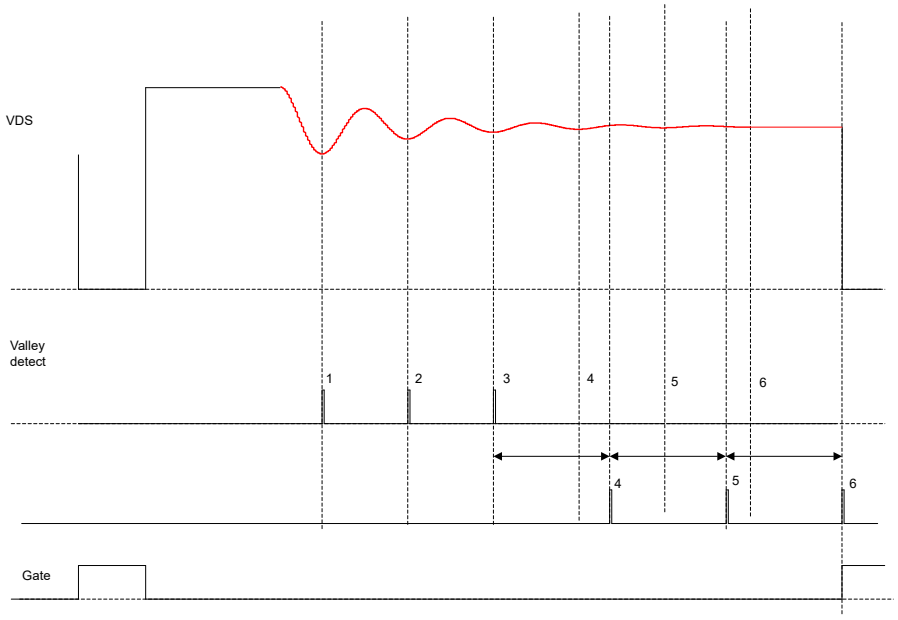

Figure 6-6. Valley counter with missing valleys

The device operates in CCM mode for maximum 4ms to support any transient output load conditions, as seen in notebook chargers and other applications. The converter returns to 1st valley QR operation after expiry of this 4ms CCM timer. At all times during operation of UCG28826, the maximum switching frequency can be limited with a frequency clamp setting programmable with a resistor from FCL pin to GND, as detailed in Section 6.3.8.

6.4.2.2 Frequency Foldback

If output power reduces while operating in 6th valley to reduce FB pin voltage below V_{THFF}, the converter transitions to frequency foldback mode and abandons valley switching. The peak current threshold is clamped to $I_{PK,MIN}$ and converter operates at higher valleys after 6th valley, depending on FB pin voltage. This causes the switching frequency to reduce further with increase in target valley number, till switching frequency reduces to and is clamped at 25kHz. Minimum switching frequency is clamped to 25kHz to prevent any audible noise, with a total switching cycle time of 40µs. Further reduction in output power takes the converter to burst mode to reduce unnecessary switching losses from periodic switching and achieve very low standby power consumption.

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6.4.2.3 Burst Mode

If output power continues to reduce while in frequency foldback mode, the device enters burst mode when FB pin voltages reaches 0.25V for the first time and the device stops switching. Due to this, depending on the output power, once FB pin voltage recovers to 0.3V is when device resumes switching in burst mode.

The UCG28826's burst mode offers three 1st valley QR switching cycles followed by a min. 70µs delay before start of next burst packet. Valley switching reduces switching losses while the delay limits power delivery in burst mode and device transitions to other modes of operation at higher power to maintain high efficiency in the range of output power. In burst mode, frequency clamp is fixed at 250kHz and primary GaN HEMT turns on at next valley after expiration of clamp timer. With this, switching losses are kept low with valley switching with limit on electromagnetic emissions with minimum peak current to pass emission standards. Burst mode switching waveforms are shown in Figure 6-7.

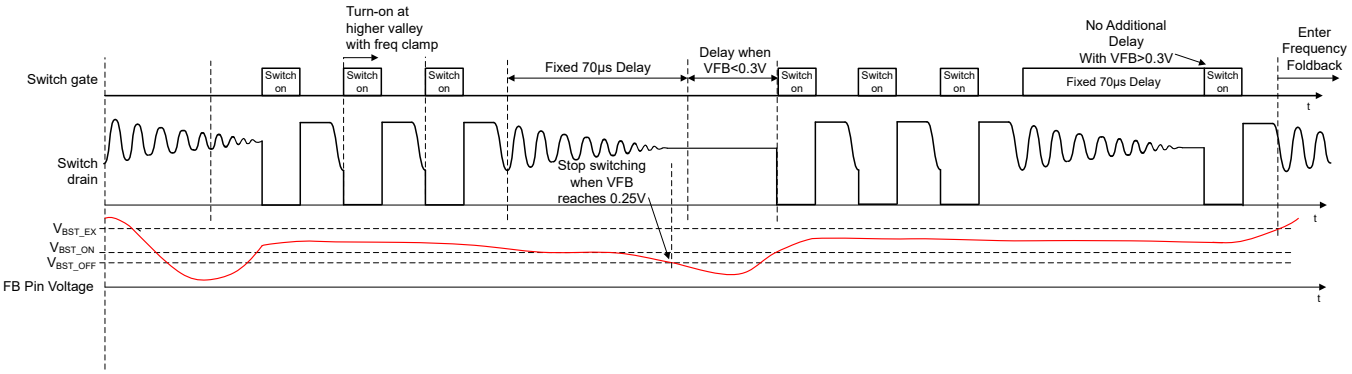

Figure 6-7. Burst Mode Entry and Exit Waveforms

6.4.2.4 Continuous Conduction Mode (CCM)

As shown in Figure 6-4, once the boundary of 1st valley QR operation is reached with increasing output power, the control clamps I_{PK} to the maximum selected value $I_{PK,MAX}$, and begins to reduce the secondary conduction time T_{OFF} in CCM mode. This reduction in T_{OFF} is proportional to increase in FB pin voltage, till 50% of the QR mode off-time to reach 1.5x the QR mode output power delivery capability. Care needs to be taken to use a primary magnetizing inductance L_M large enough to not hit the frequency clamp and avoid any subharmonic oscillations which could increase output voltage ripple, depending on application requirements. For long duration output power transients, the converter returns to 1st valley QR mode after expiry of the 4ms CCM timer and continues to deliver the largest possible output power at the transition point of QR and CCM modes, while operating in QR mode. The device offers flexibility to enable/disable CCM mode operation with a resistor from the CDX pin to GND as per values in Table 6-4.

6.4.3 GaN HEMT Switching Capability

The UCG28826's primary-side integrated GaN HEMT's switching capability is explained with the help of Figure 6-8. The figure shows the drain-source voltage (same as SW pin voltage) for the UCG28826 for two distinct switching cycles in a flyback application. The first is a normal switching cycle followed by a surge switching cycle in DCM/valley switching condition.

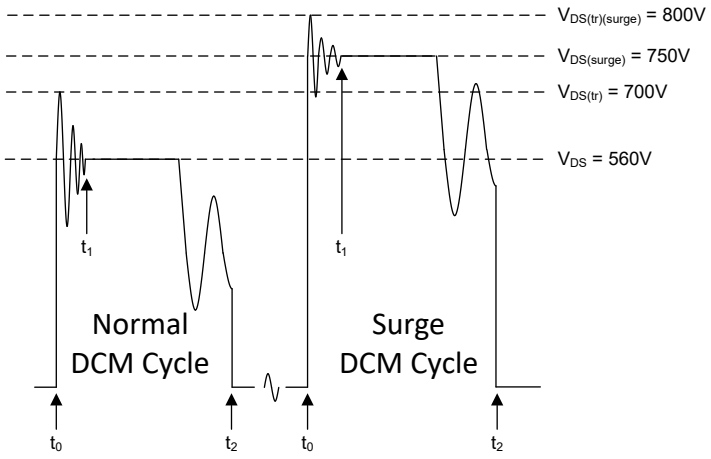

Figure 6-8. GaN HEMT Switching Capability

Each cycle starts before t_0 with the GaN HEMT in on state. At t_0, the GaN HEMT turns off and the parasitic elements cause the drain-source voltage to ring at a high frequency. The high frequency ringing has damped out by t_1. Between t_1 and t_2, the HEMT drain-source is at a flat plateau voltage with reducing secondary winding current in a flyback design. At t_2, the GaN HEMT turns on at a valley. For normal operation, the transient ring voltage is limited to 700V and the plateau is limited to 560V. For rare surge events, the transient ring voltage is limited to 800V and the plateau is limited to 750V.

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6.4.4 Soft Start

When turned on, a flyback converter starts with 0V output voltage. This can cause the feedback voltage FB to clamp to its max. value and trigger overload protections. To prevent this from happening, the UCG28826 starts in soft start mode. During this time, an internal FB voltage ramp increases in eight steps from 0V to max. value in 4ms. The max. value of internal FB ramp is at FB pin voltage equivalent of 80% of $I_{PK,MAX}$ setting and changes for different resistor settings on IPK pin. During this time, the smaller of this internal ramp voltage and actual FB pin voltage is used to determine the device operating point in the control law of Figure 6-4. Once the internal FB ramp voltage reaches the max. value is when control is transferred to FB pin voltage for output regulation. Soft start sequence is executed every time at start up or when recovering from fault (auto-retry or latch) and brown-out conditions. The minimum frequency clamp is changed to 10kHz only during soft start (which is otherwise at 25kHz during normal operation). This helps at startup when valleys are missing and the control law forces turn-on of primary GaN HEMT every 10µs from the last turn-on edge (if valleys are missing), to charge the output capacitor.

6.4.5 Frequency Clamp

The UCG28826 includes frequency clamp to limit the maximum switching frequency. This is useful during design optimizations to pass emissions standards and reduce switching losses by limiting the switching frequency to a certain value. The device offers four max. frequency clamp settings at 140kHz, 200kHz, 250kHz and 500kHz which can be selected with a resistor from FCL pin to ground as per values in Table 6-3. In no condition does the switching frequency exceed the chosen value of clamp frequency, except in burst mode when clamp frequency is set to 250kHz.

The minimum switching frequency is also clamped to a fixed 25kHz to prevent switching in the audible frequency range and noise from the flyback converter. Such low switching frequency can occur during operation in higher valleys or frequency foldback mode.

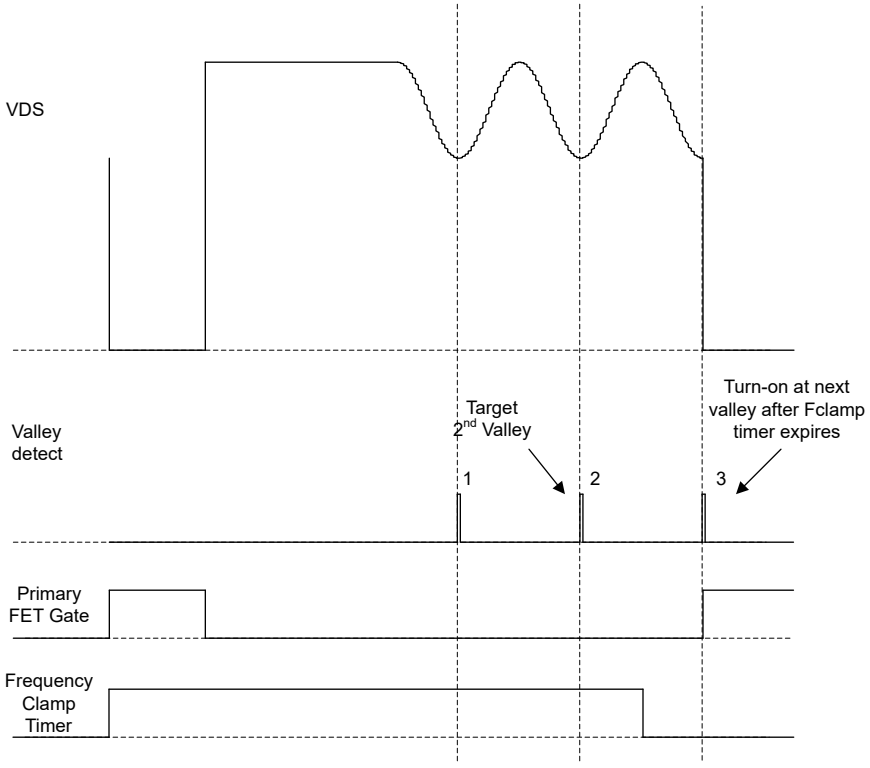

Figure 6-9. Primary GaN HEMT turn-on delay due to frequency clamp

6.4.6 Frequency Dithering

The UCG28826 includes frequency dithering to spread the energy in the spectrum around the switching frequency to reduce electromagnetic emissions making it easier to qualify various emissions standards. Since this device uses peak current mode control to turn-off the primary GAN HEMT, the dithering in frequency is achieved with small change to the value of peak current threshold in every switching cycle. This changes the peak current, and thus the on-time, off-time and switching frequency in every cycle. The per cent change to peak current threshold varies based on a fixed 390Hz triangular carrier signal with 32 steps alternating in sign at every transition from minimum (0%) to maximum value (called dithering depth, 6.25% or 12.5%) in every carrier cycle. The alternating sign of dither perturbation at each step and the low frequency output pole of flyback converter topology averages the cycle-to-cycle power delivery, causing small impact in output ripple due to dithering. The dither perturbation to peak current is asynchronous with the switching frequency and the instantaneous change in peak current is calculated based on the dithering signal during the primary GAN HEMT turn-on time.

The dithering depth can be chosen with a resistor from IPK pin to GND as given in Table 6-2. Figure 6-10 shows the dithering carrier and peak current perturbation waveforms to dither the switching frequency.

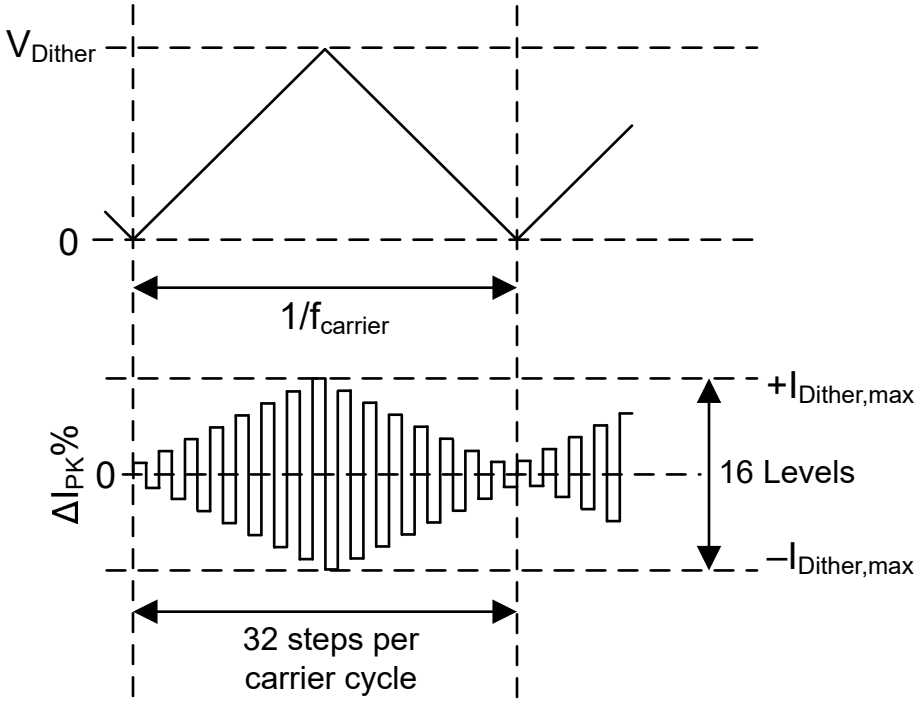

Figure 6-10. Frequency dithering to reduce emissions

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6.4.7 Slew Rate Control

The UCG28826 includes slew rate options for drain voltage reduction from switch node valley voltage to ground at the time of primary GaN HEMT turn-on. This GaN HEMT turn-on during valley switching happens at nearly zero current and incurs negligible additional losses with the slower turn-on due to slew rate control helping to meet various electromagnetic emission standards. Three slew rate options are available at 3V/ns, 5V/ns and 7V/ns, which vary marginally based on the valley voltage, as shown in Figure 6-11.

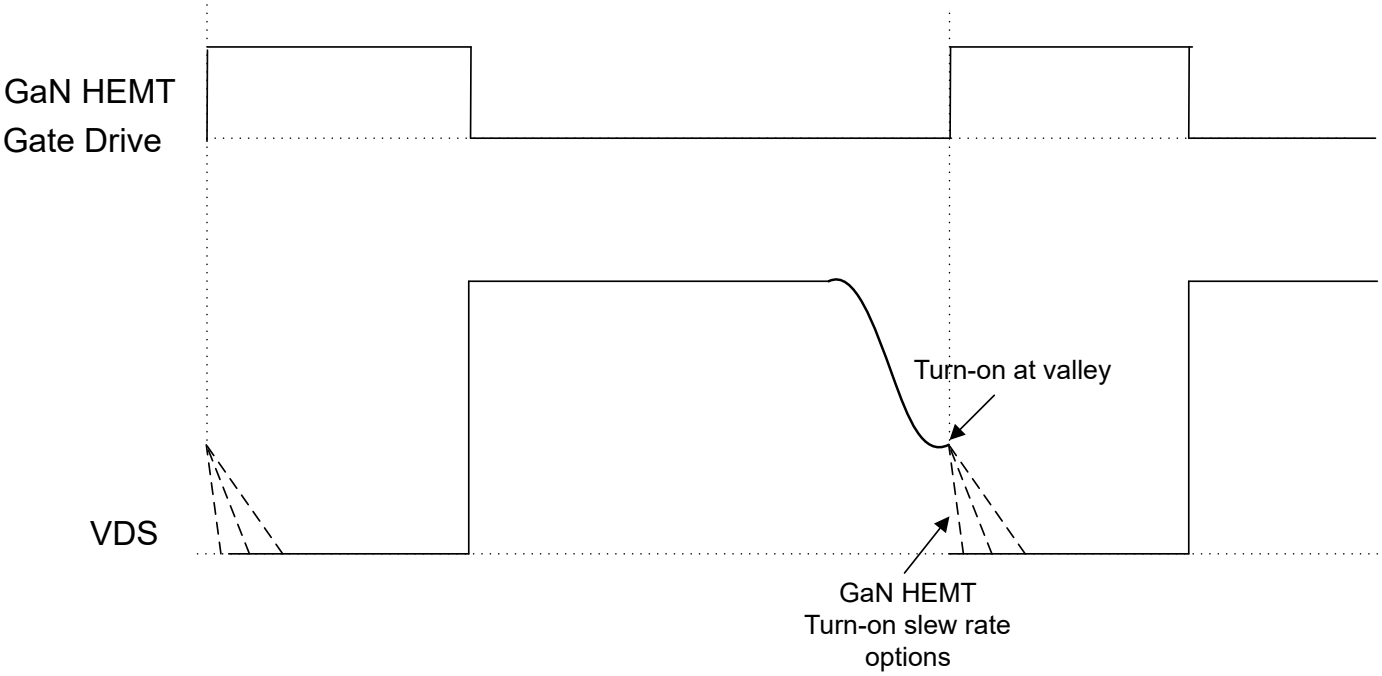

Figure 6-11. GaN HEMT Turn-on Slew Rate Control

Select the required slew rate value using a resistor from CDX pin to GND as per values in Table 6-4. At the primary GaN HEMT turn-off instant, the increase in SW node voltage depends on I_{PK} and total switch node capacitance C_{SW}. A gate drive current controlled reduction in this turn-off slew rate can increase losses significantly. If such reduction in GaN HEMT turn-off slew rate is needed, add an additional capacitor from GaN HEMT drain (switch node) to GND to reduce the rate of increase in switch node voltage at this turn-off instant.

6.4.8 Transient Peak Power Capability

The UCG28826 supports min. 2x transient peak output power capability for applications which require bursts of high power for short durations of time. This is achieved without the need for oversizing the various components such as the transformer, power FETs etc. and the same flyback design is usable for min. 2x the continuous output power rating for short durations. With this, a 65W flyback converter designed with UCG28826 can deliver min. 130W transient peak output power for max. 80 ms duration during high line and 4ms during low line operating conditions.

At high line input, the transient peak power delivery happens in DCM/QR modes of operation and is limited to max. 80ms duration as per OPPH protection described in Section 6.4.10.4. At low line input, due to limitations in power delivery from DCM/QR modes, the continuous conduction mode (CCM) extends the operation to min. 2x of the nominal power rating, and limited to max. 4ms duration. To limit from large output power delivery at high line input, the CCM mode is disabled for input bulk capacitor voltage higher than 200V DC. Further, CCM mode of operation at low line input (<200V DC) is limited to 4ms max. and device returns to 1st valley QR mode of operation if the transient output load does not reduce by the time of expiration of this 4ms timer. The CCM mode of operation is described in Section 6.4.2.4. Peak power delivery in DCM/QR modes at higher than 140W for longer than 80ms triggers OPPH fault, as detailed in Section 6.4.10.4. A min. 2x transient output power is supported, while max. instantaneous transient output power in DCM/QR/CCM modes depends on the input bulk capacitor voltage and the power stage component values and is limited in time by the respective CCM, OPPH, and OPPL timers.

6.4.9 X-Cap Discharge

Offline AC/DC power supplies use EMI filters with X-capacitors (X-cap) at the input. The UCG28826 includes an internal X-cap discharge circuit to completely discharge the X-cap and protect the user from an electric shock at the time of unplugging the power supply from mains input, as required by regulatory standards.

As shown in Figure 6-1, the X-cap is connected to the device HV pin through two diodes. No resistor is needed in this path. When the input line voltage is removed from the flyback converter, the X-cap is discharged with a current sink at the HV pin. The device ensures discharge of X-cap within <1s for line frequencies in the range from 45Hz to 66Hz for X-cap values up to 2µF.

6.4.10 Fault Protections

6.4.10.1 Brownout Protection

The device stops switching and enters brownout protection if input bulk capacitor voltage V_{BULK} reduces and stays below 98V (DC, or 70V (AC) input) for longer than 60 ms duration. This 60ms counter is reset if V_{BULK} exceeds 100V (DC) anytime before its expiration. Brownout protection avoids large primary currents and resultant conduction losses during irregular line input conditions. During low line input conditions, V_{BULK} can reduce below 98V (DC) in every line cycle with large P_{OUT}. During this time, since V_{BULK} recovers to greater than 100V (DC) in every line half cycle, the counter is reset, thereby avoiding brown-out fault from triggering and normal switching and power transfer can continue. Once brownout protection is triggered, the device auto-restarts after a 1s delay if V_{BULK} recovers to greater than 112V (DC, or 80V AC input) followed by soft start sequence to normal operation.

6.4.10.2 Short-Circuit Protection

The UCG28826 includes an overcurrent protection circuit to detect and prevent damage during overload conditions. This can occur during short-circuit of transformer windings, SR FET drain-source terminals or the flyback converter output. The device detects primary currents exceeding 4.5A (typ.) immediately after primary GaN HEMT turn-on and expiration of the leading edge blanking (LEB) time for SW node capacitance discharge to GND. If short-circuit current threshold is triggered for three consecutive cycles, a short-circuit fault is declared and switching stops. Fault response, auto-retry or latch, is as per selection with resistor on FCL pin.

6.4.10.3 Output Over Voltage Protection

The device monitors output voltage from the SW pin. If V_{OUT} exceeds 25V, an overvoltage protection (OVP) is triggered and switching stops. This protection prevents from damage to the output capacitors in an output overvoltage event, and hence this is a latched fault. Care must be taken to use the right TR pin resistor value to avoid mis-triggering this protection.

6.4.10.4 Over Power Protection (OPP, LPS)

The regulatory standards require the flyback converter output current and output power to not exceed 8A and 100W, respectively after 5s. The UCG28826 triggers over power protection (low, OPPL) for input power greater than 90W and/or output current (input referred) larger than 7A for longer than 4.2s duration, to prevent from excessive power delivery to the output in fault conditions. The device also supports transient load requirements of min. 2x the nominal output power rating (130W for 65W design) for upto 80ms beyond which over power protection (high, OPPH) is triggered. The device will work in CCM mode for V_{BULK} <200V for a max. 4ms duration.

6.4.10.5 Overtemperature Protection

The UCG28826 offers overtemperature protection to prevent system operation at excessively high temperatures and limit the components from exceeding their maximum ambient temperature ratings. The device has separate internal overtemperature protection to limit the die temperature and an external overtemperature protection to monitor and limit the system temperature using a resistor with negative temperature coefficient (NTC). The internal overtemperature fault triggers when die temperature exceeds 150℃ and switching stops. The device recovers to normal operation and switching resumes when the die temperature reduces below 140℃. The internal overtemperature protection is an auto-retry fault.

For the external overtemperature fault, connect the NTC between the FLT and AGND pins. To check for this fault, a 75µA current is sourced from the FLT pin through the external resistor to ground. This current is sourced for a 250µs on-time in every 10ms time period. An up-down counter increments every time when V_{FLT} is lower than 0.6V (typ.) with the sourced current. This counter decrements when V_{FLT} is higher than 0.66V (typ.) with a 60mV hysteresis during the 250µs duration. An external overtemperature fault is declared at a count of three, and this is a latched fault. The external overtemperature protection and 75µA sourcing current is disabled during burst mode operation to give <30mW (typ.) no-load system power consumption.

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6.4.10.6 Open FB Protection

The UCG28826 monitors for open FB pin condition to prevent from excessive power being delivered to the output with FB pin voltage clamped to max. value when this occurs. This condition can occur with a faulty or open-circuited optocoupler or even large power (greater than flyback converter's rated power) drawn for long time durations. This protection is asserted when FB pin voltage exceeds the CCM entry threshold for >80ms.

6.4.10.7 Error Codes for Protections

When the device enters fault mode after triggering one or more protections, an error code is sent on the CDX pin. This tells about the protection which is triggered, enables quick debugs during the power supply design process and faster time to market for the users. Figure 6-12 shows the error codes sent on the CDX pin for each of the protections. When a protection is triggered, the corresponding error code is sent three times on the CDX pin. If multiple protections are triggered, the output code includes multiple 1s (logic high) corresponding to the protections triggered.

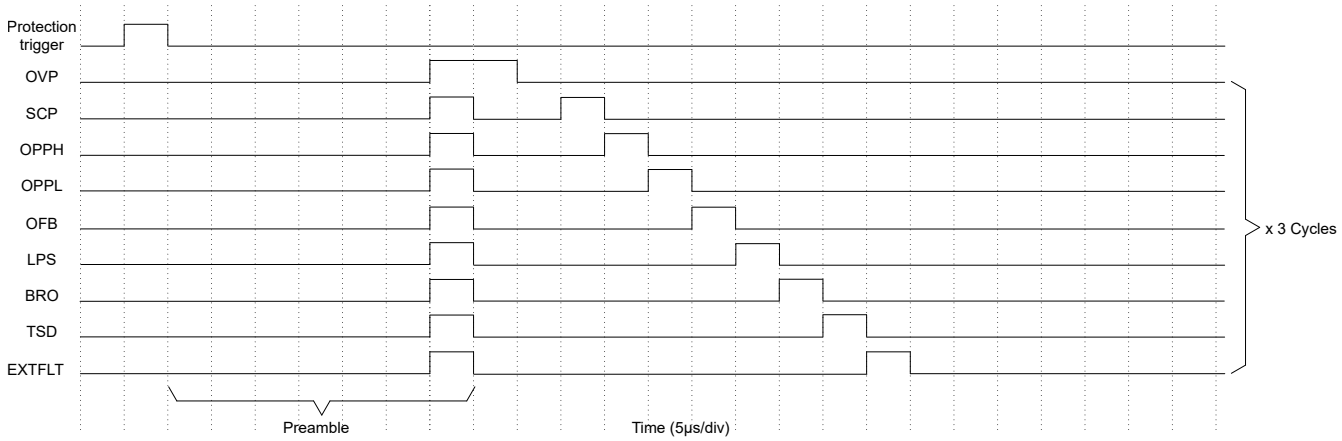

Figure 6-12. Error codes on CDX pin for various protections

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The UCG28826 is a 65W AC/DC flyback converter with integrated 700V GaN HEMT and secondary side output voltage regulation using optocoupler. The device offers self-bias and auxless sensing to eliminate the need for transformer auxiliary winding to give a simpler and lower cost solution. The UCG28826 with the integrated GaN HEMT is capable of switching upto 500kHz switching frequency to realize a small form factor and high power density flyback design.

7.2 Typical Application

The UCG28826 supports upto 65W AC/DC flyback designs which is useful for cellphone and notebook chargers, USB wall outlets, industrial power rails and server aux power supplies, amongst other applications. The integrated GaN HEMT and auxless sensing simplify the flyback design with the need to connect only key power stage components and the programming resistors to configure the design for the target application. Table 7-1 lists the design requirements for a typical 65W notebook charger.

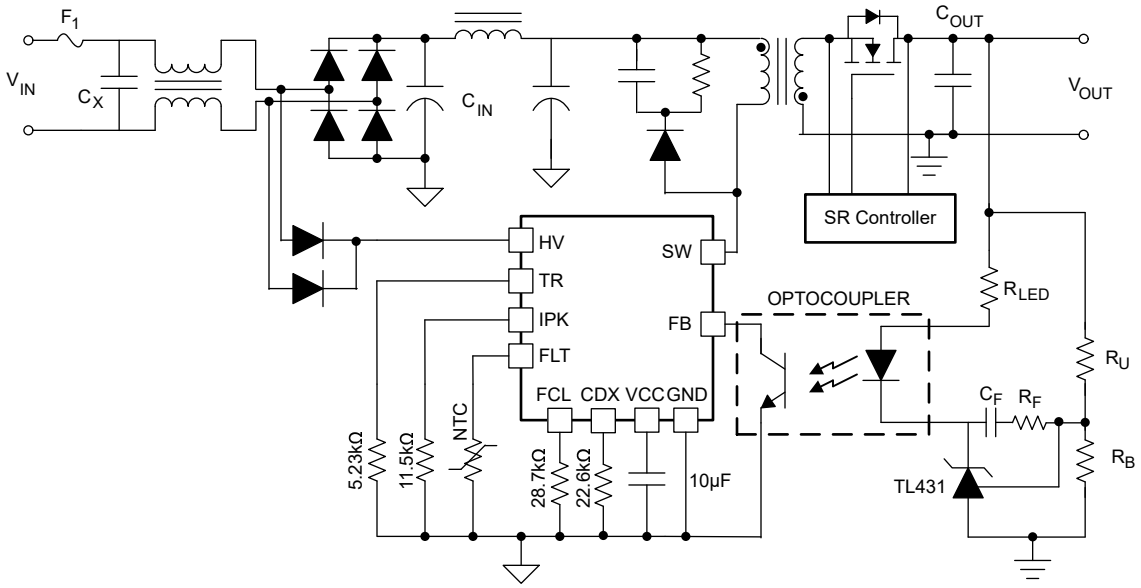

Figure 7-1. Typical Application Schematic

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7.2.1 Design Requirements

Table 7-1. Design Parameters

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line input voltage		90	115/230	264	VAC
Input bulk capacitor voltage		80			V
Line frequency		45	50/60	66	Hz
Output voltage/current	USB-PD output	5V/3A, 9V/3A, 15V/3A, 20V/3.25A			
Output power				65	W
Output ripple				200	mV
Efficiency		>93% at full load			
No-load input power				30	mW
Tiny load input power	P_{OUT} = 180mW			300	mW
Switching frequency				140	kHz

7.2.2 Detailed Design Procedure

This section describes the method for calculating the power stage component values.

7.2.2.1 Input Bulk Capacitor

The bulk capacitor includes one or more high voltage electrolytic capacitors in parallel at the output of the bridge rectifier. These are required for storing energy for the duration when instantaneous line input voltage reduces below its peak value while delivering rated output power. Input EMI filter design is outside the scope of this datasheet and not discussed.

It is required to maintain a certain minimum input bulk capacitor voltage ($V_{BULKmin}$) to prevent from triggering brown-out and ensuring sufficient power delivery. $V_{BULKmin}$ is assumed to be 75V for this design. The minimum required input bulk capacitance (C_{IN}) can be estimated using Equation 2. Its value depends on the rated input power, $V_{BULKmin}$, min. AC line input voltage and the time duration for which this capacitor needs to support the output load without reducing below $V_{BULKmin}$.

$$C_{IN} = \frac{2P_{IN}\, x \left(\frac{1}{4f_{AC}} + \frac{1}{2\pi f_{AC}} arcsin\left(\frac{V_{BULKmin}}{\sqrt{2}V_{ACmin}}\right)\right)}{\left(\sqrt{2}\, V_{ACmin}\right)^2 - \left(V_{BULKmin}\right)^2} \quad (2)$$

Using above equation, min. C_{IN} value comes to 100µF for P_{OUT} of 65W, 93% efficiency at V_{ACmin} of 85VAC. Multiple capacitors can be used in parallel to realize this value to reduce total ESR and size of these capacitors.

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7.2.2.2 Transformer Primary Inductance and Turns Ratio

The transformer turns ratio is limited by the primary GaN HEMT max. drain-source voltage (V_{DS}) rating and determines the secondary SR FET voltage rating and switching losses. The turns ratio is chosen as 6 for this design to reduce the snubber losses and improve efficiency. The UCG28826 supports turns ratio in the range from 6 to 7.875 for 20V output.

The transformer primary inductance determines the switching frequency through the range of flyback converter operation using UCG28826. For this design, the switching frequency is assumed at half of the maximum limit of 140kHz, which is 70kHz at low line input 90VAC. At this input voltage and full load 65W, the converter operates in 1st valley QR mode and the demagnetisation ringing duration is ignored to give duty cycle:

$$D_{max} = \frac{NV_{OUT}}{V_{IN} + NV_{OUT}} \tag{3}$$

where turns ratio N is given by,

$$N = \frac{N_P}{N_S} \tag{4}$$

From Equation 3 and Equation 4, the primary inductance is given by,

$$L_M = \frac{V_{BULKmin}^2 x\, D_{max}^2 x T_{SW} x\, \eta}{2P_{OUTmax}} \tag{5}$$

Based on turns ratio equal to 6, the secondary SR FET voltage and current rating are calculated using Equation 6 and Equation 7 respectively. With 25% margin, use an SR FET of at least 100V/24A rating.

$$V_{SRFET} = \frac{\sqrt{2}V_{ACmax}}{N} + V_{OUT} \tag{6}$$

$$I_{SEC,PK} = NI_{PRI,PK} \tag{7}$$

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7.2.2.3 Output Capacitor

The output capacitor value is determined based on two specifications: output voltage ripple and output transient voltage response (overshoot/undershoot). The min. capacitor value for a load step from no-load to full load is given by:

$$C_{OUT} = \frac{I_{step} x t_{response}}{\Delta V_{OUT}} \quad (8)$$

Where,

- I_{step} is the largest output current step
- $t_{response}$ is the loop response tiem
- ΔV_{OUT} is the allowable output voltage change

$$t_{response} = \frac{0.33}{f_C} + T_{SW} \quad (9)$$

Where,

- f_C is the approximate loop crossover frequency, set to 5kHz here
- T_{SW} is the switching time period at the initial load condition before the load step

For crossover frequency of 3kHz, 250kHz switching frequency in burst mode, output current step of 3.25A and voltage under/overshoot of 0.5V, the min. required output capacitor value comes to 740µF. With margin for voltage and temperature derating, an 820µF capacitor is used.

7.2.2.4 Selection Resistors

The UCG28826 offers programming options with resistors on IPK, TR, CDX and FCL pins for user to configure the device for their required configuration. Refer to Table 6-1, Table 6-2, Table 6-3 and Table 6-4 for resistor values to set a turns ratio of 6, 3.1A max. peak current, 1.03A min. peak current, CCM enabled, X-cap discharge enabled and 140kHz frequency clamp required for notebook charger application.

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7.2.3 Application Curves

The figures below are measured on the 65W, universal input evaluation module for UCG28826. The waveforms show switching at different valleys for different output powers, frequency foldback and burst mode operation and no-load to full load transients with 20V and 5V output.

Yellow: SW node, Green: Input bulk capacitor voltage, Pink: FB pin voltage

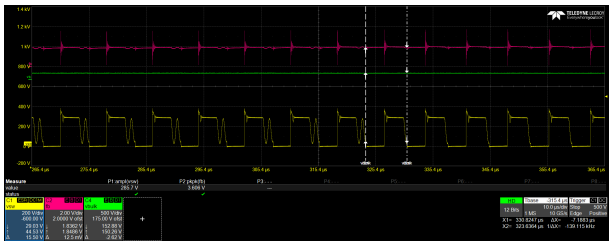


Figure 7-2. 1st Valley and 2nd Valley Operation at 115VAC

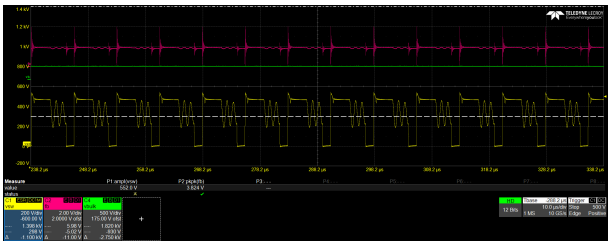


Figure 7-3. 3rd Valley Operation at 230VAC

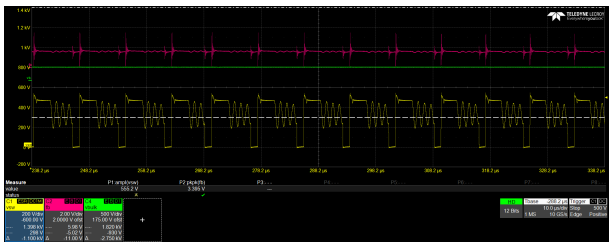


Figure 7-4. 4th Valley Operation at 230VAC

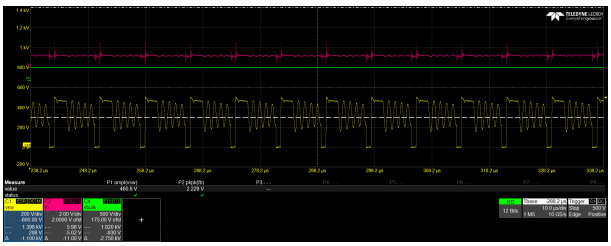


Figure 7-5. 5th Valley Operation at 230VAC

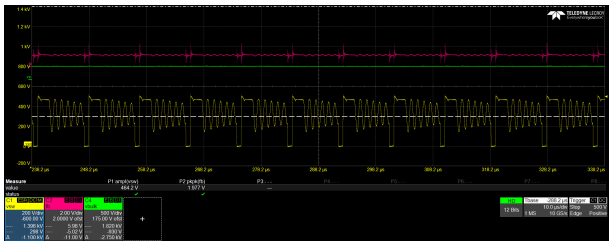


Figure 7-6. 6th Valley Operation at 230VAC

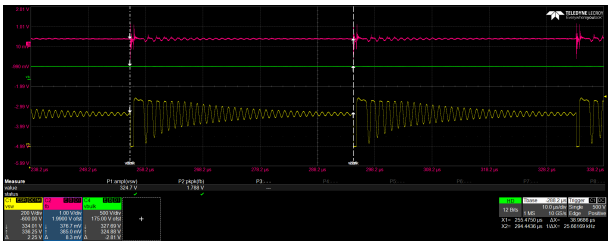


Figure 7-7. Frequency Foldback Mode at 230VAC

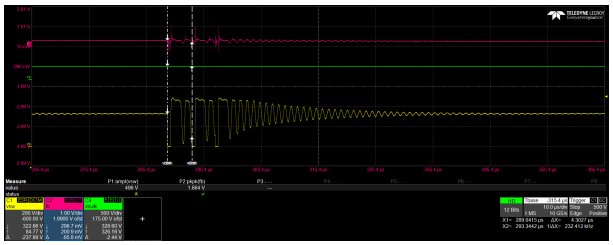
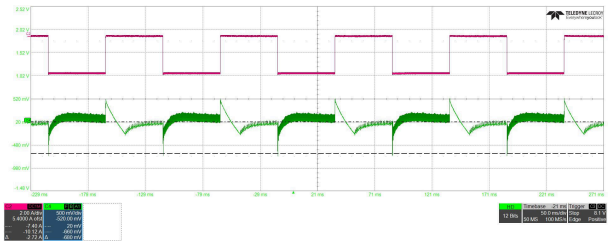


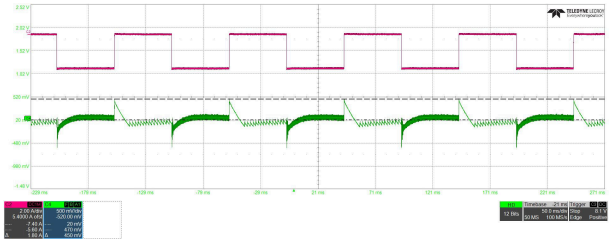
Figure 7-8. Burst Mode at 230VAC



Note

Green: V_{OUT}, Pink: Output current

Figure 7-9. Load transient at 230VAC and 20V output



Note

Green: V_{OUT}, Pink: Output current

Figure 7-10. Load transient at 230VAC and 5V output

7.3 Power Supply Recommendations

The UCG28826 is intended for use in AC/DC adapters with universal AC input in the range from 85VAC to 264VAC, 45Hz to 66Hz, using flyback topology for upto 65W output. While the UCG28826 is useful for USB-PD charger applications, this converter can also be used in other industrial applications with fixed output voltages at 12V, 24V, 36V etc. The TR pin resistor needs to be changed to accommodate such output voltages different from default 20V max. output voltage setting. On the secondary side feedback, output regulation can be achieved with a USB-PD controller or TL431 for fixed output designs.

7.4 Layout

7.4.1 Layout Guidelines

To increase the reliability and feasibility of the design it is recommended to adhere to the following guidelines for PCB layout. These guidelines are general recommendations which can be followed for any power supply design and are generally topology-agnostic. The main theme in power supply layouts is to keep high current loops as small as possible to avoid coupling and any additional losses or false switching due to inaccurate sensing caused by board parasitics.

1. Minimize the high current loops to reduce parasitic capacitances and inductances. For UCG28826, these are the primary side power loop, secondary side power loop and the leakage snubber loop.
2. Separate the device signal ground from the high current ground in order to isolate the switching noise away from the low voltage signals. For UCG28826, the components on pins 4-11 are referenced to GND pins 3 and 10 which then connect to the device thermal pad and GND power plane and follows this recommendation.
3. The bypass capacitor on VCC pin must be placed as close as possible to the VCC and GND pins of the device.

The UCG28826 Evaluation Module User's Guide can be used as a reference when designing the circuit board.

ADVANCE INFORMATION

7.4.2 Layout Example

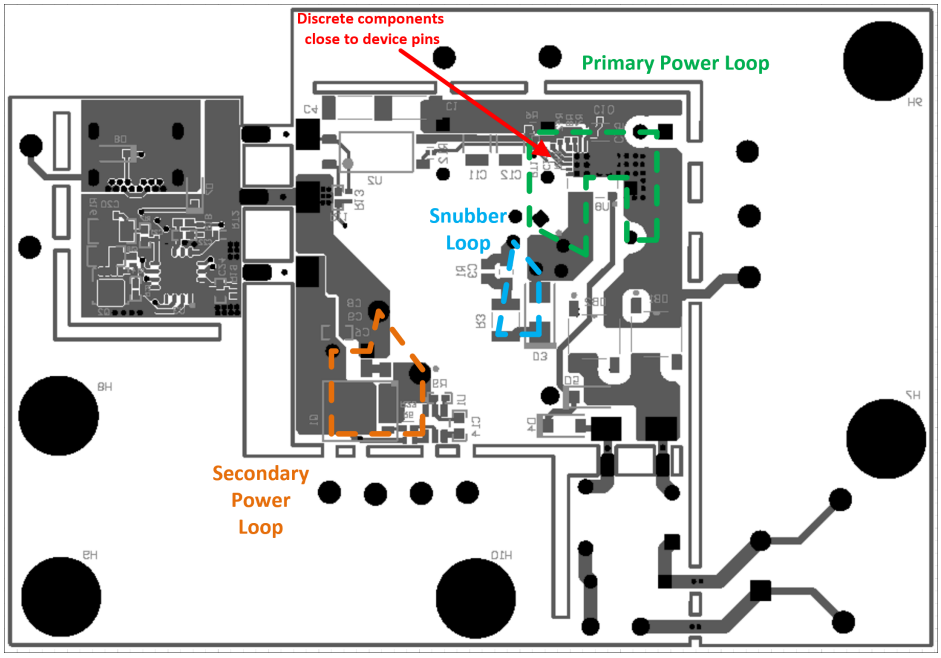


Figure 7-11. Bottom Layer Layout of UCG28826EVM-093 Evaluation Board

ADVANCE INFORMATION

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Support

8.2 Documentation Support

8.2.1 Related Documentation

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2024	*	Advance Information Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

10.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
PUCG28826-1 REZR	PREVIEW	VQFN	REZ	12	TBD	TBD	Call TI	Level-3-260C-168 HR	-40 to 105	TBD

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

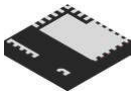
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

10.2 Mechanical Data

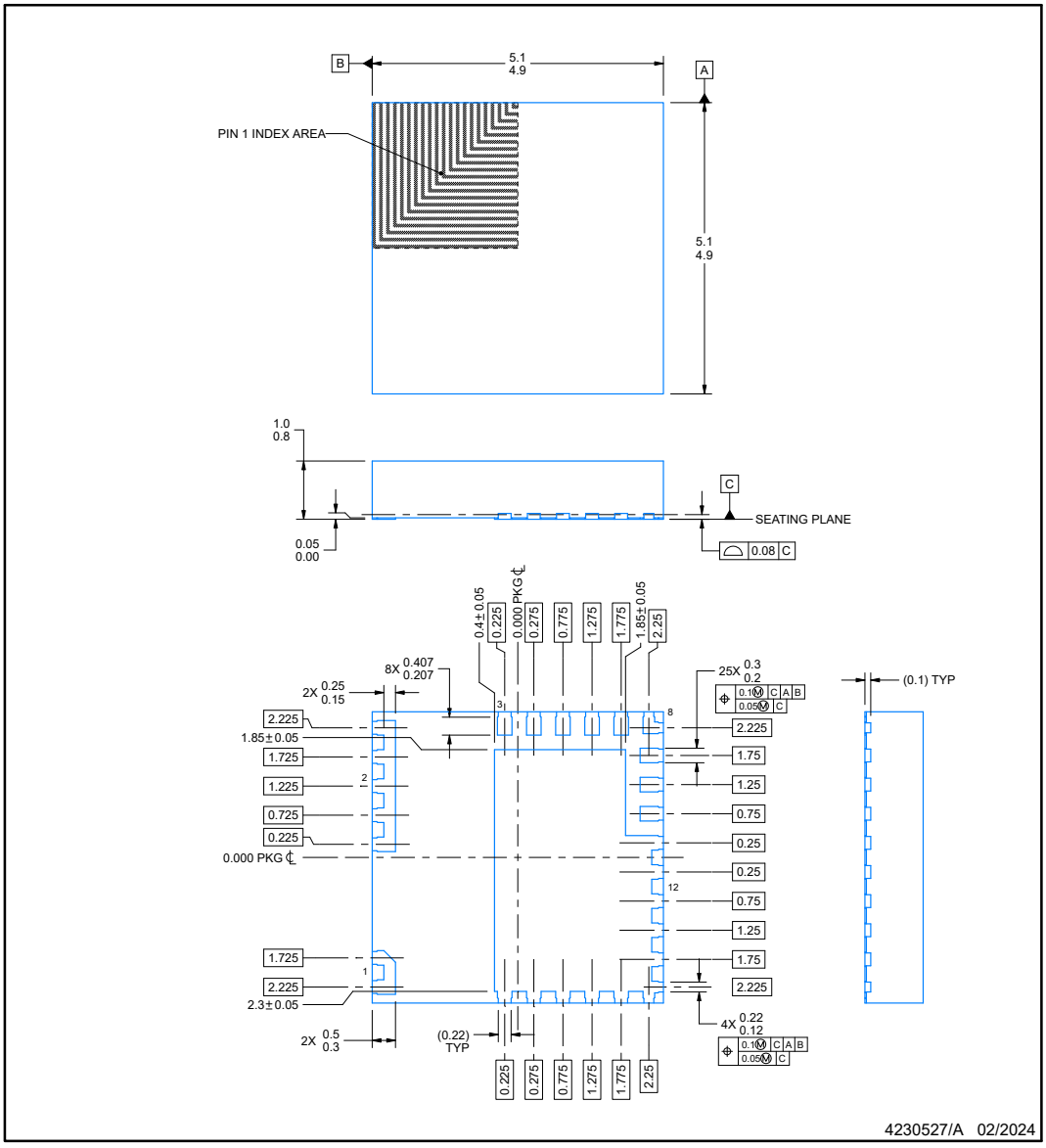
REZ0012A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

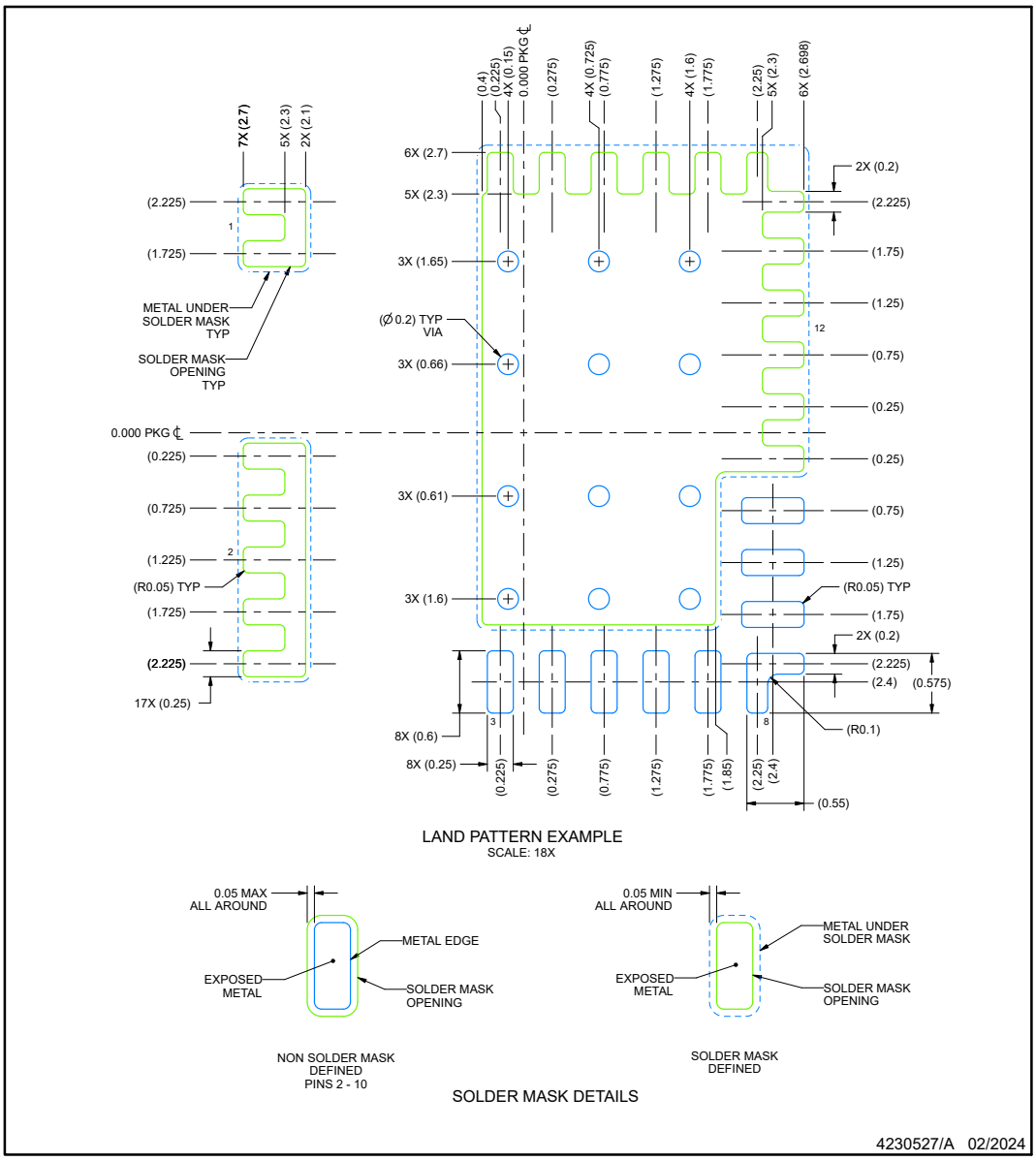
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

REZ0012A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



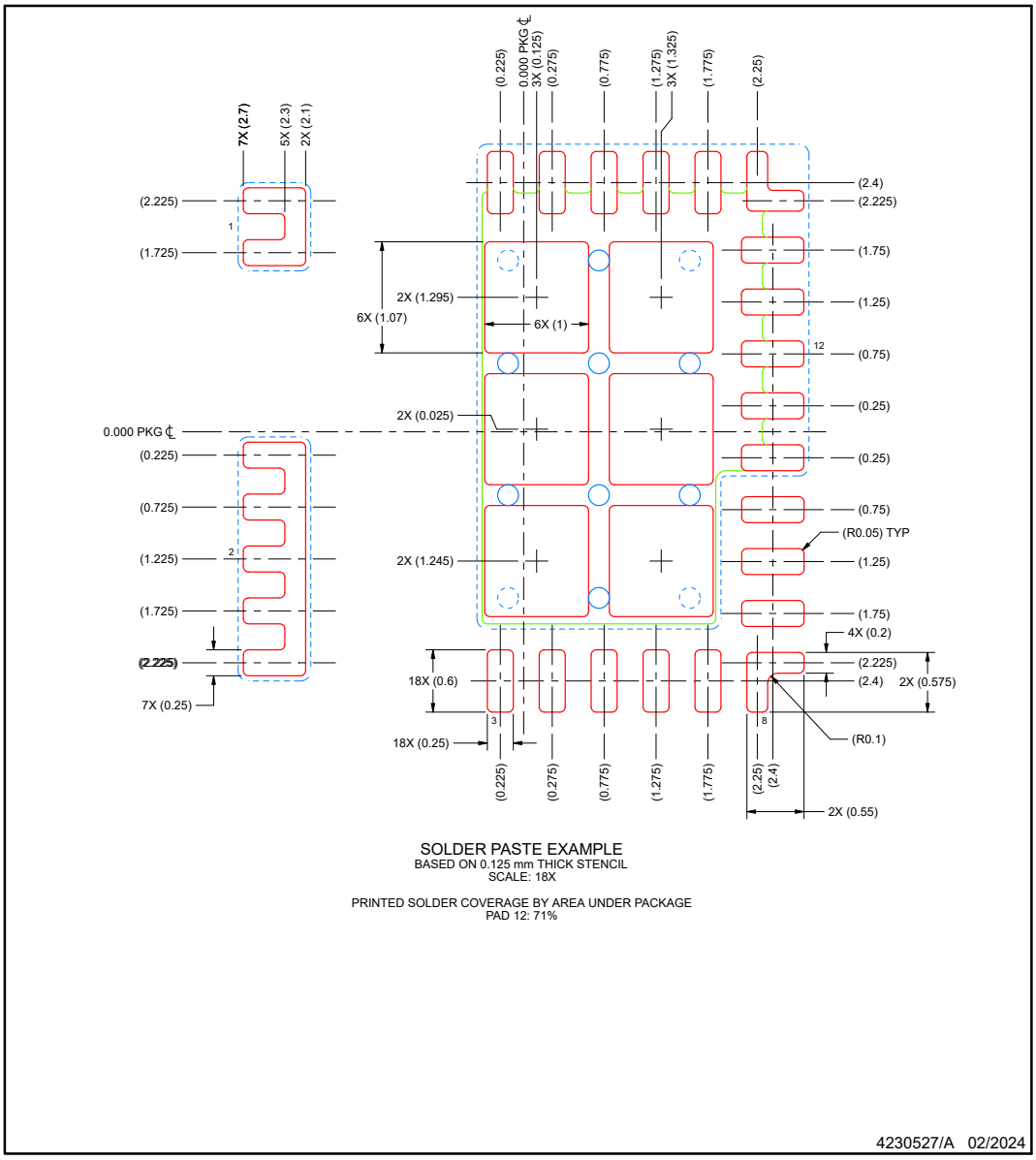
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

REZ0012A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 18X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 12: 71%

4230527/A 02/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PUCG28826-1REZR	ACTIVE	VQFN	REZ	12	100	TBD	Call TI	Call TI	-40 to 105		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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