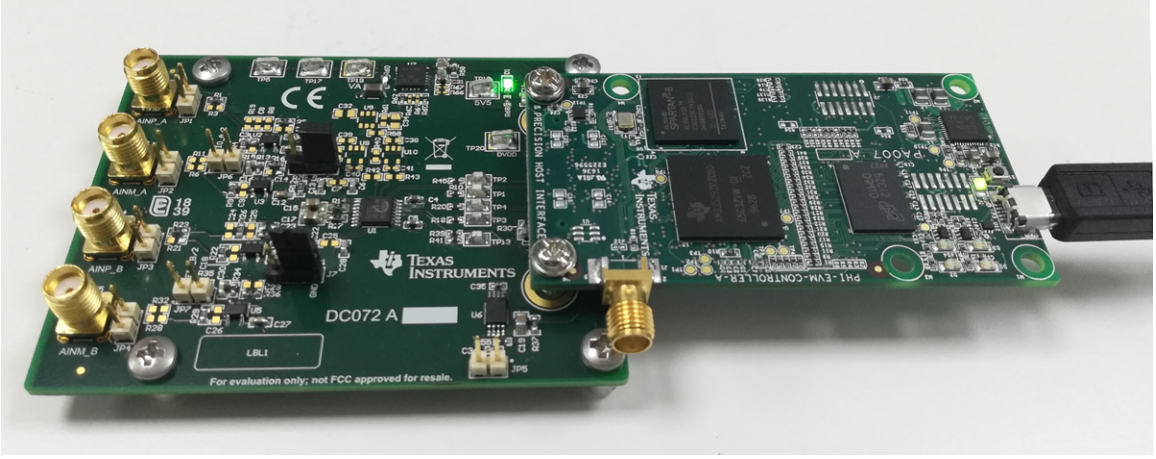
User's Guide
SBAU327–January 2019

ADS8353Q1EVM-PDK Evaluation module

This user's guide describes the characteristics, operation, and use of the ADS8353-Q1 evaluation module (EVM) performance demonstration kit (PDK). This kit is an evaluation platform for the ADS8353-Q1 device, which is a 16-bit, dual-channel, simultaneous-sampling, 600-kSPS, single-ended and pseudo-differential analog input, successive approximation register (SAR) analog-to-digital converter (ADC) that features an easy-to-use serial programming interface (SPI). The ADS8353Q1EVM-PDK eases evaluation with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials (BOM).



The following related documents are available through the Texas Instruments website.

Table 1. Related Documentation

Device	Literature Number
ADS8353-Q1	SBAS931
OPA320-Q1	SLOS884
TPS7A47-Q1	SBVS118
REF34-Q1	SBAS901A

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1 Overview

The ADS8353Q1EVM-PDK evaluation kit includes the ADS8353-Q1EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over the USB for data capture and analysis.

The ADS8353-Q1EVM board includes the ADS8353-Q1 SAR ADC, all the peripheral analog circuits, and the components required to achieve optimum performance from the ADC.

The PHI controller board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS8353-Q1 device
- Supplies power to all active circuitry on the ADS8353-Q1EVM board

Along with the ADS8353-Q1EVM and PHI controller board, this evaluation kit includes an A-to-micro-B USB cable to connect to a computer.

1.1 ADS8353Q1EVM-PDK Features

The ADS8353Q1EVM-PDK showcases the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS8353-Q1 ADC
- USB powered—no external power supply is required
- The PHI controller board provides a convenient communication interface to the ADS8353-Q1 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output
- Easy-to-use evaluation software for Microsoft® Windows® 7, 64-bit operating systems

1.2 ADS8353-Q1EVM Features

The ADS8353-Q1EVM showcases the following features:

- Onboard low-noise, low-distortion ADC input drivers optimized to meet ADC performance
- Onboard ultra-low noise, low-dropout (LDO) regulators, to generate supplies for the operation amplifier and ADC

2 Analog Interface

The ADS8353-Q1 is a low-power, dual-channel, simultaneous-sampling ADC that supports single-ended and pseudo-differential analog inputs. The ADS8353-Q1EVM uses an OPA320-Q1 to drive the analog inputs (AINP and AINM) of the ADC. The ADS8353-Q1EVM is designed for easy interfacing to analog sources. This section describes the front-end driver circuitry details, including jumper configurations for the analog input signal source.

2.1 Connectors for Analog Inputs

The ADS8353-Q1EVM has two 16-bit, simultaneous-sampling ADCs. The ADS8353-Q1EVM GUI can either be configured for individual ADC data sampling or simultaneous sampling with both ADCs. The ADS8353-Q1EVM is designed to interface to an external, analog source through either subminiature version A (SMA) connectors or 100-mil headers. Jumpers J2, J3, J4, and J5 are the SMA connectors that allow for analog signal source connectivity through coaxial cables. Alternatively, 100-mil jumper cables or mini-grabbers can be used to connect analog sources to pin 1 of connectors JP1, JP2, JP3, and JP4. Table 2 lists the analog input connectors for the individual ADCs.

Table 2. Analog Input Connector Description

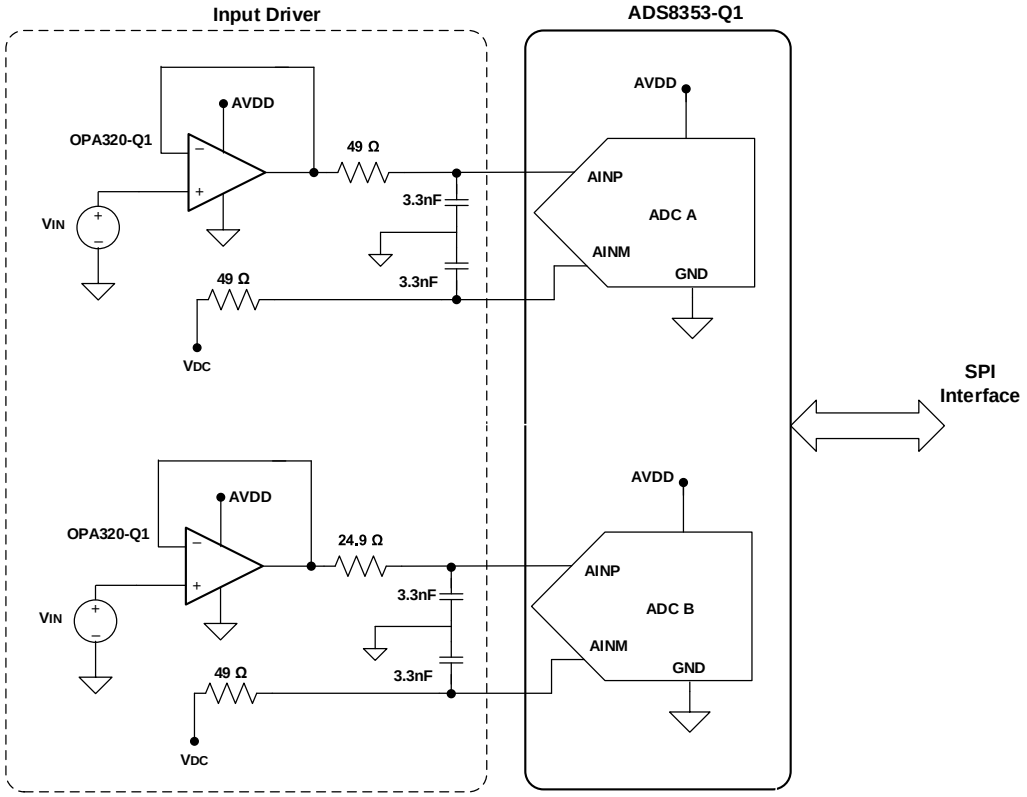
Pin Number	Signal	Description
J2 and J3	INP	Analog inputs provided at the SMA for ADC A
JP1:1 and JP2:1	INP	Alternate location to provide the analog inputs for ADC A
J4 and J5	INP	Analog inputs provided at the SMA for ADC B
JP3:1 and JP4:1	INP	Alternate location to provide the analog inputs for ADC B

2.2 ADC Input Signal Driver

The SAR ADC inputs terminate in switched-capacitor networks that create large instantaneous current loads when the switches are closed, which effectively makes the ADC inputs dynamically low impedance. The analog inputs of the ADC are therefore driven by an OPA320-Q1 used in a unity-gain buffer configuration to maintain ADC performance with maximum loading at full device throughput of the ADS8353-Q1 of 600 kSPS.

2.2.1 Input Signal Path

Figure 1 shows the signal path for the analog inputs applied to the ADS8353-Q1EVM. A separate OPA320-Q1 amplifier is used in a unity-gain buffer configuration to drive the individual analog inputs (AINP and AINM) of each ADC. There is onboard provisioning that enables configuring the OPA320-Q1 driver circuit to drive either single-ended ADC inputs or pseudo-differential ADC inputs. An RC filter with values of 49 Ω and 3.3 nF was selected to achieve a SINAD greater than 83 dB and a THD less than –100 dB for a 2-kHz sine-wave input at full throughput of the ADS8353-Q1 of 600 kSPS.



- **VDC is connected to GND for single ended configuration**
- **VDC is connected to VREF/2 or VREF for pseudo-differential configuration**

Figure 1. ADS8353-Q1EVM Analog Input Path

3 Digital Interfaces

As discussed in Section 1, the ADS8353-Q1EVM interfaces with the PHI, which in turn communicates with the computer over the USB. The three devices on the EVM that the PHI communicates with are the two ADS8353-Q1 ADCs (over the SPI) and the EEPROM (over the I^2C interface). The electrically erasable programmable read-only memory (EEPROM) comes preprogrammed with the information required to configure and initialize the ADS8353Q1EVM-PDK platform. When the hardware is initialized, the EEPROM is no longer used.

3.1 SPI for the ADC Digital I/O

The ADS8353Q1EVM-PDK supports the interface and ADC input modes detailed in the ADS8353-Q1 datasheet. The PHI is capable of operating at a 3.3-V logic level and is directly connected to the digital I/O lines of the ADC.

4 Power Supplies

The ADS8353-Q1 supports a wide range of operation on its analog supplies. The AVDD operates from 4.5 V to 5.5 V. The DVDD operates from 1.65 V to 5.5 V, independent of the AVDD supply. The analog portion of the ADS8353-Q1EVM operates from a 5.3-V supply (VA) generated using the TPS7A47-Q1 low-noise, low-dropout regulator. The same supply is used to power the OPA320-Q1 front-end driver amplifiers.

The TPS7A47-Q1 regulator can be configured to generate a VA supply other than 5.3 V through programmable pin settings. For more information, see the *Detailed Description* section of the TPS7A47-Q1 device datasheet.

The digital portion of the ADC operates from a 3.3-V EVM_DVDD supply from the PHI.

4.1 ADC Input Driver Configuration

The ADS8353-Q1 supports modes where the ADC inputs can be configured as single-ended or pseudo-differential. The ADS8353-Q1 EVM allows the user to configure the ADC input driver amplifier either to drive single-ended ADC inputs or pseudo-differential ADC inputs. In the single-ended configuration, the individual ADC AINM pins are connected to ground and a unipolar signal is applied to AINP. In the pseudo-differential configuration, the individual ADC AINM pins are driven with a DC voltage of either V_{REF} / 2 (0 V to V_{REF} range) or V_{REF} (0 V to 2 × V_{REF} range). For various analog input full-scale ranges supported by the ADS8353-Q1 in either single-ended or pseudo-differential mode, see the ADS8353-Q1 datasheet. Table 3 shows the jumper configurations required for the single-ended and pseudo-differential configurations.

Table 3. Jumper Settings for ADC Input Driver Configuration

ADC Input Type	ADC Input Full-Scale Range	Jumpers	Default Setting	Required Setting
Single-ended analog inputs	0 V to V_{REF} and 0 V to 2 × V_{REF}	J6 and J7	Open (all pins)	Short pins 2 and 3 of J6 and J7 (J6:2 ,J6:3 and J7:2, J7:3)
		JP6 and JP7	Open	Open
Pseudo-differential analog inputs	0 V to V_{REF}	J6 and J7	Open (all pins)	Short pins 1 and 2 of J6 and J7 (J6:1 ,J6:2 and J7:1, J7:2)
		JP6 and JP7	Open	Short pins 1 and 2 of jumpers JP6 and JP7
	0 V to 2 × V_{REF}	J6 and J7	Open (all pins)	Short pins 1 and 2 of J6 and J7 (J6:1 ,J6:2 and J7:1, J7:2)
		JP6 and JP7	Open	Open

4.2 ADC Voltage Reference Configuration

The ADS8353-Q1 has a low-noise, low-drift, 2.5-V internal voltage reference. By default, the ADS8353-Q1 EVM is configured to work with the ADC internal reference voltage of 2.5 V. The same reference voltage is brought on pin 1 of jumpers JP6 and JP7 that can be used to drive the ADC AINM pin when used in pseudo-differential configuration (either in 0 V to V_{REF} or 0 V to 2 × V_{REF} analog input range).

There is also a provision for using an external voltage reference for the ADC. The external reference voltage can be generated by populating the REF34-Q1 (U8) and biasing components around U8. By default, the external reference and biasing circuit around U8 is not populated on the board. When using an external reference, the ADS8353-Q1 internal voltage reference must be disabled and the device must be programmed to accept the external reference voltage on its REFIO_x pins.

5 ADS8353Q1EVM-PDK Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for proper operation of the ADS8353Q1EVM-PDK.

5.1 Default Jumper Settings

Figure 2 shows the silkscreen plot, which details the jumper locations for the ADS8353Q1EVM-PDK.

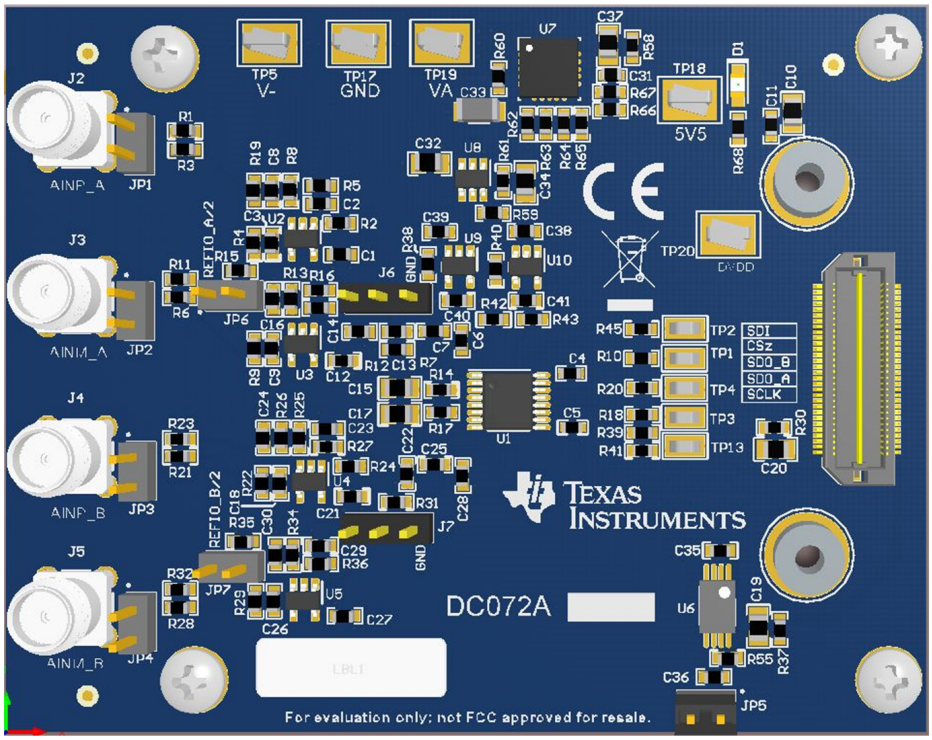


Figure 2. ADS8353Q1EVM-PDK Jumper Locations

Table 4 lists the functionality and default configuration of each jumper.

Table 4. Default Jumper Configurations

Reference Designator	Default Configuration	Description
JP1, JP2, JP3, JP4	Open	Use pin 1 of these jumpers as an alternate location to provide the analog input to ADC A and ADC B of the ADS8353-Q1.
JP5	Open	Connect this jumper to disable EEPROM write protection.
JP6, JP7	Open	Jumpers to feed either V_{REF} or V_{REF} / 2 to the OPA320-Q1 input driving the AINM pin of the ADC. See Section 7.3 for more details.
J6, J7	Open	Jumpers to configure the ADC inputs as single-ended or pseudo-differential. See Section 7.3 for more details.

5.2 EVM Graphical User Interface Software Installation

The following steps describe how to install the software for the ADS8353-Q1 EVM graphical user interface (GUI).

1. Download the latest version of the EVM GUI installer from the *Software* section of the ADS8353Q1EVM-PDK Tool Folder, and run the GUI installer to install the EVM GUI software on your computer.

> **CAUTION**
>
> Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Failure to disable antivirus software, depending on the antivirus settings, may cause an error message to appear or the *installer.exe* file may be deleted.

2. Accept the license agreements (Figure 3) and follow the on-screen instructions to complete the installation.

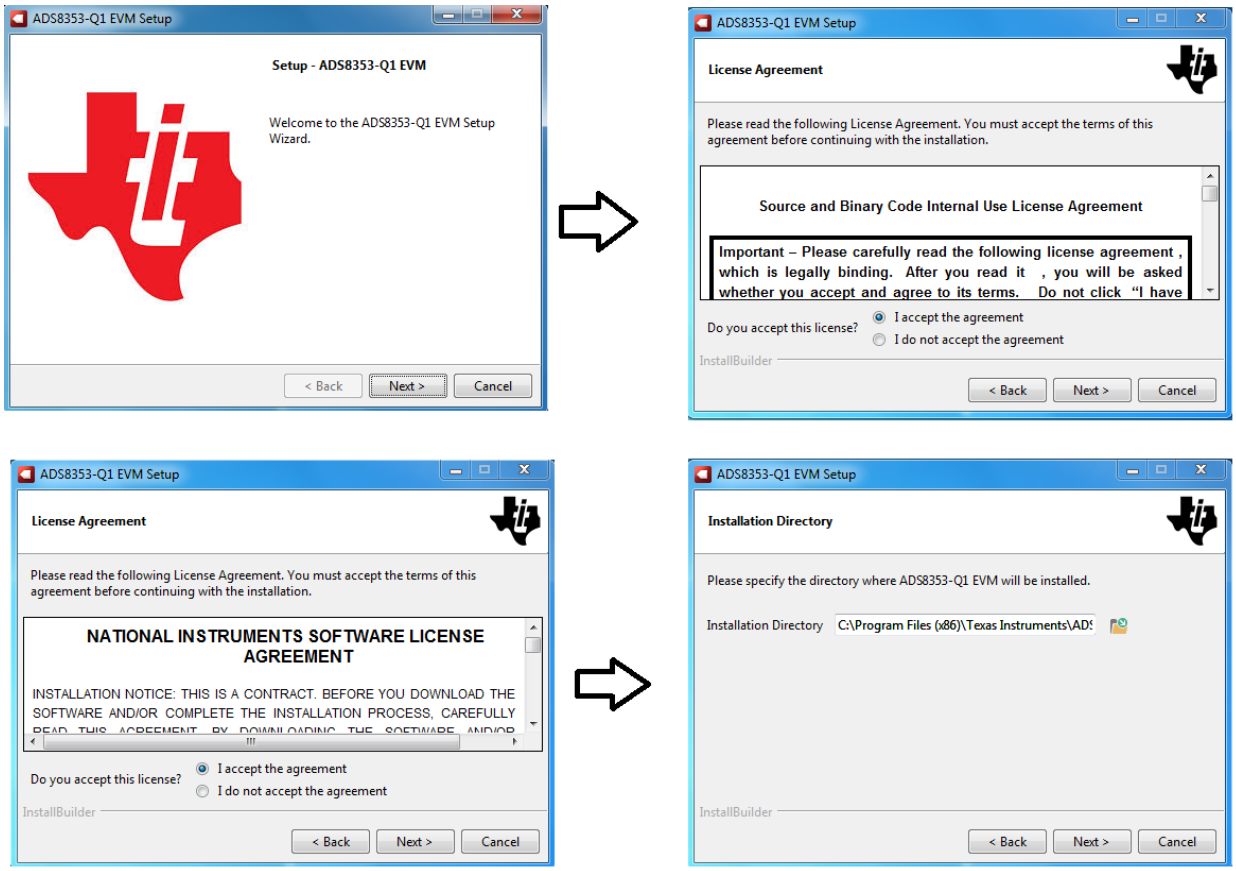


Figure 3. ADS8353-Q1EVM Software Installation Prompts

3. As a part of the ADS8353-Q1EVM GUI installation, a prompt with a Device Driver Installation Wizard (Figure 4) appears on the screen. Click the *Next* button to proceed, then click the *Finish* button when the installation is complete.

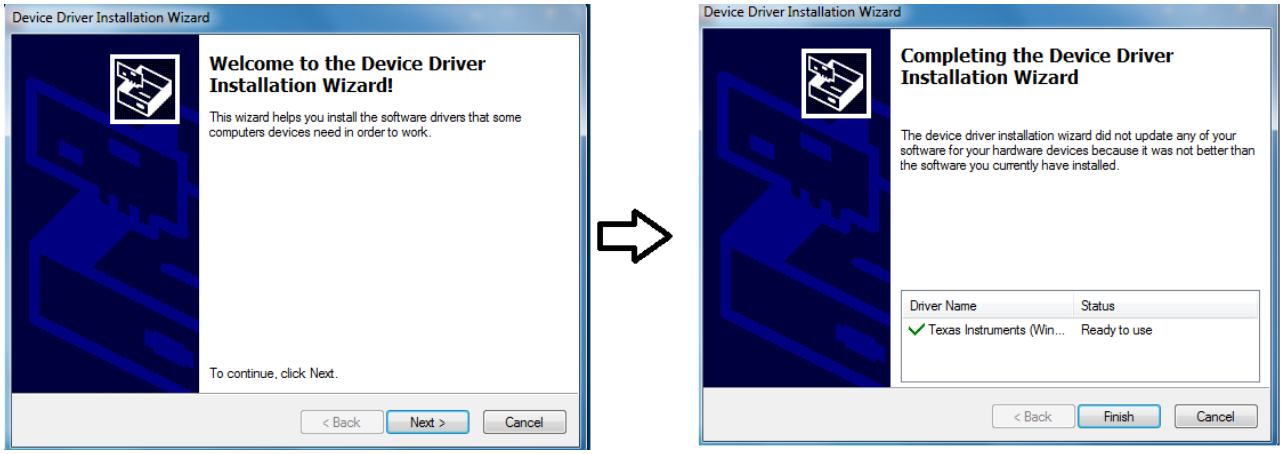


Figure 4. Device Driver Installation Wizard Prompts

NOTE: A notice may appear on the screen stating that Windows cannot verify the publisher of this driver software. Select the *Install this driver software anyway* option.

The device requires the LabVIEW™ Run-Time Engine (see Figure 5) and may prompt for the installation of this software, if not already installed.

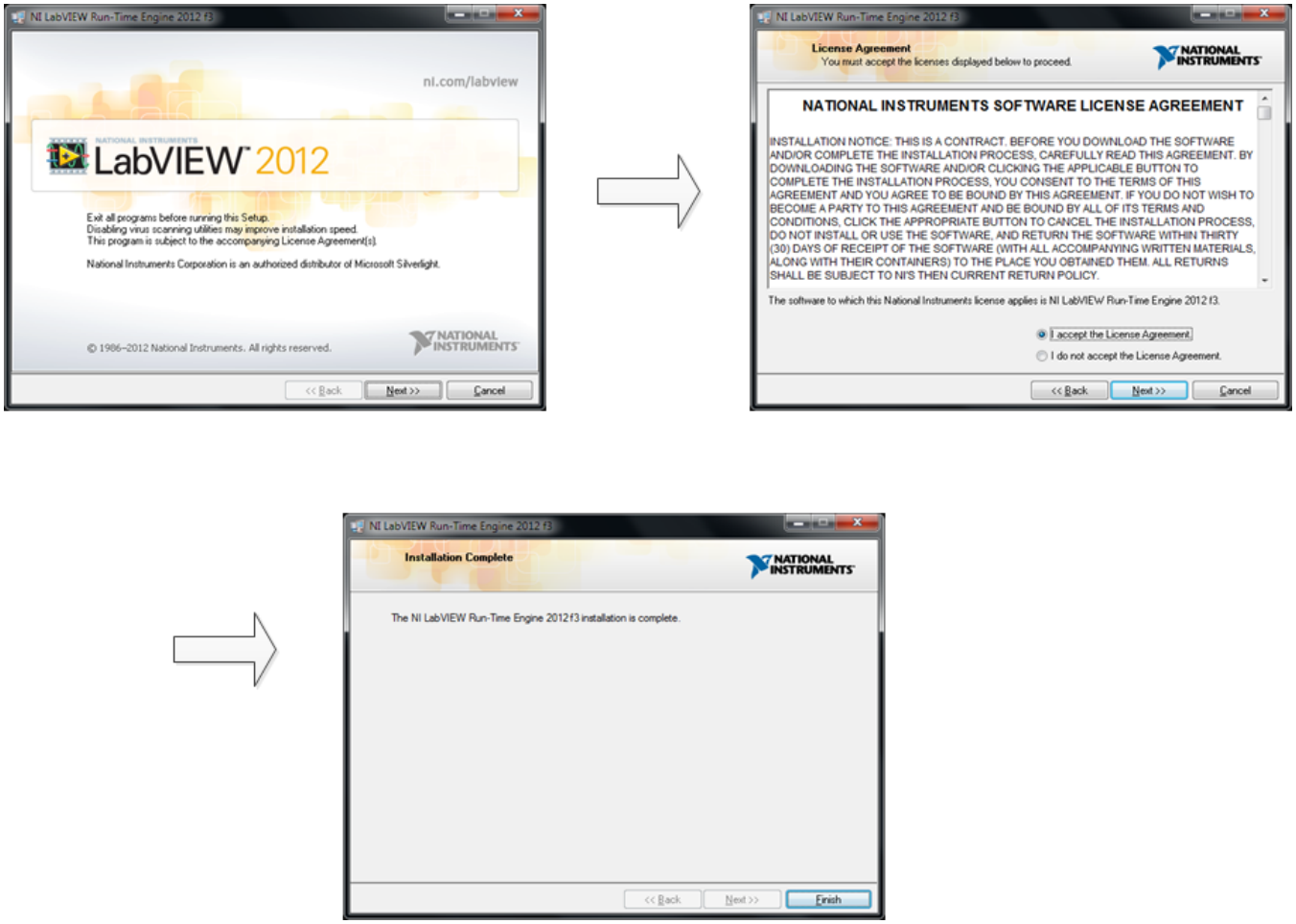


Figure 5. LabVIEW Run-Time Engine Installation

4. Check the *Create Desktop Shortcut* box, as Figure 6 shows, after these installations.

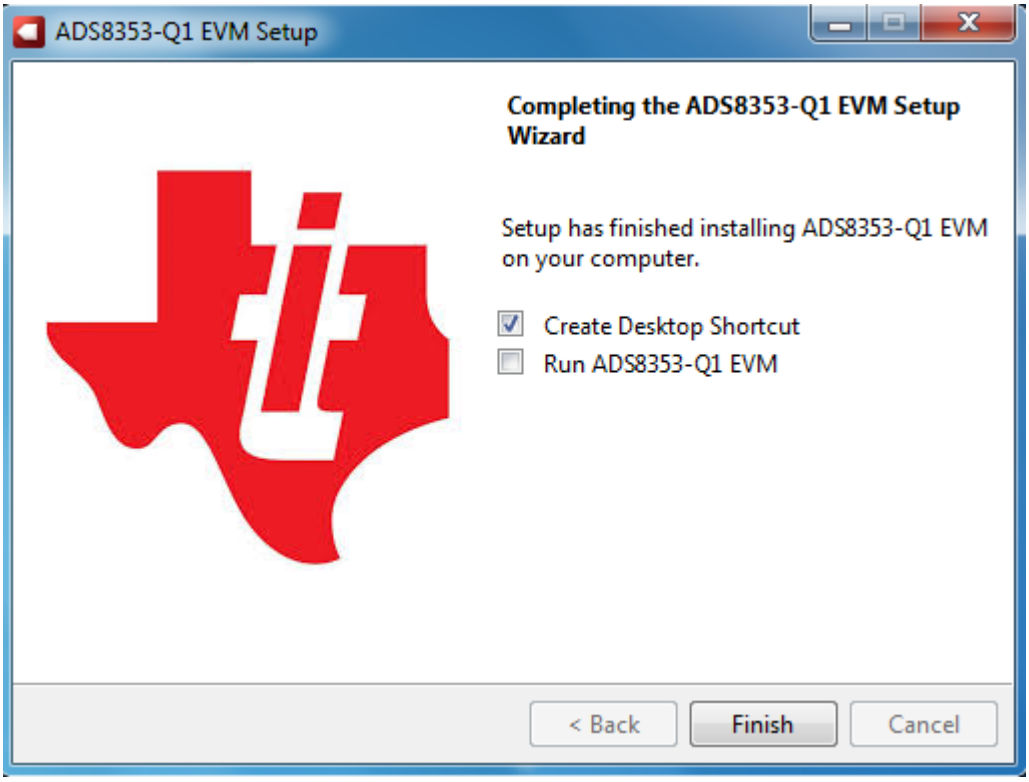


Figure 6. ADS8353Q1EVM-PDK Installation Final Step

6 ADS8353Q1EVM-PDK Operation

The following instructions are a step-by-step guide for connecting the device to a computer and evaluating the performance of the device.

1. Connect the device EVM to the PHI board. Figure 7 indicates where to two screws are to be installed.
2. Use the provided USB cable to connect the PHI to the computer.
   - LED D5 on the PHI lights up, indicating that the PHI is powered up.
   - LEDs D1 and D2 on the PHI start flashing, indicating that the PHI is booted up and communicating with the PC.

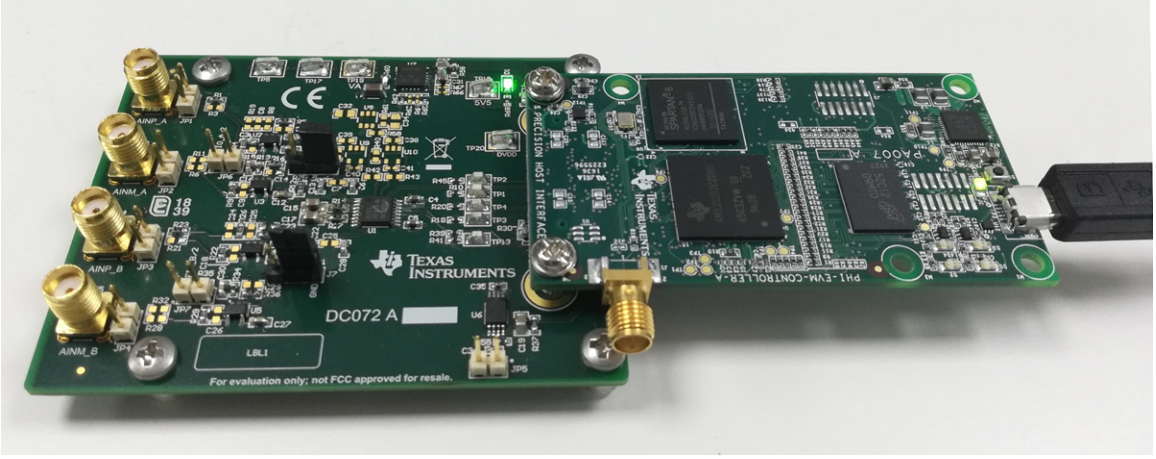


Figure 7. EVM-PDK Hardware Setup and LED Indicators

3. Launch the device EVM GUI software from the installed path, as Figure 8 shows, or by using the desktop shortcut created during installation.

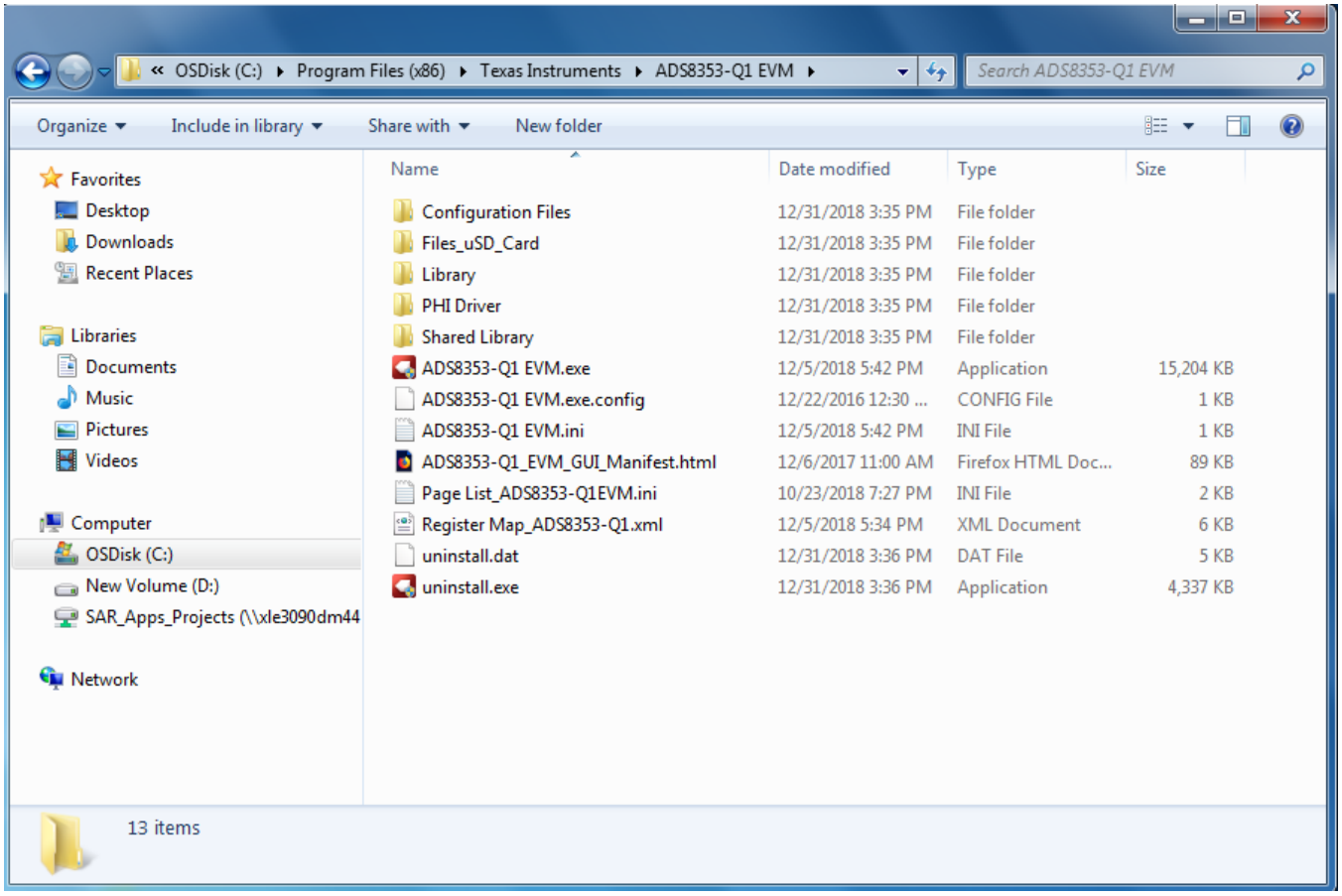


Figure 8. Launch the EVM GUI Software

6.1 EVM GUI Global Settings for ADC Control

Figure 9 shows the input parameters of the GUI (as well as their default values), through which the various functions of the ADS8353Q1EVM-PDK can be exercised. These settings are global and persist across the GUI tools listed in the top left pane (or from one page to another).

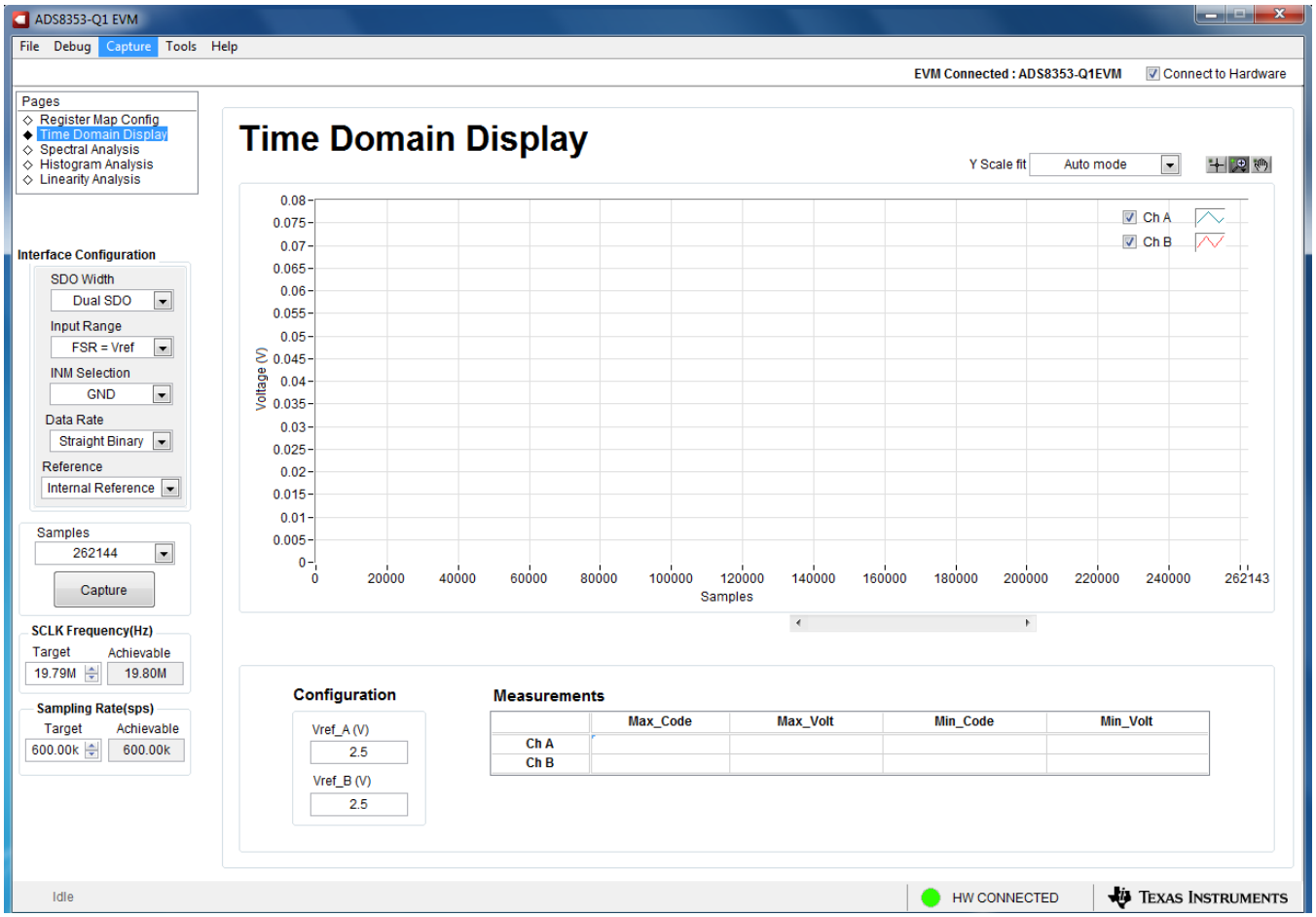


Figure 9. EVM GUI Global Input Parameters

The ADS8353-Q1 interface configurations can be selected on this page. The GUI lets the user select the ADC input range, ADC input configuration (single-ended or pseudo-differential), ADC voltage reference, and ADC data format using a drop-down menu.

The *SCLK Frequency* and *Sampling Rate* are selected on this page. The GUI lets the user enter the target values for these two parameters, and the GUI computes the closest value that can be achieved, considering the timing constraints of the device.

Select either one of the ADCs or both of the ADCs if they are configured in the simultaneous sampling scheme described in Section 2.1 by clicking on the drop-down menu titled *Channel Modes*. Specify a target SCLK frequency (Hz) and the GUI tries to match this frequency as closely as possible by changing the PHI PLL settings; however, the achievable frequency may differ from the target value entered. Similarly, the sampling rate of the ADC can be adjusted by modifying the *Target Sampling Rate* argument (Hz). The achievable ADC sampling rate can differ from the target value, depending on the applied SCLK frequency and the closest match achievable is displayed. This page, therefore, allows various settings available on the device to be tested in a repetitive fashion until arriving at the best settings for the corresponding test scenario.

6.2 Time Domain Display Tool

The *Time Domain Display* tool provides a visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or front-end drive circuits.

As per the selected interface mode settings using the *Capture* button indicated in Figure 10, the user can trigger a data capture of the selected number of samples from the ADS8353Q1EVM-PDK. The sample indices are on the x-axis, and two y-axes show the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the analysis tools described in the subsequent sections triggers calculations to be performed on the same set of data.

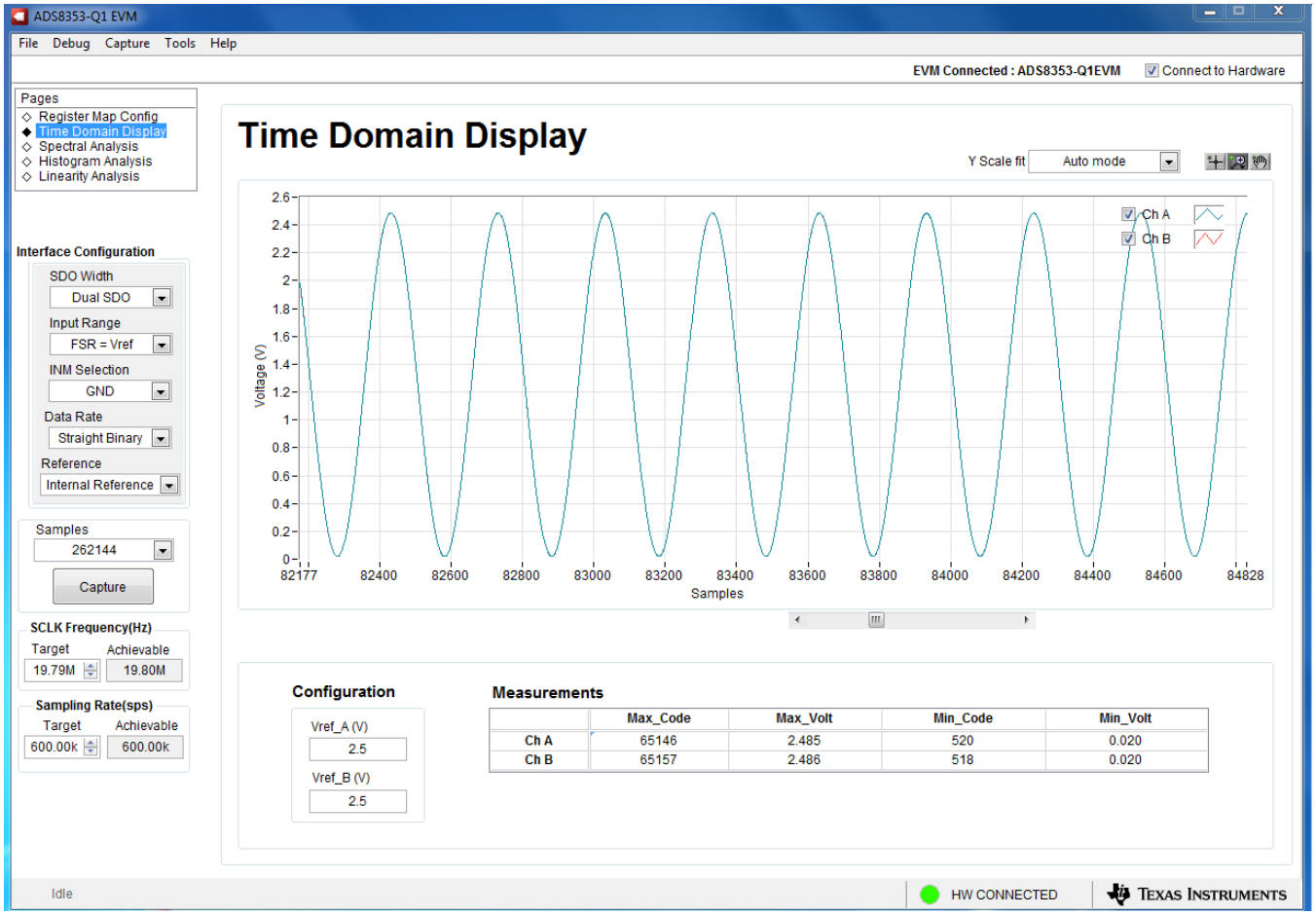


Figure 10. Time Domain Display Tool Options

6.3 Spectral Analysis Tool

The *Spectral Analysis* tool (Figure 11) is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS8353-Q1 SAR ADC through the use of a single-tone, sinusoidal signal FFT analysis, using the 7-term Blackman-Harris window setting. Alternatively, the window setting of *None* can be used to search for noise spurs over frequency in DC inputs.

For dynamic performance evaluation, the external, single-ended source must have better specifications than the ADC to ensure that the measured system performance is not limited by the performance of the signal source. Therefore, the external reference source must meet the source requirements listed in Table 5. Alternately, the user can use the Precision Signal Injector EVM that provides a low-distortion, low-noise, 2-kHz input signal for driving the input of the ADC, and pairs with most of the TI SAR ADC evaluation modules (EVMs). The board is powered over a USB, which also provides a user-interface connection to a PC.

Table 5. External Source Requirements for Device Evaluation (SNR and THD)

Specification Description	Specification Value
Signal frequency	2 kHz
External source type	Single-ended
External source common-mode	1.65 V
Minimum SNR	90 dB
Minimum THD	–115 dB

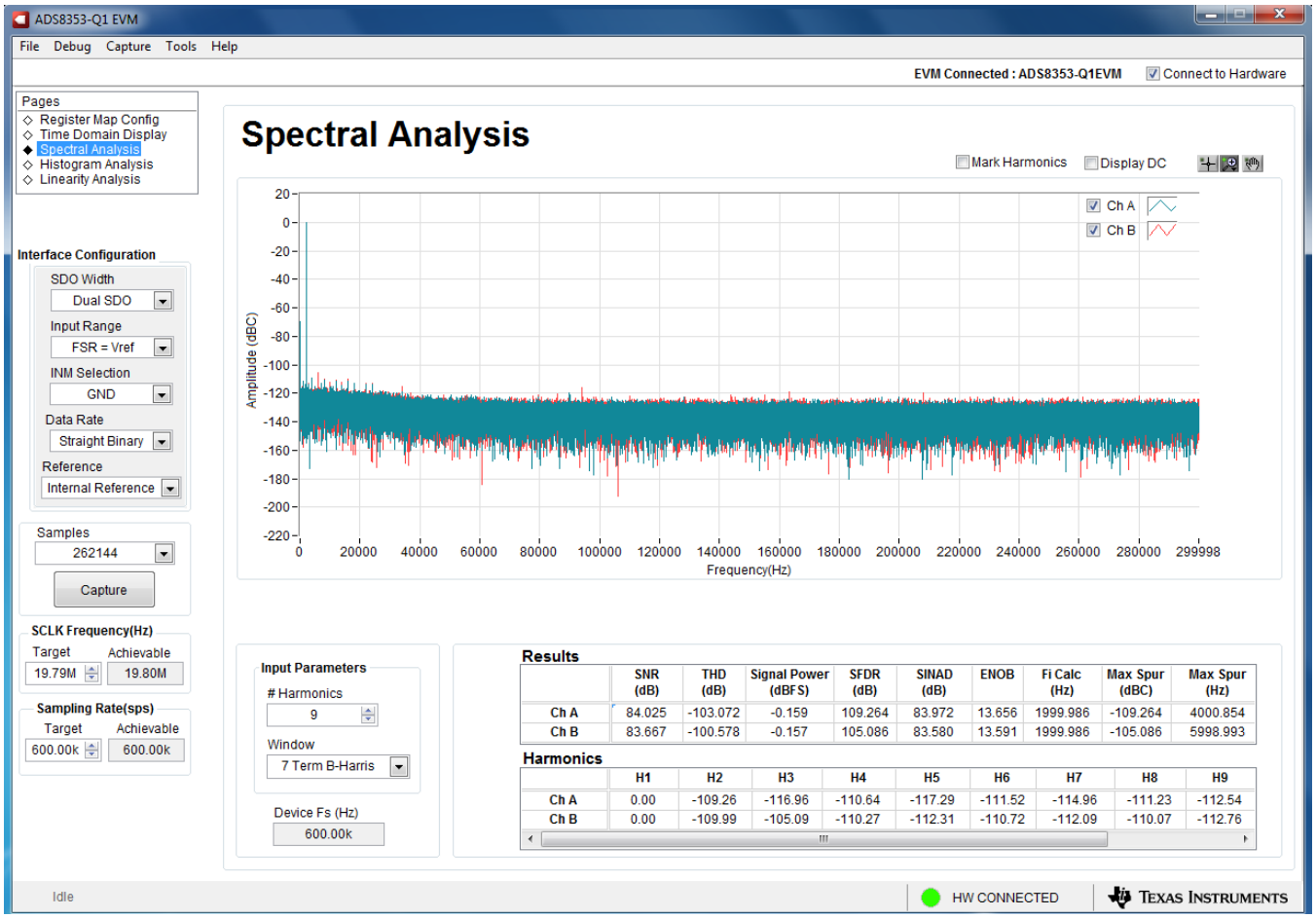


Figure 11. Spectral Analysis Tool

6.4 Histogram Analysis Tool

The *Histogram Analysis* tool can be used to estimate the effective resolution of the ADC resulting from performance degradation caused by noise. Effective resolution is an indicator of the number of bits of ADC measurement resolution resulting from performance losses caused by noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output (from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself) is reflected in the standard deviation of the ADC output code histogram obtained by performing multiple conversions of a DC input applied to a given channel.

The histogram corresponding to a DC input is displayed by clicking the *Capture* button. The example capture shown in Figure 12 is captured with the ADC configured in single-ended, 0 V to 2 × V_{REF} mode and with the AINP pin driven with the V_{REF} input voltage.

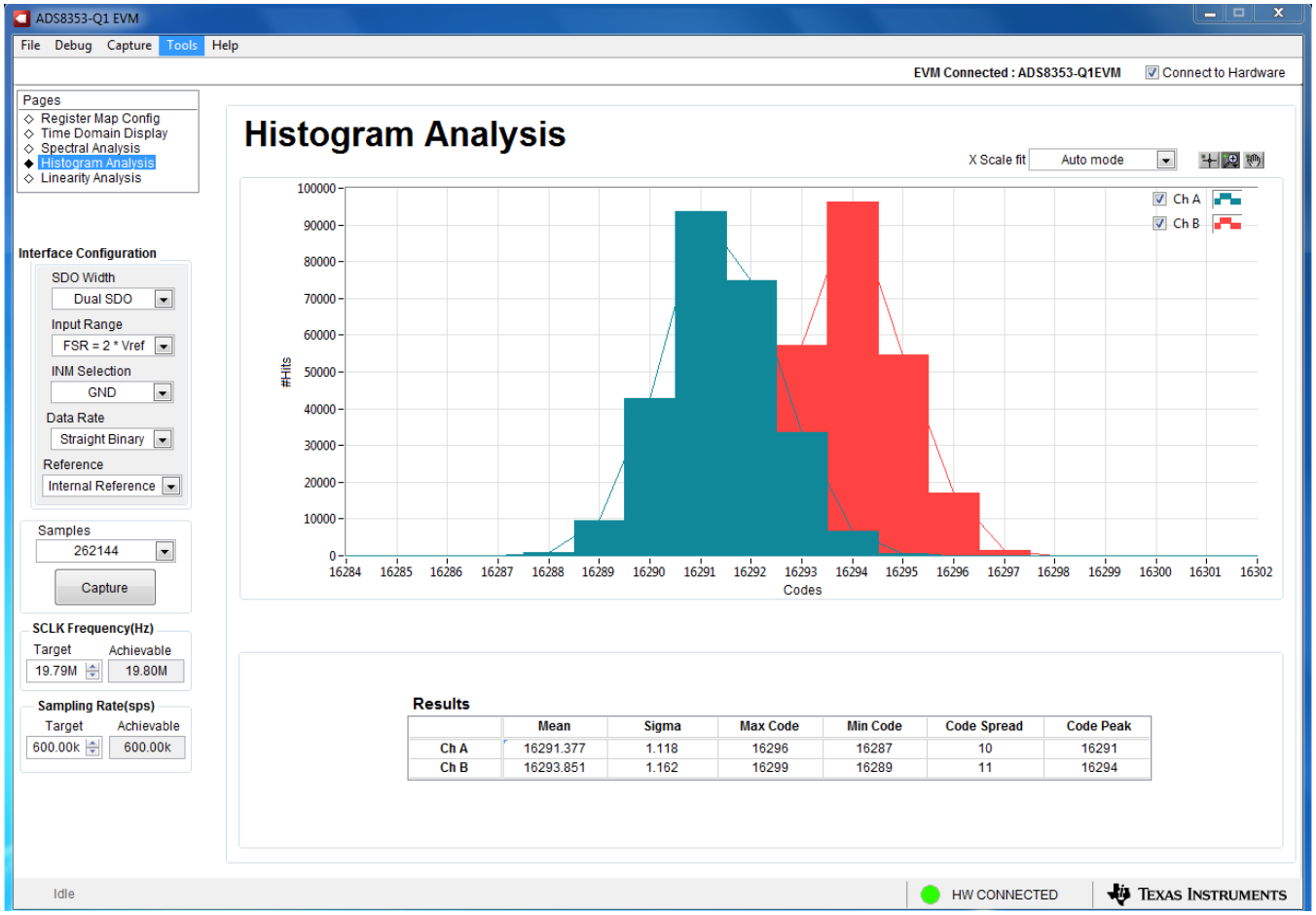


Figure 12. Histogram Analysis Tool

7 Bill of Materials, Printed-Circuit Board Layout, and Schematics

This section contains the ADS8353-Q1EVM bill of materials (BOM), printed-circuit board (PCB) layout, and schematics.

7.1 Bill of Materials

Table 6 lists the ADS8353-Q1EVM BOM.

Table 6. ADS8353-Q1EVM Bill of Materials

Manufacturer Part Number	Quantity	Reference Designators	Manufacturer	Description
DC072	1	PCB	Any	Printed Circuit Board
0603ZC103KAT2A	4	C1, C12, C21, C27	AVX	CAP, CERM, 0.01 uF, 10 V, +/- 10%, X7R, 0603
1891	4	@H1, @H2, @H3, @H4	Keystone	Hex Standoff, #4-40, Aluminum, 1/4"
RM3X4MM 2701	2	@H5, @H6	APM HEXSEAL	Machine Screw Pan PHILLIPS M3
GRM188R71E105KA12D	3	C4, C5, C31	Murata	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603
GRM1885C1H332JA01D	4	C6, C13, C22, C28	Murata	CAP, CERM, 3300 pF, 50 V, +/- 5%, C0G/NP0, 0603
GRM188R71C104KA01D	10	C8, C16, C24, C30, C35, C36, C38, C39, C40, C41	Murata	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0603
GRM21BR71A106KE51L	6	C10, C15, C17, C19, C20, C37	Murata	CAP, CERM, 10 uF, 10 V, +/- 10%, X7R, 0805
GRM1885C1H102FA01J	1	C11	Murata	CAP, CERM, 1000 pF, 50 V, +/- 1%, C0G/NP0, 0603
C3216X5R1E476M160AC	1	C33	TDK	CAP, CERM, 47 uF, 25 V, +/- 20%, X5R, 1206_190
APT2012LZGCK	1	D1	Kingbright	LED, Green, SMD
GRM155R71E104KE14D	2	C19, C38	Murata	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0402
GRM155R61A104KA01D	1	C23	Murata	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X5R, 0402
PMSSS 440 0025 PH	4	H1, H2, H3, H4	B&F Fastener Supply	MACHINE SCREW PAN PHILLIPS 4-40
9774050360R	2	H5, H6	Wurth Elektronik	ROUND STANDOFF M3 STEEL 5MM
5-1814832-1	4	J2, J3, J4, J5	TE Connectivity	SMA Straight PCB Socket Die Cast, 50 Ohm, TH
PBC03SAAN	2	J6, J7	Sullins Connector Solutions	Header, 100mil, 3x1, Gold, TH
QTH-030-01-L-D-A	1	J4	Samtec	Header(Shrouded), 19.7mil, 30x2, Gold, SMT
HTSW-102-07-G-S	7	JP1, JP2, JP3, JP4, JP5, JP6, JP7	Samtec	Header, 100mil, 2x1, Gold, TH
RMCF0603ZT0R00	8	R1, R5, R14, R16, R17, R23, R27, R36	Stackpole Electronics Inc	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
ERJ-3EKF49R9V	4	R2, R7, R24, R31	Panasonic	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
ERJ-3GEY0R00V	10	R10, R18, R20, R37, R39, R41, R45, R58, R62, R65	Panasonic	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603
RT0603BRD071KL	4	R4, R9, R22, R29	Yageo America	RES, 1.00 k, 0.1%, 0.1 W, 0603
RT0603BRD07100KL	2	R12, R26	Yageo America	RES, 100 k, 0.1%, 0.1 W, 0603
RMCF0603FT10K0	6	R13, R15, R34, R35, R55, R68	Stackpole Electronics Inc	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
CRCW06035R11FKEA	1	R30	Vishay-Dale	RES, 5.11, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
ERJ-3RSFR10V	1	R60	Panasonic	RES, 0.1, 1%, 0.1 W, 0603
881545-2	1	SH-J1	TE Connectivity	Shunt, 100mil, Gold plated, Black
5015	1	TP1, TP2, TP3, TP4, TP13	Keystone	Test Point, Miniature, SMT
5016	1	TP5, TP17, TP18, TP19, TP20	Keystone	Test Point, Compact, SMT
ADS8353QPWRQ1	1	U1	Texas Instruments	SAR ADC, Dual, 600 kSPS, 16 Bit, Simultaneous Sampling ADC
OPA320AQDBVRQ1	3	U2, U3, U4	Texas Instruments	Automotive Qualified Precision, Zero-Crossover, 20MHz, 0.9pA Ib, RRIO, CMOS Operational Amplifier, DBV0005A (SOT-23-5)
BR24G32FVT-3AGE2	1	U6	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8

Table 6. ADS8353-Q1EVM Bill of Materials (continued)

Manufacturer Part Number	Quantity	Reference Designators	Manufacturer	Description
TPS7A4701QRGWTQ1	1	U7	Texas Instruments	Automotive 35V, 1A, 4.2μVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)
0603ZC103KAT2A	0	C2, C14, C23, C29	AVX	CAP, CERM, 0.01 uF, 10 V, +/- 10%, X7R, 0603
06035A101FAT2A	0	C3, C9, C18, C26	AVX	CAP, CERM, 100 pF, 50 V, +/- 1%, C0G/NP0, 0603
GRM1885C1H332JA01D	0	C7, C25	Murata	CAP, CERM, 3300 pF, 50 V, +/- 5%, C0G/NP0, 0603
0805ZC105KAT2A	0	C32	AVX	CAP, CERM, 1 uF, 10 V, +/- 10%, X7R, 0805
GRM21BR71A106KE51L	0	C34	Murata	CAP, CERM, 10 uF, 10 V, +/- 10%, X7R, 0805
102-1092-BL-00100	0	H5	CnC Tech	Cable, USB-A to micro USB-B, 1 m
RT0603BRD071KL	0	R3, R6, R21, R28	Yageo America	RES, 1.00 k, 0.1%, 0.1 W, 0603
RC0603FR-07100RL	0	R8, R25	Yageo America	RES, 100, 1%, 0.1 W, 0603
RMCF0603ZT0R00	0	R11, R32, R38, R40, R42, R43	Stackpole Electronics Inc	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
RT0603BRD07100KL	0	R19	Yageo America	RES, 100 k, 0.1%, 0.1 W, 0603
CRCW06031K00FKEA	0	R59	Vishay-Dale	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
ERJ-3RQFR22V	0	R61	Panasonic	RES, 0.22, 1%, 0.1 W, 0603
ERJ-3GEY0R00V	0	R63, R64, R66, R67	Panasonic	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603
OPA320AQDBVRQ1	0	U5, U9, U10	Texas Instruments	Automotive Qualified Precision, Zero-Crossover, 20MHz, 0.9pA Ib, RRIO, CMOS Operational Amplifier, DBV0005A (SOT-23-5)
REF3425IDBVR	0	U8	Texas Instruments	2.5V Low-Drift Low-Power Small-Footprint Series Voltage Reference, DBV0006A (SOT-23-6)

7.2 PCB Layout

Figure 13 through Figure 16 show the EVM PCB layout.

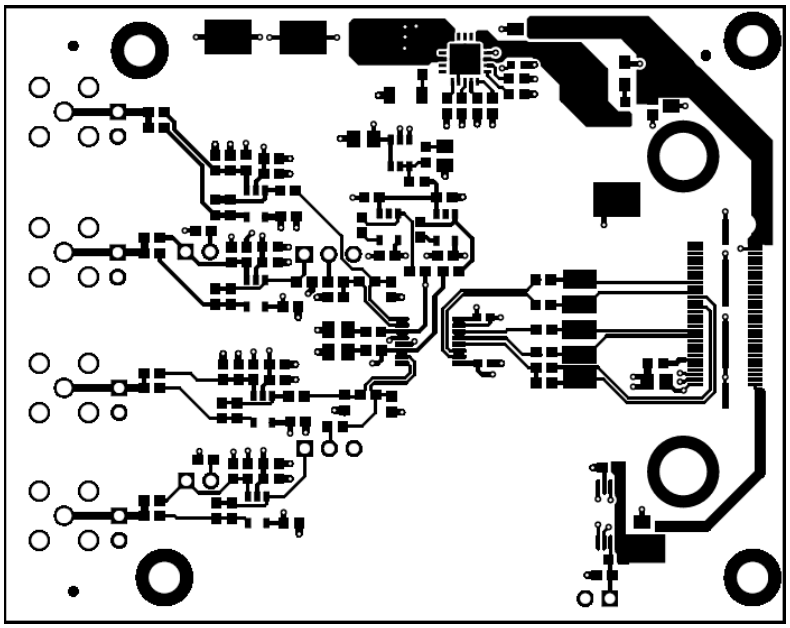


Figure 13. ADS8353-Q1EVM PCB Layer 1: Top Layer

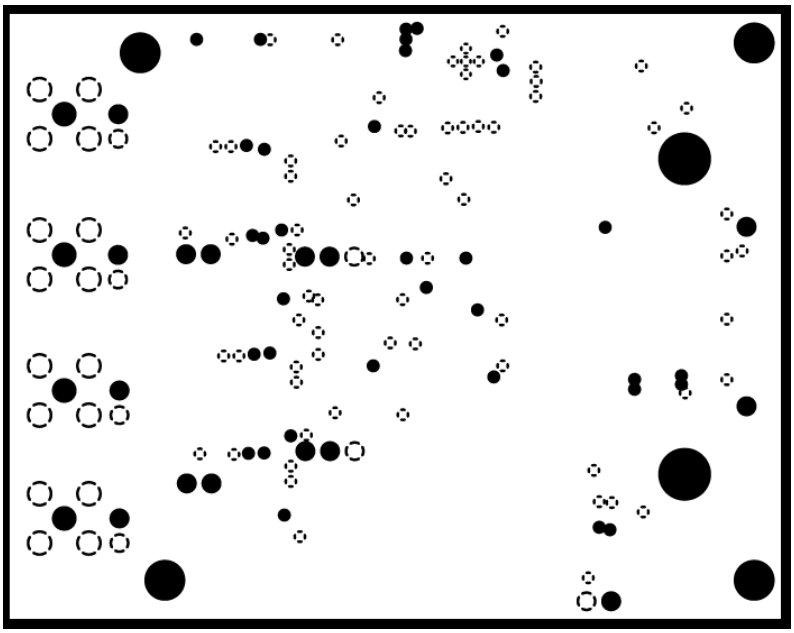


Figure 14. ADS8353-Q1EVM PCB Layer 2: GND Plane

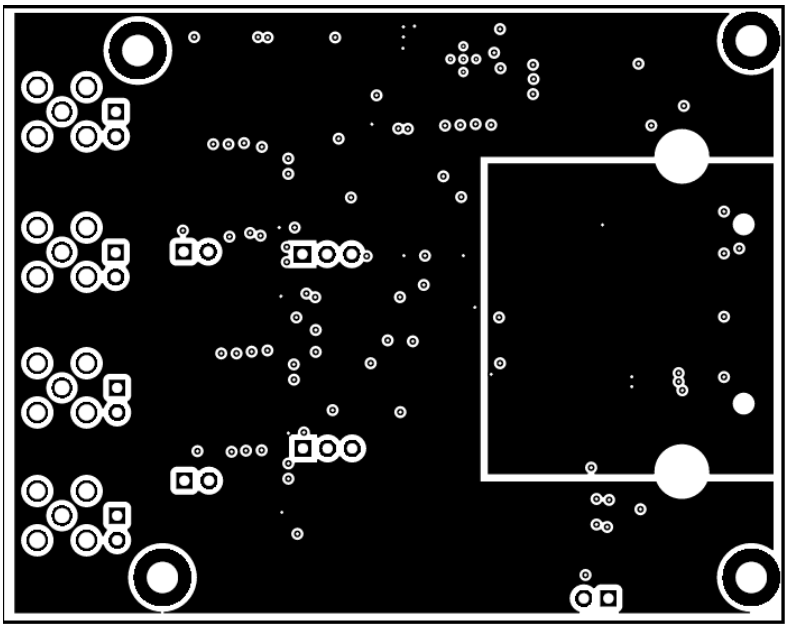


Figure 15. ADS8353-Q1EVM PCB Layer 3: Power Planes

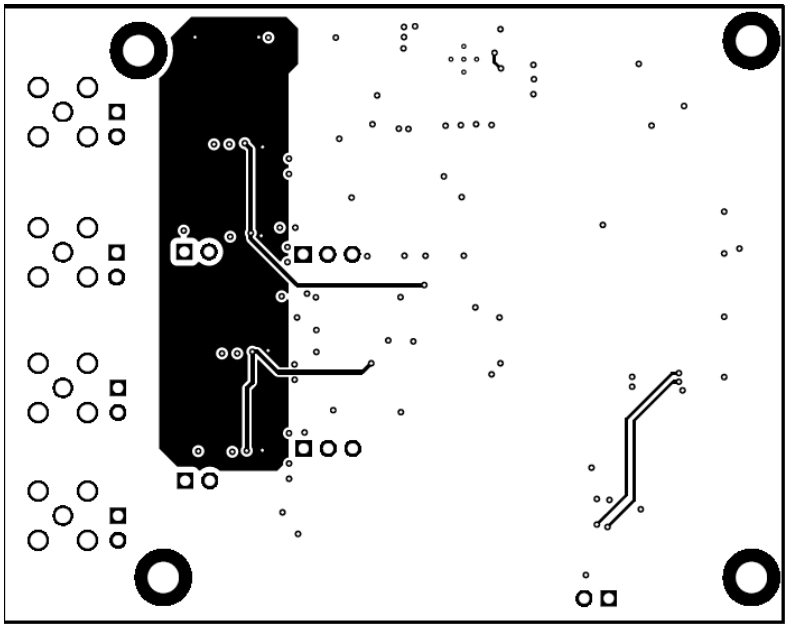


Figure 16. ADS8353-Q1EVM PCB Layer 4: Bottom Layer

7.3 Schematics

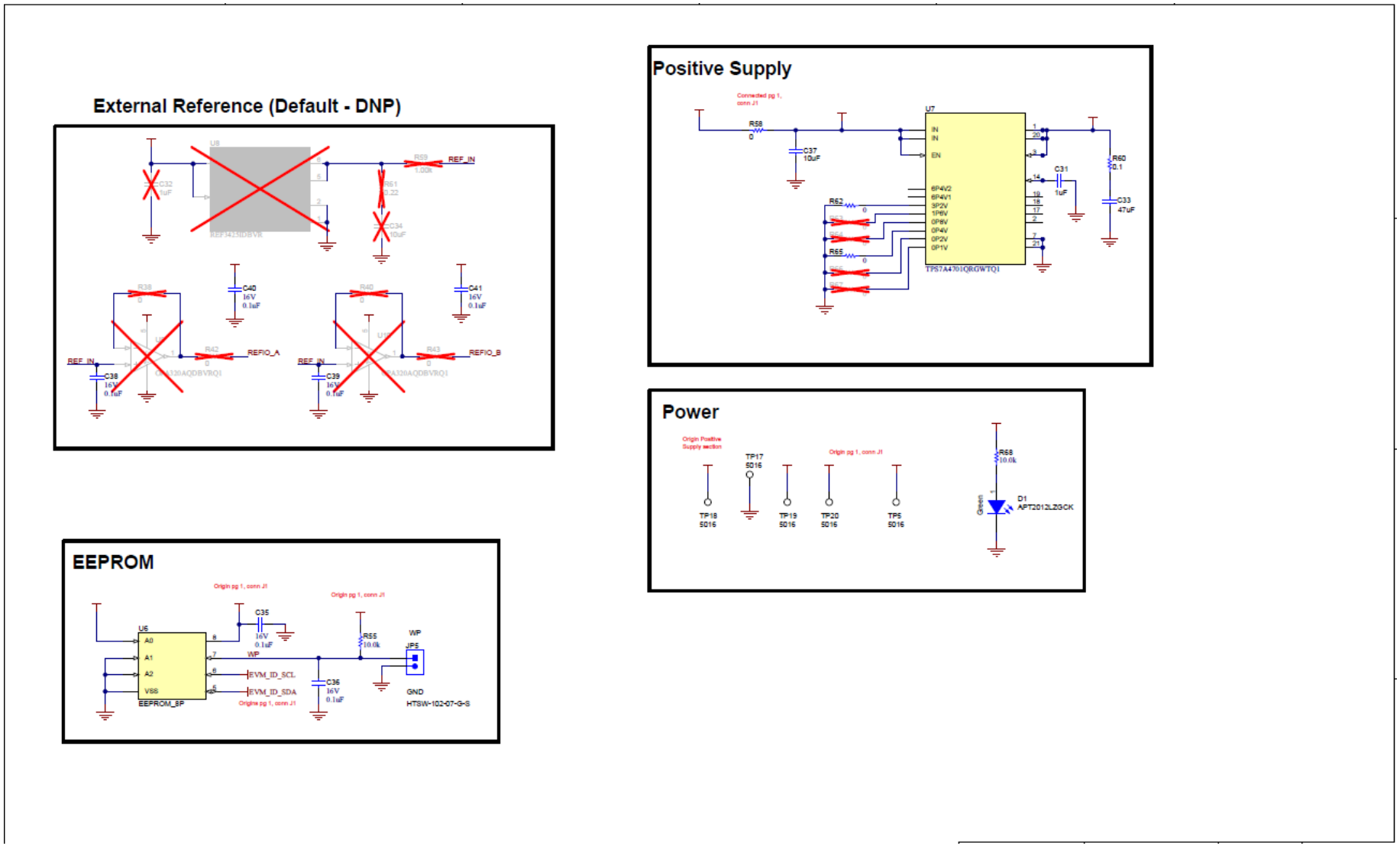


Figure 17. Schematic Diagram (Page 1) of the ADS8353-Q1EVM PCB

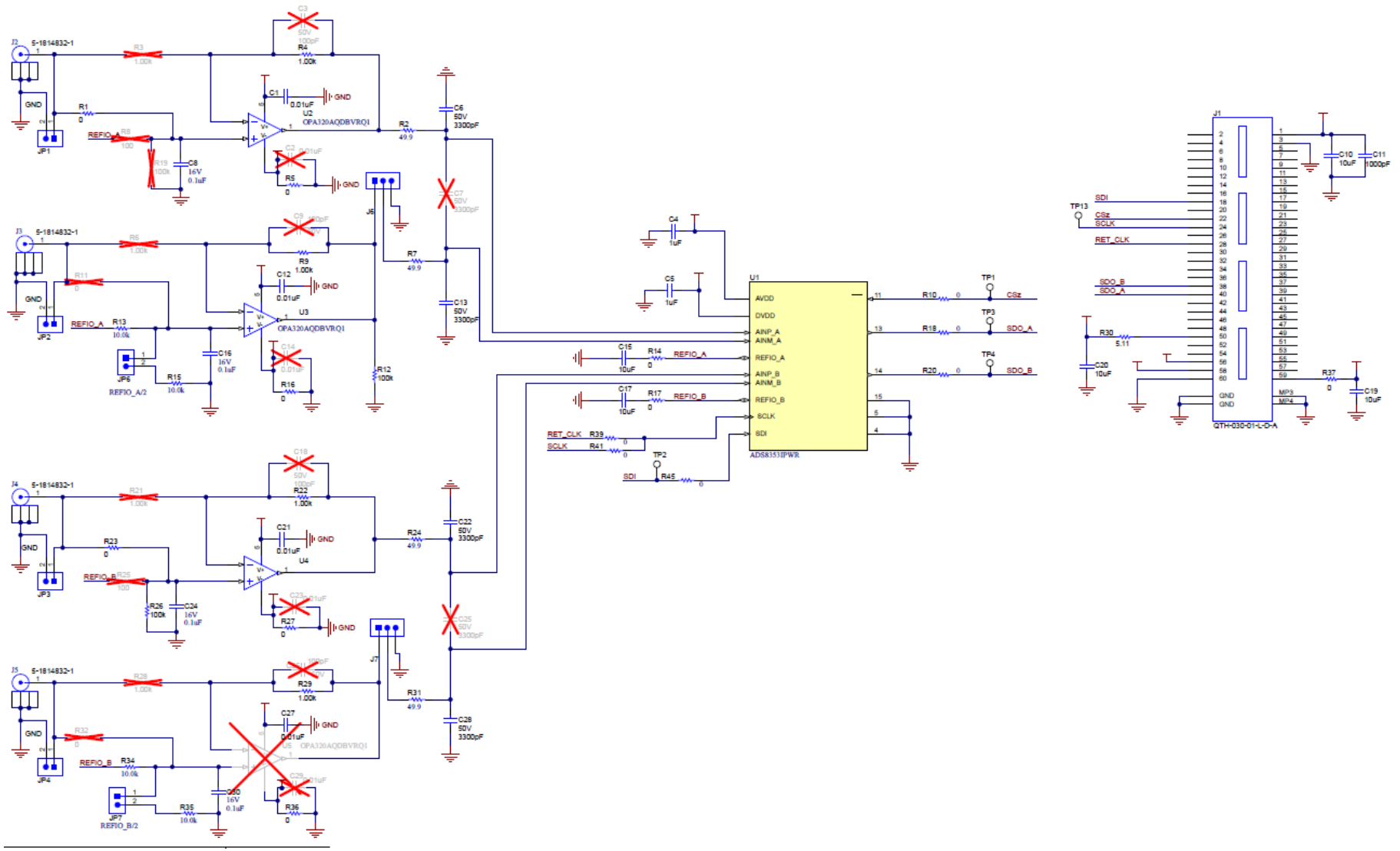


Figure 18. Schematic Diagram (Page 2) of the ADS8353-Q1EVM PCB

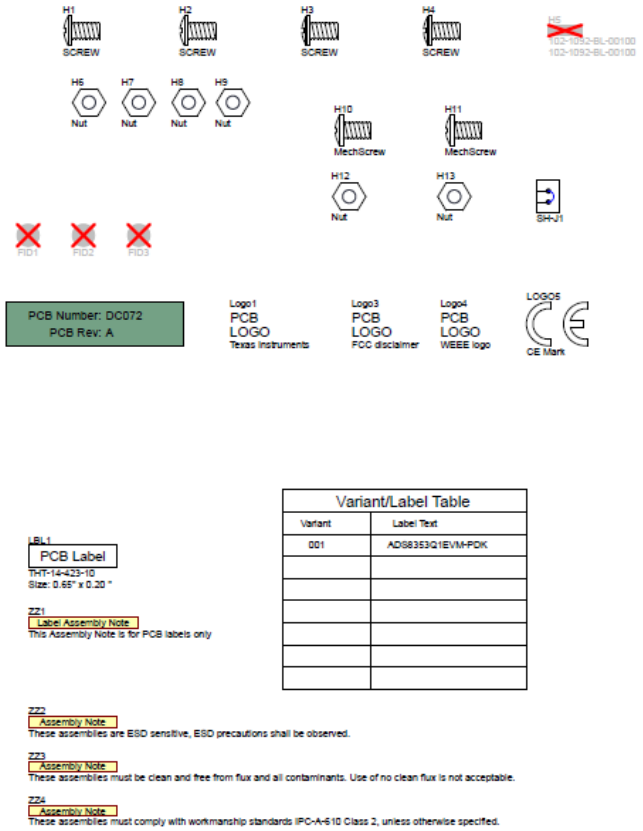


Figure 19. Schematic Diagram (Page 3) of the ADS8353-Q1EVM PCB

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