



## ABSTRACT

The AFE79-LMH9-EVM evaluation module (EVM) is evaluation board for evaluating the performance of the AFE79xx family of integrated RF Sampling transceivers interfaced with the LMH9xxx family of active BALUNs, both from Texas Instruments. The AFE79xx devices support up to four-transmit, four-receive, and two feedback channels (4T4R2F) and integrates phase-locked loop (PLL) and voltage-controlled oscillator (VCO) for generating data-converter clocks. The AFE79xx device integrates eight JESD204B-, JESD204C-compatible serializer/deserializer (SerDes) transceivers capable of running up to 29.5 Gbps to transmit and receive digital data through the onboard FPGA mezzanine card (FMC) connector. LMH9xxx devices are band-specific gain block amplifiers with BALUNs integrated that either drive the ADC of receive paths (LMH92xx) or are driven by the DAC of the transmit path (LMH91xx). The EVM includes the LMK04828 clock generator to provide reference clocks and SYSREF to the analog front end (AFE) and capture card (field-programmable gate array, FPGA). The evaluation module (EVM) works off a single 5.5-V input and includes complete power management circuitry. External clocking options include support for feeding the reference clock (for the on-chip PLL). The design interfaces with the TI pattern and capture card solution (TSW14J56, TSW14J57), as well as many FPGA development kits.

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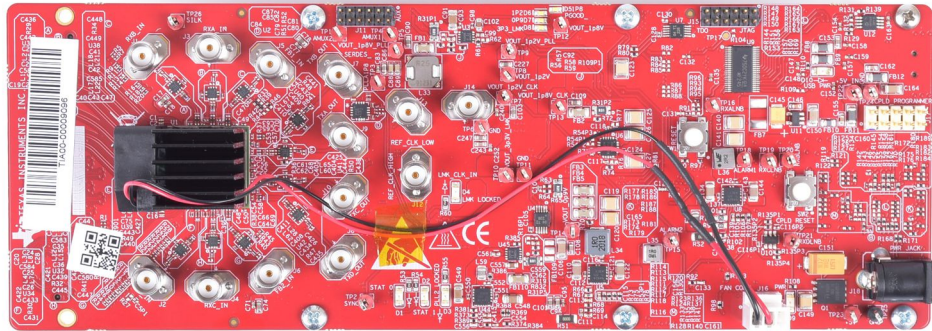
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## 1 EVM Overview

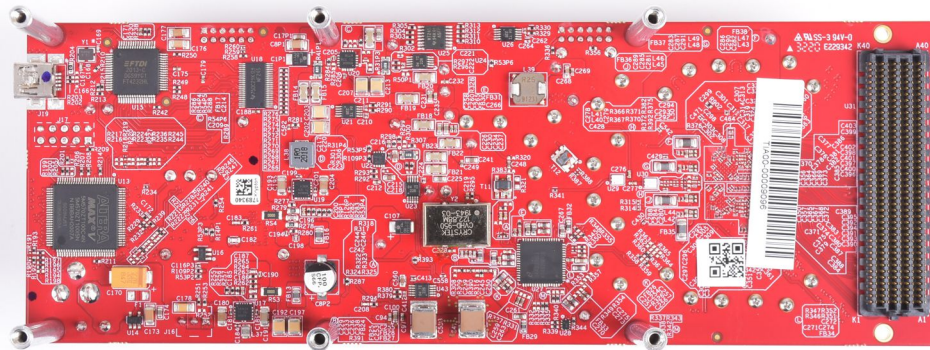
The AFE79-LMH9-EVM includes a clocking and power solution and runs off a single 5.5-V supply. As [Figure 1-1](#) shows, the RF inputs and outputs using subminiature version A (SMA) connectors are on the top side of the EVM. A reference clock (for example, 10 MHz) to lock the onboard voltage-controlled crystal oscillator (VCXO) with the LMK04828, PLL-1 can be provided to the connector named LMK CLKIN (SMA J19).<sup>1</sup>

SMA J12 (REF\_CLK\_HIGH) or SMA J13 (REF\_CLK\_LOW) can be used to feed an external reference clock to lock the PLLs in the AFE79xx. The USB connector and the 5.5-V connector are on the right side of the board.



**Figure 1-1. AFE79-LMH9-EVM Top View**

[Figure 1-2](#) shows the bottom view of the AFE79-LMH9-EVM.



**Figure 1-2. AFE79-LMH9-EVM Bottom View**

The capture card to be used along with the AFE79-LMH9-EVM is typically the TSW14J56 or TSW14J57. The TSW14J56 supports a SerDes speed of up to 12.5 Gbps and the TSW14J57 goes as high as 15 Gbps. The choice of the TSW14J56 or TSW14J57 EVM depends on the AFE79xx JESD204 configuration and the associated SerDes rate.

<sup>1</sup> Many typical lab equipments have 10-MHz oscillator output to synchronize multiple lab systems. The onboard LMK04828 can accept the 10 MHz from external lab equipment to ensure synchronization and coherency of the data capture and generation to the AFE79-LMH9-EVM.

## 1.1 Hardware

Two bench power supplies are required to power the AFE79-LMH9-EVM and the TSW14J5x EVM. A PC to program the EVM and capture card is required. See [Section 1.1.1](#) for more information. All lab equipment requirements (such as signal source, signal analyzer, and so forth) are left to the users' discretion.

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### Note

Typically, the bench power supply with a rating of 5.5 V is used to power the AFE79-LMH9-EVM. The nominal EVM power supply voltage is 5 V. The additional 0.5-V overhead is added to compensate for the power cable loss as the AFE79-LMH9-EVM and the TSW14J56/TSW14J57 are to be configured to full operating mode to accommodate the voltage drop associated with power cable loss.

---

### 1.1.1 Recommended Test Environment

- Power supply at 5.5 V, 4 A maximum for the AFE79-LMH9-EVM
- Power supply at 5.5 V, 3 A maximum for the TSW14J56 EVM
- Power supply at 12 V, 3 A maximum for the TSW14J57 EVM (optional evaluation)
- A PC that supports USB 3.0 for fast file transfer from ADC capture and DAC pattern loading
- High-quality RF signal generator that supports RF frequency of interest for evaluation. The example set-up uses Keysight PSG series of signal generator.
- High-quality RF spectrum analyzer that supports RF frequency of interest for evaluation. The example set-up uses Rohde & Schwarz FSQ-26 series of spectrum analyzer.

### 1.1.2 Required Hardware

- TSW14J56 EVM (optional: TSW14J57 EVM)
- AFE79-LMH9-EVM
- USB 3.0 cable
- USB 2.0 Mini-B cable
- Two power supply cables

## 1.2 Required Software

The software used to configure the AFE79-LMH9-EVM is called *Latte*. The latest version of *Latte* is available for download from TI's MySecure website, you can request the software after signing into myTI [at this link](#). The installer file is called *AFE79xx\_EVM\_GUI\_v1p4p4p1*.

The TSW14J5x is controlled by the HSDC Pro software that can be downloaded from [www.ti.com/tool/dataconverterpro-sw](http://www.ti.com/tool/dataconverterpro-sw). HSDC Pro version 5.0 or higher is required.

### 1.2.1 Software Installation Sequence

1. Install High-Speed Data Converter Pro software. Follow all the instructions within the installer execution process. Note the directory to which the High-Speed Data Converter Pro software is installed.

---

#### Note

The default HSDC PRO software directory is in:

C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro

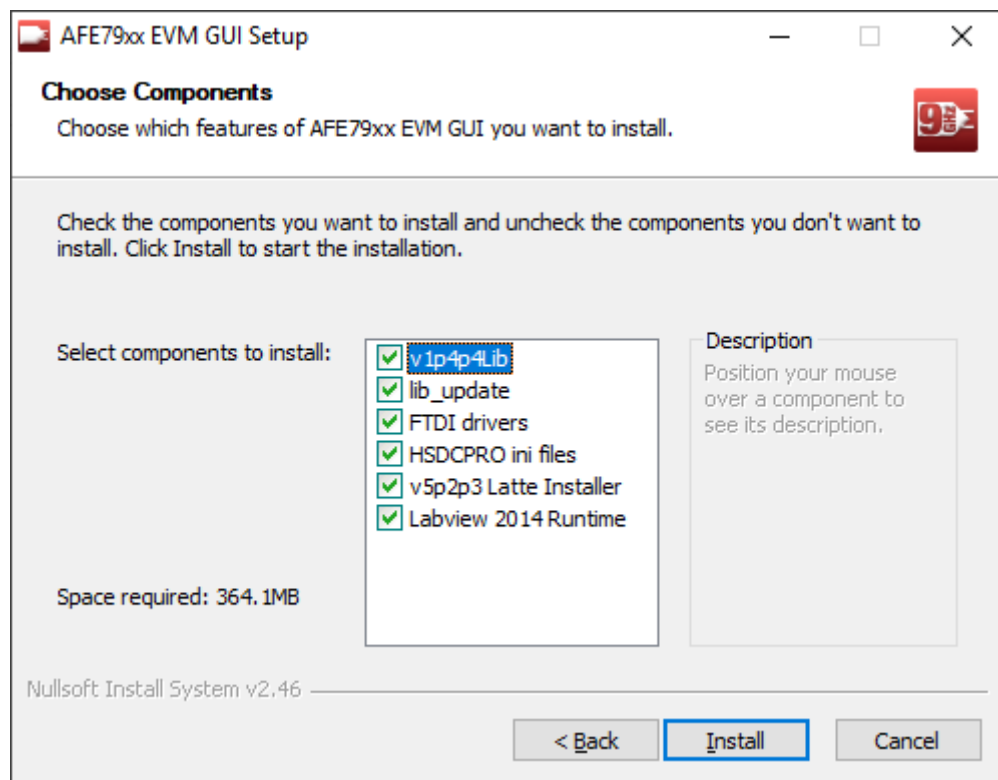
2. Install AFE79xxEVM\_GUIv1p4p4p1.exe. Follow all the instructions within the installer execution process. As shown in [Figure 1-3](#), the installer will install the following:
  - Latte 5.2.3
  - AFE79xx Latte Library v1.44

---

#### Note

Both the base Latte software and the AFE79xx Latte Library will be updated as needed throughout the product development process.

- National Instruments LabVIEW™ Runtime Engine 2014
- Associated HSDC PRO INI Files required for AFE79-LMH9-EVM.



**Figure 1-3. Latte Installer Options**

3. Note the directory to which the Latte software is installed.

---

#### Note

The Default Latte Software Directory is in:

C:\Users\“User ID”\Documents\Texas Instruments\Latte

Replace the “User ID” with the proper Windows login ID.

---

### 1.2.2 Software Installation Checks

After installing Latte, the AFE79xx.ini files appear in the respective folders in the HSDC Pro directory. Verify these files were properly installed by inspecting the relevant directories. The .ini files to look for are AFE79xx\_1x2FB\_44210.ini, AFE79xx\_2x2RX\_24410.ini, and AFE79xx\_2x2TX\_44210.ini.

For the TSW14J56:

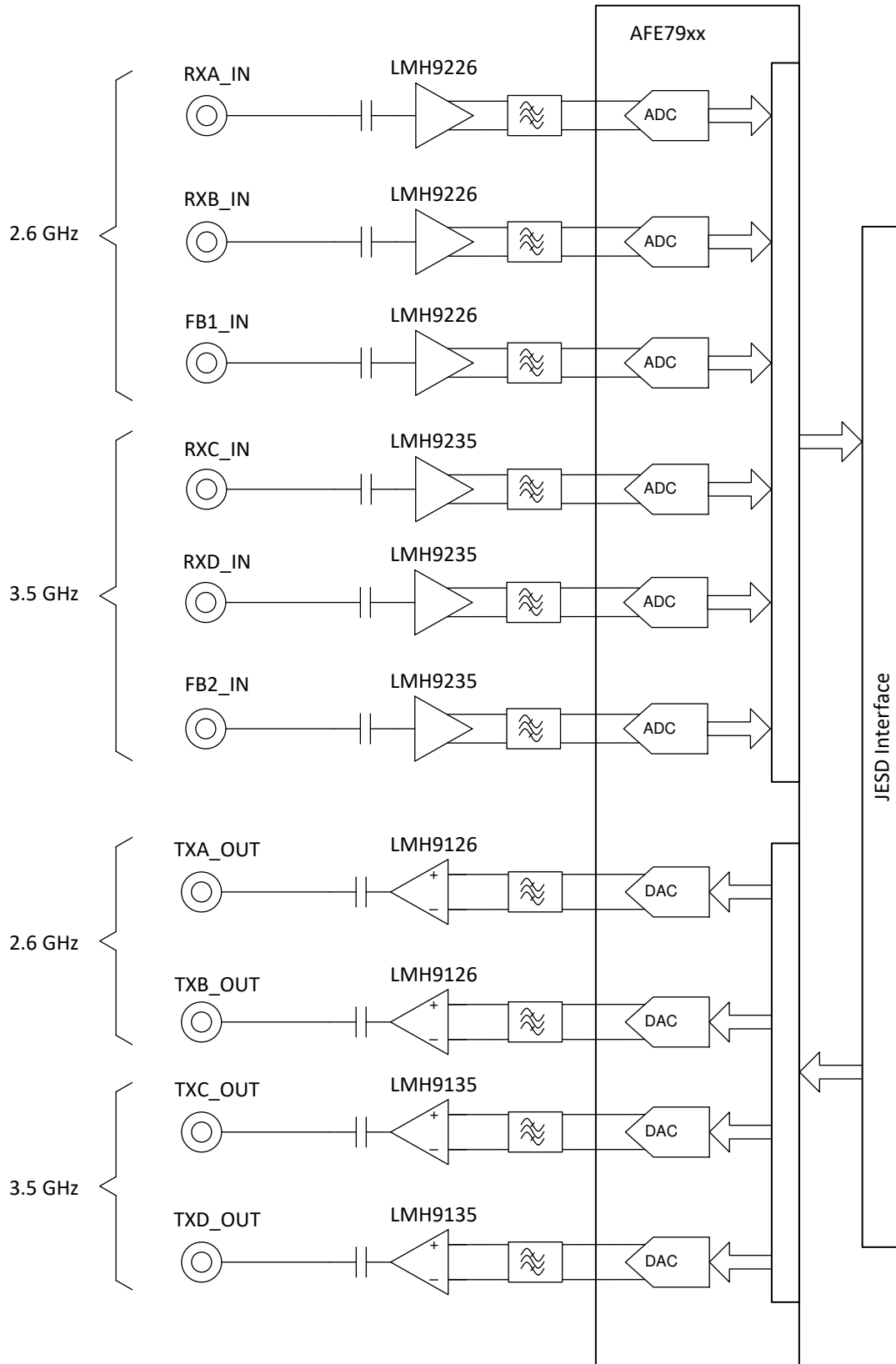
- C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J56revD Details\ADC files
- C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J56revD Details\DAC files

For the TSW14J57:

- C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J57revE Details\ADC files
- C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J57revE Details\DAC files

### 1.3 Signal Chain of the EVM Board

[Figure 1-4](#) illustrates the signal chain of the board.



**Figure 1-4. AFE79 + LMH9 EVM Block Diagram**

## 2 Hardware Setup (TSW14J56 Used as an Example)

### 2.1 Power Supply Setup

1. Connect 5.5-V power supply to the power jack (PWR\_JACK) connector (J18) of the AFE79-LMH9-EVM. The 5.5-V supply may be dropped to 5 V if power cable loss is not significant in the setup.
2. Check the D9 (PWR) LED. It should be lit up. The power supply should draw about 550 mA to 650 mA.
3. Connect a USB Type Mini-B Cable from the PC to the USB port (J19) of the AFE79-LMH9-EVM.
4. Check the D10 (USB\_PWR) LED. It should be lit up. The LED light may be weak depending on the USB cable length. If the LED is not lit up, use a shorter USB cable. TI tested a three foot long USB cable in this setup.
5. The power supply sequencer on the AFE79-LMH9-EVM has power status for each rail. If the power good (PGOOD) is in logic HI, the corresponding power supply rail is powered correctly. The respective LED will light up. Check the following LEDs to see if they are lit.
  - D5 (1P8) LED
  - D6 (1P2) LED
  - D7 (0p9) LED
  - D8 (3p3\_LMK) LED

### 2.2 AFE79-LMH9-EVM and TSW14J56 EVM Connections

1. Connect FMC connector U31 of AFE79-LMH9-EVM to FMC connector J4 of TSW14J56 EVM.
2. With the power supply in powered down mode, connect 5.5-V, 3-A maximum power supply to J11 “+5V IN” connector of the TSW14J56EVM.
3. Connect USB 3.0 cable from the PC to the J9 connector of the TSW14J56 EVM.
4. With the power supply in powered down mode, connect the 5.5-V, 4-A maximum power supply to J18 “CONN JACK PWR” connector of the AFE79-LMH9-EVM.
5. Connect the USB 2.0 cable from the PC to the J19 connector of the AFE79-LMH9-EVM.
6. Optionally: Connect 10-MHz lab equipment reference to J14, LMK\_CLK\_IN connector.

### 2.3 RF Test Equipment Setup

RF Test Setup requires RF Signal Generators, Spectrum Analyzer, Attenuator pads, Power Combiners, cables and so forth. Depending on the type of the test, appropriate setup can be used. The following user-guides show examples of the RF Test Setup:

- [LMH9126 EVM](#)
- [LMH9226 EVM](#)
- [LMH9135 EVM](#)
- [LMH9235 EVM](#)



### 3 Latte Overview

1. Launch the Latte GUI from the desktop shortcut or from All Programs->Texas Instruments. [Figure 3-1](#) shows how the Latte GUI appears.

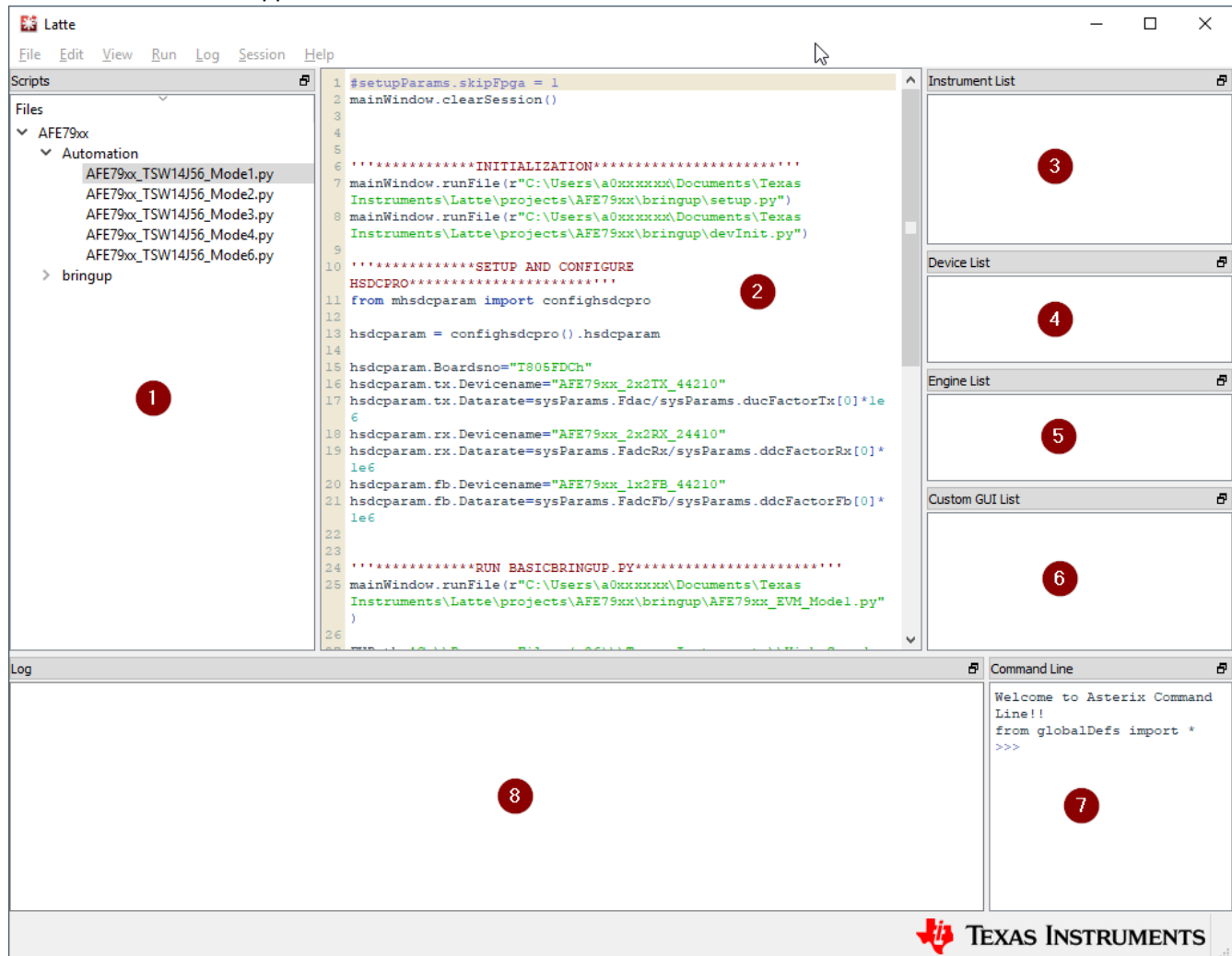


Figure 3-1. Latte GUI Overview

#### 3.1 Latte User Interface

The Latte UI is split into eight windows (labeled 1 to 8 in [Figure 3-1](#)) with the following functionality:

- **Window 1:**  
This window (also called *Scripts*) shows the list of python scripts available that generate the register commands to configure the AFE79-LMH9-EVM. The script files shown are located in the ..\Documents\Texas Instruments\Latte\projects\AFE79xx\bringup folder. Modify and create new scripts as necessary, which appear in this sub-window when you restart Latte.
- **Window 2:**  
This window (also called *Editor*) shows the code in the script currently selected and can be used to modify and save the code as necessary.
- **Window 3 to 6:**  
These windows get updated as you run the scripts to configure the AFE79-LMH9-EVM and mostly are informational.



- **Window 7:**

This window (also called *Command Line*) is used to enter and run individual commands. Examples of such commands include changing the TX, RX, and FBRX DSA, NCOs, and so forth.

- **Window 8:**

This window (also called *Log*) displays messages during execution of scripts to display the current status. This window is also used for troubleshooting.

### 3.2 Useful Latte Short-Cuts

**Run Script file:** Run a script file by first selecting the file in the Scripts window and then by pressing F5 (or selecting *Run* and then *Buffer* in the menu bar).

**Run part of script:** Run part of a script file by selecting the lines in the Editor window and then by pressing F7 (or selecting *Run* and then *Run Selection* in the menu bar).

**Stop Execution:** Stop the current execution by pressing F10 (or selecting *Run* and then *Stop* in the menu bar).

**Clear Session:** The current session can be cleared to reset the Latte UI to its initial state by pressing Ctrl-T (or selecting *Session* and then *Clear Session* in the menu bar). This process is equivalent to a restart and can be used to restart a session without closing the GUI.

## 4 AFE79-LMH9-EVM Automatic Configuration

This section guides you through the sequence of steps to automatically bring up the AFE79-LMH9-EVM through the automation python routine. The example used in this section will be the default AFE79-LMH9-EVM Mode 1. [Table 4-1](#) shows the default Mode 1 configuration overview.

**Table 4-1. AFE79-LMH9-EVM Mode 1 Configuration Overview**

Mode	Default Programming
TX (transmitter)	4 TXDACs are enabled, DSA = 0, LMFSHd_2TX = 44210, 6 × interpolation, 491.52-MSPS data rate
RX (receiver)	4 RXADCs are enabled, DSA = 0, LMFSHd_2RX = 24410, 12 × decimation, 245.76-MSPS data rate
FBRX (feedback receiver)	2 FBADCs are enabled, DSA = 0, LMFSHd_1FB = 22210, 6 × decimation, 491.52-MSPS data rate
SerDes	8 lanes running at 9830.4 Mbps
Data Converter Clock Rates	$F_{RXADC} = 2949.12$ MSPS, $F_{FBADC} = 2949.12$ MSPS, $F_{TXDAC} = 8847.36$ MSPS
Status	RX AGC is disabled, RX, TX DSA step impairments is uncorrected, DAC in interleaved mode

[Table 4-2](#), [Table 4-3](#), and [Table 4-4](#) show the TSW14J5x INI files to be used to evaluate the RXADC, FBADC, and the TXDAC portion of the AFE79xx. The tables also show the associated channel mapping with respect to the AFE79-LMH9-EVM.

**Table 4-2. RXADC TW14J5x INI Mapping (AFE79xx\_2x2RX\_24410)**

ADC Channel Number in HSDC PRO ADC Panel <sup>(1)</sup>	AFE79-LMH9-EVM Connector	Associated AFE79xx Input
1,2	J3, RXA_IN	1RX
3,4	J1, RXB_IN	2RX
5,6	J4, RXC_IN	3RX
7,8	J2, RXD_IN	4RX

(1) For complex quadrature output (I/Q) of the RXADC, the odd number is the real channel, while the even number is the imaginary channel.

**Table 4-3. FBADC TW14J5x INI Mapping (AFE79xx\_1x2FB\_44210)**

ADC Channel Number in HSDC PRO ADC Panel <sup>(1)</sup>	AFE79-LMH9-EVM Connector	Associated AFE79xx Input
1,2	J5, FB1_IN	1FB
3,4	J6, FB2_IN	2FB

(1) For complex quadrature output (I/Q) of the FBADC, the odd number is the real channel, while the even number is the imaginary channel.

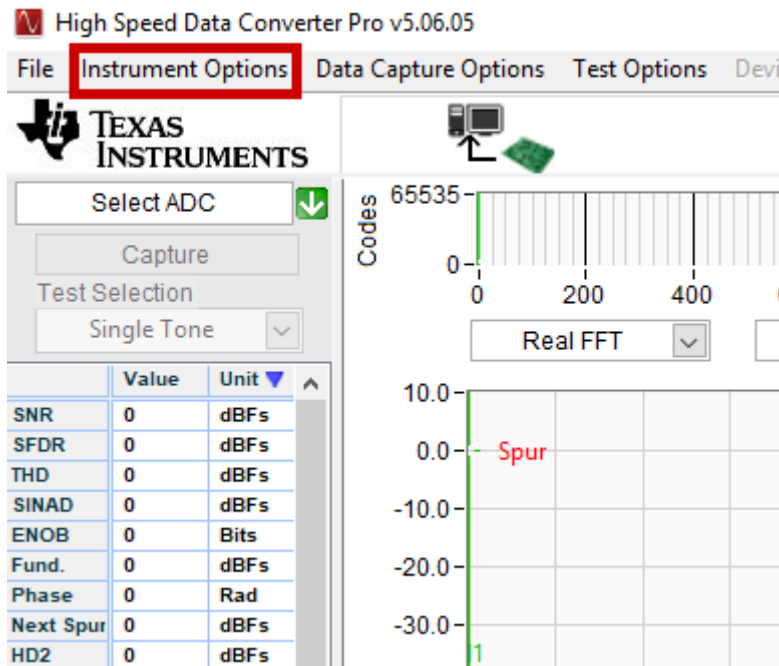
**Table 4-4. TXDAC TSW14J5x INI Mapping (AFE79xx\_2x2TX\_44210)**

DAC Channel Number in HSDC PRO DAC Panel <sup>(1)</sup>	AFE79xx EVM Connector	Associated AFE79xx Input
1,2	J9, TXA_OUT	1TX
3,4	J7, TXB_OUT	2TX
5,6	J10, TXC_OUT	3TX
7,8	J8, TXD_OUT	4TX

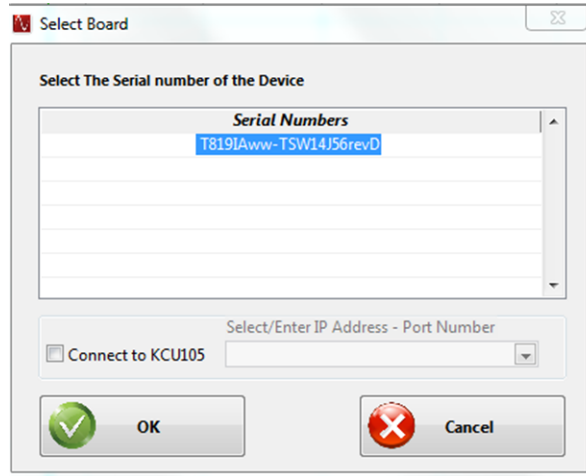
(1) For complex quadrature output (I/Q) of the TXDAC, the odd number is the real channel, while the even number is the imaginary channel.

## 4.1 Steps to Start Automatic Configuration

1. Within the Microsoft® Windows® PC, start the HSDC PRO software by going to Start -> Texas Instruments -> High Speed Data Converter Pro. Ensure that the High-Speed Data Converter Pro started properly as shown in [Figure 4-1](#). Take note of the *Serial Numbers* of the TSW14J56 EVM after the device is connected.

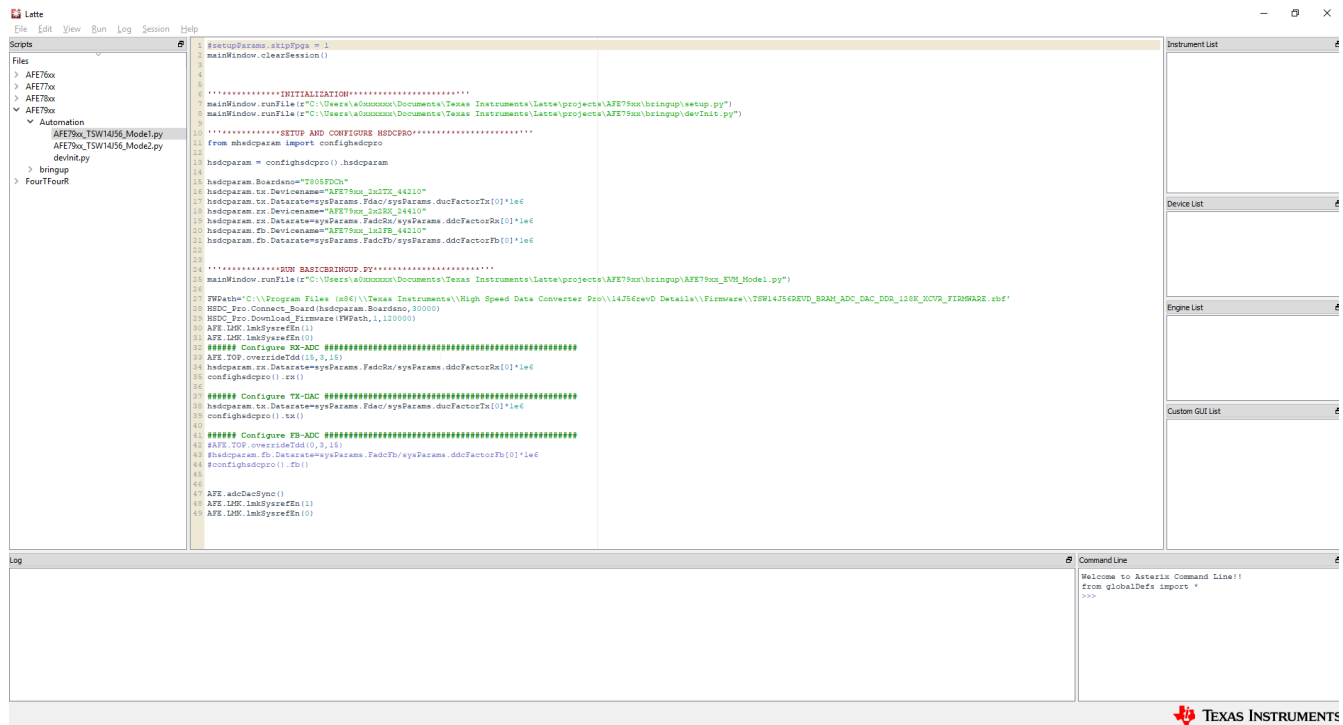

**Figure 4-1. Connecting to TSW14J56 From HSDC PRO**

2. Press the OK button to proceed the connection of the TSW14J56 EVM to the PC.



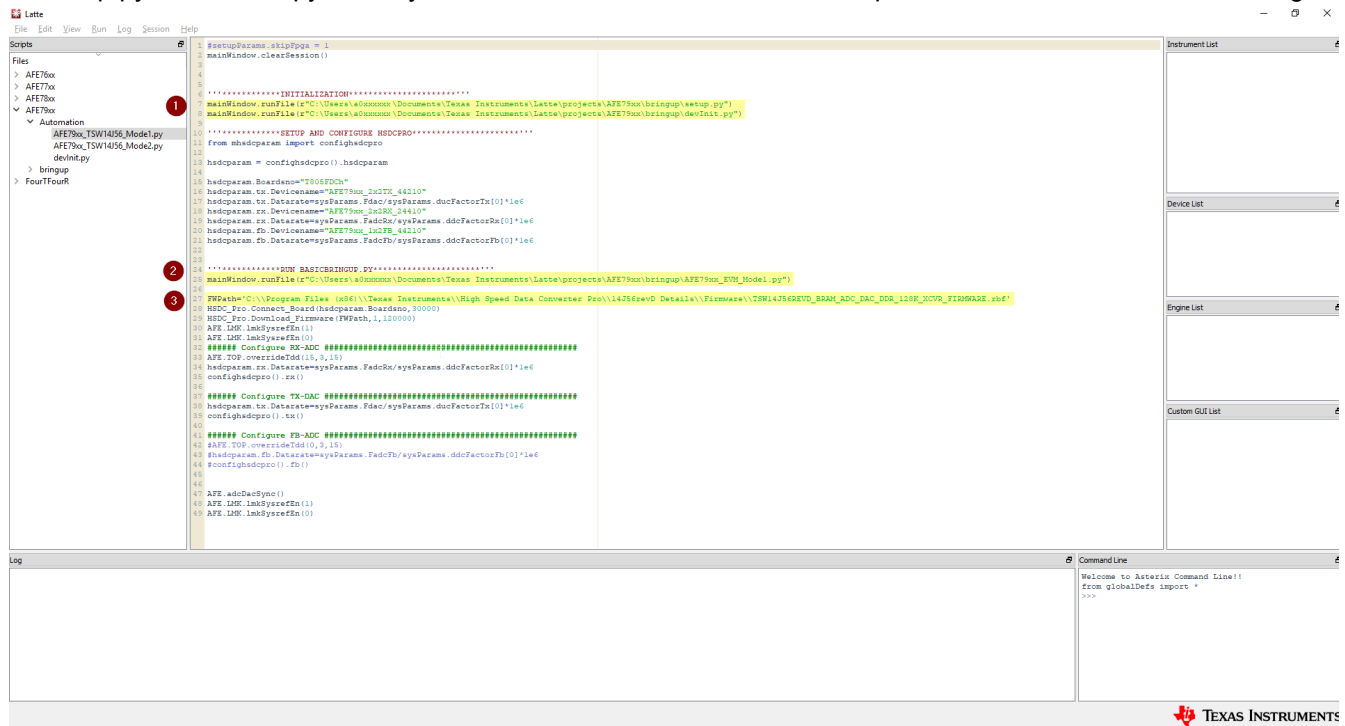
**Figure 4-2. HSDC Pro Connect to Board**

3. Within the Microsoft Windows PC, start the Latte software by going to Start -> Texas Instruments -> Latte. Ensure that the Latte software had started properly.
4. On the left hand side of the Latte, within the Scripts window, expand AFE79xx -> Automation -> AFE79xx\_TSW14J56\_Mode1.py. The python script is shown in [Figure 4-3](#):



**Figure 4-3. AFE79xx Mode 1 Automatic Configuration Script**

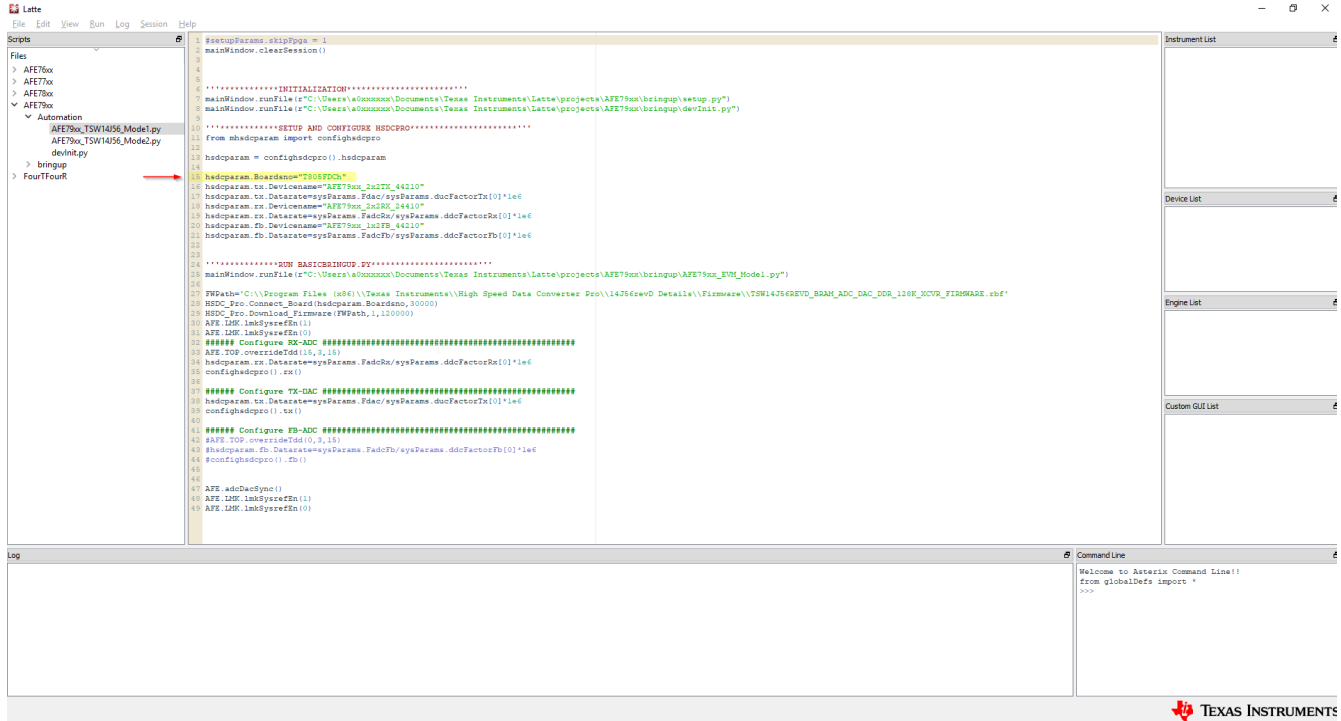
- Three parameters within the AFE79xx\_TSW14J56\_Mode1.py must be changed per the directory being used by the High-Speed Data Converter Pro software and the Latte software.
- Change item #1 and #2 as highlighted in Figure 4-4 to reflect the location of the Latte install directory for the setup.py and devInit.py. Usually the area where “a0xxxxxx” must be replaced with the Windows user ID login.



**Figure 4-4. Directory Parameter to be Changed in the Automation Script**

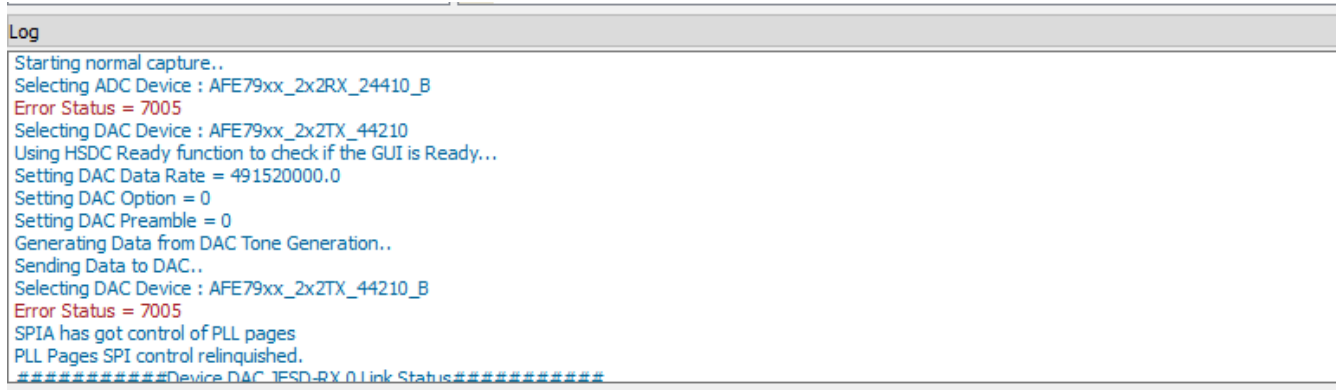
- Change item #3 as highlighted in Figure 4-4 to reflect the location of the High-Speed Data Converter Pro directory for the TSW14J56 firmware.

8. Enter the serial number of the TSW14J56 EVM per the highlighted location in [Figure 4-5](#).



**Figure 4-5. TSW14J56 EVM Serial Number Location**

- With the `AFE79xx_TSW14J56_Mode1.py` highlighted, press the F5 button to execute the script. The script will automate both High-Speed Data Converter Pro software and Latte software to automatically bring up the JESD204B link.
- After the script runs, expect the following two error messages (shown in [Figure 4-6](#) and [Figure 4-7](#)):



**Figure 4-6. Latte Error 1**

```
Log
#####Device DAC JESD-RX 0 Link Status#####
CS State TX0: 0b10101010 . It is expected to be 0b10101010
FS State TX0: 0b01010101 . It is expected to be 0b01010101
Could get the link up for device RX: 0
#####
#####Device DAC JESD-RX 1 Link Status#####
CS State TX0: 0b10101010 . It is expected to be 0b10101010
FS State TX0: 0b01010101 . It is expected to be 0b01010101
Could get the link up for device RX: 1
#####
#Done executing .. AFE79xx/Automation/AFE79xx_TSW14J56_Mode1.py
#End Time 2019-08-30 15:57:56.910000
#Execution Time = 163.04700017 s
#===== ERRORS:2, WARNINGS:0 =====#
```

**Figure 4-7. Latte Error 2**

11. The default AFE79-LMH9-EVM has the following RF frequency matching network:
  - a. RXA, RXB, FBAB, TXA, and TXB = 2600 MHz
  - b. RXC, RXD, FBAB, TXC, and TXD = 3500 MHz
12. The example script to change the NCO to match the default RF frequency matching network is the following:

```
AFE.updateTxNco(0,2600,0,0)
AFE.updateTxNco(1,2600,0,0)
AFE.updateTxNco(2,3500,0,0)
AFE.updateTxNco(3,3500,0,0)
AFE.updateRxNco(0,2600,0,0)
AFE.updateRxNco(1,2600,0,0)
AFE.updateRxNco(2,3500,0,0)
AFE.updateRxNco(3,3500,0,0)
AFE.updateFbNco(0,2600,0)
AFE.updateFbNco(1,3500,0)
```

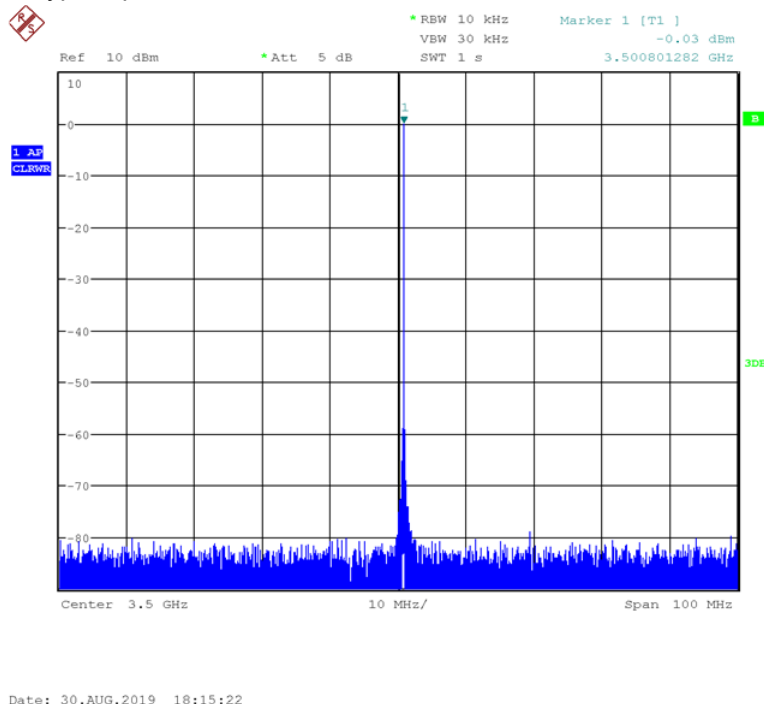
13. Enter the commands in the command line prompt as shown in [Figure 4-8](#) or execute AFE79xx\_DC101\_NCO\_Setup.py (under Automation Folder of AFE79xx) in the Latte through F5 key.

```
Command Line
Welcome to Asterix Command Line!!
from globalDefs import *
>>> AFE.updateTxNco(0,2600,0,0)
>>> |
```

**Figure 4-8. Latte Command Prompt for Updating TXNCO**

## 4.2 TXDAC Evaluation

1. Connect the spectrum analyzer to J9 (TXA), J7 (TXB), J10 (TXC), or J8 (TXD) to monitor the TXDAC output. See [Figure 4-9](#) for typical performance measurement.



**Figure 4-9. Typical TXDAC Single-Tone Performance at 3.5 GHz**

2. The user may now change the DAC patterns or load custom DAC patterns through external files (see [Section 7.1](#)).

## 4.3 RXADC and FBADC Evaluation

1. Before starting the RXADC and FBADC performance capture, the test option of the HSDC PRO must be setup. Go to *Test Options* to enter the *Filter Parameters* menu. By default, there are 25 bins to remove on either side of fundamental and 25 bins to remove. Change the number of bins to remove on either side of fundamental to 100 bins (see [Figure 4-10](#)).
  - a. With 245.76 MSPS of data rate for RXADC at 16384 sample points, this removes 1.5 MHz of bins on either side of the fundamental.
  - b. With 491.52 MSPS of data rate for FBADC at 16384 sample points, this removes 3.0 MHz of bins on either side of the fundamental.
  - c. The number of bins to be removed is a standard recommendation from TI to remove the effect of the ADC sampling clock in-band phase noise from affecting the broadband noise used to calculate the SNR through the FFT engine. The number of bins must be adjusted based on the end-application standard.



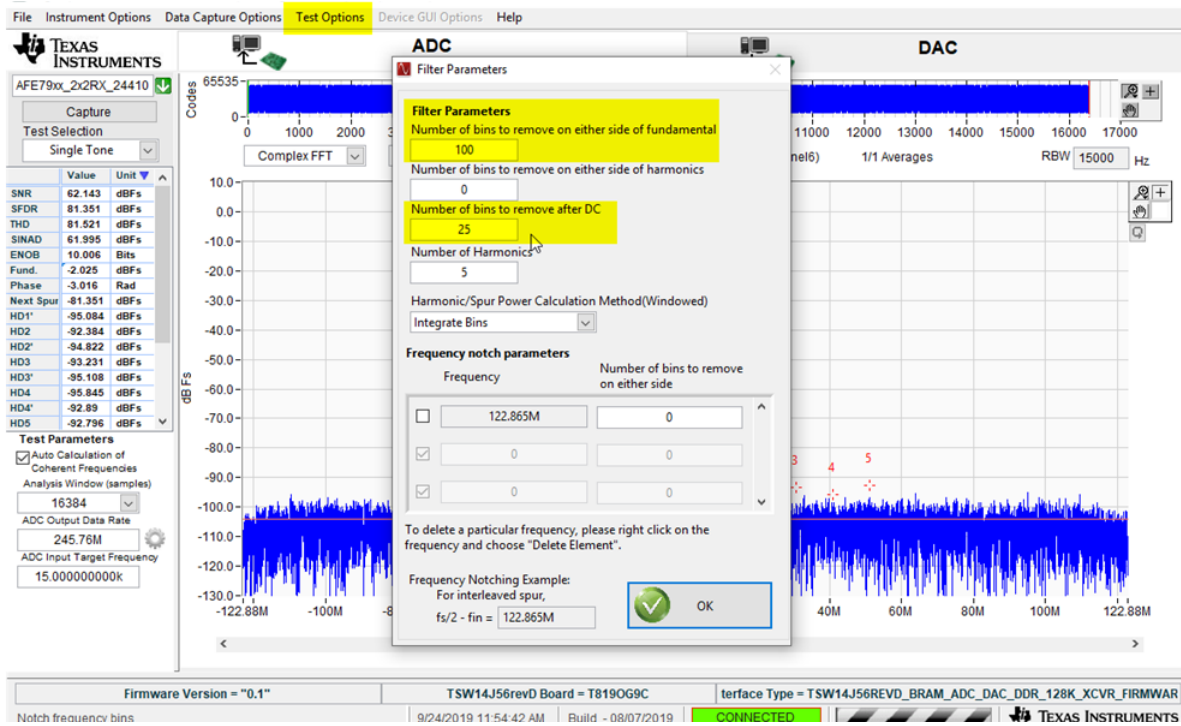


Figure 4-10. HSDC PRO ADC Performance FFT Binning Configuration

- Connect the RF signal generator output to J3 (RXA\_IN), J1 (RXB\_IN), J4 (RXC\_IN), and J2 (RXD\_IN) to capture the RF input to the ADC. On the High-Speed Data Converter Pro, press the *Capture* button to capture the ADC data. This is shown in Figure 4-11.

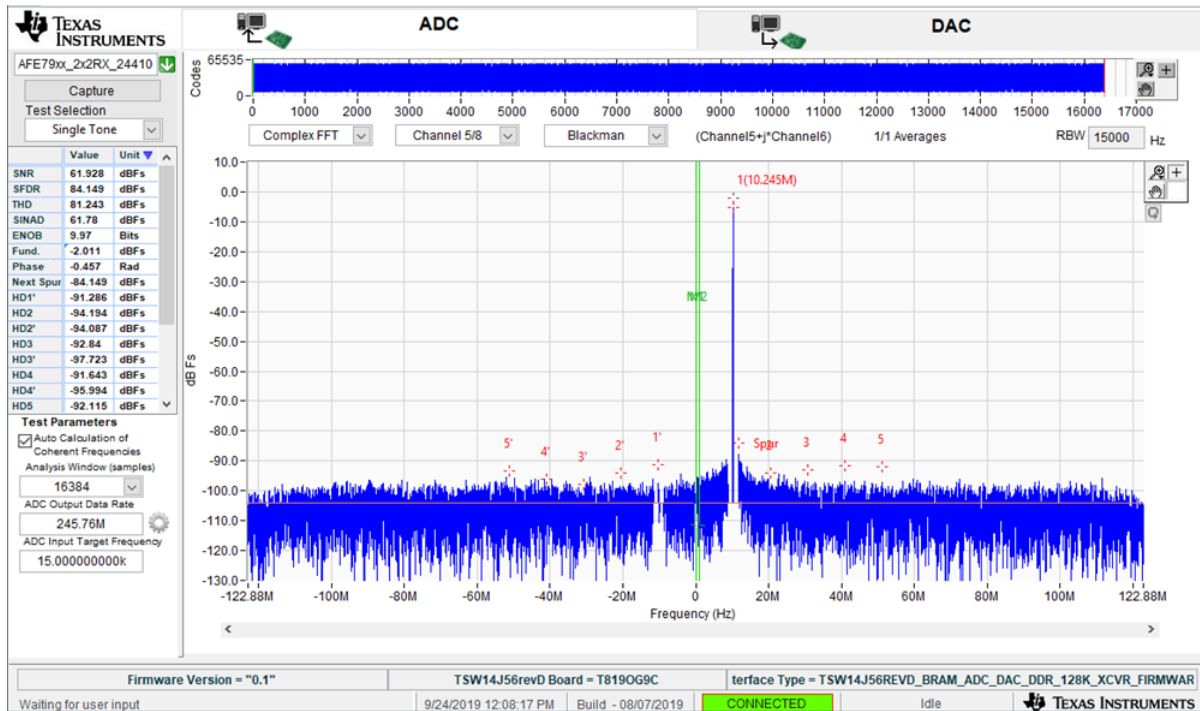


Figure 4-11. HSDC PRO ADC Data Capture and Typical Single Tone 3.5-GHz Performance for RXADC

3. For RXA\_IN, RXB\_IN, and FB1\_IN, input 2610 MHz at -20 dBm
  - a. RXA\_IN is Channel 1 and 2 in FFT Channel Selection
  - b. RXB\_IN is Channel 3 and 4 in FFT Channel Selection
  - c. FB1\_IN is Channel 1 and 2 in FFT under FB mode Channel Selection
4. For RXC\_IN, RXD\_IN, and FB2\_IN, input 3510 MHz at -20 dBm
  - a. RXC\_IN is Channel 5 and 6 in FFT Channel Selection
  - b. RXD\_IN is Channel 7 and 8 in FFT Channel Selection
  - c. FB2\_IN is Channel 3 and 4 in FFT under FB mode Channel Selection
5. For Feedback ADC, execute the following commands or execute AFE79xx\_FB\_Capture.py through the F5 key.
  - a. 

```
##### Configure FB-ADC
#####
AFE.TOP.overrideTdd(0,3,0)
hscparam.fb.Datarate=sysParams.FadcFb/sysParams.ddcFactorFb[0]*1e6confighscpro().fb()
```

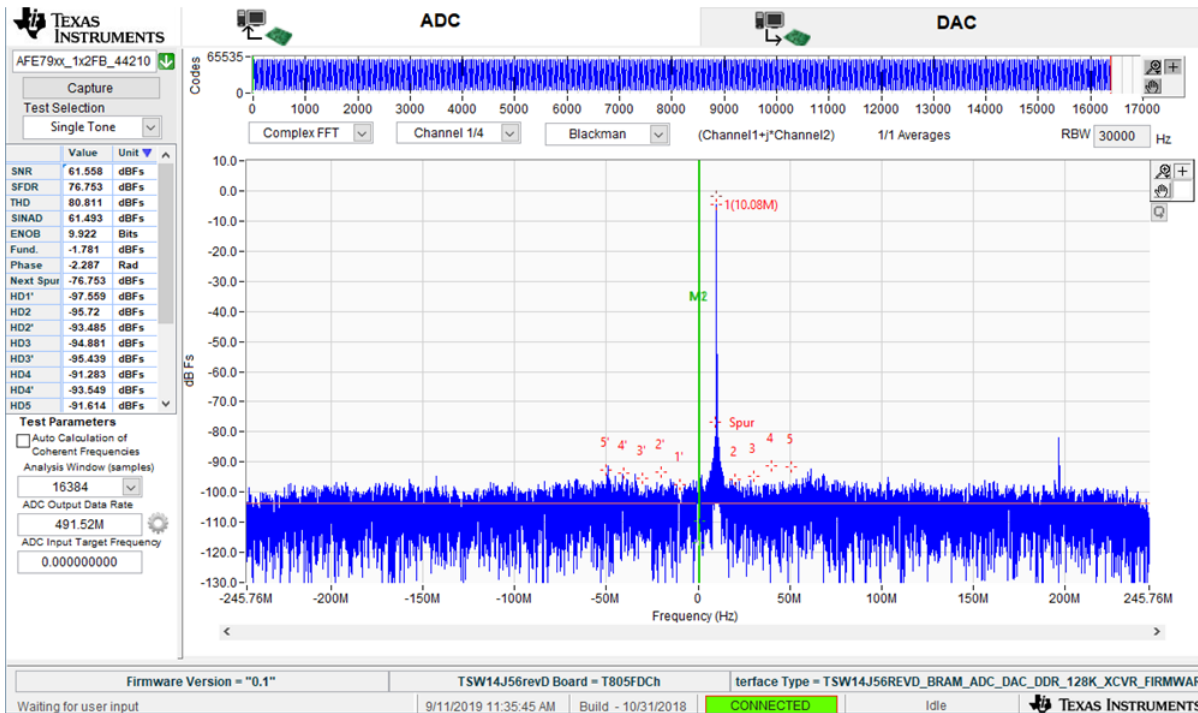


Figure 4-12. Typical Single Tone 3.5-GHz Performance for FBADC

## 5 Status Check and Troubleshooting Guidelines

This section provides a general guideline on the status indicators of the AFE79-LMH9-EVM and also the respective troubleshooting guidelines.

### 5.1 AFE79-LMH9-EVM Status Indicators

The green LED D3 should be lit at this point. D3 indicates that PLL loop 2 of the LMK04828 is locked. Optionally, the LED D4 indicates that PLL loop 1 of the LMK04828 is locked. If there are external equipment providing 10-MHz reference to the LMK04828 for lab equipment synchronization, then this LED D4 must be lit. The EVM is still functional without PLL loop 1 running, but PLL loop 2 is necessary for a successful bringup.

- If PLL loop 1 is not running, check the 10-MHz reference. This is necessary to achieve signal coherency with the signal generators and spectrum analyzer.
- If PLL loop 2 is not locked, contact TI applications for additional support.

## 5.2 TSW14J56 EVM

TSW14J56EVM – D1 and D3 should not be lit. D2 and D4 should be flashing. These are necessary requirements for the JESD204B transceiver mode to work. D2 flashing indicates the TXDAC JESD204B link has been established, while D4 flashing indicates the RXADC or FBADC JESD204B link has been established.

AFE79-LMH9-EVM – Data transmission on the DAC and data capture on the ADC should be enabled at this point. The RXNCO, FBNCO, and TXNCO can now be adjusted.

RXDSA, FBDSA, and TXDSA can be adjusted.

```
##RXDSA Adjustment
AFE.DSA.setRxDsa(chNo,dsaSetting) ##chNo: ranges 0-3. dsaSetting: DSA
setting in dB

##FBDSA Adjustment
AFE.DSA.setFbDsa(chNo,dsaSetting) ##chNo: ranges 0-1. dsaSetting: DSA
setting in dB

##TXDSA Adjustment
AFE.DSA.setTxDsa(chNo,dsaSetting) ##chNo: ranges 0-3. dsaSetting: DSA
setting in dB
```

## 6 AFE79-LMH9-EVM Manual Configuration

This section guides you through the sequence of steps to manually bring up the AFE79-LMH9-EVM. The automatic setup process is broken down in this section to allow the user to understand the process and make modifications accordingly.

### 6.1 TSW14J5x DAC Pattern Setup

Configure the HSDC Pro GUI to send a DAC pattern from the TSW14J5x board. See [Section 7.1](#) and [Section 7.2](#), if needed.

---

#### Note

Send a digital-to-analog converter (DAC) pattern to the AFE79-LMH9-EVM before configuring the EVM to provide the proper training SERDES signal for the adaptation algorithm of the AFE79xx SerDes RX equalizer. The DAC pattern can be sent from the TSW14J5x board controlled through the HSDC Pro GUI.

---

### 6.2 Connect Latte to Board

This step establishes a connection between the PC running Latte and the AFE79-LMH9-EVM.

1. In the scripts window, select *setup.py* and press F5 to run the program.
2. Check the Log window to ensure there are no errors where the following line should be displayed four times: *Kintex RegProgrammer - USB Instrument created.*
3. Missing or obsolete drivers for the FT4232H chip in the AFE79-LMH9-EVM is a common error source. Use the device manager to verify a connection between the PC and the EVM by checking the USB instantiations.
4. Update your PC with the appropriate driver, if necessary.

## 6.3 Compile Libraries

In this step, the library of scripts packaged with the Latte UI is compiled and takes approximately half a minute to run.

1. In the scripts window, select *devInit.py*.
2. Press F5 to run the program
3. Check the Log window for status and errors.

## 6.4 Program AFE79-LMH9-EVM

In this step, the LMK04828 and AFE79xx on the AFE79-LMH9-EVM is programmed.

1. Click on the script named *AFE79xx\_EVM\_Mode1.py* and press F5. No errors are expected, but warnings regarding SPI control, relinquish, and reset property can be ignored. This step takes a few minutes.
2. Check the Log window to monitor any errors. This step completes the AFE79-LMH9-EVM configuration. Current consumption into the AFE79-LMH9-EVM is approximately 3 A.
3. An LOS error indicates that the SerDes RX is electrically idle and, in that case, the TX output will not be normal. This error can be resolved by resending the data (the DAC pattern) and reconfiguring the AFE79-LMH9-EVM (that is, run *basicBringup.py* again).
4. GPIO warnings or sysref errors usually indicate supply voltage or current limitations. Verify the power supply to the AFE79-LMH9-EVM and ensure a 5.5-V supply voltage and a 4-A current limit is used. Restart the Latte UI and rerun the scripts.

## 6.5 Modify Configuration

The examples in the previous sections configure the AFE79xx with the default mode set in Latte scripts. You can change the mode by modifying a set of parameters.

### 6.5.1 Data Rate and JESD Parameters

Data rates in the signal chain are often connected with the JESD mode (LMFS, SerDes rate), and a list of compatible modes are provided in the device data sheet. The following parameters in the *basicBringup.py* script can be used to modify the configuration. Rerun the script after assigning new values to the following parameters.

```
## In below parameters, each element sets the particular LMFS-Hd for the particular channels.
# JESD and Serdes Parameters
sysParams.LMFSHdRx           = ["24410", "24410", "24410", "24410"]
sysParams.LMFSHdFb          = ["22210", "22210"]
sysParams.LMFSHdTx           = ["44210", "44210", "44210", "44210"]
# Decimation and interpolation parameters for the data converter signal chains.
sysParams.ddcFactorRx        = [12, 12, 12, 12]
sysParams.ddcFactorFb        = [6, 6]
sysParams.ducFactorTx        = [6, 6, 6, 6]
```

### 6.5.2 Data Converter Clocks Settings

This parameter is used to configure the data converter clocks and clock distribution path.

```
#Configures the reference input frequency to the on-chip PLL of the AFE7920.
sysParams.FRef               = 491.52
#Configures the RXADC converter sample rate.
sysParams.FadcRx             = 2949.12
#Configures the FBADC converter sample rate.
sysParams.FadcFb             = 2949.12
#Configures the TXDAC converter sample rate.
sysParams.Fdac               = 2949.12*3
#Sets the clock source for the RXADC converters. The source is now from the on-chip PLL.
sysParams.externalClockRx    = False
#Sets the clock source for the TXDAC converters. The source is now from the on-chip PLL.
sysParams.externalClockTx    = False
```

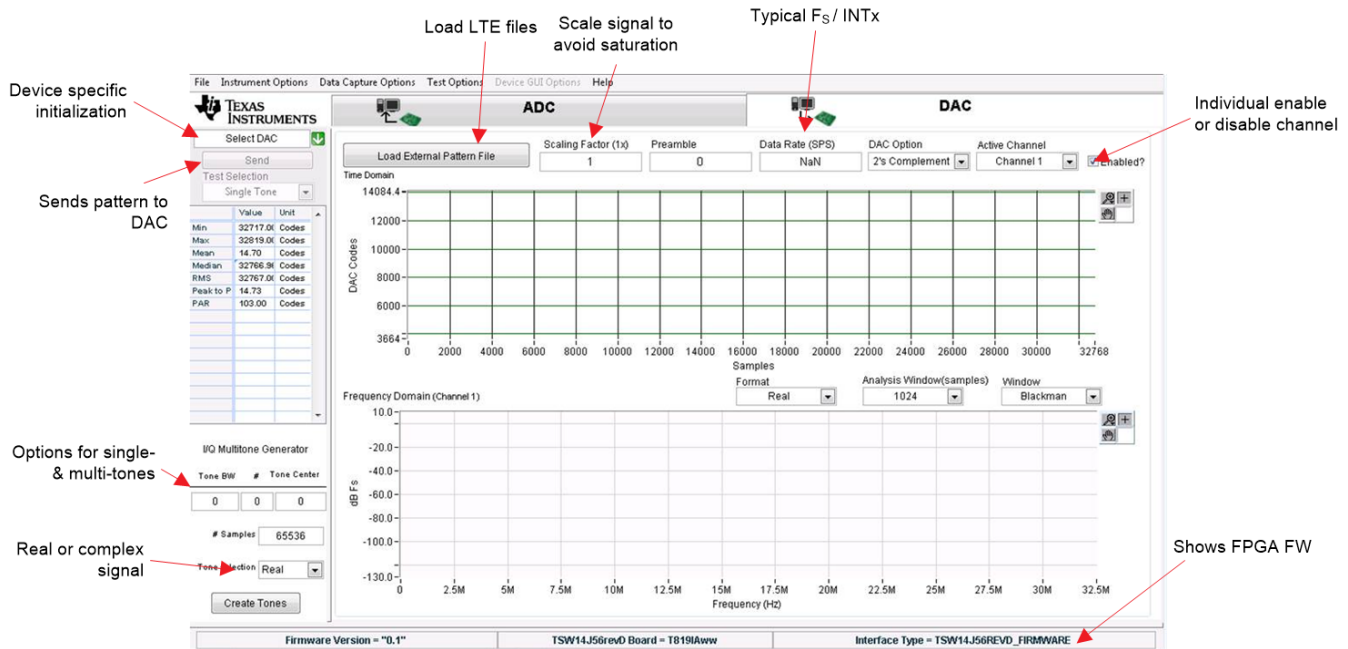
## 7 Setup the TSW14J5x With the HSDC Pro

This chapter is intended to serve as a quick-start guide for users not familiar with the TSW14J5x and the HSDC Pro GUI. See the [High Speed Data Converter Pro GUI User's Guide](#) for more details.

### 7.1 DAC Pattern Setup and Send

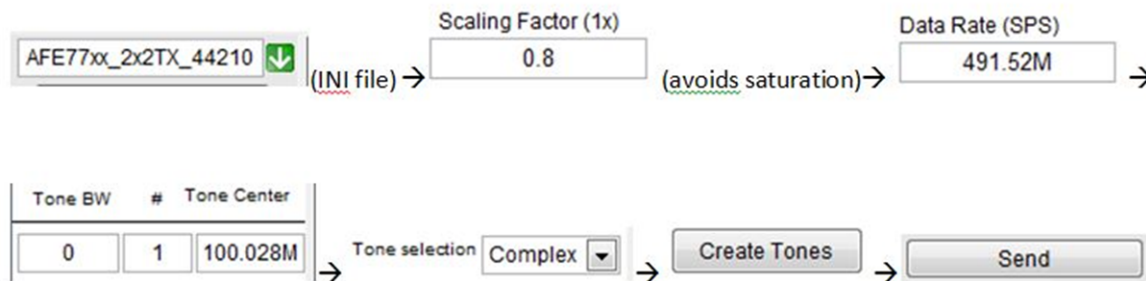
This section lists the steps to create and send a DAC pattern from the TSW14J5x board.

1. Click on the HSDC Pro DAC tab. [Figure 7-1](#) shows a brief description of the DAC tab.



**Figure 7-1. HSDC Pro DAC Tab Overview**

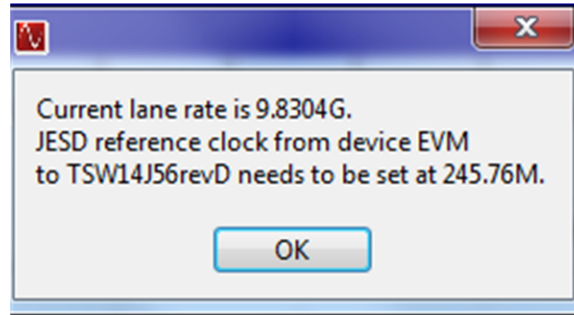
2. A pictorial representation to create and send a sinusoid is shown in [Figure 7-2](#) followed by the steps in detail.



**Figure 7-2. Setup a Sinusoid**

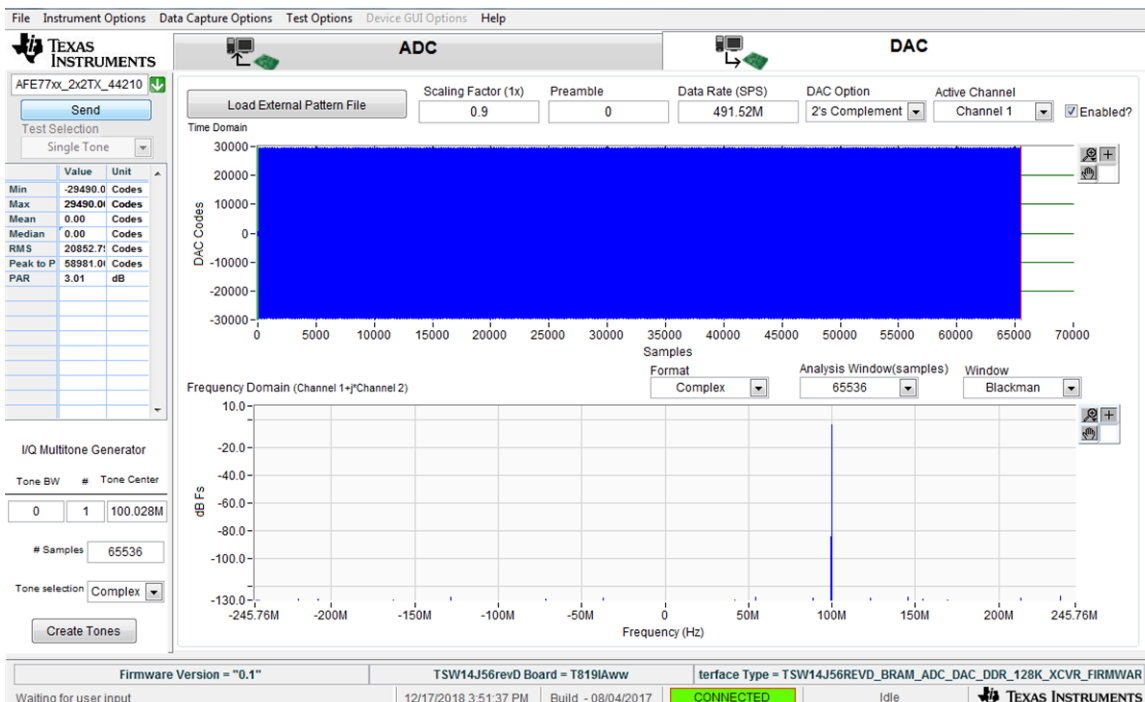
3. In the device-specific initialization option, select *AFE79xx\_2x2TX\_44210*. Click Yes if prompted to download the firmware (FW). The default option is to run the board in the transceiver mode of operation, which enables simultaneous operation of the TX and the RX and FBRX. The FW used in transceiver mode has the letters *XCVR* in its name.
4. Enter "491.52 M" as the data rate and "0.9" for a scaling factor.
5. Create a sinusoid by entering the frequency in the *Tone Generator* section of the HSDC Pro window.

- Press *Send* to transmit the DAC pattern to the AFE79-LMH9-EVM. **Figure 7-3** shows the resulting message with the lane rate and reference clock expected in the FPGA. Click OK.



**Figure 7-3. HSDC Pro Lane and Reference Clock Rate Pop-Up**

**Figure 7-4** shows an example setup with a 100-MHz sinusoid.



**Figure 7-4. HSDC Pro CW**

Alternately, a pattern file (for example, LTE) can be loaded and sent using the *Load External Pattern File* button.

The DAC setup is now complete.

## 7.2 DAC Synchronization Check

- LED D2 on the TSW14J56 board blinks to indicate a successful JESD link on the DAC side.
- If the LED is not blinking, send the DAC pattern again.



### 7.3 ADC Data Capture

This section shows the steps to capture the ADC output.

1. Click on the HSDC Pro ADC tab. Figure 7-5 shows a brief description of the ADC tab.

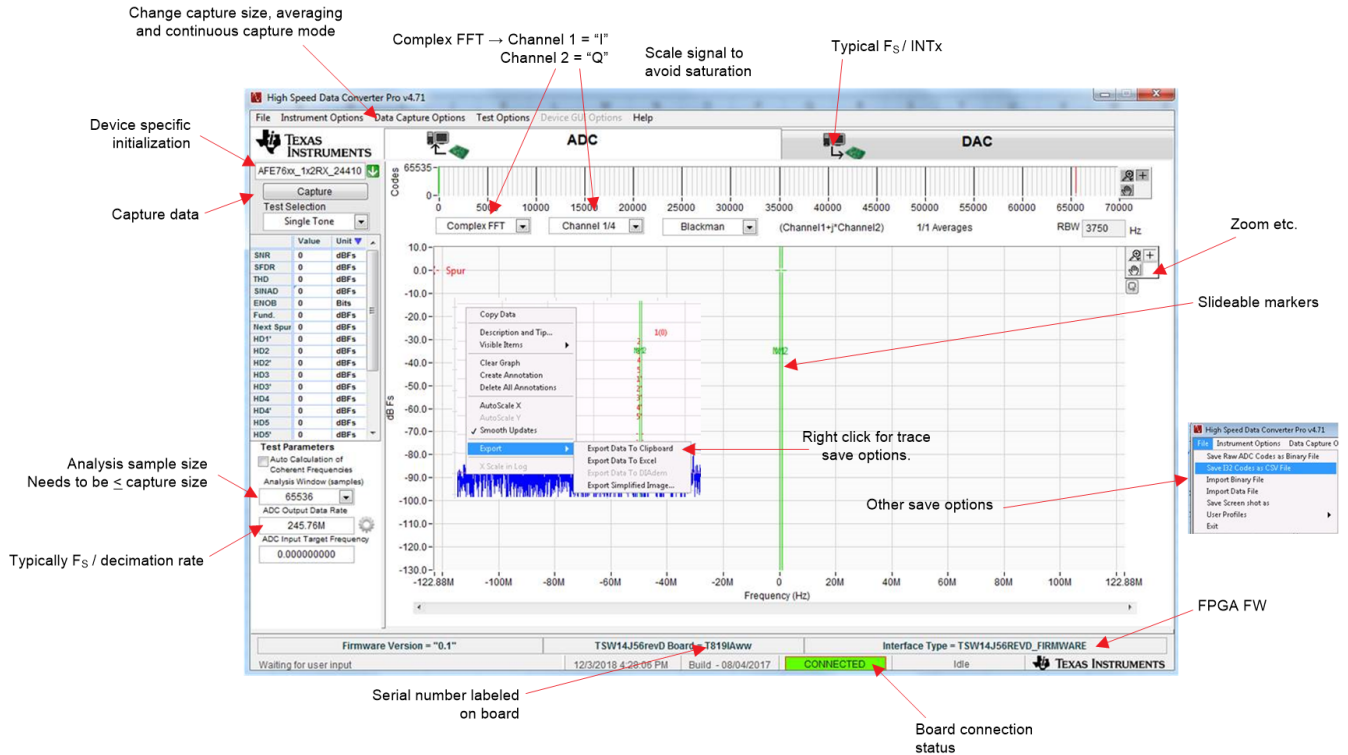


Figure 7-5. HSDC Pro ADC Tab Overview

2. Select *AFE79xx\_2x2RX\_24410* as your device.
3. Go to *Data Capture Options* in the menu bar and choose the *Capture* option. Set #samples (per channel) to 16384. Click the *OK* button.
4. Select *16384* in the *Analysis* window located in the lower left section of the GUI.
5. Enter "245.76 M" for ADC output data rate
6. Click the *Capture* button.

The capture size is set to a lower value (such as 16K) because of the limited BRAM memory available in the FPGA.

### 7.4 ADC Synchronization Check

After a successful capture on the ADC side, LED D4 on the TSW14J56 board blinks to indicate a successful JESD link on the ADC side. You should also see the FFT output. A timeout on the ADC capture indicates a unsuccessful bringup of the AFE79xx. Try again after rerunning the AFE79xx configuration.



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**NOTE:**

**EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGRADATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.**

### 3 Regulatory Notices:

#### 3.1 United States

##### 3.1.1 Notice applicable to EVMs not FCC-Approved:

**FCC NOTICE:** This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

##### 3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

#### **CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

#### **FCC Interference Statement for Class A EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

#### **FCC Interference Statement for Class B EVM devices**

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

#### 3.2 Canada

##### 3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

#### **Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

#### **Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### **Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

### Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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[http://www.tij.co.jp/lstds/ti\\_ja/general/eStore/notice\\_01.page](http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page)

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

- 
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    - 4.3 *Safety-Related Warnings and Restrictions:*
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      - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
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