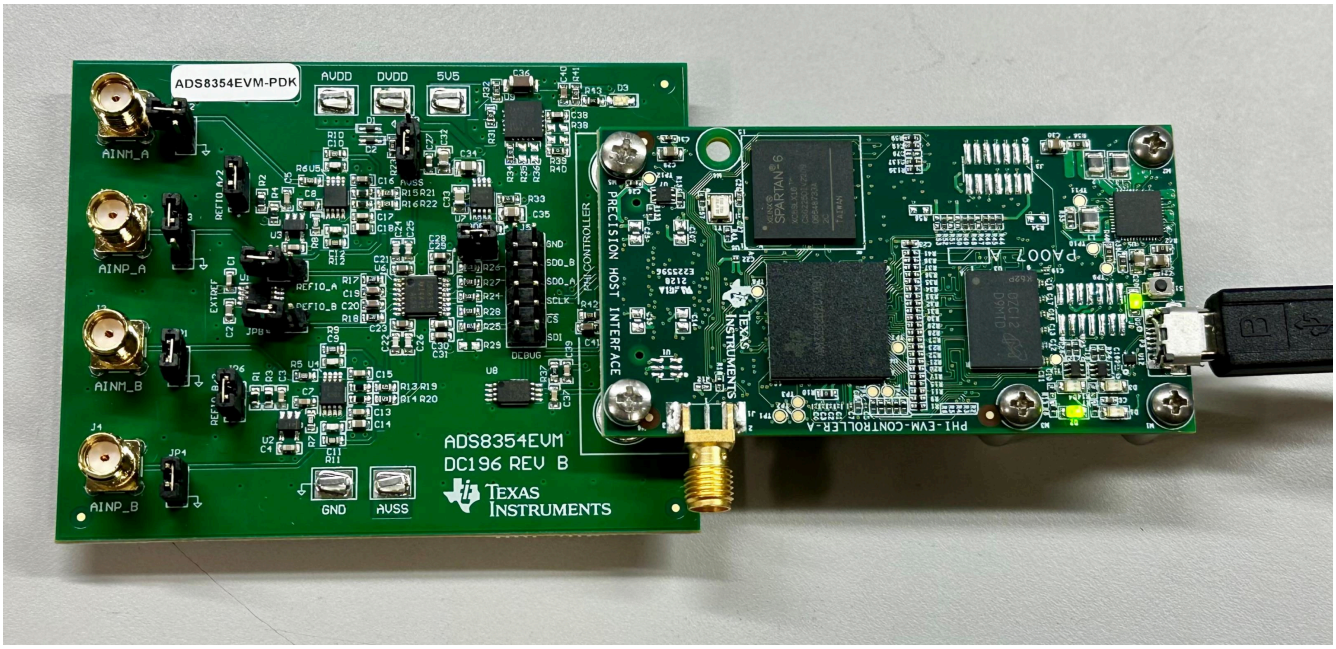
User's Guide

ADS8354EVM-PDK Evaluation Module

ABSTRACT

This user's guide describes the characteristics, operation, and use of the ADS8354 evaluation module (EVM) performance demonstration kit (PDK). This kit is an evaluation platform for the ADS8354 device, which is a 16-bit, dual-channel, simultaneous-sampling, 700-kSPS, differential analog input, successive approximation register (SAR) analog-to-digital converter (ADC) that features an easy-to-use serial programming interface (SPI). The ADS8354EVM-PDK eases evaluation with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials (BOM). Throughout this document, the terms *evaluation board*, *evaluation module*, and *EVM* are synonymous with the ADS8354EVM-PDK.



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1 Overview

The ADS8354EVM-PDK evaluation kit includes the ADS8354EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over the USB for data capture and analysis.

The ADS8354EVM board includes the ADS8354 SAR ADC, all the peripheral analog circuits, and the components required to achieve optimum performance from the ADC.

The PHI controller board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS8354 device
- Supplies power to all active circuitry on the ADS8354EVM board

Along with the ADS8354EVM and PHI controller board, this evaluation kit includes an A-to-micro-B USB cable to connect to a computer.

1.1 ADS8354EVM-PDK Features

The ADS8354EVM-PDK showcases the following features:

- Hardware and software required for diagnostic testing and accurate performance evaluation of the ADS8354 ADC
- USB powered—no external power supply is required
- The PHI controller board provides a convenient communication interface to the ADS8354 ADC over USB 2.0 (or higher) for power delivery and digital input and output
- Easy-to-use evaluation software for Microsoft® Windows® 7, 64-bit operating systems

1.2 ADS8354EVM Features

The ADS8354EVM showcases the following features:

- Onboard low-noise, low-distortion ADC input drivers optimized to meet ADC performance
- Onboard ultra-low noise, low-dropout (LDO) regulators to generate supplies for the operation amplifiers and ADC

1.3 Related Documentation From Texas Instruments

The documents in Table 1-1 provide information regarding Texas Instruments integrated circuits used in the assembly of the ADS8354EVM-PDK. This user's guide is available from the TI web site under literature number SBAU407. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions may be available from the TI web site at www.ti.com, or call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center at (972) 644-5580. When ordering, identify the document by both title and literature number.

Table 1-1. Related Documentation

Device	Literature Number
ADS8354 product data sheet	SBAS556
THS4561 product data sheet	SBOS874
OPA320 product data sheet	SLOS884
TPS7A47-Q1 product data sheet	SBVS118
REF6025 product data sheet	SBOS708
LM7705 product data sheet	SNVS420

2 Analog Interface

The ADS8354 is a low-power, dual-channel, simultaneous-sampling ADC that supports differential analog inputs. The ADS8354EVM uses two THS4561 fully-differential amplifiers to drive the differential ADC channel inputs (AINP_A, AINM_A and AINP_B, AINM_B) and to center the input signal around the required common-mode voltage for the ADS8354. An OPA320 device is used to buffer the selected common-mode voltage (VOCM). The ADS8354EVM is designed for easy interfacing to analog sources. This section describes the front-end driver circuitry details, including jumper configurations for the analog input signal source.

2.1 Connectors for Analog Inputs

The ADS8354EVM has two 16-bit, simultaneous-sampling ADCs. The ADS8354EVM GUI can either be configured for individual ADC data sampling or simultaneous sampling with both ADCs. The ADS8354EVM is designed to interface to an external, analog source through either subminiature version A (SMA) connectors or 100-mil headers. Jumpers J1, J2, J3, and J4 are the SMA connectors that allow for analog signal source connectivity through coaxial cables. Alternatively, 100-mil jumper cables or mini-grabbers can be used to connect analog sources to pin 1 of connectors JP1, JP2, JP3, and JP4. Table 2-1 lists the analog input connectors for the individual ADCs.

Table 2-1. Analog Input Connector Description

Pin Number	Signal	Description
J1 and J2	AINM_A, AINP_A	Analog inputs provided at the SMA for ADC A
JP2[1] and JP3[1]	AINM_A, AINP_A	Alternate location to provide the analog inputs for ADC A
J3 and J4	AINM_B, AINP_B	Analog inputs provided at the SMA for ADC B
JP1[1] and JP4[1]	AINM_B, AINP_B	Alternate location to provide the analog inputs for ADC B

2.2 ADC Input Signal Driver

The SAR ADC inputs terminate in switched-capacitor networks that create large instantaneous current loads when the switches are closed, which effectively makes the ADC inputs dynamically low impedance. The analog inputs of the ADC are therefore driven by an THS4561 used with a gain of 1 V/V configuration to maintain ADC performance with maximum loading at full device throughput of the ADS8354 of 700 kSPS.

2.2.1 Input Signal Path

Figure 2-1 shows the signal path for the analog inputs applied to the ADS8354EVM. Separate THS4561 amplifiers are used with a gain of 1 V/V configuration to drive the individual analog inputs (AINP and AINM) of each ADC. The OPA320 amplifier circuits help drive the common-mode voltage (VOCM) of the THS4561 amplifiers. An RC filter, with values of R_{filt} = 13 Ω, differential C_{filt} = 820 pF, and common-mode C_{filt} = 10 pF, was selected to achieve a SINAD greater than 88 dB and a THD less than –97 dB for a 2-kHz sine-wave input at full throughput of the ADS8354 of 700 kSPS.

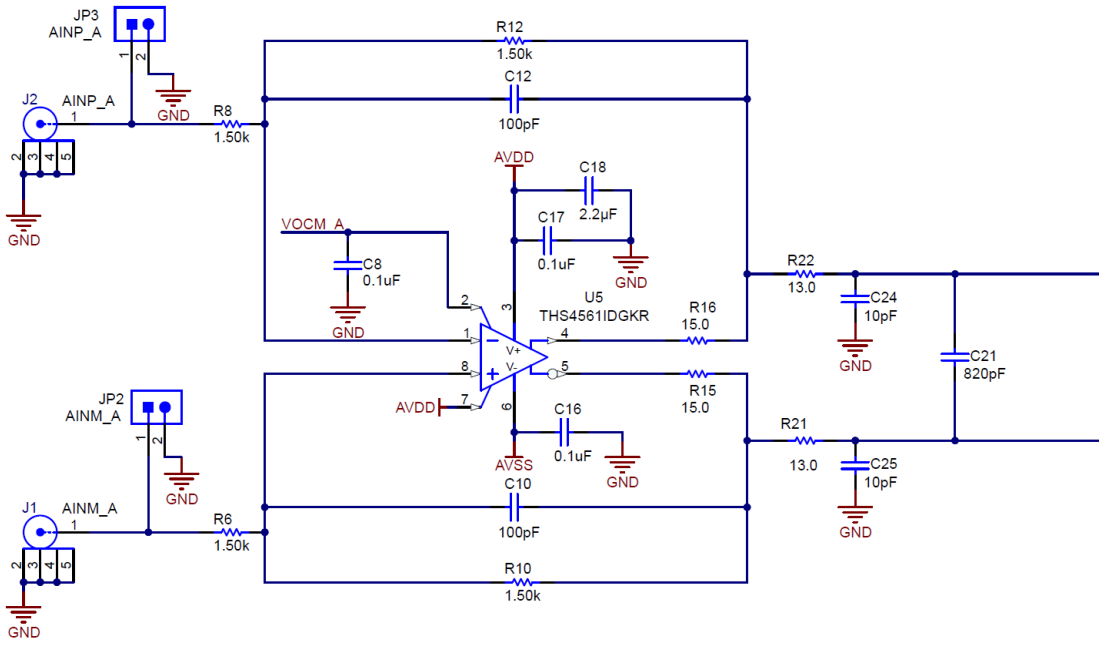


Figure 2-1. ADS8354EVM Analog Input Path

As shown in Figure 2-2, the ADS8354EVM offers two options to provide the output common-mode voltage (VOCM) of the THS4561 amplifiers. By default, JP7 and JP8 are left open and JP5 and JP6 are installed. This configuration selects the ADS8354 internal reference voltage (REFIO_A and REFIO_B) and divides the output by 2 to use REFIO_y / 2 as VOCM (y = A or B), which is required for the default input range of ±VREF. When using the 2xVREF input range, uninstall the jumpers on JP5 and JP6 such that VOCM = REFIO_y.

Alternatively, the REF6025 (U1) can be used in place of the REFIO_A, REFIO_B voltage to serve as the ADC reference and to set the VOCM voltage. Disable the internal reference voltage on the ADS8354 by setting the REF_SEL bit in the CFG register to 0b (external reference) and install jumpers on JP7 and JP8.

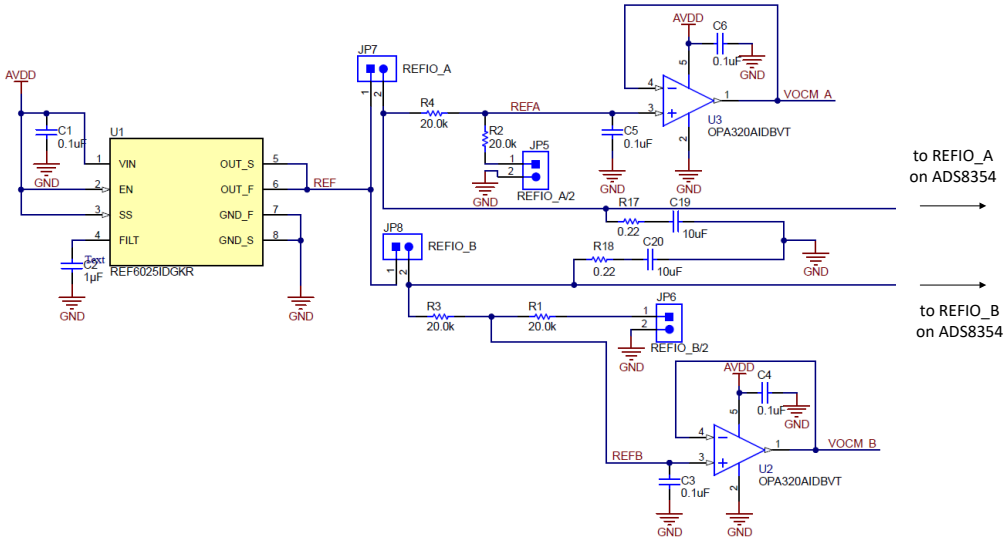


Figure 2-2. ADS8354EVM Common-Mode Voltage Buffer Circuit

3 Digital Interfaces

As discussed in Section 1, the ADS8354EVM interfaces with the PHI, which in turn communicates with the computer over the USB. The PHI also communicates with the EEPROM over the I^2C interface. The electrically erasable programmable read-only memory (EEPROM) comes preprogrammed with the information required to configure and initialize the ADS8354EVM-PDK platform. When the hardware is initialized, the EEPROM is no longer used.

3.1 SPI for the ADC Digital I/O

The ADS8354EVM-PDK supports the interface and ADC input modes detailed in the ADS8354 data sheet. The PHI is capable of operating at a 3.3-V logic level and is directly connected to the digital I/O lines of the ADC.

As shown in Figure 3-1, a debug header (J5) with the digital I/O lines is included on the ADS8354EVM. This header can facilitate connections to logic analyzer probes, oscilloscope probes, or external controllers.

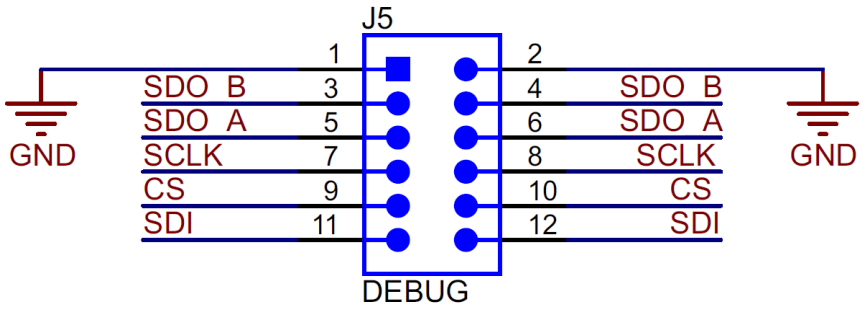


Figure 3-1. ADS8354EVM Debug Header

4 Power Supplies

AVDD operates from 4.5 V to 5.5 V. DVDD operates from 1.65 V to 5.5 V, independent of the AVDD supply. The analog portion of the ADS8354EVM operates from a 5-V supply (VA) generated using the TPS7A47-Q1 low-noise, low-dropout regulator. The same supply is used to power the positive supply of the THS4561 front-end driver amplifiers, and the negative –232-mV supply (AVSS) is generated using the LM7705 low-noise negative bias generator. AVSS can also be set to GND by shorting pins 2 and 3 of JP9.

The TPS7A47-Q1 regulator can be configured to generate a VA supply other than 5 V through programmable pin settings. For more information, see the *Detailed Description* section of the TPS7A47-Q1 device data sheet.

The digital portion of the ADC operates from a 3.3-DVDD supply from the PHI.

4.1 ADC Input Driver Configuration

The ADS8354 only supports fully differential inputs. The ADS8354EVM allows the user to apply a fully-differential signal on the SMA or jumpers mentioned in the input signal path, as discussed in Section 2.2.1. A provision for a single-ended to differential conversion exists by populating JP1 or JP2 and applying a single-ended signal on the unpopulated jumper. The THS4561 common-mode voltage (VOCM) is set by the REF56025. REFIO / 2 can be used for VOCM by populating JP5 for ADCA and JP6 for ADCB. For various analog input full-scale ranges supported by the ADS8354 in fully-differential mode, see the ADS8354 data sheet. Table 4-1 shows the jumper configurations required for single-ended and fully differential analog inputs.

Table 4-1. Jumper Settings for ADC Input Driver Configuration

ADC Input Type	ADC Input Full-Scale Range	Required Jumper Settings	Description
Single-ended analog inputs	$\pm V_{REF}$	JP3, JP4 = Open	Apply single-ended input at J2, J4 or JP3[1], JP4[1]
		JP1, JP2 = Closed	Ground unused inputs
		JP5, JP6 = Closed	Sets VOCM as V_{REF} / 2
	$\pm 2 \times V_{REF}$	JP3, JP4 = Open	Apply single-ended input at J2, J4 or JP3[1], JP4[1]
		JP1, JP2 = Closed	Ground unused inputs
		JP5, JP6 = Open	Sets VOCM as V_{REF}
Fully differential analog inputs	$\pm V_{REF}$	JP1, JP2, JP3, JP4 = Open	Apply differential input signals to J1, J2, J3, J4 or JP1[1], JP2[1], JP3[1], JP4[1]
		J5, J6 = Closed	Sets VOCM as V_{REF} / 2
	$\pm 2 \times V_{REF}$	JP1, JP2, JP3, JP4 = Open	Apply differential input signals to J1, J2, J3, J4 or JP1[1], JP2[1], JP3[1], JP4[1]
		JP5, JP6 = Open	Sets VOCM as V_{REF}

4.2 ADC Voltage Reference Configuration

The ADS8354 has a low-noise, low-drift, 2.5-V internal voltage reference. By default, the ADS8354EVM is configured to work with the ADC internal reference voltage of 2.5 V. The same reference voltage is brought on pin 2 of jumpers JP7 and JP8 that can be used to drive the THS4561 common-mode voltage (VOCM) pin.

There is also a provision for using an external voltage reference for the ADC. The external reference voltage can be generated by populating JP7 and JP8 jumpers. When using an external reference, the ADS8354 internal voltage reference must be disabled and the device must be programmed to accept the external reference voltage on the REFIO_x pins.

5 ADS8354EVM-PDK Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for proper operation of the ADS8354EVM-PDK.

5.1 Default Jumper Settings

Figure 5-1 shows the silkscreen plot, which details the jumper locations for the ADS8354EVM-PDK.

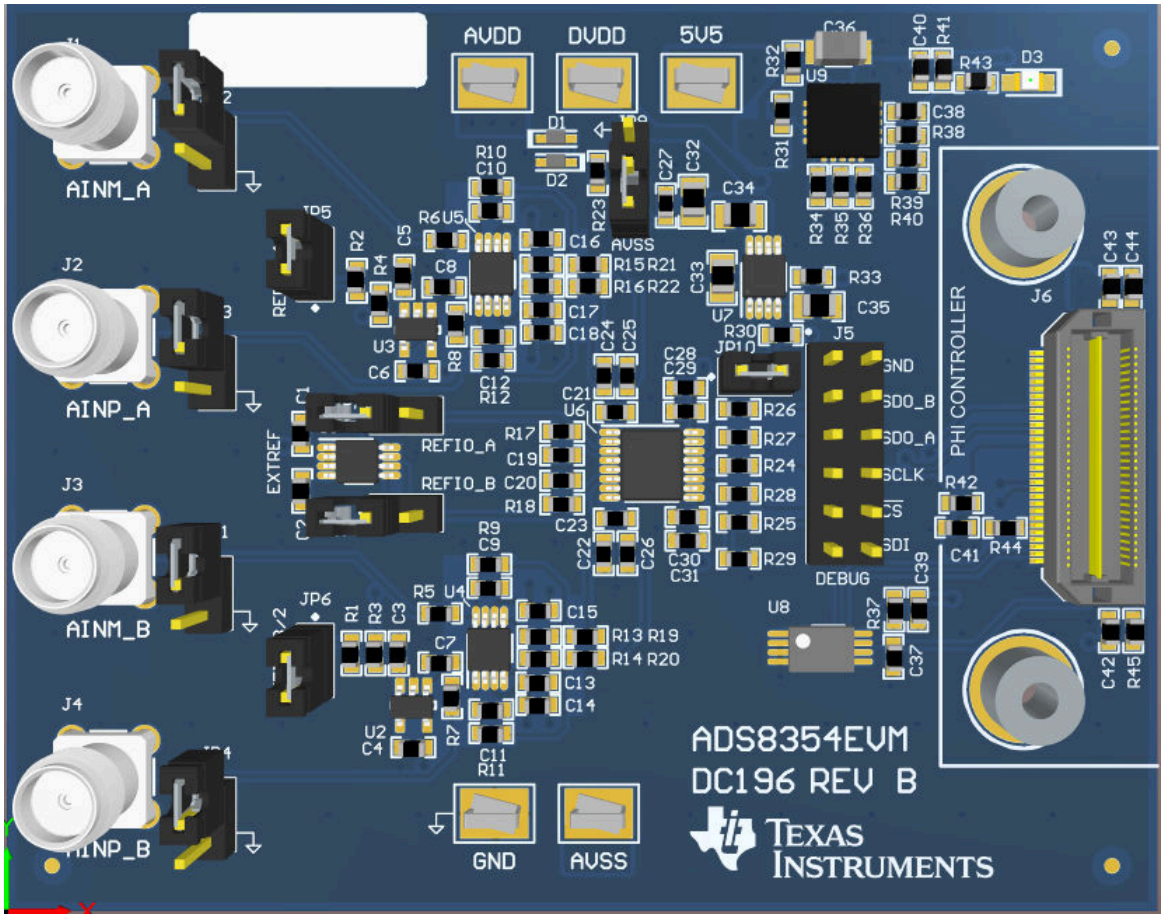


Figure 5-1. ADS8354EVM-PDK Jumper Locations

Table 5-1 lists the functionality and default configuration of each jumper.

Table 5-1. Default Jumper Configurations

Reference Designator	Default Configuration	Description
JP1, JP2, JP3, JP4	Open	Use pin 1 of these jumpers as an alternate location to provide the analog input to ADC A and ADC B of the ADS8354.
JP5, JP6	Closed	Jumpers to feed either V_{REF} or V_{REF} / 2 to the OPA320 input driving the THS4561 common-mode voltage (VOCM) pin. See Section 7.3 for more details.
JP7, JP8	Open	Short these pins to use the REF6025 external reference voltage. See Section 4.2 for more details.
JP9	Closed [1-2]	By default, AVSS (negative supply rail of the THS4561) is set to a –232-mV supply generated by the LM7705. Shorting JP9[2-3] sets AVSS to GND.
JP10	Closed	Jumpers to feed either GND or 5.5 V to the shutdown (SD) pin of the LM7705. By default, GND is used to keep the SD pin low, so the LM7705 device is on. See the LM7705 data sheet for more details.

5.2 EVM Graphical User Interface Software Installation

The following steps describe how to install the software for the ADS8354EVM graphical user interface (GUI).

1. Download the latest version of the ADS835xEVM GUI installer from the *Order & start development* section of the ADS8354EVM-PDK Tool Folder, and run the GUI installer to install the EVM GUI software on your computer.

> **CAUTION**
>
> Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Failure to disable antivirus software, depending on the antivirus settings, may cause an error message to appear or the *installer.exe* file may be deleted.

2. Accept the license agreements (Figure 5-2) and follow the on-screen instructions to complete the installation.

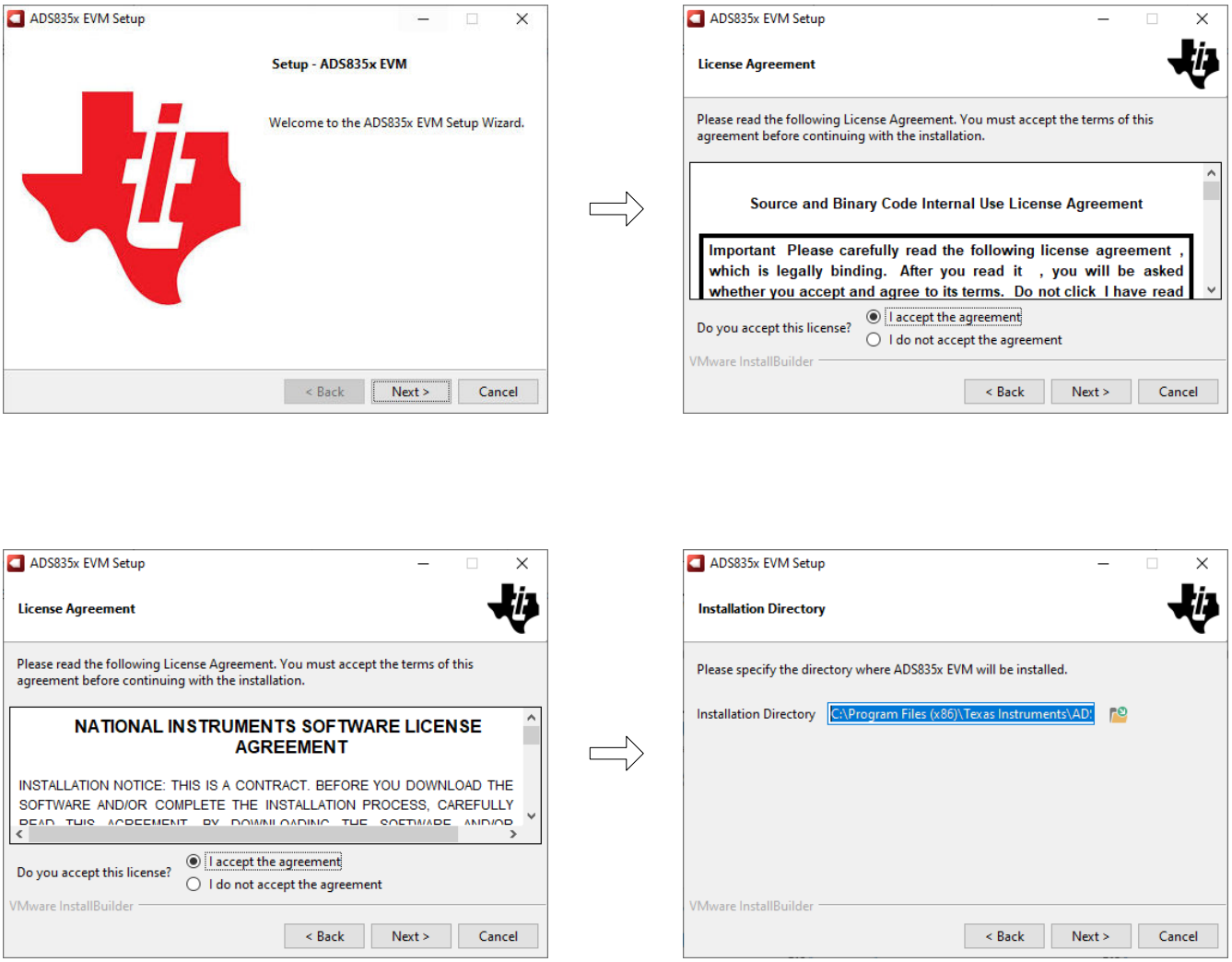


Figure 5-2. ADS835xEVM Software Installation Prompts

3. As a part of the ADS835xEVM GUI installation, a prompt with a *Device Driver Installation Wizard* (Figure 5-3) appears on the screen. Click the **Next** button to proceed, then click the **Finish** button when the installation is complete.

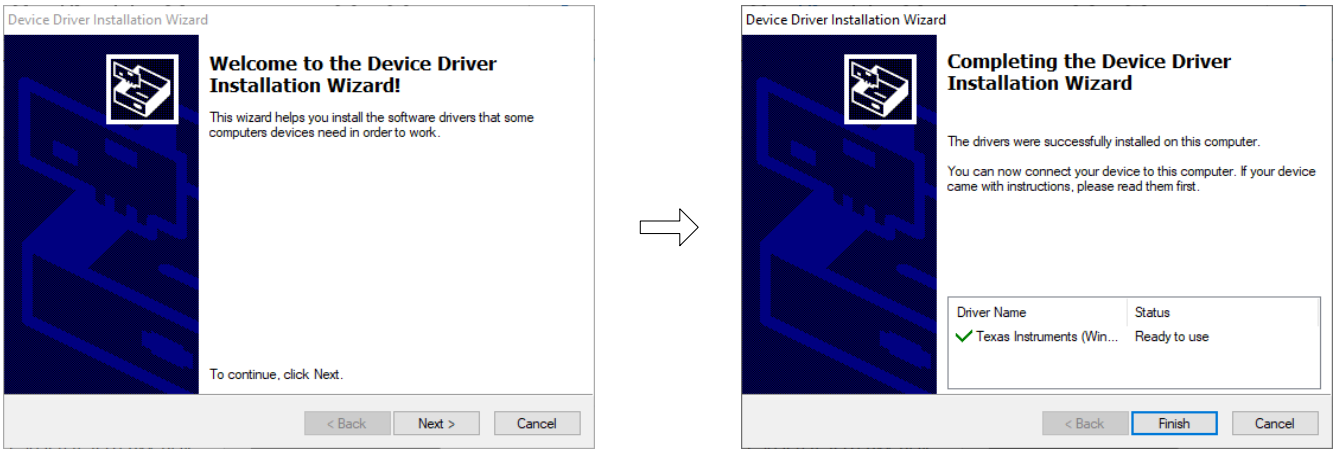


Figure 5-3. Device Driver Installation Wizard Prompts

Note

A notice may appear on the screen stating that Windows cannot verify the publisher of this driver software. Select the *Install this driver software anyway* option.

The device requires the LabVIEW™ run-time engine (see Figure 5-4) and may prompt for the installation of this software, if not already installed.

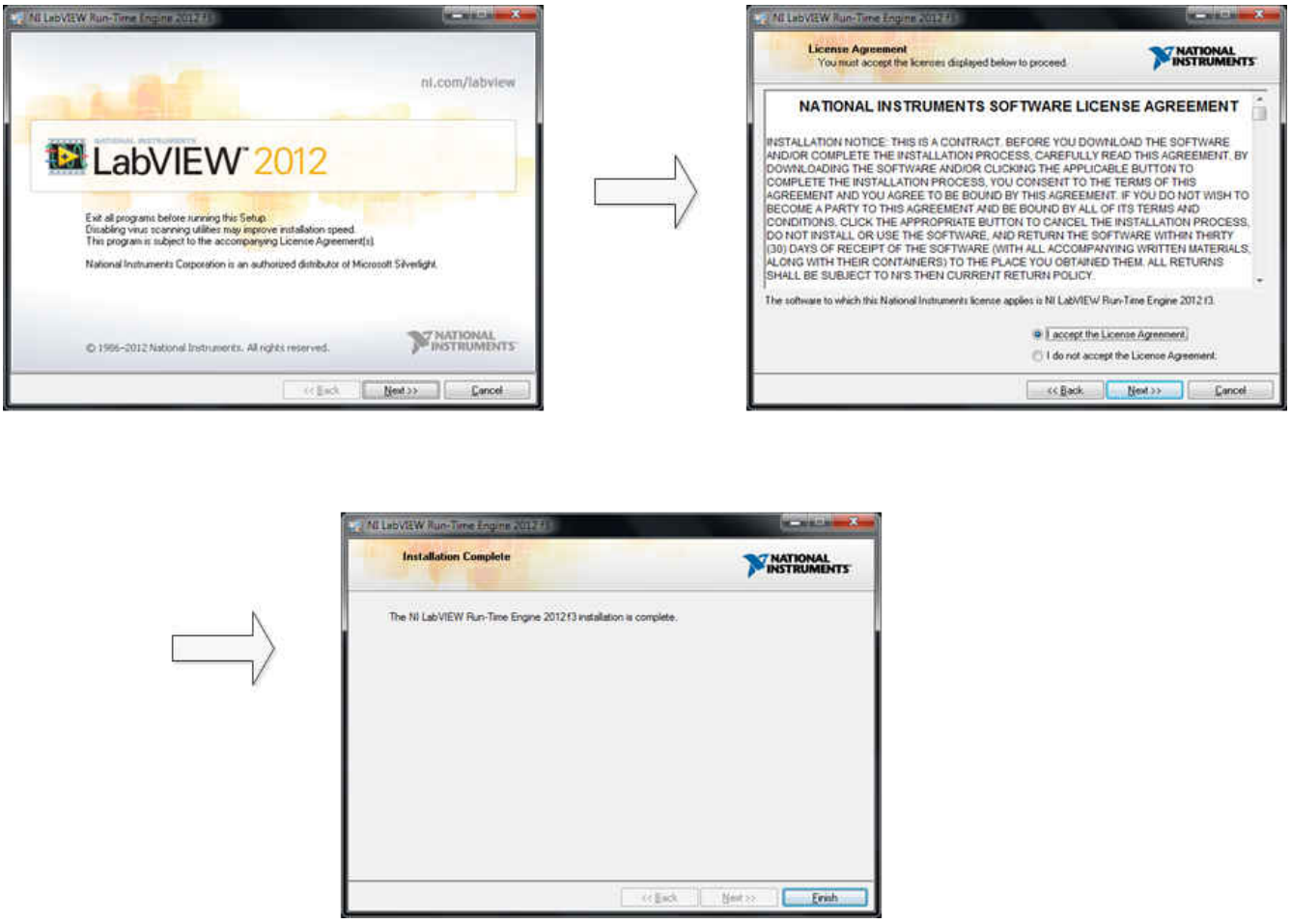


Figure 5-4. LabVIEW Run-Time Engine Installation

4. Check the *Create Desktop Shortcut* box, as Figure 5-5 shows, after these installations.

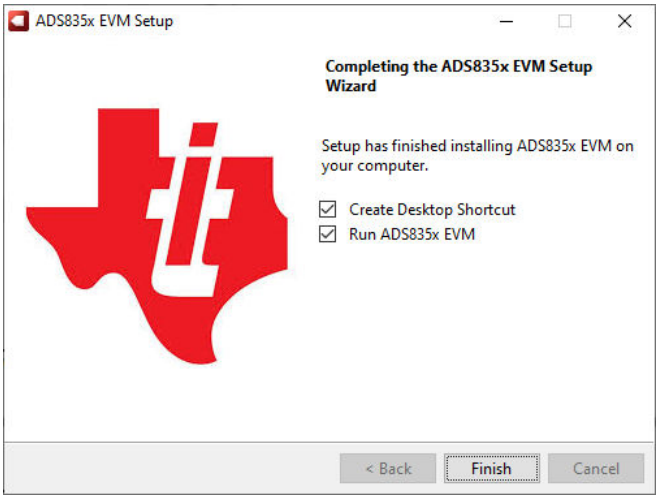


Figure 5-5. ADS8354EVM-PDK Installation Final Step

6 ADS8354EVM-PDK Operation

The following instructions are a step-by-step guide for connecting the device to a computer and evaluating the performance of the device.

1. Connect the device EVM to the PHI board. Figure 6-1 indicates where the screws are to be installed.
2. Use the provided USB cable to connect the PHI to the computer.
   - LED D5 on the PHI lights up, indicating that the PHI is powered up.
   - LEDs D1 and D2 on the PHI start flashing, indicating that the PHI is booted up and communicating with the PC.

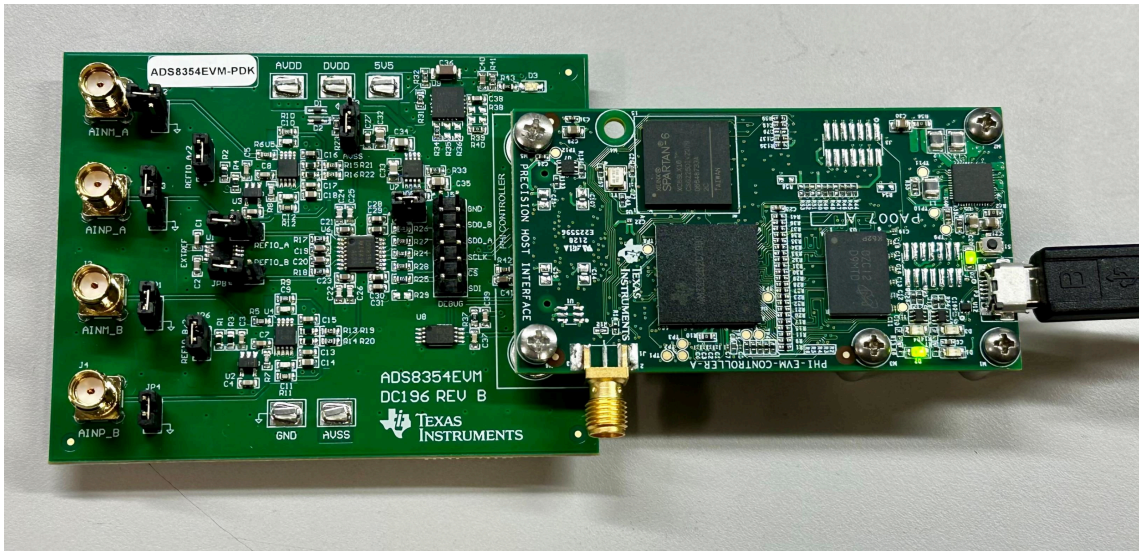


Figure 6-1. EVM-PDK Hardware Setup and LED Indicators

3. Launch the device EVM GUI software from the installed path, as Figure 6-2 shows, or by using the desktop shortcut created during installation.

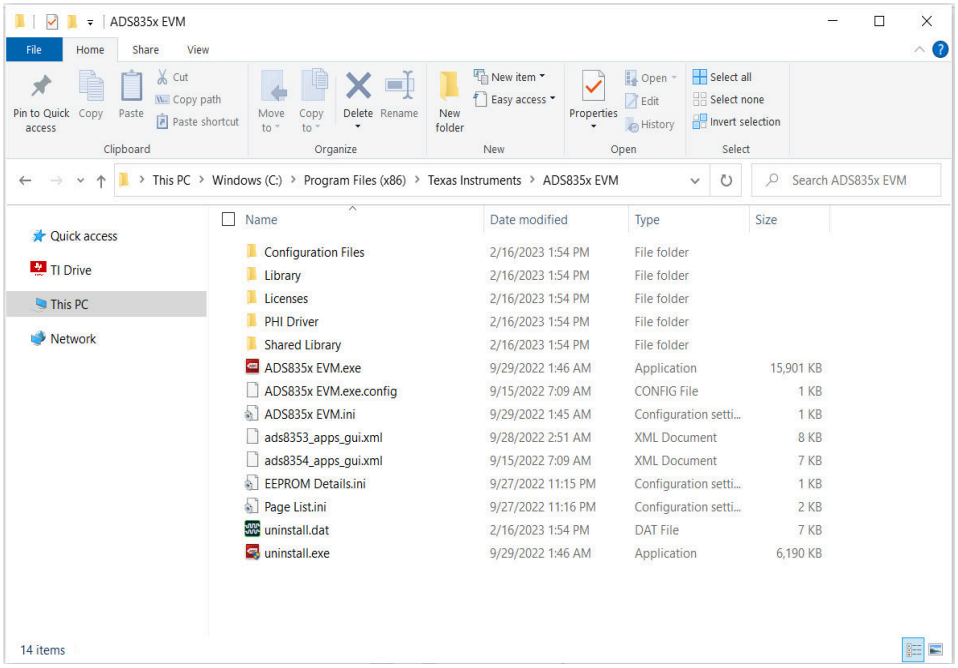


Figure 6-2. Launch the EVM GUI Software

6.1 EVM GUI Global Settings for ADC Control

Figure 6-3 shows the input parameters of the GUI (and the default values), through which the various functions of the ADS8354EVM-PDK can be exercised. These settings are global and persist across the GUI tools listed in the top left pane (or from one page to another).

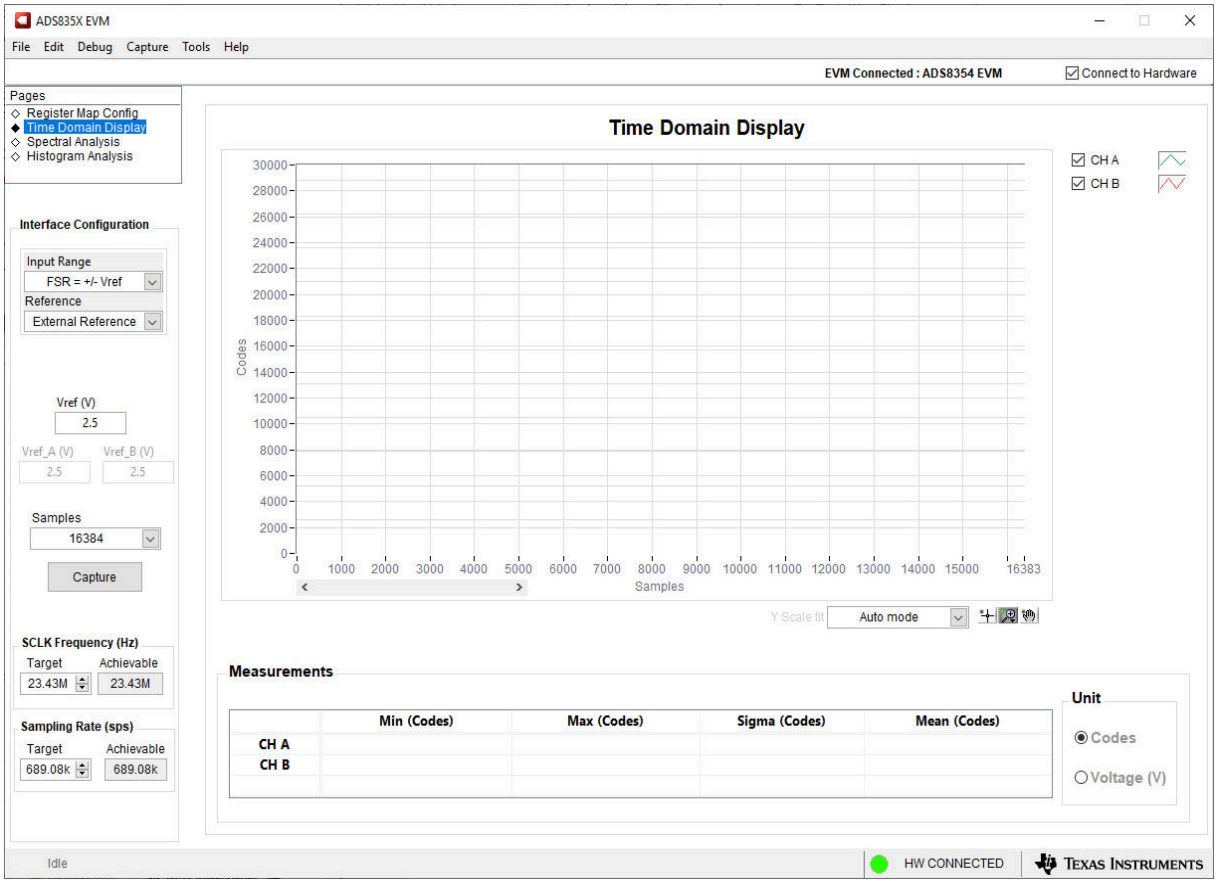


Figure 6-3. EVM GUI Global Input Parameters

The ADS8354 interface configurations can be selected on this page. The GUI lets the user select the ADC input range, ADC INM input configuration, ADC voltage reference, and ADC data format using a drop-down menu.

The *SCLK Frequency* and *Sampling Rate* are selected on this page. The GUI lets the user enter the target values for these two parameters, and the GUI computes the closest value that can be achieved, considering the timing constraints of the device.

Select either one of the ADCs or both of the ADCs if they are configured in the simultaneous-sampling scheme described in Section 2.1 by clicking on the drop-down menu titled *Channel Modes*. Specify a target SCLK frequency (Hz) and the GUI tries to match this frequency as closely as possible by changing the PHI PLL settings; however, the achievable frequency can differ from the target value entered. Similarly, the sampling rate of the ADC can be adjusted by modifying the *Target Sampling Rate* argument (Hz). The achievable ADC sampling rate can differ from the target value, depending on the applied SCLK frequency and the closest match achievable is displayed. This page, therefore, allows various settings available on the device to be tested in a repetitive fashion until arriving at the best settings for the corresponding test scenario.

6.2 Time Domain Display Tool

The *Time Domain Display* tool provides a visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or front-end drive circuits.

As per the selected interface mode settings using the **Capture** button indicated in Figure 6-4, the user can trigger a data capture of the selected number of samples from the ADS8354EVM-PDK. The sample indices are on the x-axis, and two y-axes show the corresponding output codes and the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the analysis tools described in the subsequent sections triggers calculations to be performed on the same set of data.

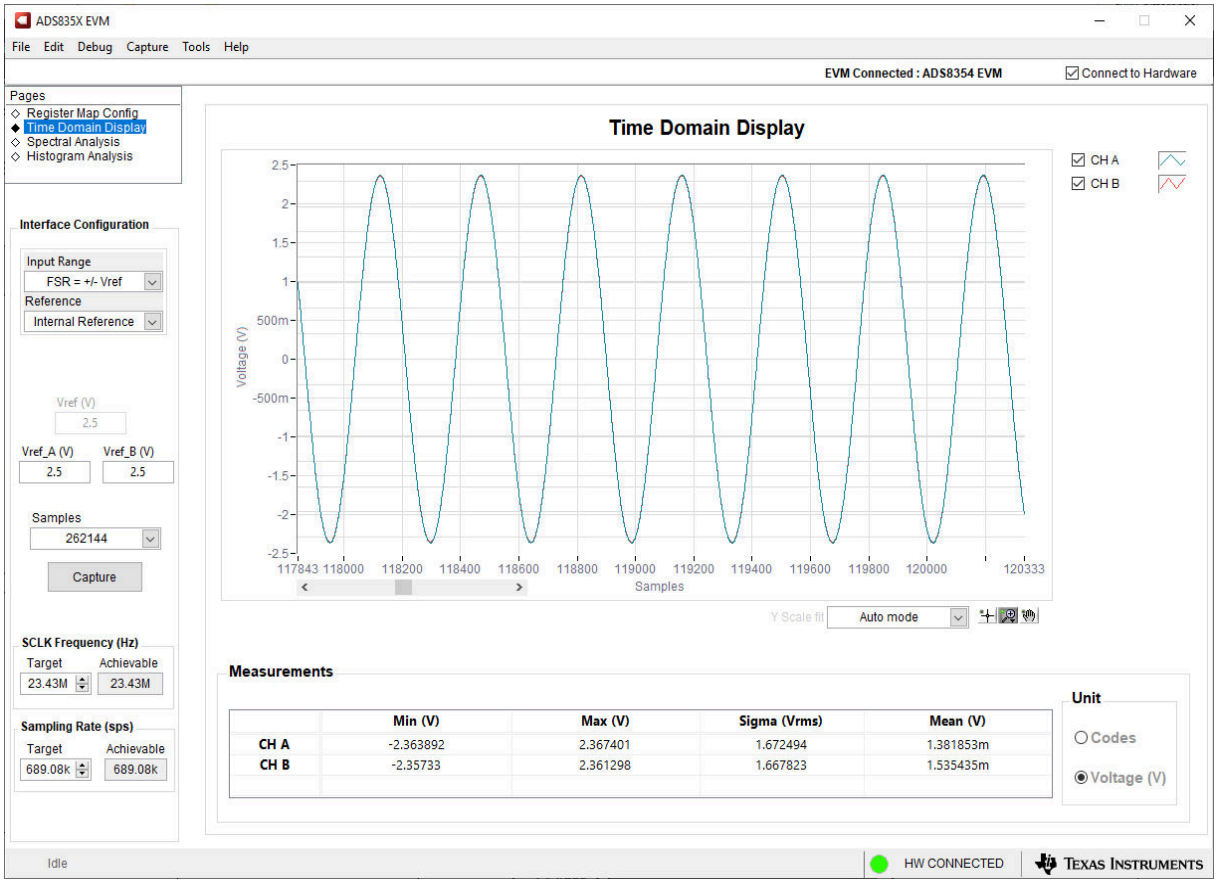


Figure 6-4. Time Domain Display Tool Options

Both channel A and channel B waveforms are displayed in Figure 6-4. These channels are identical and overlapped.

6.3 Spectral Analysis Tool

The *Spectral Analysis* tool (Figure 6-5) is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS8354 SAR ADC through the use of a single-tone, sinusoidal signal FFT analysis, using the 7-term Blackman-Harris window setting. Alternatively, the window setting of *None* can be used to search for noise spurs over frequency in DC inputs.

For dynamic performance evaluation, the external, fully differential source must have better specifications than the ADC to make sure that the measured system performance is not limited by the performance of the signal source. Therefore, the external reference source must meet the source requirements listed in Table 6-1. Alternately, the user can use the precision signal injector EVM that provides a low-distortion, low-noise, 2-kHz input signal for driving the input of the ADC, and pairs with most of the TI SAR ADC evaluation modules (EVMs). The board is powered over a USB, which also provides a user-interface connection to a PC.

Table 6-1. External Source Requirements for Device Evaluation (SNR and THD)

Specification Description	Specification Value
Signal frequency	2 kHz
External source type	Fully differential
External source common-mode	0 V
Minimum SNR	90 dB
Minimum THD	–115 dB

Figure 6-5. Spectral Analysis Tool

6.4 Histogram Analysis Tool

The *Histogram Analysis* tool can be used to estimate the effective resolution of the ADC resulting from performance degradation caused by noise. Effective resolution is an indicator of the number of bits of ADC measurement resolution resulting from performance losses caused by noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output (from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC) is reflected in the standard deviation of the ADC output code histogram obtained by performing multiple conversions of a DC input applied to a given channel.

The histogram corresponding to a DC input is displayed by clicking the **Capture** button. The example capture shown in Figure 6-6 is captured with the EVM configured by remove jumpers from pin 1 and 2 of jumper JP5 and JP6, shorting pin [1-2] of JP1, JP2, JP3, and JP4 using 100-mil jumpers.

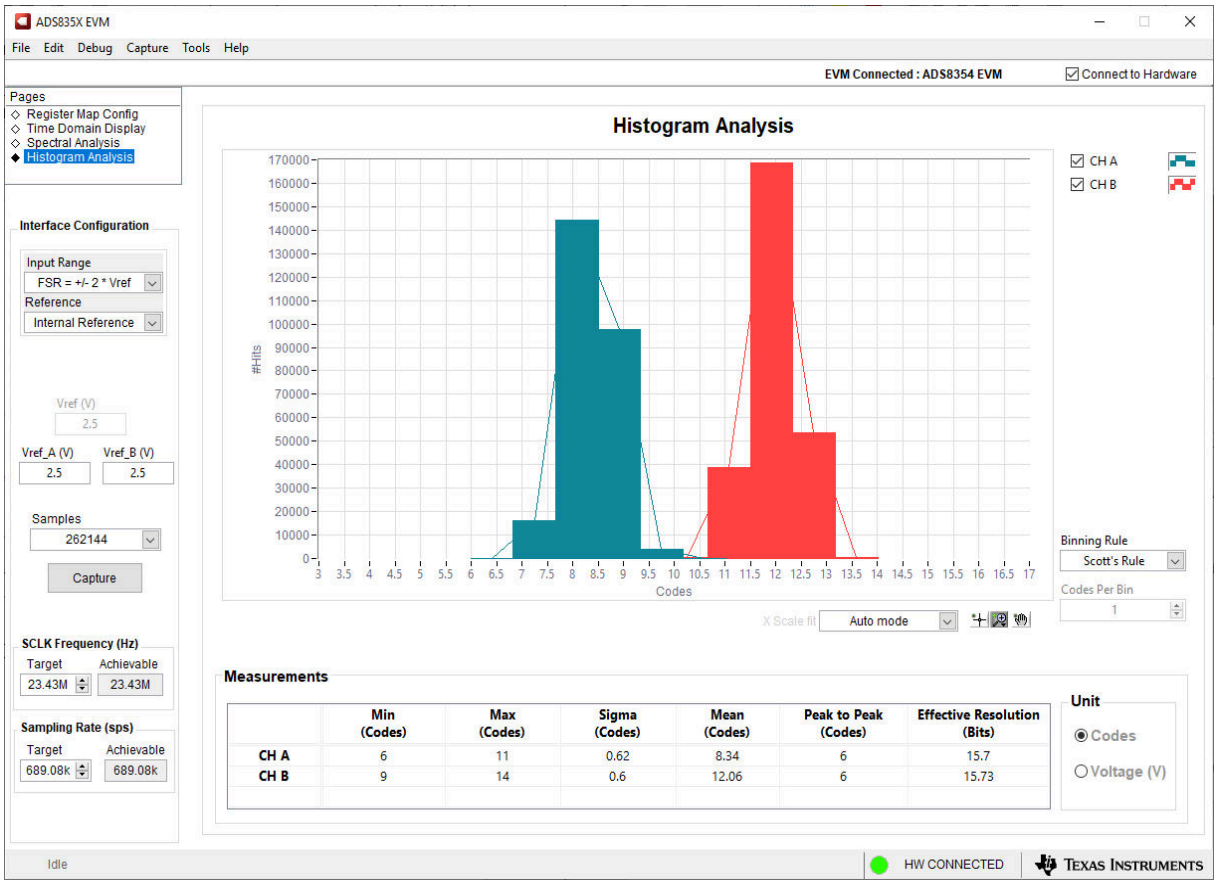


Figure 6-6. Histogram Analysis Tool

7 Bill of Materials, Printed-Circuit Board Layout, and Schematics

This section contains the ADS8354EVM bill of materials (BOM), printed-circuit board (PCB) layout, and schematics.

7.1 Bill of Materials

Table 7-1 lists the ADS8354EVM BOM.

Table 7-1. ADS8354EVM Bill of Materials

Manufacturer Part Number	Quantity	Reference Designators	Manufacturer	Description
DC196	1	PCB		Printed Circuit Board
0603YC104JAT2A	15	C1, C3, C4, C5, C6, C7, C8, C13, C15, C16, C17, C28, C31, C37, C39	KYOCERA AVX	CAP, CERM, 0.1 uF, 16 V, +/- 5%, X7R, 0603
06033C105KAT2A	1	C2	KYOCERA AVX	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603
C0603C101J5GACTU	4	C9, C10, C11, C12	KEMET	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603
EMK107BB7225MA-T	2	C14, C18	Taiyo Yuden	CAP, CERM, 2.2 uF, 16 V,+/- 10%, X7R, 0603
C1608X5R1E106M080AC	6	C19, C20, C40, C41, C42, C44	TDK Corporation	CAP, CERM, 10 uF, 25 V, +/- 20%, X5R, 0603
GRM1885C1H821JA01D	2	C21, C23	KEMET	CAP, CERM, 820 pF, 50 V, +/- 5%, C0G/NP0, 0603
C0603C100F5GAC7867	4	C22, C24, C25, C26	KEMET	CAP, CERM, 10 pF, 50 V, +/- 1%, C0G/NP0, 0603
GRM188R61C474KA93D	1	C27	KEMET	CAP, CERM, 0.47 uF, 16 V, +/- 10%, X5R, 0603
CGA3E1X7R1E105K080AD	3	C29, C30, C38	TDK Corporation	CAP, CERM, 1 µF, 25 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603
CL21A226KOQNNNE	1	C32	Samsung Electro-Mechanics	CAP, CERM, 22 µF, 16 V,+/- 10%, X5R, 0805
CL21A475KOFNNNE	2	C33, C34	Samsung Electro-Mechanics	CAP, CERM, 4.7 µF, 16 V,+/- 10%, X5R, 0805
CL21B106KOQNNNE	1	C35	Samsung Electro-Mechanics	CAP, CERM, 10 uF, 16 V, +/- 10%, X7R, 0805
C3216X5R1E476M160AC	1	C36	TDK Corporation	CAP, CERM, 47 uF, 25 V, +/- 20%, X5R, 1206_190
GRM1885C1H102FA01J	1	C43	Murata Electronics	CAP, CERM, 1000 pF, 50 V, +/- 1%, C0G/NP0, 0603
1N4148WT	2	D1, D2	Yangzhou Yangjie Electronic Technology Co.,Ltd	Diode, Switching, 75 V, 0.3 A, SOD-523F
APT2012LZGCK	1	D3	Kingbright	LED, Green, SMD
9774050360R	2	H1, H2	Würth Elektronik	ROUND STANDOFF M3 STEEL 5MM
SJ-5303 (CLEAR)	4	H3, H4, H5, H6	3M	Bumpon, Hemisphere, 0.44 X 0.20, Clear
RM3X4MM 2701	2	H10, H11	APM Hexseal	Machine Screw Pan PHILLIPS M3
5-1814832-2	4	J1, J2, J3, J4	TE Connectivity AMP Connectors	SMA Straight PCB Socket Die Cast, 50 Ohm, TH
TSW-106-07-G-D	1	J5	Samtec Inc.	Header, 100mil, 6x2, Gold, TH
QTH-030-01-L-D-A	1	J6	Samtec Inc.	Header(Shrouded), 19.7mil, 30x2, Gold, SMT
TSW-102-07-G-S	9	JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP10	Samtec Inc.	Header, 100mil, 2x1, Gold, TH
TSW-103-07-G-S	1	JP9	Samtec Inc.	Header, 100mil, 3x1, Gold, TH
THT-14-423-10	1	LBL1	Brady Corporation	Thermal Transfer Printable Labels, 0.650
RC0603FR-0720KL	4	R1, R2, R3, R4	YAGEO	RES, 20.0 k, 1%, 0.1 W, 0603
RC0603FR-071K5L	8	R5, R6, R7, R8, R9, R10, R11, R12	YAGEO	RES, 1.50 k, 1%, 0.1 W, 0603
CRCW060315R0FKEA	4	R13, R14, R15, R16	Vishay Dale	RES, 15.0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
ERJ-3RQFR22V	2	R17, R18	Panasonic Electronic Components	RES, 0.22, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
RC0603FR-0713RL	4	R19, R20, R21, R22	YAGEO	RES, 13.0, 1%, 0.1 W, 0603
ERJ-3GEY0R00V	2	R23, R41	Panasonic Electronic Components	RES, 0, 5%, 0.1 W, 0603

Table 7-1. ADS8354EVM Bill of Materials (continued)

Manufacturer Part Number	Quantity	Reference Designators	Manufacturer	Description
CRCW060333R0JNEA	6	R24, R25, R26, R27, R28, R42	Vishay Dale	RES, 33, 5%, 0.1 W, AEC-Q200 Grade 0, 0603
RMCF0603FT10K0	3	R30, R37, R43	Stackpole Electronics Inc	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
ERJ-3GEY0R00V	5	R31, R34, R40, R44, R45	Panasonic Electronic Components	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603
ERJ-3RSFR10V	1	R32	Panasonic Electronic Components	RES, 0.1, 1%, 0.1 W, 0603
RMCF0603ZT0R00	1	R33	Stackpole Electronics Inc	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
60900213421	10	SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10	Würth Elektronik	Shunt, 2.54mm, Gold, Black
5016	5	TP1, TP2, TP3, TP4, TP5	Keystone Electronics	Test Point, Compact, SMT
REF6025IDGKR	1	U1	Texas Instruments	5ppm/C High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)
OPA320AIDBVT	2	U2, U3	Texas Instruments	Precision, 20 MHz, 0.9 pA Ib, RRIO, CMOS Operational Amplifier, 1.8 to 5.5 V, -40 to 125 degC, 5-pin SOT23 (DBV5), Green (RoHS & no Sb/Br)
THS4561IDGKR	2	U4, U5	Texas Instruments	Low-Power, High Supply Range, 60-MHz, Fully Differential Amplifier, DGK0008A (VSSOP-8)
ADS8354IPWR	1	U6	Texas Instruments	SAR ADC, Dual, 700 kSPS, 16 Bit, Simultaneous Sampling, PW0016A (TSSOP-16)
LM7705MM/NOPB	1	U7	Texas Instruments	Low Noise Negative Bias Generator, 8-pin Mini SOIC, Pb-Free
BR24G32FVT-3AGE2	1	U8	Rohm Semiconductor	I2C BUS EEPROM (2-Wire), TSSOP-B8
TPS7A4701QRGWRQ1	1	U9	Texas Instruments	Automotive 35V, 1A, 4.2?VRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)

7.2 PCB Layout

Figure 7-1 through Figure 7-4 show the EVM PCB layout.

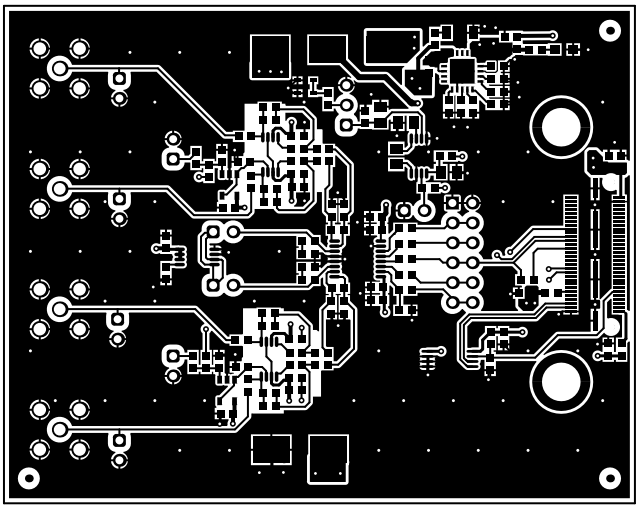


Figure 7-1. ADS8354EVM PCB Layer 1: Top Layer

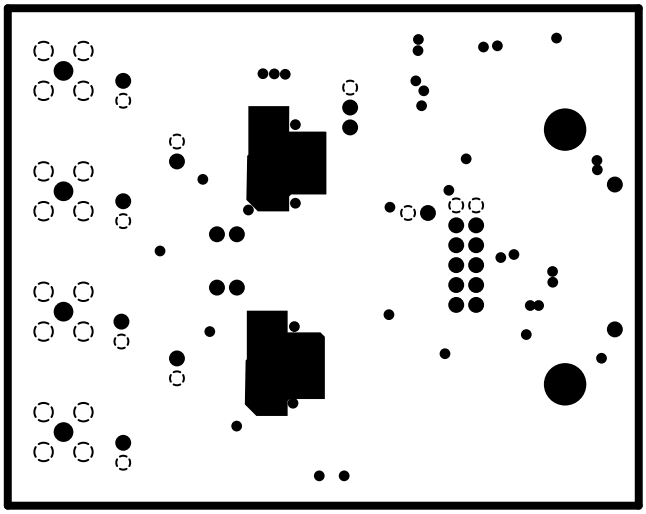


Figure 7-2. ADS8354EVM PCB Layer 2: GND Plane

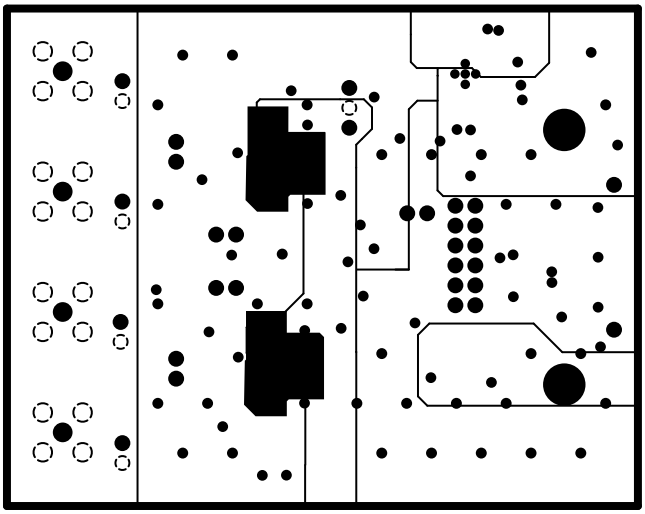


Figure 7-3. ADS8354EVM PCB Layer 3: Power Plane

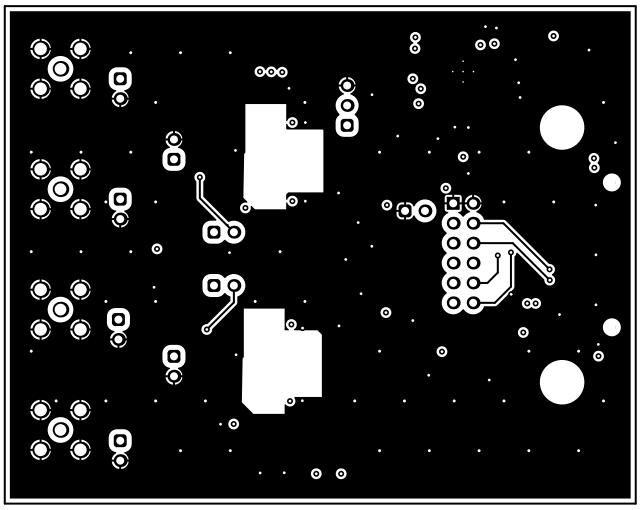


Figure 7-4. ADS8354EVM PCB Layer 4: Bottom Layer

7.3 Schematics

Figure 7-5 through Figure 7-7 illustrate the schematics for the ADS8354EVM-PDK.

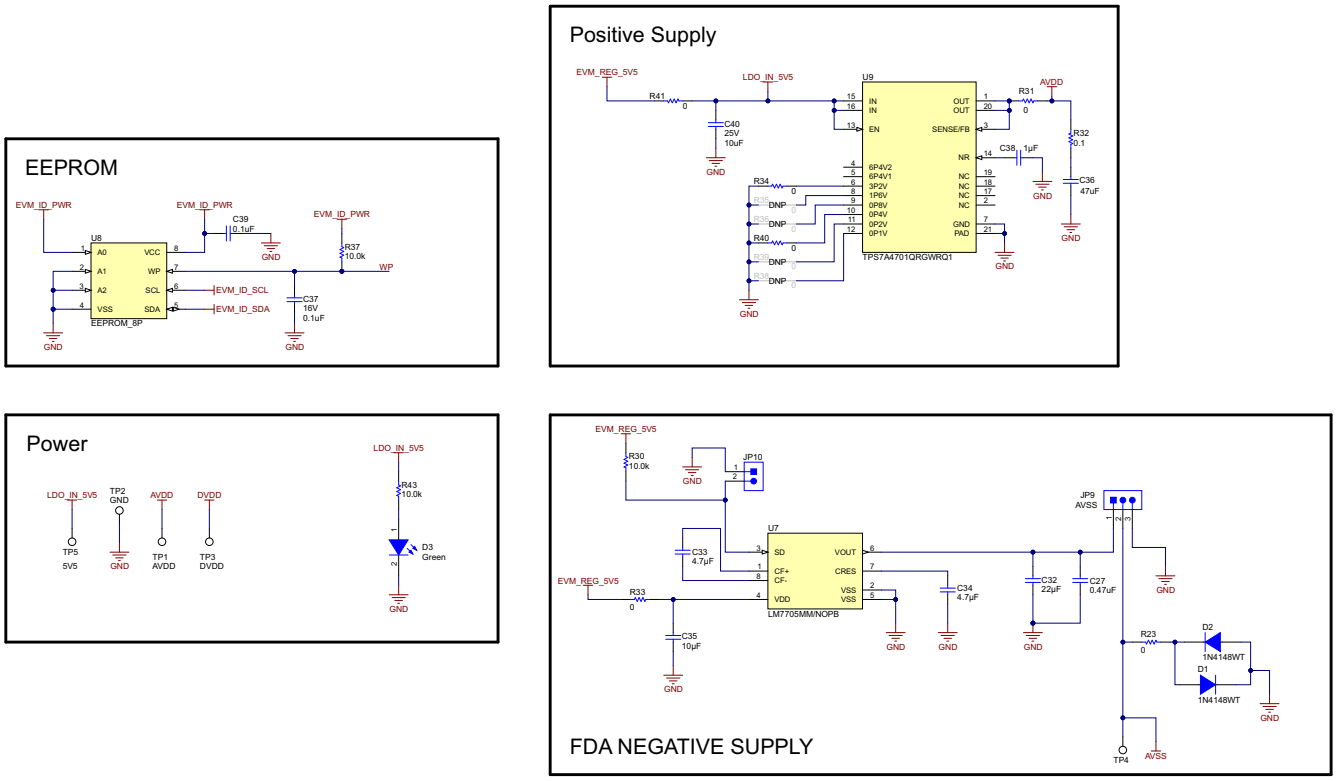


Figure 7-5. Schematic Diagram (Page 1): EEPROM, Power Supplies

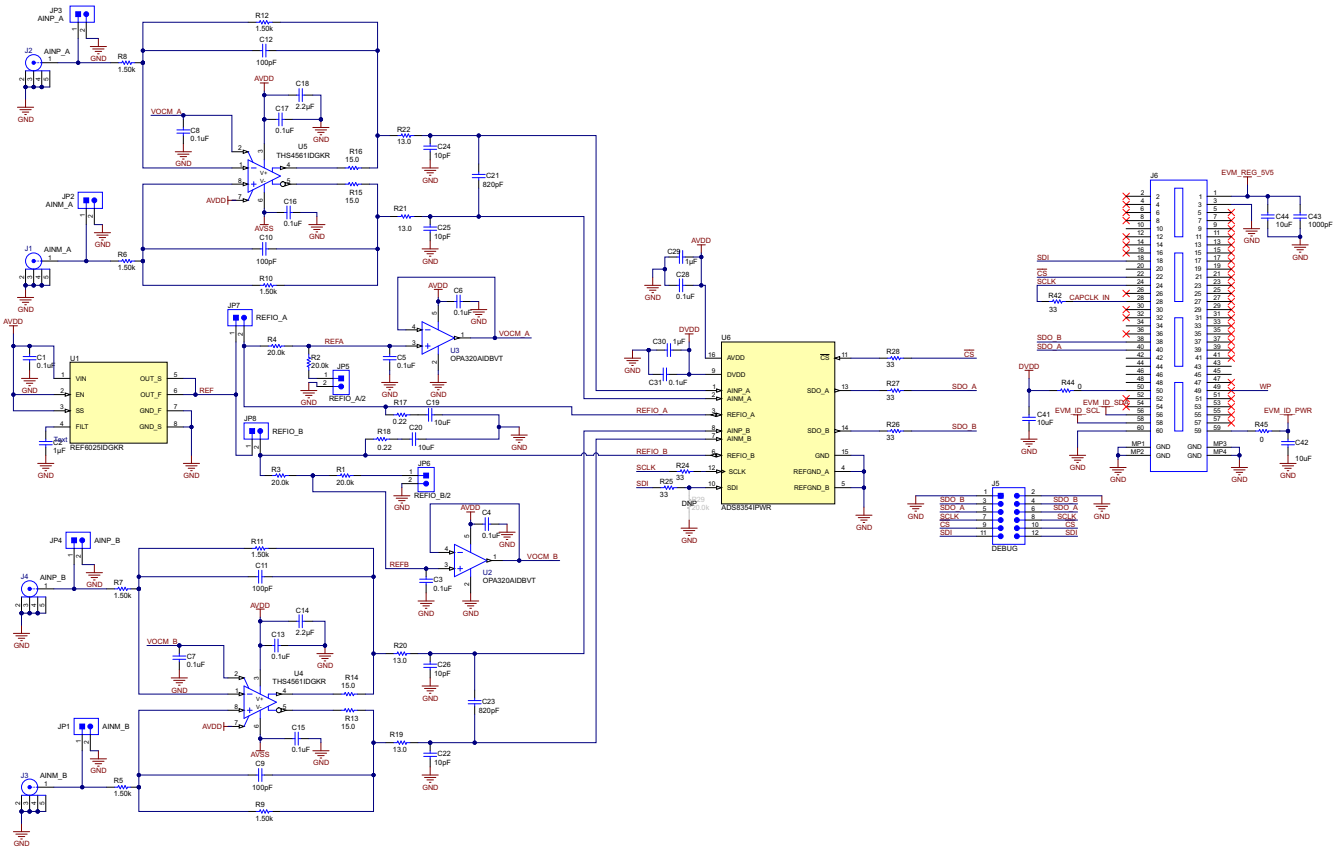
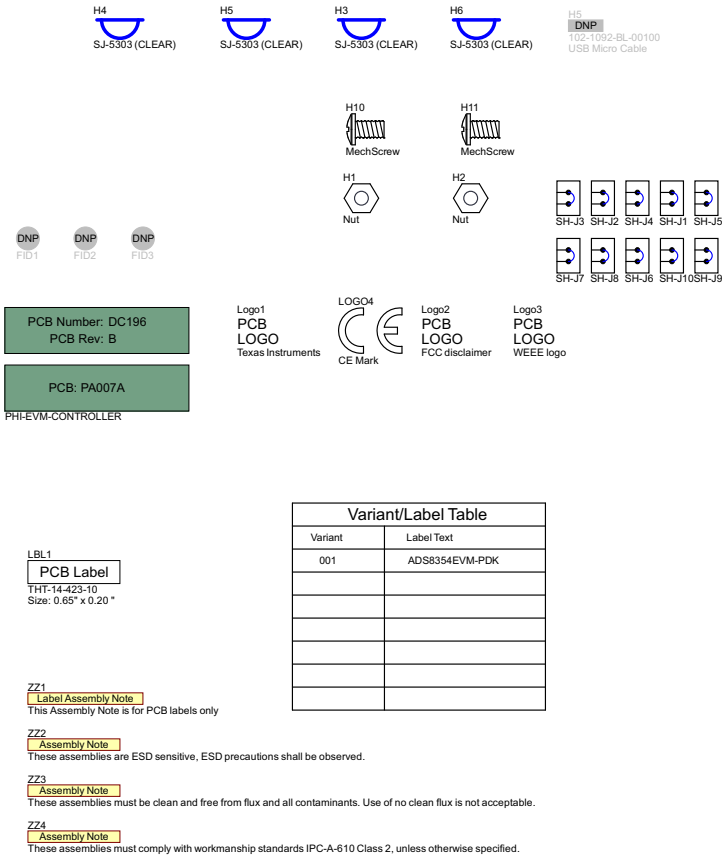


Figure 7-6. Schematic Diagram (Page 2): Analog Inputs, ADC Main, External Reference, PHI Connector



Variant/Label Table	
Variant	Label Text
001	ADS8354EVM-PDK

LBL1
PCB Label
THT-14-423-10
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Figure 7-7. Schematic Diagram (Page 3): Hardware Components

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2 *Limited Warranty and Related Remedies/Disclaimers*:

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   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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西新宿三井ビル

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

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4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

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