EVM User's Guide: ADS9813EVM, ADS9817EVM

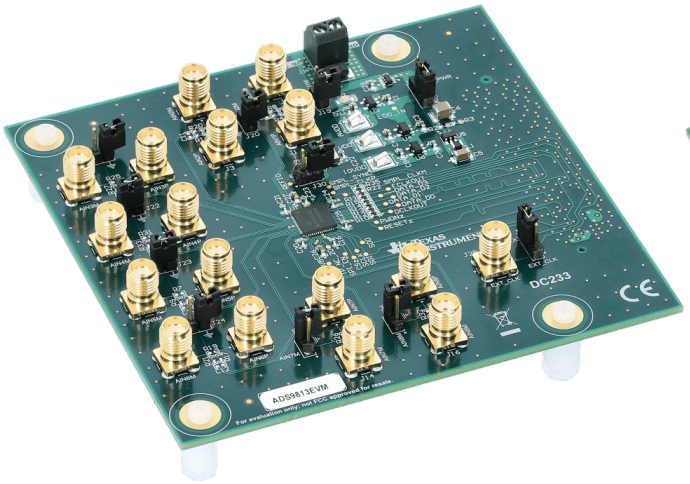
ADS9813 and ADS9817 Evaluation Modules

Description

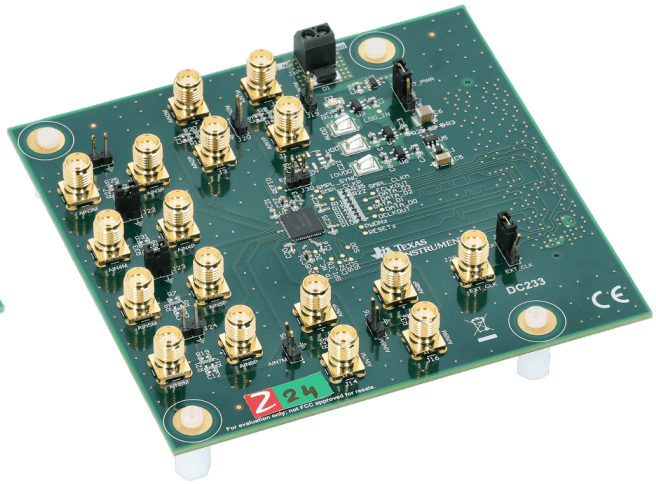
The ADS9813 and ADS9817 evaluation modules (EVM) are platforms for evaluating the performance of the ADS9813 and ADS9817, 8-channel, 18-bit, 2 MSPS/channel SAR ADC with integrated analog front-end and ADC reference. The ADS9817EVM includes a standard FMC connector that can interface with standard FPGA development boards. Computer software that works with the TSWDC155EVM (sold separately) is provided to enable the user to communicate with the ADC over universal serial bus (USB), capture data, and perform data analysis.

Features

- EVM hardware features all required support circuitry for ADS9813, including external sample clock and ADC reference voltage options
- Easy-to-use evaluation software for Windows 10 64-bit operating systems; software suite includes graphical tools for data capture and analysis
- Software for communications is facilitated with TSWDC155EVM data capture card (sold separately)



ADS9813EVM



ADS9817EVM

1 Evaluation Module Overview

1.1 Introduction

This user's guide describes the characteristics, operation, and use of the ADS9813 and the ADS9817 evaluation modules (EVM). These are evaluation platforms for the ADS9813 and ADS9817, respectively. Both devices are 8-channel, 18-bit, 2-MSPS per channel, successive approximation register (SAR) analog-to-digital converters (ADC). The EVMs ease the evaluation of the ADS9813 and ADS9817 devices with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials (BOM). Throughout this document, the terms *demonstration kit*, *evaluation board*, *evaluation module*, *and EVM* are synonymous with the ADS9813EVM and the ADS9817EVM.

1.2 Kit Contents

The ADS9817EVM kit comes with an evaluation module for ADS9817. The ADS9813EVM kit comes with an evaluation module for ADS9813.

The ADS9817EVM/ADS9813EVM may be paired with the TSWDC155EVM (sold separately). The TSWDC155EVM is a digital controller board that is necessary for the included EVM software GUI to communicate with the device, graph measured results, and compute common figures of merit (for example, SNR and THD).

1.3 Specification

The ADS9813EVM and ADS9817EVM both include the following features:

- ADS9813EVM has the hardware required for diagnostic testing and accurate performance evaluation of the ADS9813 ADC.
- ADS9817EVM has the hardware required for diagnostic testing and accurate performance evaluation of the ADS9817 ADC.
- The TSWDC155EVM controller (sold separately) provides all necessary digital I/O signals and power rails required for operating the ADS9813EVM and the ADS9817EVM.
- Easy-to-use evaluation GUI for Microsoft® Windows® 10, 64-bit operating systems requires the TSWDC155EVM (sold separately) for operation.
- The included software suite features graphical tools for data capture, histogram analysis, spectral analysis, and linearity measurements.

Figure 1-2 depicts the connections and basic subsystems of the EVM.

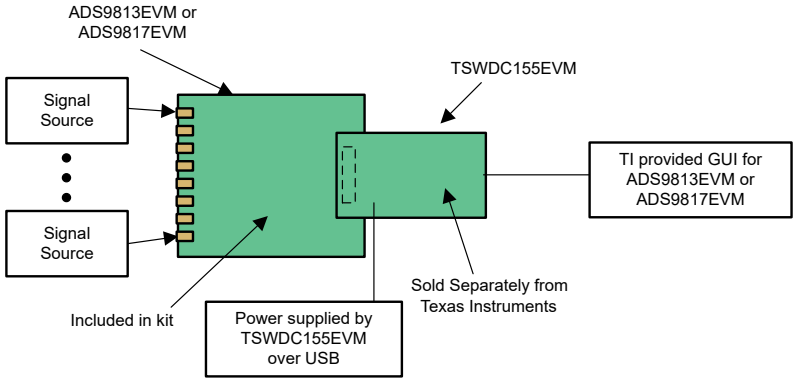


Figure 1-1. System Using GUI and TSWDC155EVM

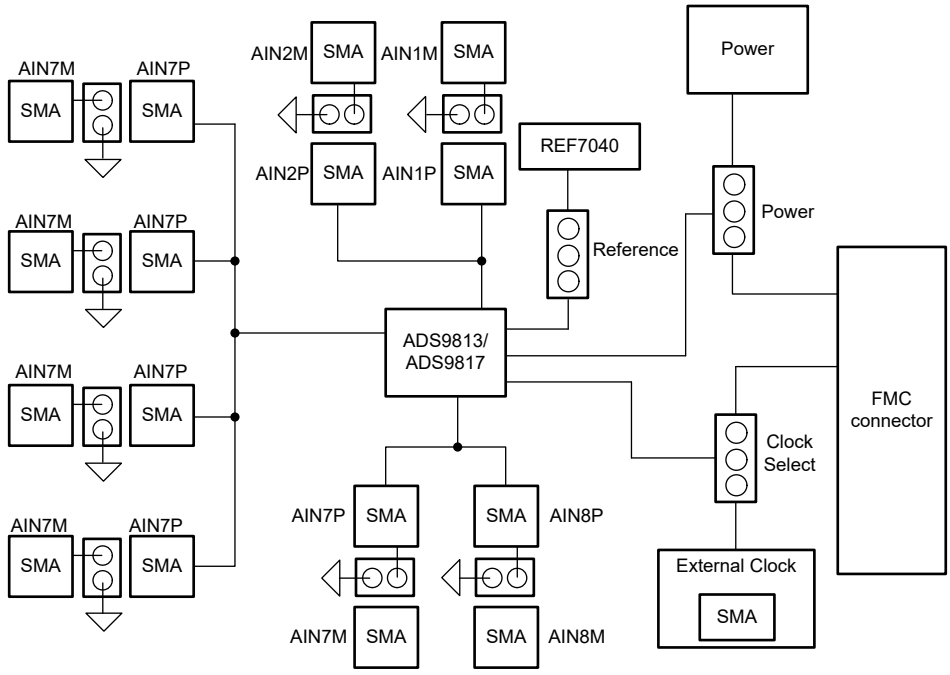


Figure 1-2. ADS9813EVM and ADS9817EVM Block Diagram

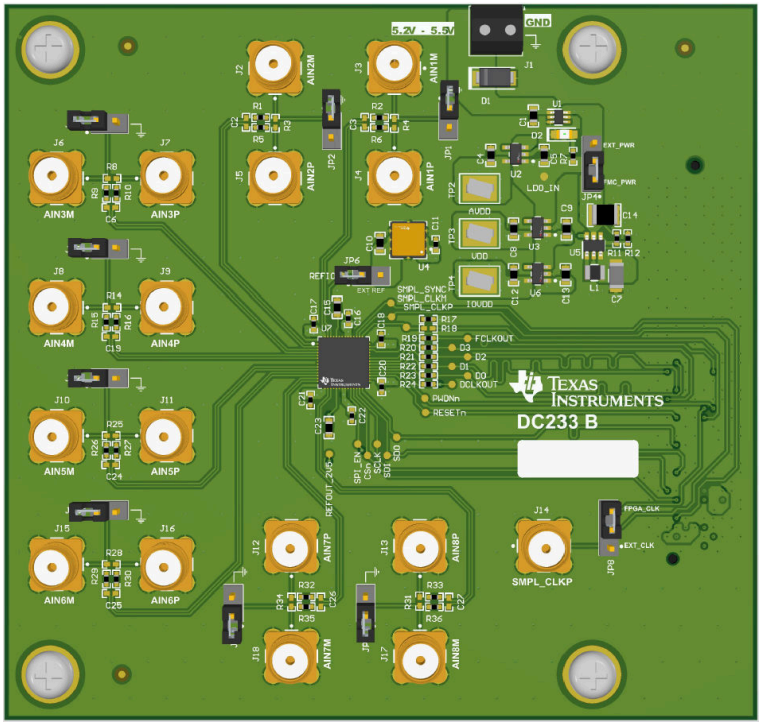
1.4 Device Information

The ADS9813EVM and the ADS9817EVM are platforms for evaluating the performance of the ADS9813 and ADS9817 SAR ADCs, both of which include a PGA front-end to support input voltages of ±12 V, ±10 V, ±7 V, ±5 V, ±3.5 V, and ±2.5 V, both in single-ended and differential configurations. Both ADC cores support 18-bit resolution at 2-MSPS/channel. The ADS9813 ADC features a simultaneous-sampling input structure, while the ADS9817 ADC features a multiplexed input structure.

Both the ADS9813EVM and ADS9817EVM include a standard FMC connector on the bottom of the PCB. The FMC connector can be used to mate with standard FPGA kits, including the TSWDC155EVM (sold separately). The TSWDC155EVM is a digital controller board that is necessary for the included EVM software GUI to communicate with the device, graph measured results, and compute common figures of merit (for example, SNR and THD).

2 Hardware

2.1 Additional Images



ADS9813EVM and ADS9817EVM Evaluation Module

2.2 ADS9813EVM and ADS9817EVM Quick Start Guide

The following instructions are a step-by-step guide to connecting the ADS9817EVM to the computer and evaluating the performance of the ADS9817. The same steps can be used for setting up the ADS9813EVM.

1. Review the default jumper settings in Figure 2-1 and the power guidelines in Section 2.5.1.
2. Physically connect J1 of the TSWDC155EVM to J27 of the ADS9817EVM. This component is the digital communications and power signal connection in default configuration.
3. Set jumper J18 to the FMC_PWR position so the TSWDC155EVM provides power. Otherwise, set J18 to EXT_PWR and connect an external 5.2V to 5.5V supply on screw terminal connection J17.
4. Bypass any external USB hub and connect the USB on the TSWDC155EVM directly to the computer.

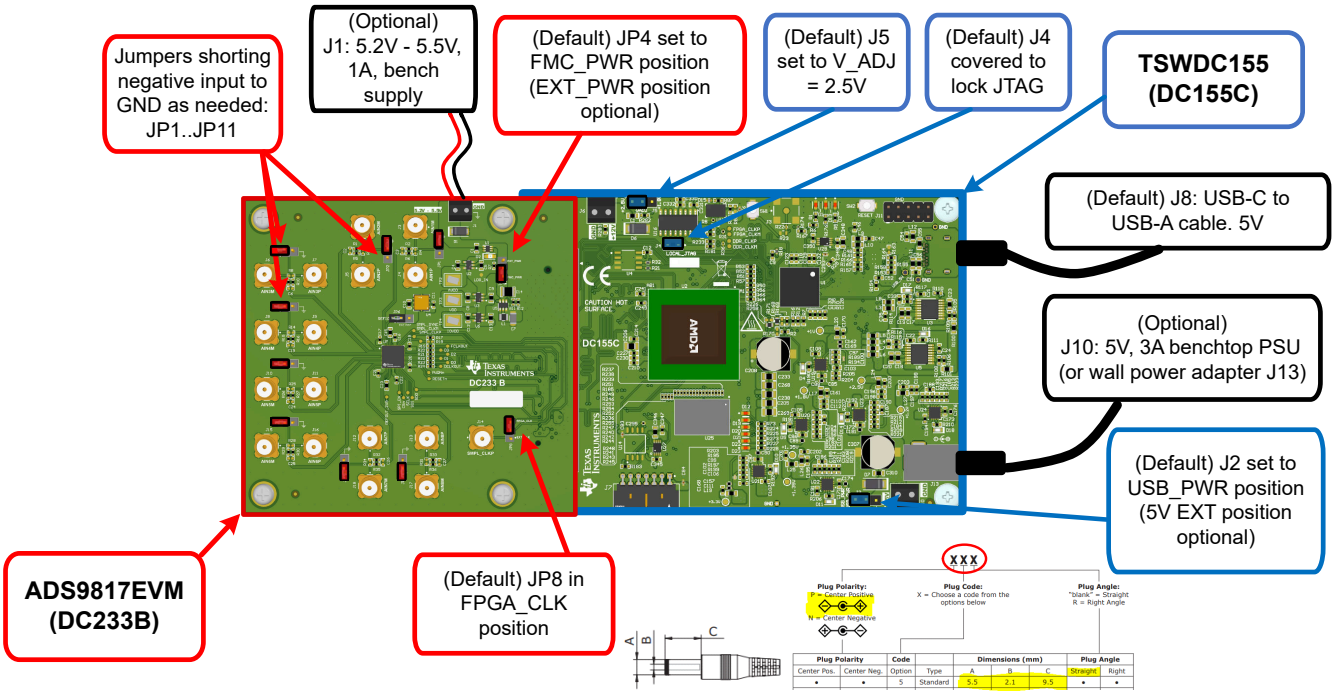


Figure 2-1. Connecting the Hardware

1. Install the GUI as described in Section 3.1.
2. Install the necessary USB drivers as described in Section 3.1.1.
3. Launch the GUI.
4. For ADS9817EVM and GUI, press the *Initialize USB*, *Power Up*, *Program FPGA*, and *Initialize ADS98xx* buttons, in order from top to bottom, on the *Config* tab to power up and configure the EVM, (see Section 3.2.1 for details).

   The steps for ADS9813EVM and GUI can be found in Section 3.3.1.
5. Connect a $10V_{PP}$, single-ended sine wave signal from a function generator to any AINxP SMA input connector.
6. Press the *EN SYNC* button on the *Capture* tab.
7. Select the number of samples to be at least 32k points, and choose the Hanning window type for best frequency domain results.
8. Press the *Start Capture* button to collect and analyze the data displayed on the appropriate CHx tab; see Section 3.2 or Section 3.3 for more details.

2.3 Analog Interface

This section details the analog input connections to the ADS9813EVM and ADS9817EVM.

2.3.1 ADC Input SMA Connections

Each ADC channel is connected to two SMA input connectors. 0402 footprints are provided to add a first-order, low-pass filter network on all ADC channels. By default, the filter capacitors are uninstalled and the filter resistors are populated with 0 ohms. Use NP0/C0G type capacitors and low-tolerance resistors to maintain AC performance when choosing to populate these footprints with a low-pass filter circuit.

Additionally, the ADC negative input connectors (for example, AIN1M) have the option to be shorted to GND with a jumper to allow for single-ended input signals. Figure 2-2 shows the input connections for a digital interface.

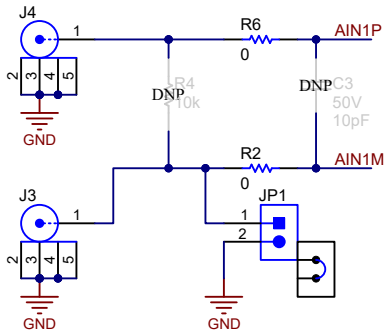


Figure 2-2. Input SMA Connections Digital Interface

2.3.2 Voltage Reference

The ADS9813 and ADS9817 both use an internal 4.096V reference voltage, which can be measured on the REFIO pin when configured as an output (default). For applications which require improved drift performance, configure the REFIO pin as an input and apply an external reference voltage to the pin.

The ADS9813EVM and ADS9817EVM include a provision for evaluating the REF7040 reference IC. The REF70xx family of high precision series voltage references offers the industry's lowest noise (0.23ppm$_{p-p}$), very low temperature drift coefficient (2ppm/°C), and high accuracy (±0.025%). In addition, these precision reference devices feature high PSRR, low drop-out voltage and excellent load and line regulation to help meet strict transient requirements. The REF7040 on the EVM is the 4.096V output voltage option. To connect the REF7040 to the ADS9813 or the ADS9817, configure the REFIO pin as an input via the GUI and then install a shunt on jumper JP6.

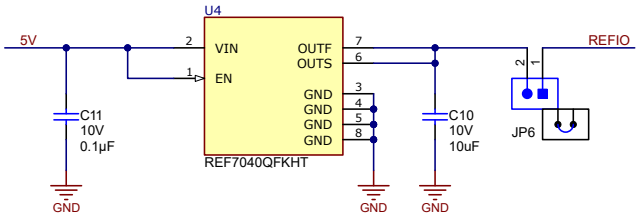


Figure 2-3. REF7040

2.4 Digital Interface and Clock Inputs

This section details the digital interface connections and clocking options for the ADS9813EVM and ADS9817EVM.

2.4.1 Digital Interface Connections

The ADS9813 and ADS9817 use SPI to configure the internal device registers (SCLK, SDI, SDO, CSn, and SPI_EN). A separate CMOS interface is used for capturing conversion data for each ADC channel using up to four output data lanes (D0, D1, D2, and D3). The SPI and CMOS interface signals connect to the FMC connector. Figure 2-4 provides the FMC connector signal definition. These signals are also available via test points for scope measurements as indicated in PCB silkscreen.

The FMC connector pinout below can also be interfaced with standard FPGA development kits. Note that the TI-provided software GUI is only compatible with the TSWDC155EVM and third-party software development is not supported.

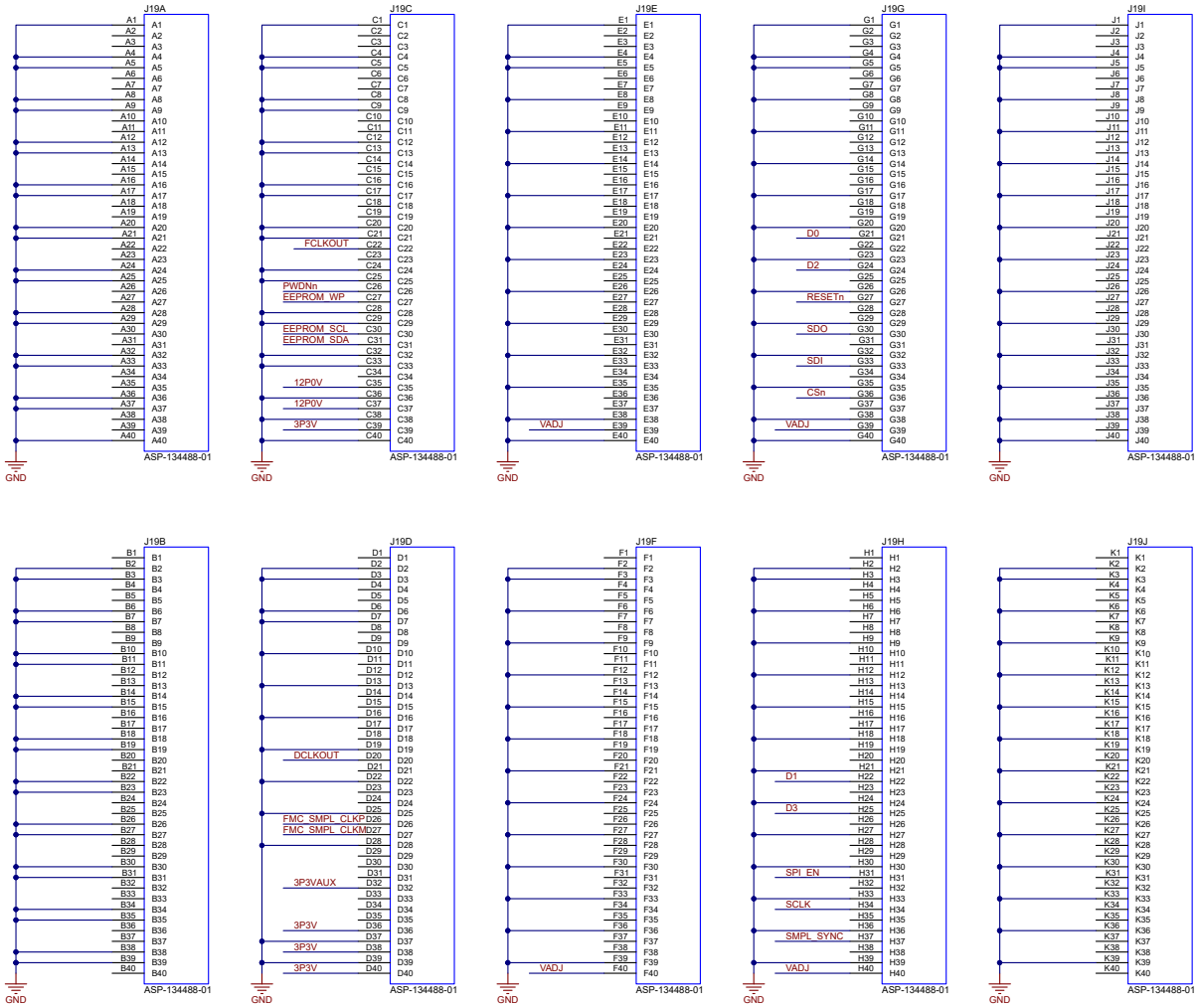


Figure 2-4. Digital I/O

The digital communication lines for the ADS9817 ADC (shown in Figure 2-5) are CMOS interface and are connected with optional termination resistors. The digital communication lines for the ADS9813 ADC are identical and can be seen in Figure 2-5. A digital serial peripheral interface (SPI) port is used to configure registers in the device. Figure 2-5 also shows the necessary decoupling capacitors for analog supplies, digital supplies, and ADC reference voltages.

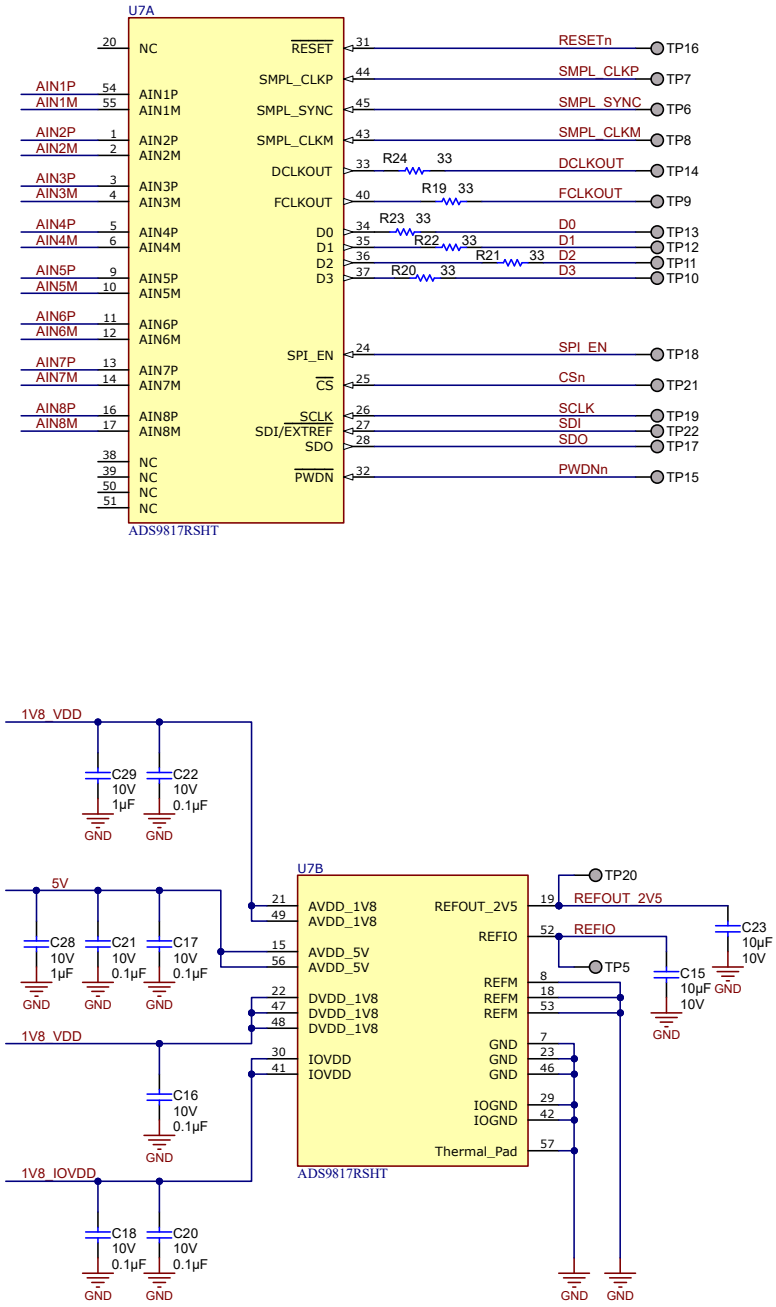


Figure 2-5. Connections to ADS9817

2.4.2 Clock Select

The ADS9813EVM and ADS9817EVM use single-ended sampling clock for ADC conversions. The positive sampling clock input (SMPL_CLKP) is selected using jumper JP8. Install a shunt in the [2-3] position (default) to source the clock signal from the TSWDC155EVM through the FMC connector. This allows the user to select the clock frequency from the options listed in the EVM GUI.

An external clock source can also be used to control ADC conversions. Connect a low-jitter clock source to SMA connector J14 and install a shunt in the [1-2] position on JP8.

The negative source of the sample clock (SMPL_CLKM) can be sourced from either the FMC connector (FMC_SMPL_CLKM) or GND through R18 or R17, respectively. By default, R17 is populated and R18 is uninstalled.

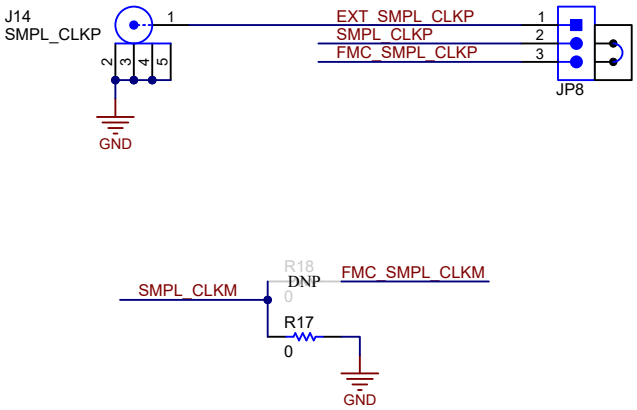


Figure 2-6. Sample Clock Selection

2.5 Power Supplies

By default, the TSWDC155EVM provides the ADS9813EVM and ADS9817EVM with a 3.3V supply (*3P3V*). The ADS9813EVM and ADS9817EVM both have a TPS61070 boost converter that boosts the 3.3V supply to 5.4V. By default, this voltage is applied to low-dropout regulators (LDOs) to derive the AVDD, DVDD, and IOVDD supplies when JP4 is in the [1-2] position. U2 (TPS7A2050) provides the 5V AVDD supply and U3 and U6 (TPS7A2018) provide the 1.8V DVDD and IOVDD supplies, respectively. The LDO input voltage (LDO_IN) can be changed to an external source (5.2V to 5.5V) applied to terminal block J1 by placing a shunt on JP4 in the [2-3] position. In this case, U1 (LM66100) provides reverse polarity protection if the connection is wired incorrectly. Figure 2-7 shows the power tree schematic for the ADS9813EVM and ADS9817EVM.

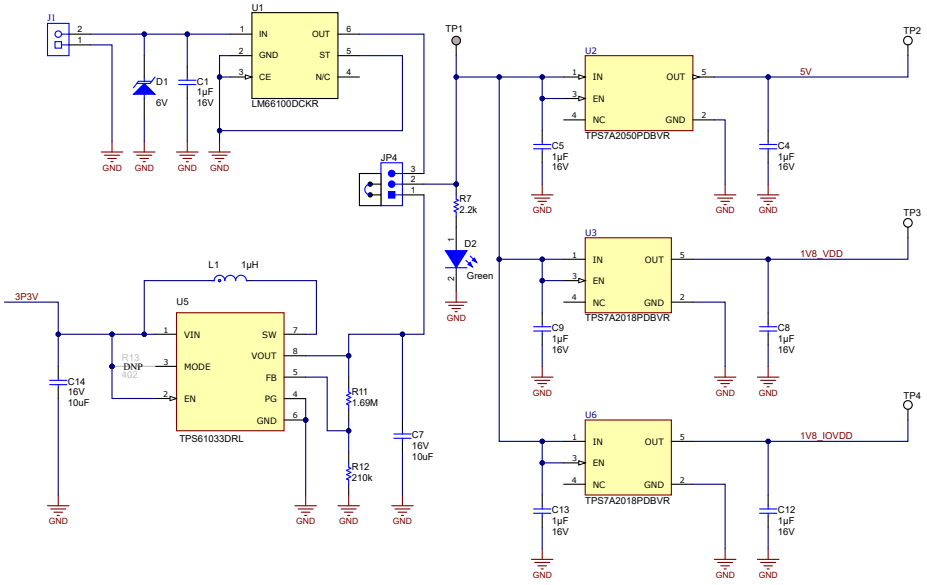


Figure 2-7. Power Entry and Regulators

2.5.1 USB Power and When to Power the Board Externally

As discussed in Section 2.2, the USB-C® connector is able to provide power to the TSWDC155EVM and ADS9813EVM or ADS9817EVM using the default configuration. The combined peak current consumption reaches 600mA (typical) during the ADC conversion process and 520mA RMS (typical) after the ADS9813EVM or the ADS9817EVM is initialized in the GUI, as described in Section 3.2.1.

The TWDC155EVM is a high-power SuperSpeed (USB 3.0) device. This means a PC supplies up to 900mA from a compliant USB 3.0 port. However, many PC USB port configurations allow much less than this limit depending on the unit load handshake process, usually resulting from other devices on the bus. Tripping the current limit on a USB can result in cutting power to the USB port, excessive power dissipation or heating, depending on the PC port configuration. As a result, TI highly recommends to consider switching to an externally powered ADS9813EVM or ADS9817EVM and/or TSWDC155EVM if:

- Only USB 1.0 or USB 2.0 ports are available.
- There are multiple devices connected to the PC by USB at the same time.
- The USB 3.0 port configuration for the PC is unknown.

To switch to the external power configuration on the ADS9813EVM or ADS9817EVM, move the jumper on JP4 to the EXT_PWR position and use the J1 terminal block to provide the required 5.2V to 5.5V supply. To switch to the external power configuration on TSWDC155EVM, move the jumper on J2 to the 5V (external) position and use the J10 terminal block or barrel jack connector to provide the required 5V supply.

USB hubs can cause possible device enumeration issues and are not recommended when communicating through the TSWDC155EVM.

3 Software

3.1 ADS9817EVM and ADS9813EVM Software Installation

This section details the installation and operation of the ADS9813EVM and ADS9817EVM software graphical user interfaces (GUI). These software require the TSWDC155EVM (sold separately) controller to operate. The first step to installing the software (as shown in Figure 3-1) is to download the latest version of the EVM GUI installer as per Table 3-1.

Table 3-1. EVM GUI Installers

EVM	Software Download Link
ADS9813EVM	ADS98XXEVM-GUI
ADS9817EVM	ADS9817EVM-GUI

Accept all the license agreements and choose the destination location, project directory, and start menu. Typically, the default values work, but these values can be customized as needed based on the user's requirements.

Note

The GUI installer and GUI buttons can differ slightly depending on which specific GUI is being installed.

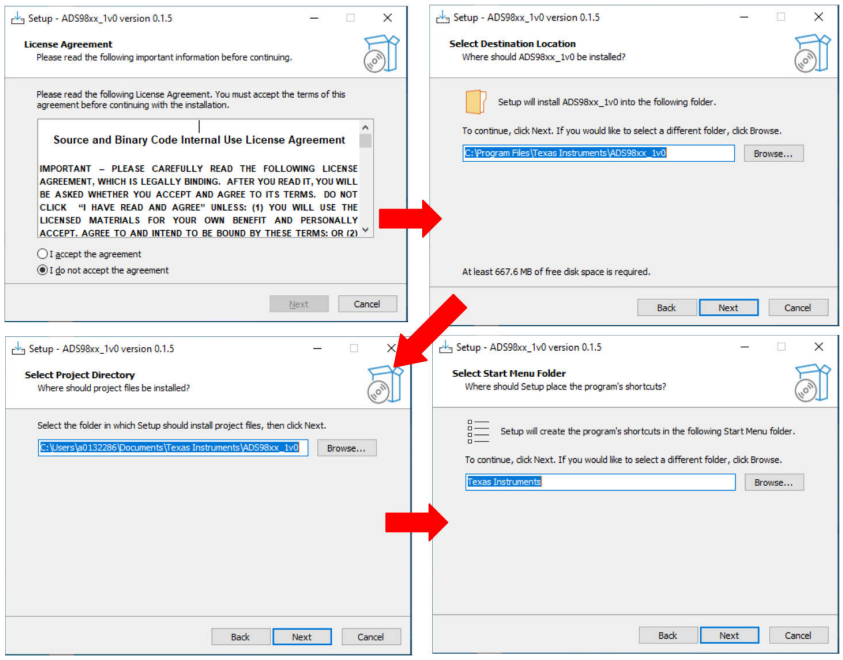


Figure 3-1. Initial Software Installation

Next, the installer prompts the user to create a desktop icon and summarize the installation plan. Clicking **Install** begins copying software onto the computer. This process takes a few minutes. At completion, the user can launch a readme text file and the application. Figure 3-2 shows these steps.

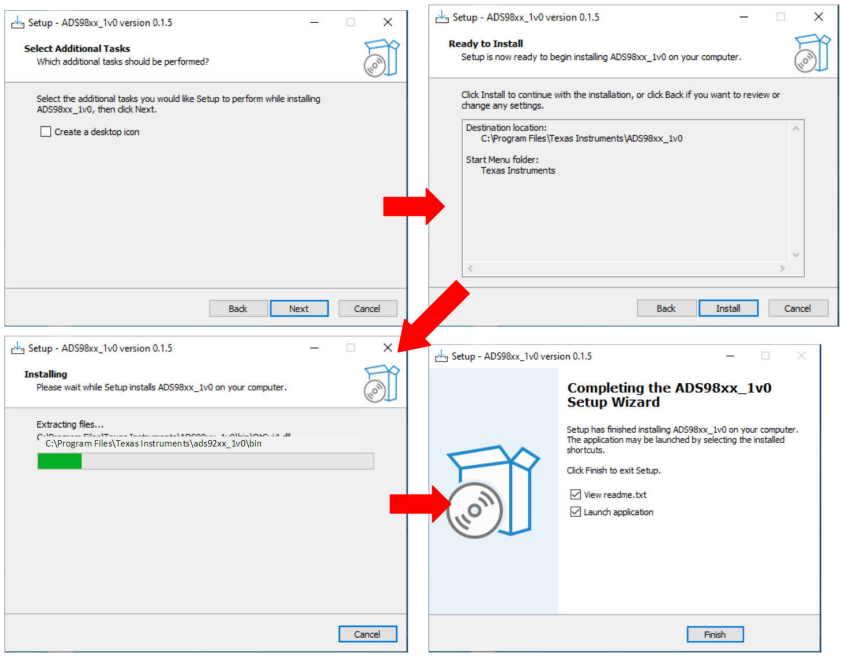


Figure 3-2. Installation Process

3.1.1 USB Driver Installation

This section describes the steps for installing the USB driver.

1. For the TSWDC155, connect J8 to the workstation using a USB-C to USB-A cable.
2. Bypass any USB hub and connect directly to the computer.
3. Open the Windows® Device Manager, as shown in Figure 3-3, and right-click on the *WestBridge* folder in the Device Manager window and select the *Update Driver* button (see Figure 3-4).
4. In the next window that appears, select *Browse my computer for driver software*.
5. Then select *Let me pick from a list of available drivers on my computer* in the next pop-up window.
6. Click on *Have Disk* in the pop-up window and navigate to:
   a. For ADS9813EVM: *C:\Program Files\Texas Instruments\ADS98XX EVM GUI\extras\Sparrow\Bootloader*
   b. For ADS9817EVM: *C:\Program Files\Texas Instruments\ADS98xx_1v0\bin\proj_lib\Sparrow\Bootloader*

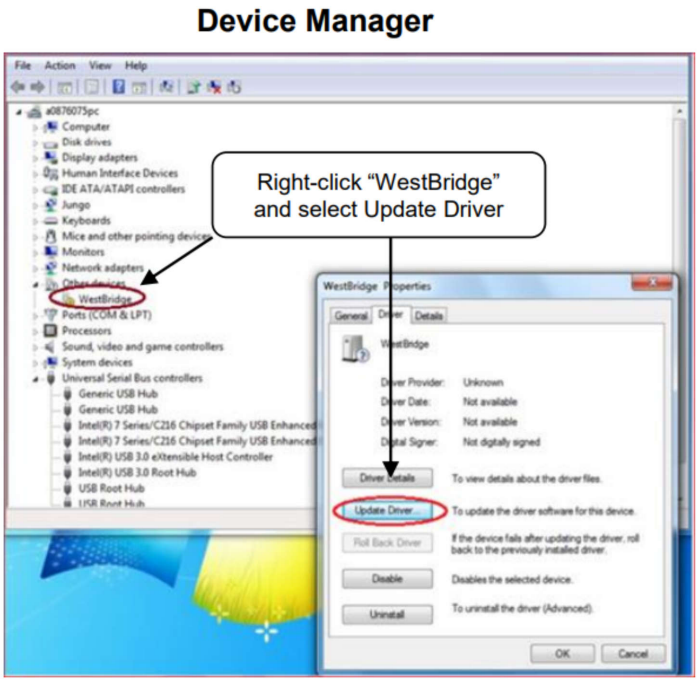


Figure 3-3. Open Device Manager

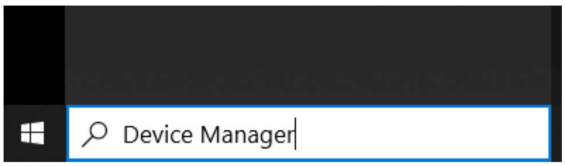


Figure 3-4. Update Driver With Device Manager

3.2 ADS9817EVM Software (ADS9817EVM-GUI)

3.2.1 Using the CONFIG Tab

After the EVM GUI is started, press the following buttons in the order shown in Figure 3-5 below. Confirm that each step is completed before proceeding by monitoring the Status message. For the Power Up and Program FPGA buttons, some status LEDs on the hardware illuminate. After all four buttons are pressed, the power on the ADS9817EVM is on and the ADS9817 device registers are configured.

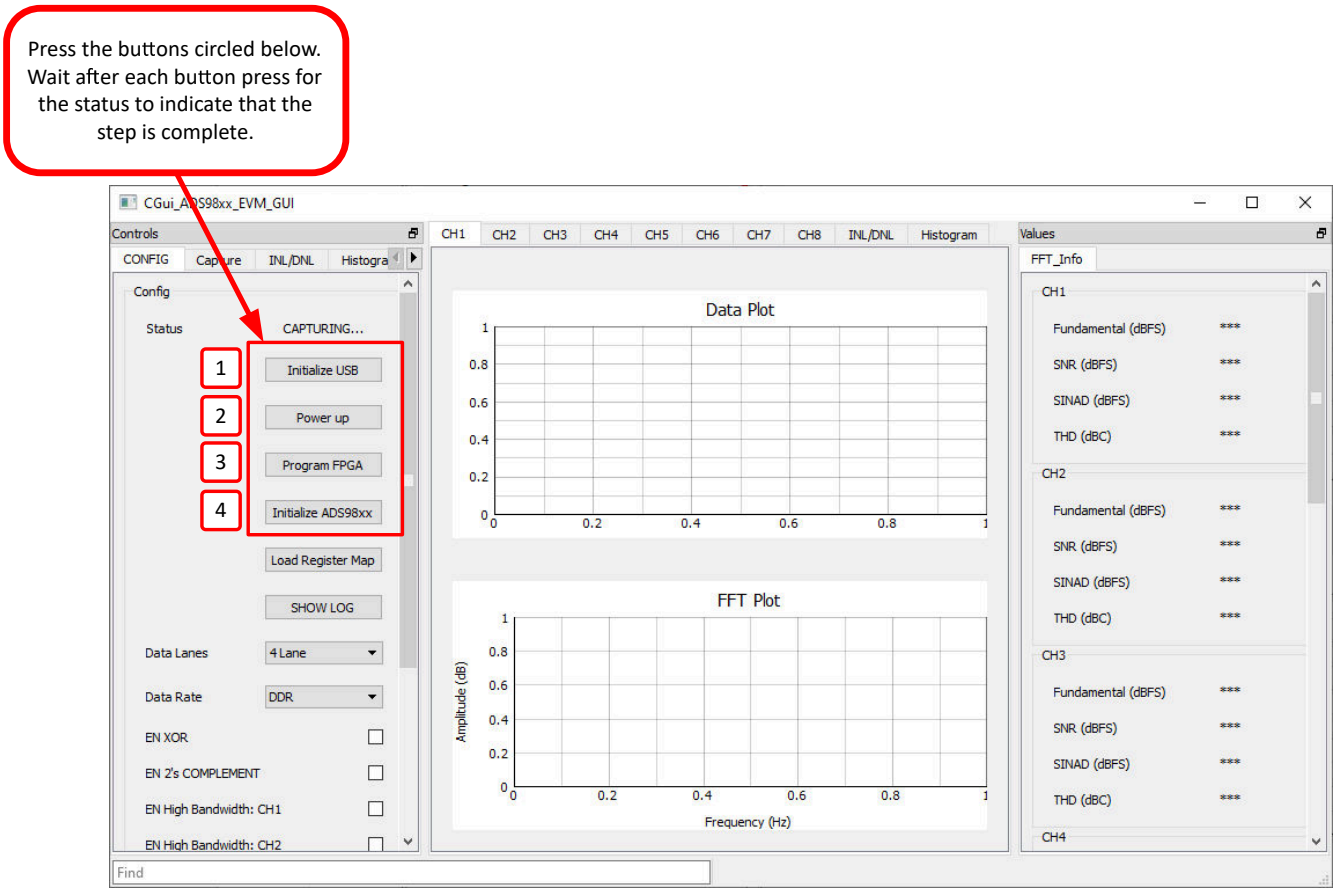


Figure 3-5. Initial Required Setup on the Config Tab

3.2.2 Using the Capture Tab

In Figure 3-6, shows an example data capture display. In this step, the necessary updates to the *Capture* settings are made to capture the time domain data and to get a good frequency domain result. First, the EN SYNC button is clicked to generate a synchronization (SYNC) signal. The SYNC signal is only required once during power-up. The SYNC signal resets the internal analog channel selection logic and aligns the FCLKOUT signal to the data frame. Next, update the number of samples to at least 32k to get good frequency domain results (for example, accurate FFT display, SNR data, and THD data). Finally, select the Hanning type window to eliminate spectral leakage in the FFT result.

When these changes are made, press the Start Capture button to collect time domain and frequency domain data. Select the appropriate tab to view data for channel 1 or channel 2.

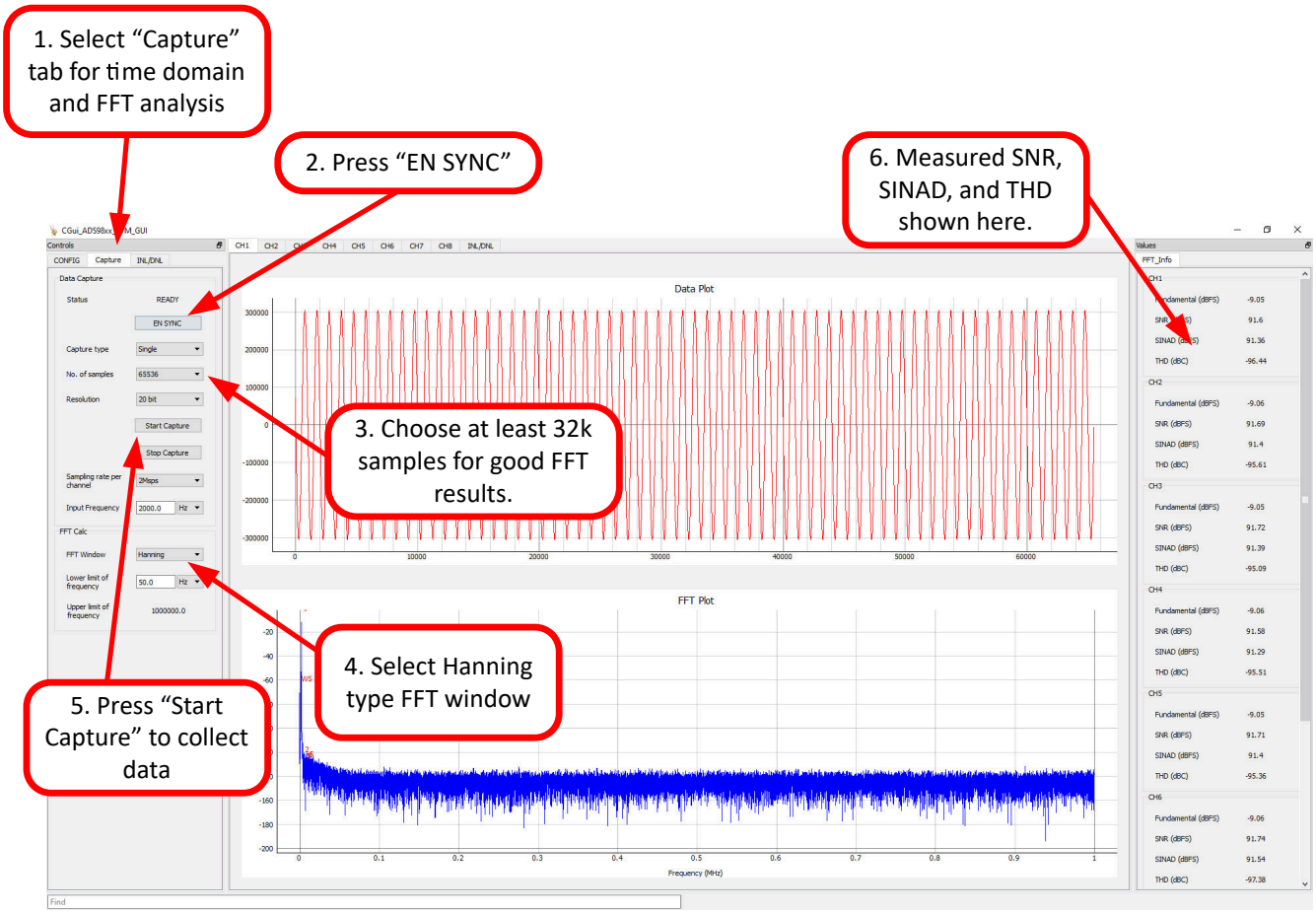


Figure 3-6. Initial Required Setup on the Capture Tab

3.2.3 Using the INL/DNL Tool

The INL/DNL tool measures the linearity of the of the ADS9817EVM by applying a full-scale, low-distortion sinusoidal input signal. The accuracy improves if the number of *hits per code* is increased at the cost of extra test time. Select the channel to measure and the *hits per code*. An input signal greater than full-scale is required to verify that all ADC codes are tested. An input signal of +0.1 dBFS is sufficient. Then press the GET INL/DNL button to run this tool as shown in Figure 3-7.

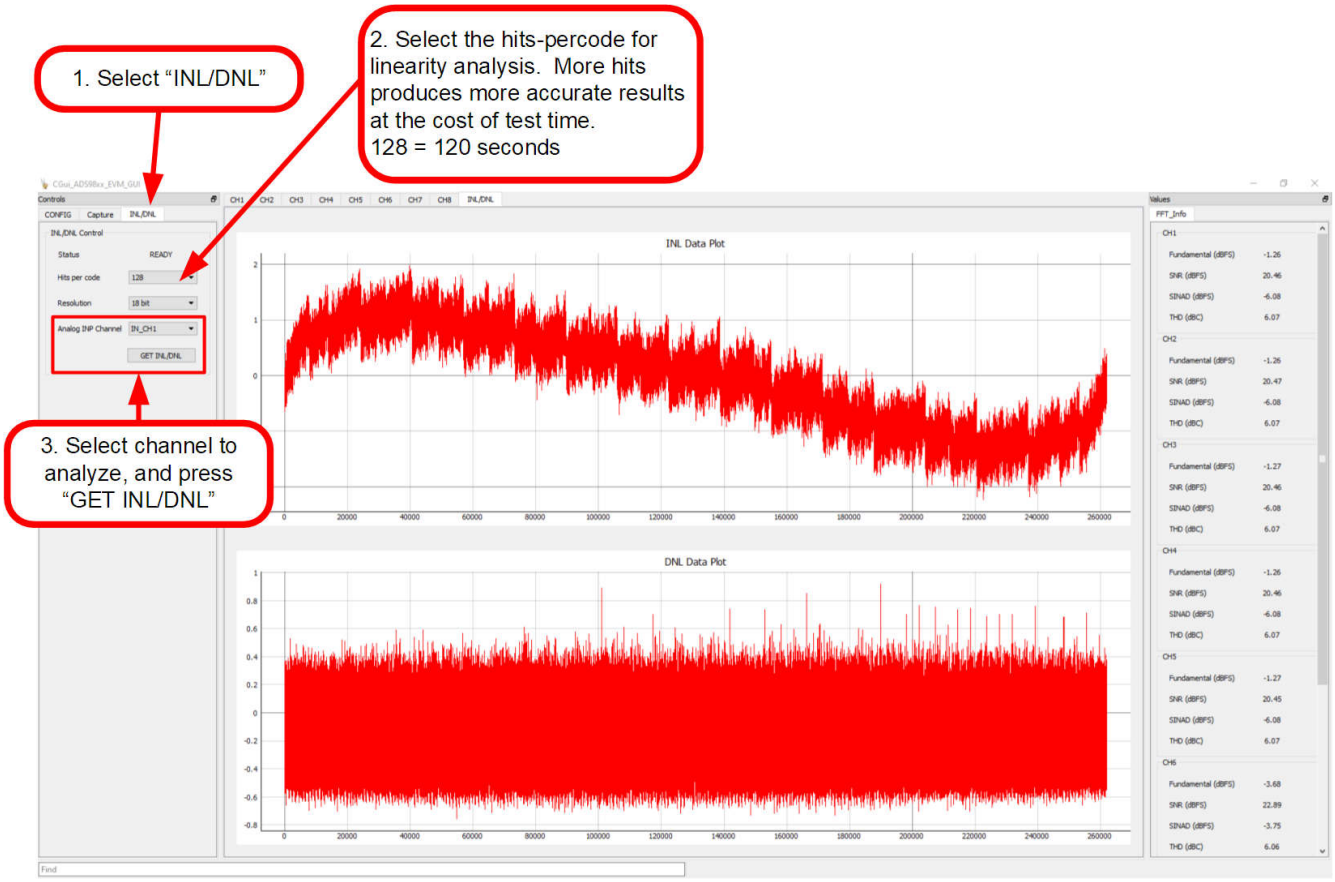


Figure 3-7. Using the INL/DNL Tool

3.2.4 Using the Histogram Tab

The Histogram tool represents the distribution of ADC output codes for a given sample set. The accuracy of the statistical summary can be improved by increasing *hits per code*, which increases the sample size at the cost of extra test time. Select the channel to measure and configure the *hits per code*, *channel*, *resolution*, and enter the reference voltage value. Then, press the *GET HISTOGRAM* button as shown in Figure 3-8.

The cumulative effect of noise coupling to the ADC output comes from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC. The total noise is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a DC input applied to a given channel. Selecting the correct reference voltage gives the result in units of voltage instead of codes.

Note that any data collected the histogram tab is not saved or stored on the *Capture Tab*. As a result, switching between the tabs results in lost data. Saving data on this screen does not provide the raw ADC codes but instead saves the histogram data presented on this tab in codes per bin. To save the raw ADC output values, use the *Capture* tab.

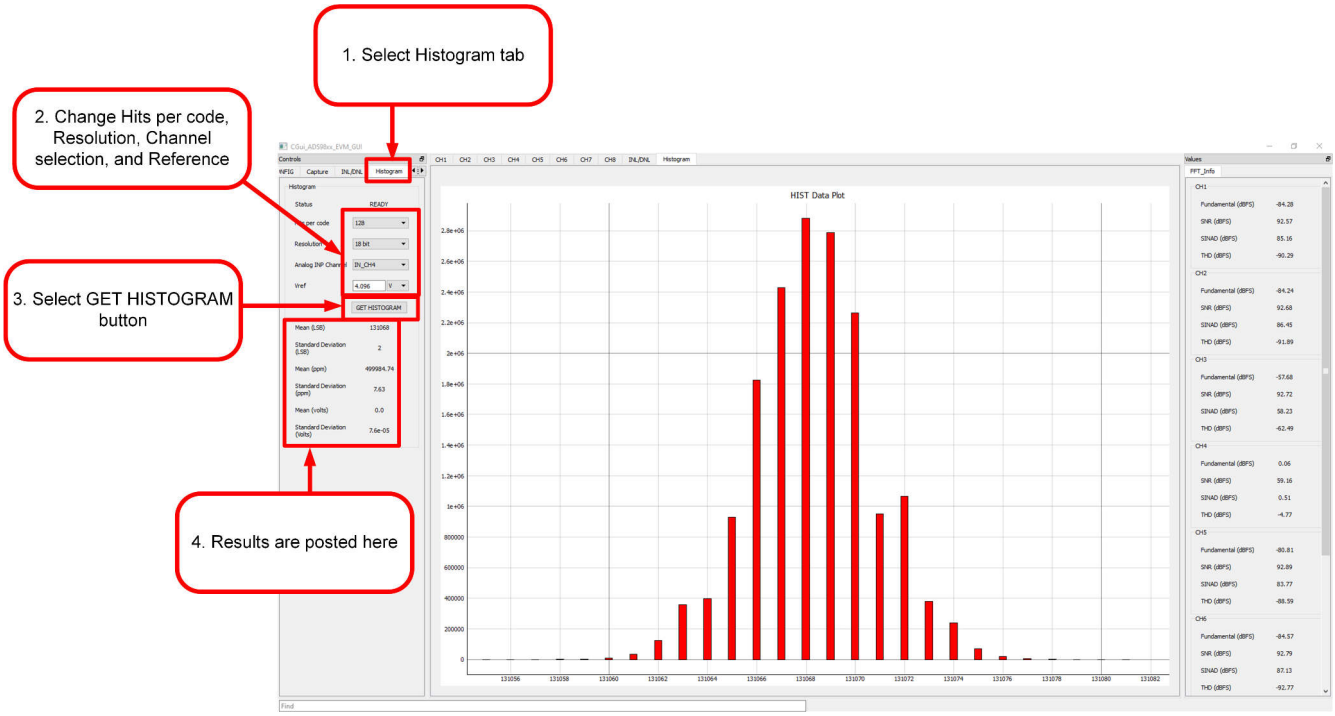


Figure 3-8. Using the Histogram Tab

3.3 ADS9813EVM Software (ADS98XXEVM-GUI)

3.3.1 Using Configuration Tab

After the EVM GUI is started, press the following buttons in the order shown below. After selecting the desired ADC from the drop-down menu, click *BOARD STARTUP*. After the *USB Status*, *FPGA Power*, and *FPGA Program* lights are green, click *INITIALIZE DEVICE*.

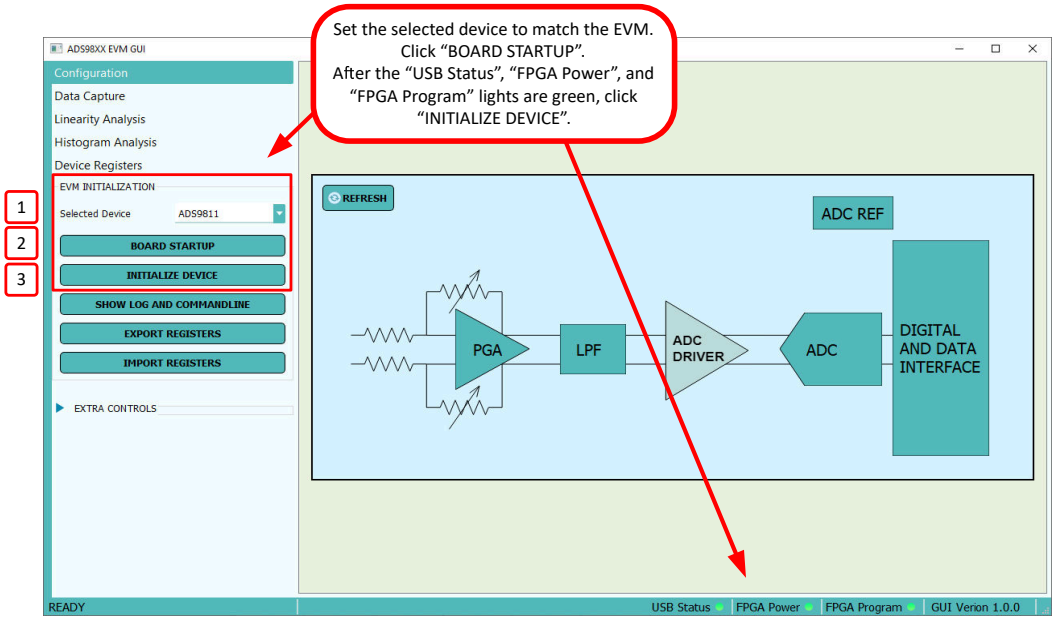


Figure 3-9. FPGA and ADC Initialization

The block diagram figures can be used to configure certain settings of the device. The "Device Registers" Tab may be used for more comprehensive device configuration. Press *REFRESH* on the block diagram to reflect updated device register settings.

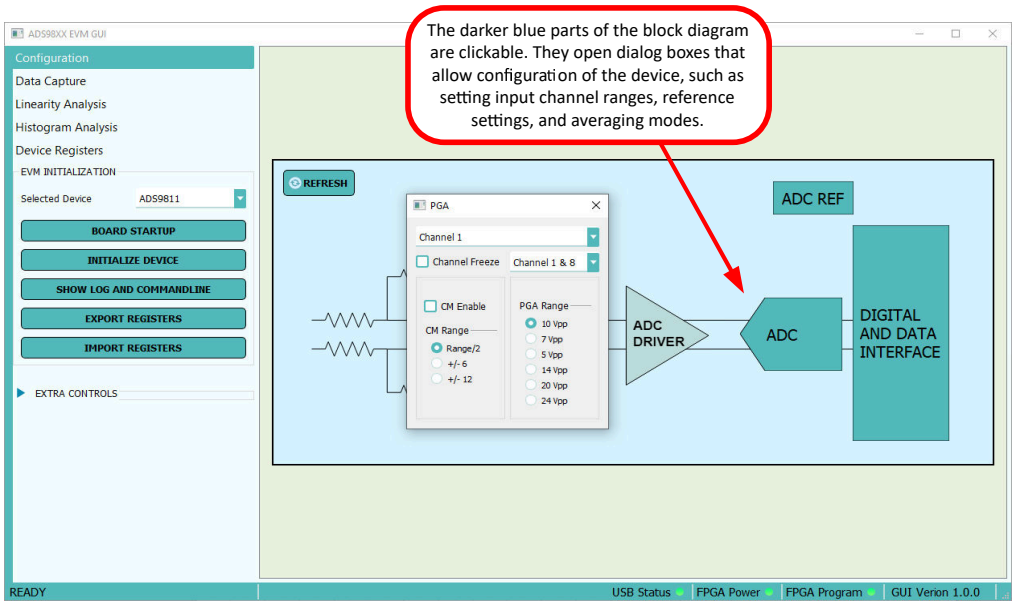


Figure 3-10. GUI Block Diagram

3.3.2 Using the Data Capture Tab

Figure 3-11 and Figure 3-12 show example data capture time-domain display and FFT display, respectively. In this step, the necessary updates to the *Data Capture* settings are made to capture the time domain data and to get a good frequency domain result. First, the ENABLE SYNC button is clicked to generate a synchronization (SYNC) signal. The SYNC signal is only required once during power-up, or if the SMPL_CLK frequency is changed. The SYNC signal resets the internal analog channel selection logic and aligns the FCLKOUT signal to the data frame. Next, update the number of samples to at least 32k to get good frequency domain results (for example, accurate FFT display, SNR data, and THD data). The *Input Frequency* needs to be set to the frequency of the applied input signal.

When these changes are made, press the *Start Capture* button to collect time domain and frequency domain data. The Data Plot tab shows the time domain data and the FFT Plot tab shows the frequency domain data. The FFT plot window also shows the SNR, THD and SINAD performance measurements. Different channel data can be shown or hidden using the *Channels* tab above the plot.

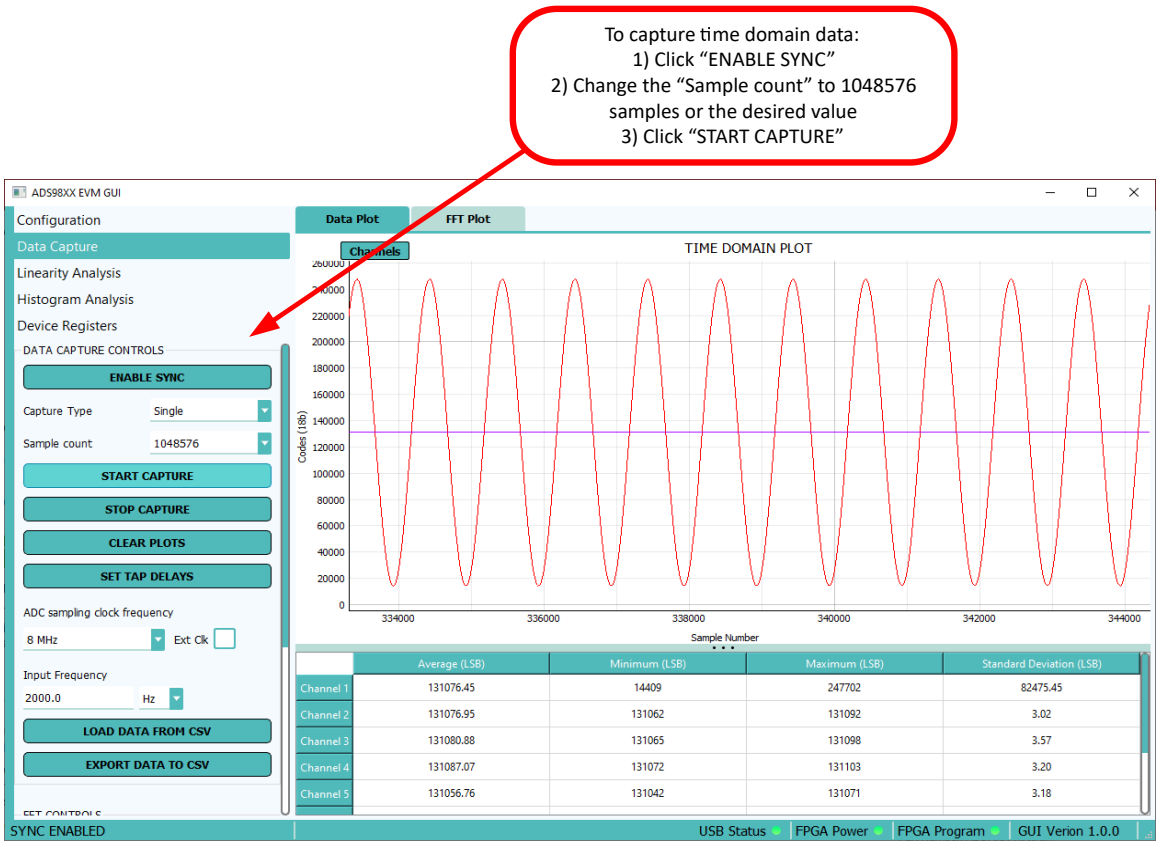


Figure 3-11. Time Domain Data

Figure 3-12. FFT Data

3.3.3 Using the Linearity Analysis Tab

The INL and DNL tool measures the linearity of the of the ADS9813EVM by applying a full-scale, low-distortion sinusoidal input signal. The accuracy improves if the number of *hits per code* is increased at the cost of extra test time. Select the channel to measure and the *hits per code*. An input signal greater than full-scale is required to verify that all ADC codes are tested. An input signal of +0.1 dBFS is sufficient. Then press the *GET INL/DNL* button to run this tool as shown in Figure 3-13. Users can use the listed coherent sampling frequency for either the SMPL_CLK or the input signal for best INL and DNL performance.

Figure 3-13. INL, DNL Data

3.3.4 Using the Histogram Analysis Tab

The Histogram tool represents the distribution of ADC output codes for a given sample set. The accuracy of the statistical summary can be improved by increasing *number of samples*, which increases the sample size at the cost of extra test time. Select the channel to measure and configure the *number of samples*, *Vref*, and *ADC Full-scale*. Then, press the *GET HISTOGRAM* button as shown in .

The cumulative effect of noise coupling to the ADC output comes from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC. The total noise is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a DC input applied to a given channel. Selecting the correct reference voltage gives the result in units of voltage instead of codes.

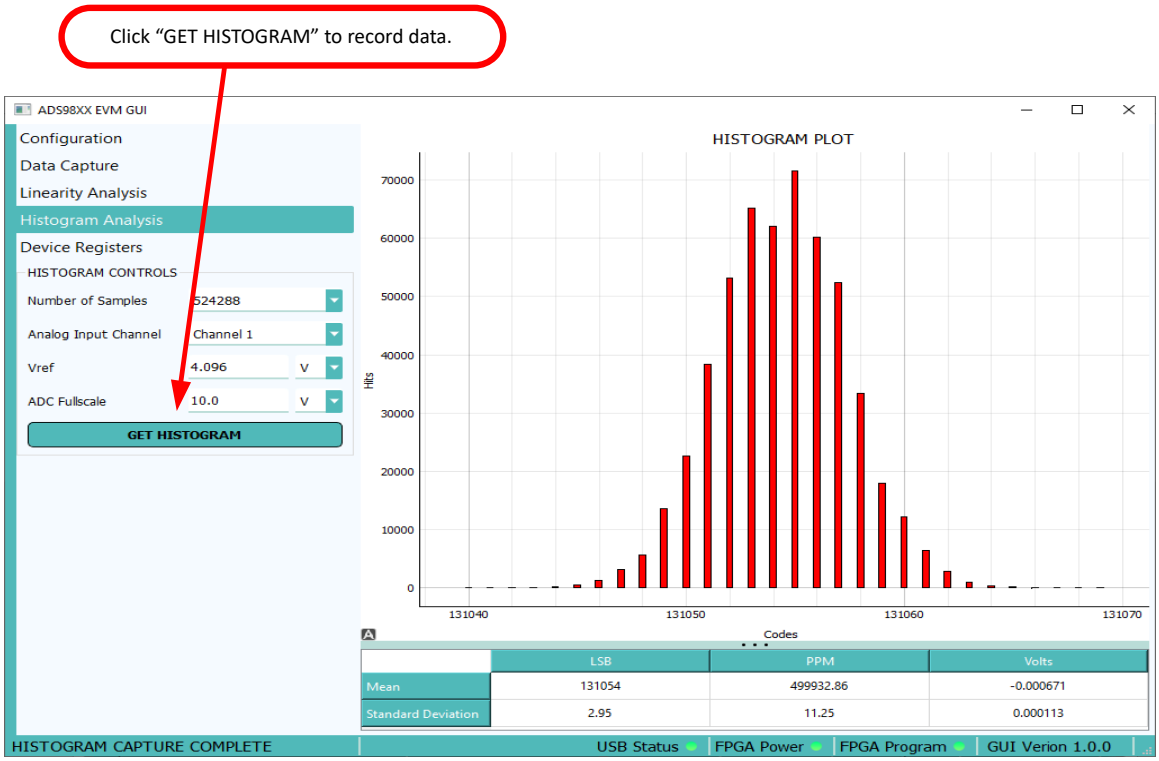


Figure 3-14. Histogram Data

4 Hardware Design Files

4.1 Schematics

4.1.1 ADS9813EVM Schematics

The schematics below show the various connections to the ADS9813 device. The digital signals connect to J19, as shown in Figure 4-3, and the analog signals connect to SMA connectors and input filtering. Figure 4-1 also shows the decoupling for the device.

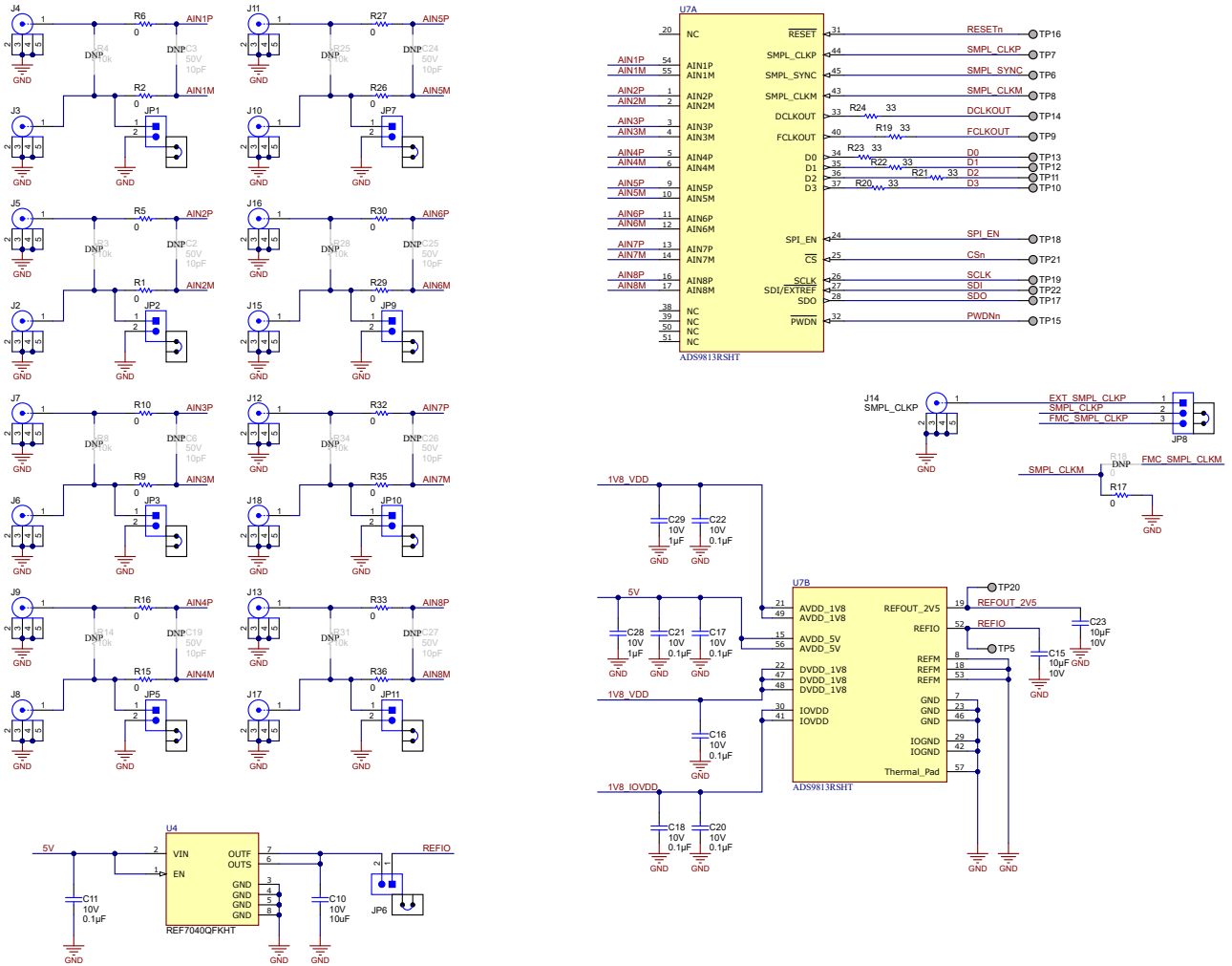


Figure 4-1. ADS9813 Device Connections Schematic

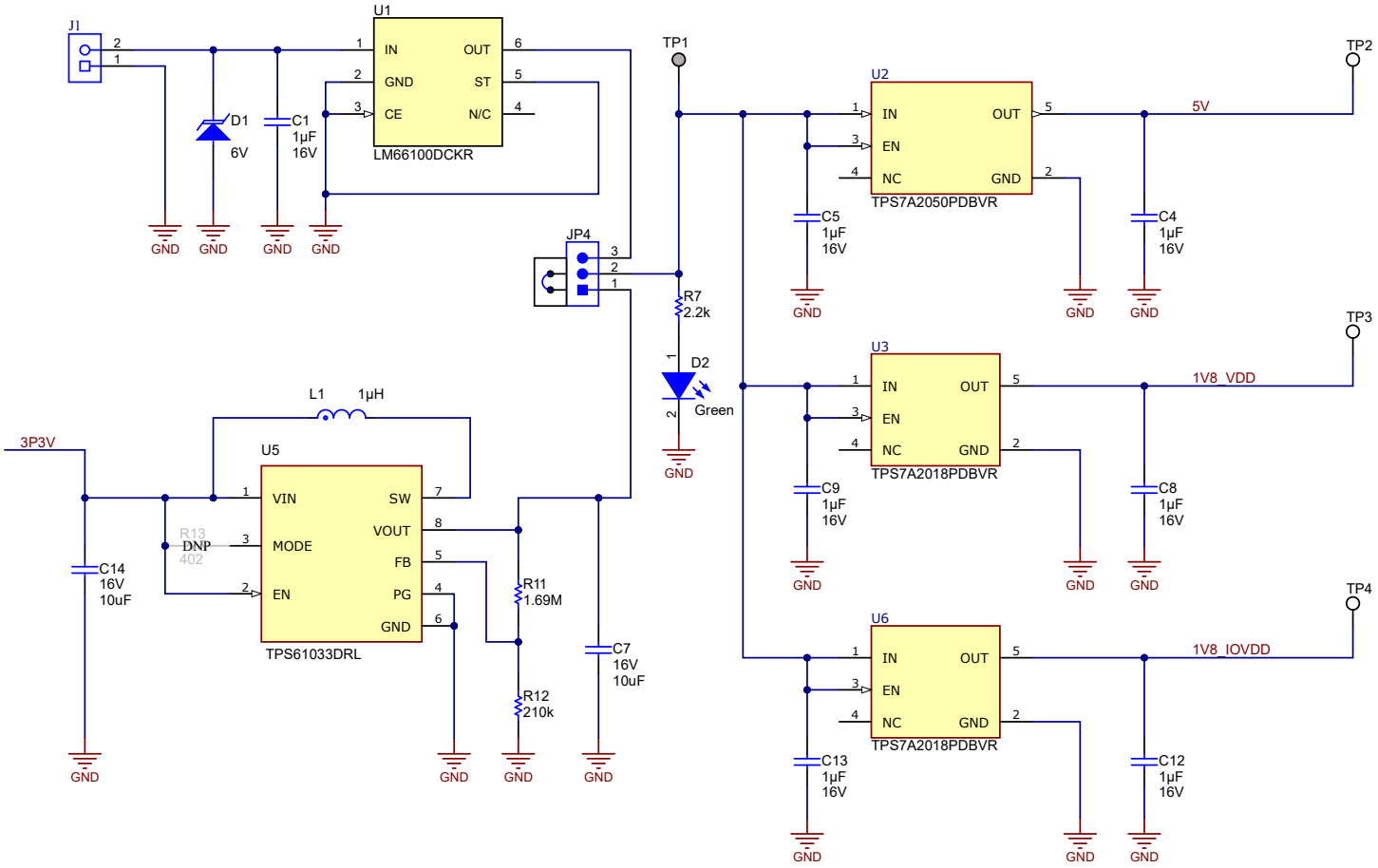


Figure 4-2. Power Connections and Regulators Schematic

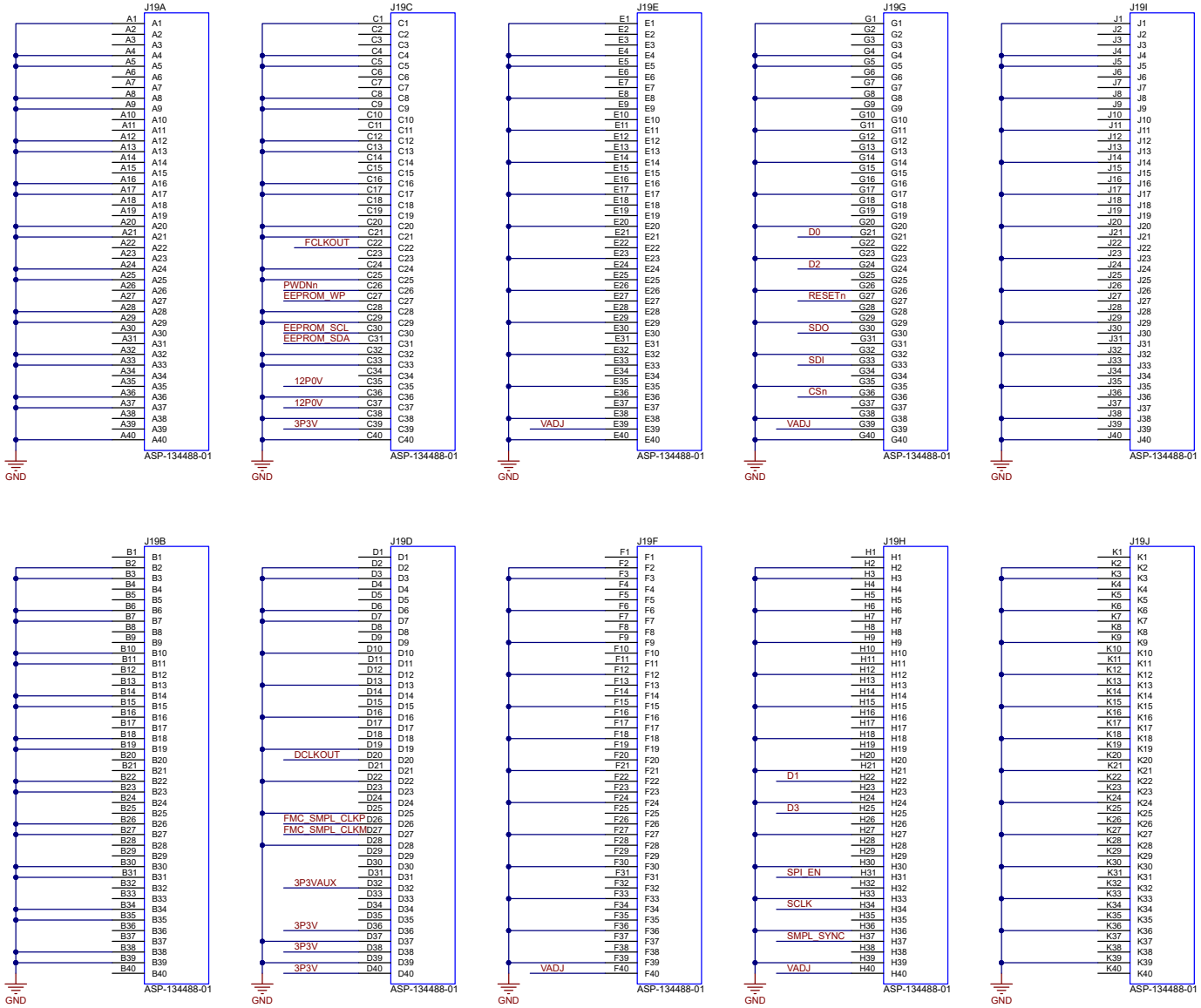


Figure 4-3. Digital Connector Schematic

4.1.2 ADS9817EVM Schematics

The schematics below show the various connections to the ADS9817 device. The digital signals connect to J19, as shown in Figure 4-6, and the analog signals connect to SMA connectors and input filtering. Figure 4-4 also shows the decoupling for the device.

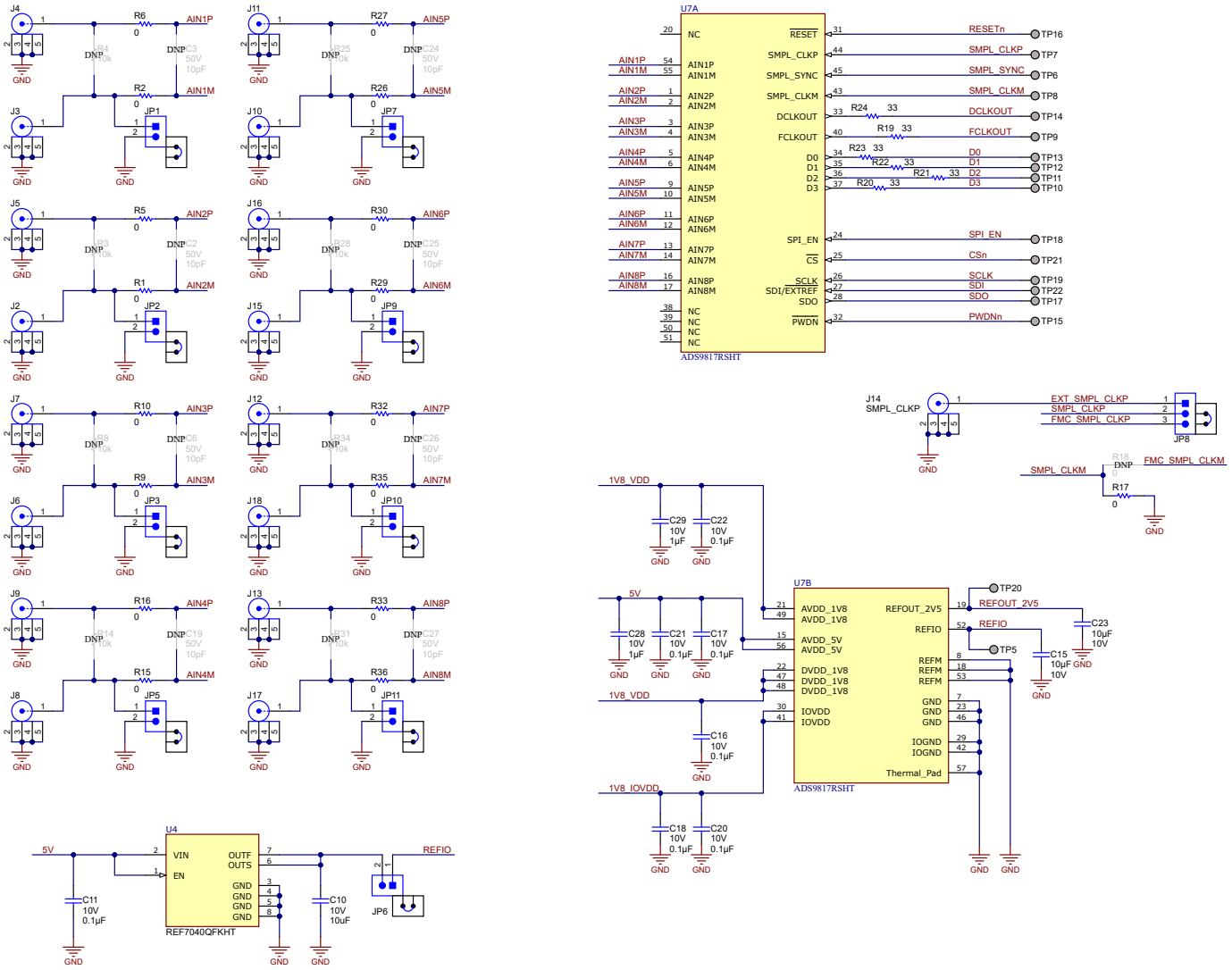


Figure 4-4. ADS9817 Device Connections Schematic

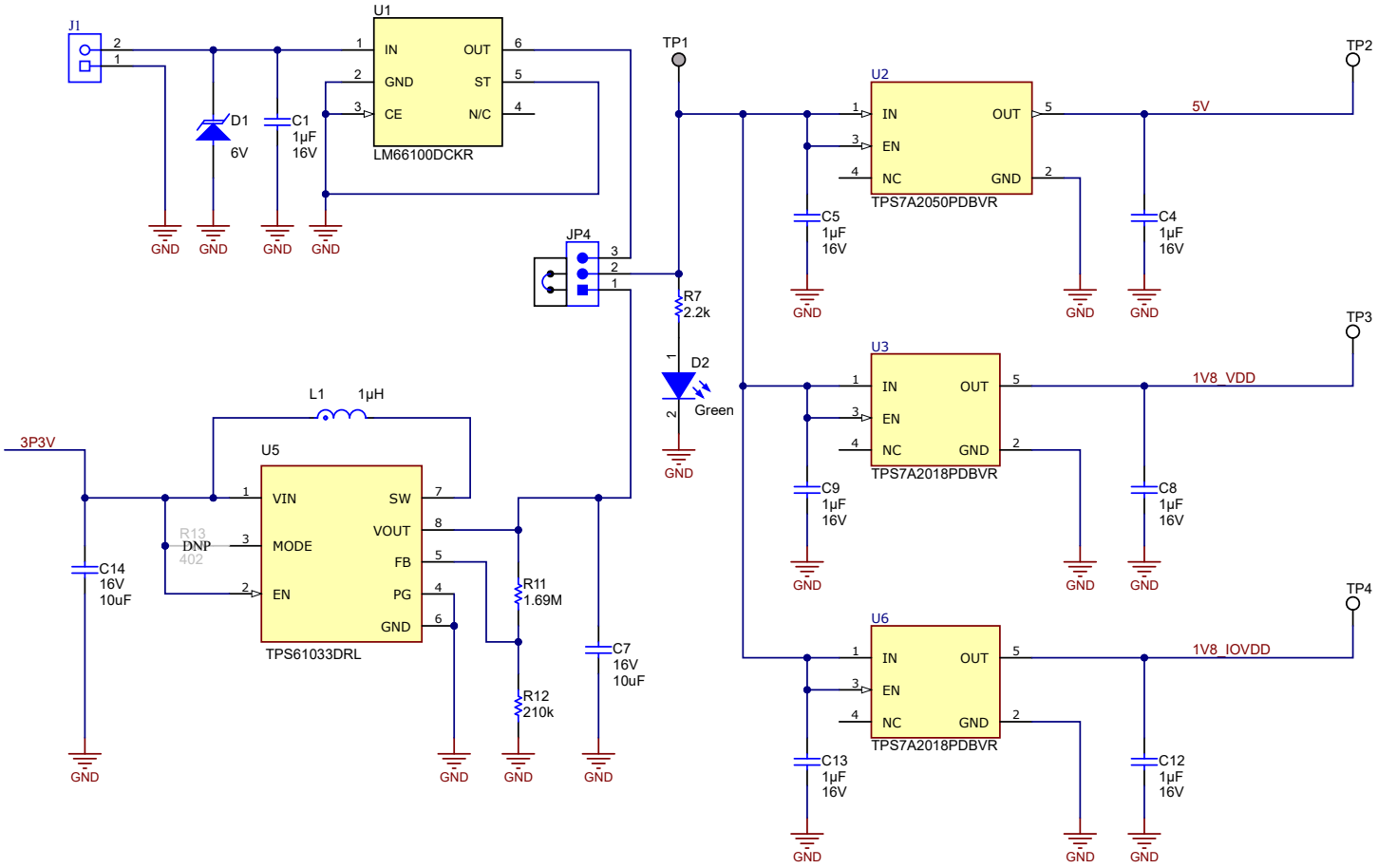


Figure 4-5. Power Connections and Regulators Schematic

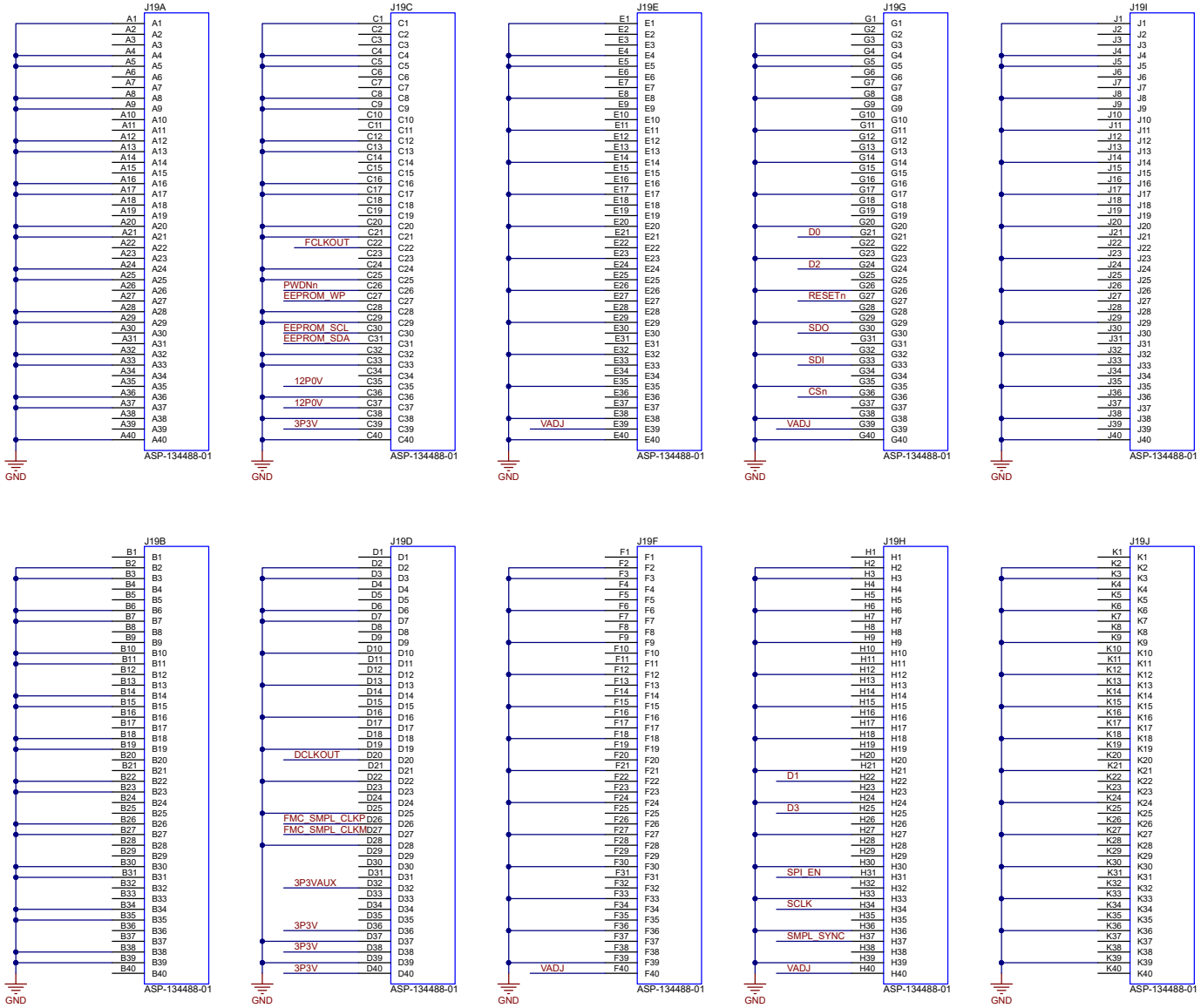


Figure 4-6. Digital Connector Schematic

4.2 Layout

Figure 4-7 through Figure 4-12 show the PCB layer plots for the ADS9813EVM and the ADS9817EVM.

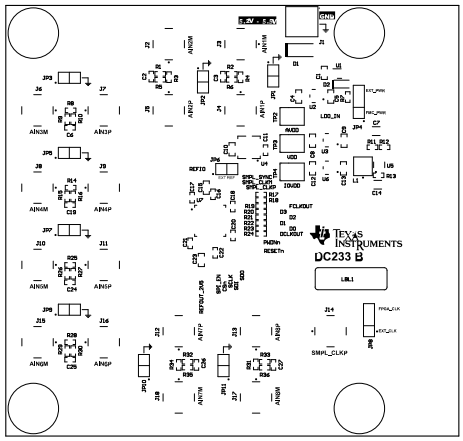


Figure 4-7. Top Overlay

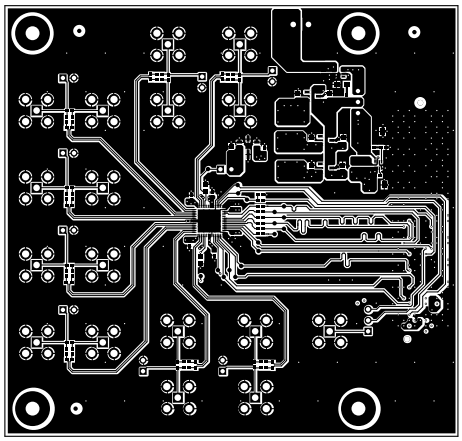


Figure 4-8. Top Layer

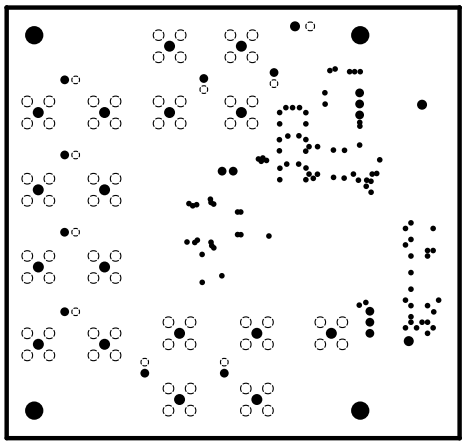


Figure 4-9. GND1 Layer

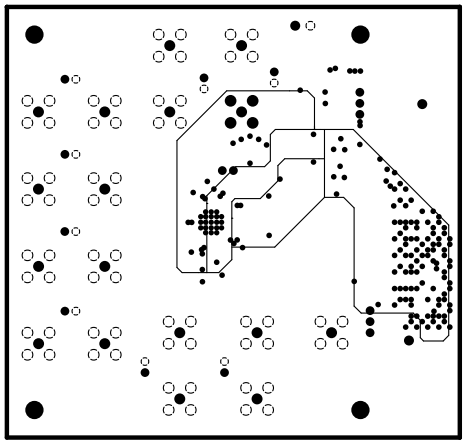


Figure 4-10. GND2 Layer

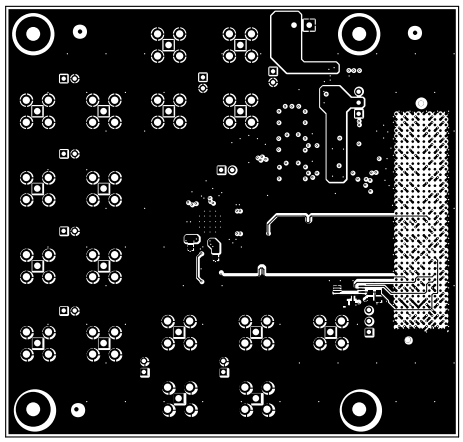


Figure 4-11. Bottom Layer

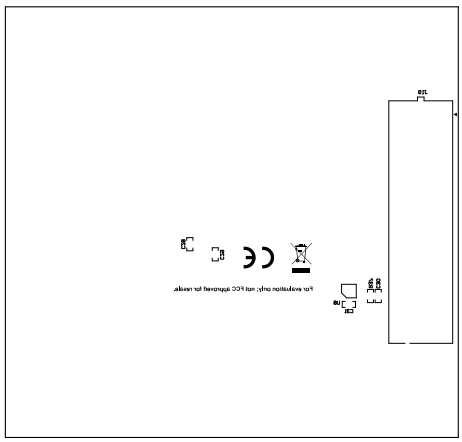


Figure 4-12. Bottom Overlay

4.3 Bill of Materials (BOM)

4.3.1 ADS9813EVM Bill of Materials (BOM)

Table 4-1 lists the ADS9813EVM bill of materials.

Table 4-1. ADS9813EVM Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C1, C4, C5, C8, C9, C12, C13	7	1uF	CAP, CERM, 1uF, 16V, +/- 10%, X7R, 0603	0603	C1608X7R1C105K080AC	TDK
C7	1	10uF	CAP, CERM, 10uF, 16V, +/- 10%, X7R, 1206	1206	GRM31CR71C106KAC7L	MuRata
C10	1	10uF	CAP, CERM, 10uF, 10V, +/- 20%, X6S, 0603	0603	GRM188C81A106MA73D	MuRata
C11, C16, C17, C18, C20, C21, C22	7	0.1uF	CAP, CERM, 0.1µF, 10V,+/- 10%, X7R, 0402	0402	C0402C104K8RACTU	Kemet
C14	1	22uF	CAP, CERM, 22µF, 25V,+/- 10%, X7R, AEC-Q200 Grade 1, 1210	1210	TMK325B7226KMHP	Taiyo Yuden
C15, C23	2	10uF	CAP, CERM, 10uF, 10V, +/- 20%, X7R, 0603	0603	GRM188Z71A106MA73D	MuRata
C28, C29	2	1uF	CAP, CERM, 1µF, 10V,+/- 10%, X7R, 0603	0603	0603ZC105KAT4A	AVX
D1	1	6V	Diode, TVS, Uni, 6V, 10.3 Vc, 400W, 38.8A, SMA	SMA	SMAJ6.0A	Littelfuse
D2	1	Green	LED, Green, SMD	LED_0805	APT2012LZGCK	Kingbright
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1	1		Terminal Block, 3.5mm Pitch, 2x1, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18	17		SMA Connector Jack, Female Socket 50Ohm Through Hole Solder	CONN_SMA_PTH	6.0312E+13	Wurth Electronics
J19	1		Connector, 1.27mm, 40x10, Black, SMT	Connector, 1.27mm, 40x10, SMT	ASP-134488-01	Samtec
JP1, JP2, JP3, JP5, JP6, JP7, JP9, JP10, JP11	9		Header, 100mil, 2x1, Gold, TH	Header, 100mil, 2x1, TH	HTSW-102-07-G-S	Samtec
JP4, JP8	2		Header, 100mil, 3x1, Gold, TH	Header, 100mil, 3x1, TH	HTSW-103-07-G-S	Samtec
L1	1	10uH	Inductor, Wirewound, Ceramic, 10uH, 0.48A, 0.36 ohm, SMD	2.5x1.8x1.8mm	CBC2518T100M	Taiyo Yuden
R1, R2, R5, R6, R9, R10, R15, R16, R17, R26, R27, R29, R30, R32, R33, R35, R36	17	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GE0R00X	Panasonic
R7	1	2.2k	RES, 2.2 k, 5%, 0.063 W, 0402	0402	CRCW04022K20JNED	Vishay-Dale

Table 4-1. ADS9813EVM Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
R11	1	1.96Meg	RES, 1.96M, 1%, 0.063W, 0402	0402	CRCW04021M96FKED	Vishay-Dale
R12	1	200k	RES, 200 k, 1%, 0.063 W, 0402	0402	CRCW0402200KFKED	Vishay-Dale
R19, R20, R21, R22, R23, R24	6	33	RES, 33, 5%, 0.063 W, 0402	0402	CRCW040233R0JNED	Vishay-Dale
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11	11		Shunt, 2.54mm, Gold, Black	Shunt, 2.54mm, Black	60900213421	Wurth Elektronik
TP2, TP3, TP4	3		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone Electronics
U1	1		+/-6V, Low IQ Ideal Diode with Input Polarity Protection, DCK0006A (SOT-SC70-6)	DCK0006A	LM66100DCKR	Texas Instruments
U2	1		300mA, ultra-low-noise, low-IQ, low-dropout (LDO) linear regulator with high PSRR 5-SOT-23 -40 to 125	SOT23-5	TPS7A2050PDBVR	Texas Instruments
U3, U6	2		Linear Voltage Regulator IC Positive Fixed 1 Output 300mA SOT-23-5	SOT23-5	TPS7A2018PDBVR	Texas Instruments
U4	1		2ppm/°C Maximum Drift, 0.23 ppmp-p 1/f Noise, Precision Voltage Reference	LCCC8	REF7040QFKHT	Texas Instruments
U5	1		Adjustable, 600mA Switch, 90% Efficient PFM/PWM Boost Converter in ThinSOT-23, DDC0006A (SOT-23-T-6)	DDC0006A	TPS61070DDCR	Texas Instruments
U7	1		18-Bit, 8-MSPS, Dual, Simultaneous-Sampling ADC With Integrated Analog Front-End	VQFN56	ADS9813RSHT	Texas Instruments
C2, C3, C6, C19, C24, C25, C26, C27	0	10pF	CAP, CERM, 10pF, 50V,+/- 1%, C0G/NP0, 0402	0402	GRM1555C1H100FA01D	MuRata
R3, R4, R8, R14, R25, R28, R31, R34	0	10k	RES, 10 k, 5%, 0.063 W, 0402	0402	CRCW040210K0JNED	Vishay-Dale
R18	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GE0R00X	Panasonic

4.3.2 ADS9817EVM Bill of Materials (BOM)

Table 4-2 lists the ADS9817EVM bill of materials.

Table 4-2. ADS9817EVM Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C1, C4, C5, C8, C9, C12, C13	7	1uF	CAP, CERM, 1uF, 16V, +/- 10%, X7R, 0603	0603	C1608X7R1C105K080AC	TDK
C7	1	10uF	CAP, CERM, 10uF, 16V, +/- 10%, X7R, 1206	1206	GRM31CR71C106KAC7L	MuRata
C10	1	10uF	CAP, CERM, 10uF, 10V, +/- 20%, X6S, 0603	0603	GRM188C81A106MA73D	MuRata
C11, C16, C17, C18, C20, C21, C22	7	0.1uF	CAP, CERM, 0.1µF, 10V,+/- 10%, X7R, 0402	0402	C0402C104K8RACTU	Kemet
C14	1	22uF	CAP, CERM, 22µF, 25V,+/- 10%, X7R, AEC-Q200 Grade 1, 1210	1210	TMK325B7226KMHP	Taiyo Yuden
C15, C23	2	10uF	CAP, CERM, 10uF, 10V, +/- 20%, X7R, 0603	0603	GRM188Z71A106MA73D	MuRata
C28, C29	2	1uF	CAP, CERM, 1µF, 10V,+/- 10%, X7R, 0603	0603	0603ZC105KAT4A	AVX
D1	1	6V	Diode, TVS, Uni, 6V, 10.3 Vc, 400W, 38.8A, SMA	SMA	SMAJ6.0A	Littelfuse
D2	1	Green	LED, Green, SMD	LED_0805	APT2012LZGCK	Kingbright
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1	1		Terminal Block, 3.5mm Pitch, 2x1, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18	17		SMA Connector Jack, Female Socket 50Ohm Through Hole Solder	CONN_SMA_PTH	6.0312E+13	Wurth Electronics
J19	1		Connector, 1.27mm, 40x10, Black, SMT	Connector, 1.27mm, 40x10, SMT	ASP-134488-01	Samtec
JP1, JP2, JP3, JP5, JP6, JP7, JP9, JP10, JP11	9		Header, 100mil, 2x1, Gold, TH	Header, 100mil, 2x1, TH	HTSW-102-07-G-S	Samtec
JP4, JP8	2		Header, 100mil, 3x1, Gold, TH	Header, 100mil, 3x1, TH	HTSW-103-07-G-S	Samtec
L1	1	10uH	Inductor, Wirewound, Ceramic, 10uH, 0.48A, 0.36 ohm, SMD	2.5x1.8x1.8mm	CBC2518T100M	Taiyo Yuden
R1, R2, R5, R6, R9, R10, R15, R16, R17, R26, R27, R29, R30, R32, R33, R35, R36	17	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GE0R00X	Panasonic
R7	1	2.2k	RES, 2.2 k, 5%, 0.063 W, 0402	0402	CRCW04022K20JNED	Vishay-Dale
R11	1	1.96Meg	RES, 1.96M, 1%, 0.063W, 0402	0402	CRCW04021M96FKED	Vishay-Dale
R12	1	200k	RES, 200 k, 1%, 0.063 W, 0402	0402	CRCW0402200KFKED	Vishay-Dale

Table 4-2. ADS9817EVM Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
R19, R20, R21, R22, R23, R24	6	33	RES, 33, 5%, 0.063 W, 0402	0402	CRCW040233R0JNED	Vishay-Dale
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11	11		Shunt, 2.54mm, Gold, Black	Shunt, 2.54mm, Black	60900213421	Wurth Elektronik
TP2, TP3, TP4	3		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone Electronics
U1	1		+/-6V, Low IQ Ideal Diode with Input Polarity Protection, DCK0006A (SOT-SC70-6)	DCK0006A	LM66100DCKR	Texas Instruments
U2	1		300mA, ultra-low-noise, low-IQ, low-dropout (LDO) linear regulator with high PSRR 5-SOT-23 -40 to 125	SOT23-5	TPS7A2050PDBVR	Texas Instruments
U3, U6	2		Linear Voltage Regulator IC Positive Fixed 1 Output 300mA SOT-23-5	SOT23-5	TPS7A2018PDBVR	Texas Instruments
U4	1		2ppm/°C Maximum Drift, 0.23 ppmp-p 1/f Noise, Precision Voltage Reference	LCCC8	REF7040QFKHT	Texas Instruments
U5	1		Adjustable, 600mA Switch, 90% Efficient PFM/PWM Boost Converter in ThinSOT-23, DDC0006A (SOT-23-T-6)	DDC0006A	TPS61070DDCR	Texas Instruments
U7	1		18-Bit, 8-MSPS, Dual, Simultaneous-Sampling ADC With Integrated Analog Front-End	VQFN56	ADS9817RSHT	Texas Instruments
C2, C3, C6, C19, C24, C25, C26, C27	0	10pF	CAP, CERM, 10pF, 50V,+/- 1%, C0G/NP0, 0402	0402	GRM1555C1H100FA01D	MuRata
R3, R4, R8, R14, R25, R28, R31, R34	0	10k	RES, 10 k, 5%, 0.063 W, 0402	0402	CRCW040210K0JNED	Vishay-Dale

5 Additional Information

5.1 Trademarks

Microsoft® and Windows® are registered trademarks of Microsoft Corporation.
USB-C® is a registered trademark of USB Implementers Forum.
All trademarks are the property of their respective owners.

6 Related Documentation

The following related documents are available for download through the Texas Instruments web site at www.ti.com.

Table 6-1. Related Documentation

Device	Literature Number
TSWDC155EVM	SLAU870
TPS61070	SLVS510
TPS7A20	SBVS338
LM66100	SLVSEZ8
REF7040	SNAS781

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2024) to Revision C (March 2024) **Page**

- Updated GUI for ADS9813EVM.... 18
- Updated schematics.... 23
- Updated Layout images.... 29

Changes from Revision A (July 2023) to Revision B (January 2024) **Page**

- Added a second variant EVM (ADS9813EVM).... 2
- Updated software download instructions.... 11
- Added ADS9813EVM schematic.... 23
- Added ADS9813EVM bill of materials.... 30

Changes from Revision * (November 2022) to Revision A (July 2023) **Page**

- Deleted all mention of PDK.... 2
- Changed input voltage range in *Device Information* section.... 3
- Added *Quick Start Guide* section.... 5
- Added *Voltage Reference* section.... 6
- Added information about clock source in *Digital Interface* section.... 7
- Added *Clock Select* section.... 9
- Added *USB Power and When to Power the Board Externally* section.... 10
- Added *Using the Histogram Tab* section.... 17
- Changed schematic images.... 26
- Changed Layout images.... 29
- Changed the *Bill of Materials* table.... 30

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Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

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EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

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東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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