EVM User's Guide: ADS127L18EVM-PDK

ADS127L18EVM-PDK Evaluation Module

Description

The ADS127L18 is an eight channel, 24-bit, simultaneous sampling delta-sigma (ΔΣ) analog-to-digital converter (ADC), supporting data rates up to 512 kSPS (wideband filter) and data rates up to 1.365 MSPS (low-latency filter). The ADS127L18 offers excellent ac and dc performance, along with multiple internal digital filter options. The evaluation kit includes the ADS127L18EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over the USB for data capture, configuration, and analysis.

Get Started

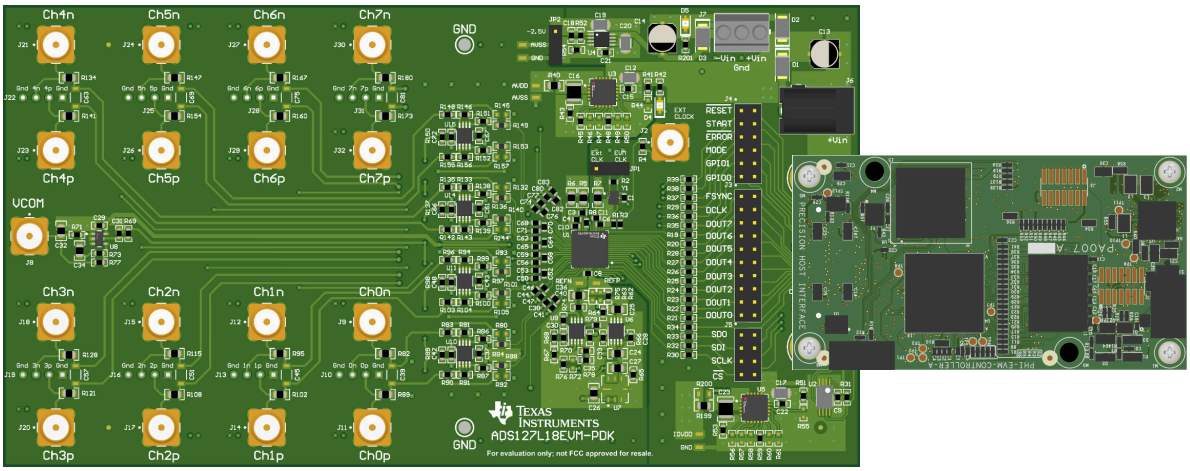
1. Order ADS127L18EVM-PDK from ti.com
2. Download the ADS127L18EVM-PDK-GUI software
3. Connect a user supplied external 6V supply power to the ADS127L18 EVM
4. Connect the ADS127L18 EVM to the computer with the included USB cable
5. Launch the ADS127L18 EVM GUI from the start menu
6. Refer to the ADS127L18 data sheet for IC details
7. Visit the E2E forums for support and questions

Features

- Simultaneously measure eight channels
- Data rate up to 512 kSPS (wideband filter)
- Data rate up to 1.365 MSPS (low-latency filter)
- AC performance with DC precision:
  - 111.5dB dynamic range at 256 kSPS
  - -120dB THD
  - 0.9ppm of Full Scale INL
  - 50nV/°C offset drift
  - 0.6ppm/°C gain drift
- Power-scalable speeds from 512 kSPS (28 mW/ch) to 50 kSPS (3.3 mW/ch)

Applications

- Test and measurement:
  - Data acquisition (DAQ)
  - Shock and vibration instruments
  - Acoustics and dynamic strain gauges
- Factory automation and control:
  - Condition monitoring
- Aerospace and defense:
  - SONAR
- Medical:
  - Electroencephalogram (EEG)
- Grid infrastructure:
  - Power quality analyzer



Copyright © 2024 Texas Instruments Incorporated

1 Evaluation Module Overview

1.1 Introduction

The ADS127L18EVM is a platform for evaluating the performance of the ADS127L18, an 8-channel, simultaneous sampling, 24-bit, high-speed, wide-bandwidth ΔΣ ADC. The ADS127L18EVM board includes the ADS127L18 ADC and all the peripheral analog circuits and components required to extract optimum performance from the ADC. The PHI board primarily serves two functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS127L18 ADC

This user's guide describes the characteristics, operation, and use of the ADS127L18 evaluation module (EVM). The ADS127L18EVM eases the evaluation of the device with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS127L18 EVM.

1.2 Kit Contents

The ADS127L18 evaluation module kit includes the following features (Figure 1-1):

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS127L18 ADC.
- The PHI controller that provides a convenient communication interface to the ADS127L18 ADC over USB 2.0 (or higher)
- Windows® 10 or 11 operating systems.
- Easy-to-use evaluation software for 64-bit Microsoft® Windows®.
- The software suite includes graphical tools for data capture, histogram analysis, spectral analysis, and custom configuration of the ADS127L18. This suite also has a provision for exporting data to a text file for post-processing.

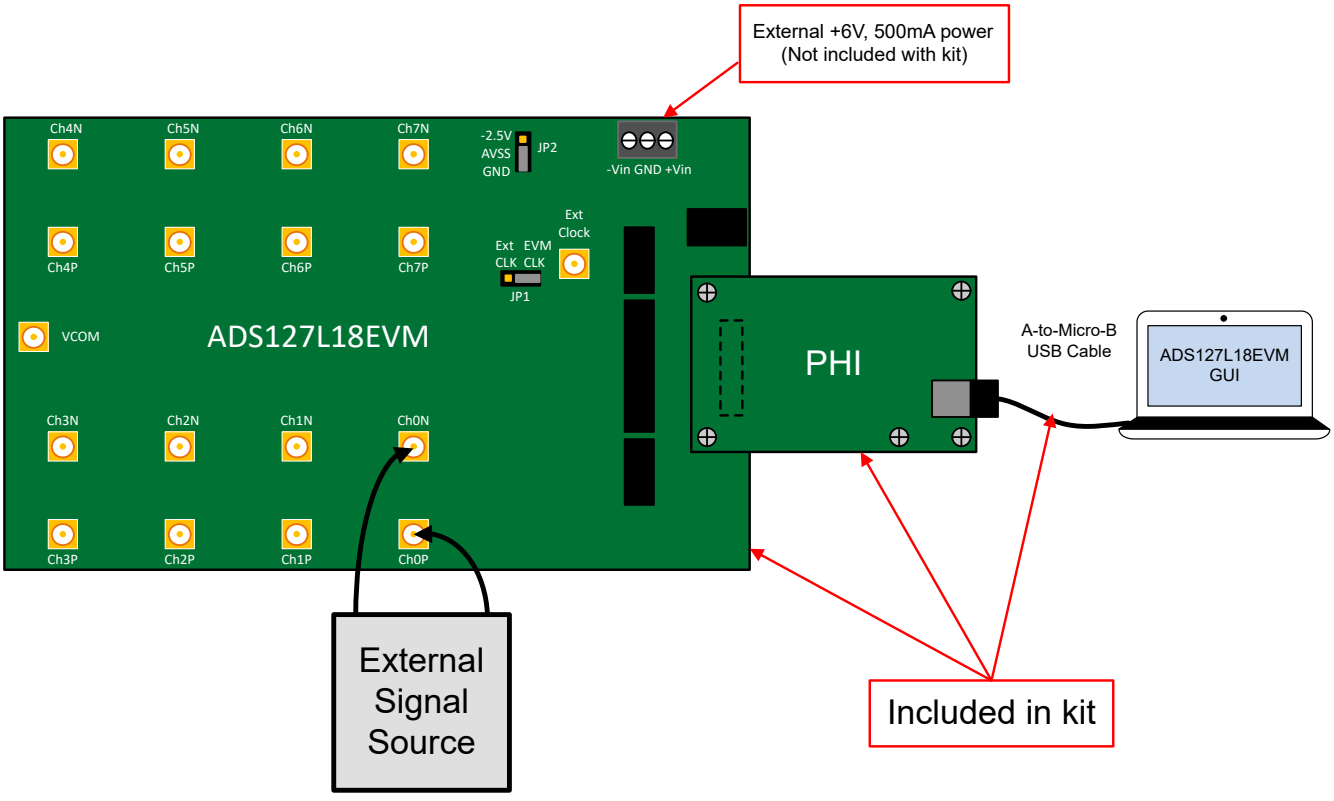


Figure 1-1. System Connection for Evaluation

Copyright © 2024 Texas Instruments Incorporated

1.3 Specification

The following specifications are applicable to the ADS127L18EVM board and the PHI board.

Table 1-1. ADS127L18EVM-PDK Specifications

PARAMETER	CONDITIONS		VALUE
Temperature	Recommended operating free-air temperature range, T_A		15°C ≤ T_A ≤ 35°C
Power supply input range (unipolar)	Recommended voltage input range for J6 or J7 (+Vin) verses GND		5.5V ≤ +Vin ≤ 6.5V
	Supply current range $\|I_s\|$		0.25A ≤ $\|I_s\|$ ≤ 0.5A
Power supply input range (bipolar)	Recommended voltage input range for J7 (-Vin) verses GND		-6.5V ≤ -Vin ≤ -5.5V
	Supply current range $\|I_s\|$		0.25A ≤ $\|I_s\|$ ≤ 0.5A
Input voltage range	Absolute input voltage verses GND for ChxP and ChxN SMA inputs		-5V ≤ Chx ≤ 5V
VCOM output	Maximum fault voltage verses GND (external source fault applied to SMA J8)		0V ≤ V_{COM} ≤ 2.6V
	VCOM output voltage verses GND (SMA J8)		2.4V ≤ V_{COM} ≤ 2.6V
EXT clock	Recommended voltage range (V_{CLK}) verses GND	Logic Level High (V_{CLKh})	1.2V ≤ V_{CLKh} ≤ 1.9V
		Logic Level Low (V_{CLKl})	0V ≤ V_{CLKl} ≤ 0.5V
	Recommended frequency range (f_{CLK})		0.5MHz ≤ f_{CLK} ≤ 33.6MHz
External digital IO	External logic levels connected to headers J3, J4, J5 verses GND	Logic Level High (V_{IOh})	1.2V ≤ V_{IOh} ≤ 1.9V
		Logic Level Low (V_{IOl})	0V ≤ V_{IOl} ≤ 0.5V
ADS127L18 AVDD1 to AVSS	Recommended voltage range (R5 removed), external source	Max-speed mode	4.5V ≤ AVDD1 ≤ 5.5V
		High-speed mode	4.5V ≤ AVDD1 ≤ 5.5V
		Mid-speed mode	3V ≤ AVDD1 ≤ 5.5V
		Low-speed mode	2.85V ≤ AVDD1 ≤ 5.5V
ADS127L18 AVDD1 to GND	Recommended voltage range (R5 removed), external source, DGND = GND		1.65V ≤ AVDD1
ADS127L18 |AVSS/AVDD1| ratio to GND	Recommended absolute ratio range, external source, DGND = GND		|AVSS/AVDD1| ≤ 1.2V/V
ADS127L18 AVDD2 to AVSS	Recommended voltage range (R6 removed), external source		1.74V ≤ AVDD2 ≤ 5.5V
ADS127L18 AVSS to GND	Recommended voltage range (JP2 2-3 position), DGND = GND		-2.75V ≤ AVSS ≤ 0V
ADS127L18 IOVDD to GND	Recommended voltage range (R7 removed), external source, DGND = GND		1.65V ≤ IOVDD ≤ 1.95V
ADS127L18 Reference REFP to AVSS	Recommended voltage range (R62, R63, R75 removed), external source	Low ref range	0.5V ≤ REFP ≤ 2.75V
		High ref range	1V ≤ REFP ≤ AVDD1

1.4 Device Information

Please refer to ADS127L18 data sheet for complete specifications.

Table 1-2. ADS127L18 Specifications

DEVICE SPECIFICATION	VALUE
Package size	7.00mm x 7.00mm
Operating temperature range	-40°C to 125°C
AVDD1 (AVSS = DGND) supply voltage	2.85V to 5.5V, Low-speed mode
AVDD2 (AVSS = DGND) supply voltage	1.74V to 5.5
IOVDD to DGND supply voltage	1.65V to 1.95V
Voltage reference inputs	0.5V to AVDD1 (AVSS = DGND)

Copyright © 2024 Texas Instruments Incorporated

2 Hardware

The ADS127L18EVM is designed for easy interfacing with analog sources. This section covers the details of the front-end circuit, including jumper configuration for different input test signals and board connectors for signal sources.

2.1 EVM Analog Input Options

For best performance, differential analog input signals can be connected through the SMA connectors CHxP and CHxN (x denotes channel numbers 0 through 7). For single-ended inputs, CHxN can be shorted to system ground using an SMA terminator plug, or shorting pins 1-2 of the corresponding channel header. The input driver circuit uses the THS4551 fully-differential amplifier in a unity-gain configuration with a single-pole RC filter at the output.

Using the default EVM reference voltage of 2.5V, each of the differential input pairs can accept up to a 5Vpp differential signal, with an offset (common mode) voltage from 0V up to +2.5V. Refer to Figure 2-1 for details.

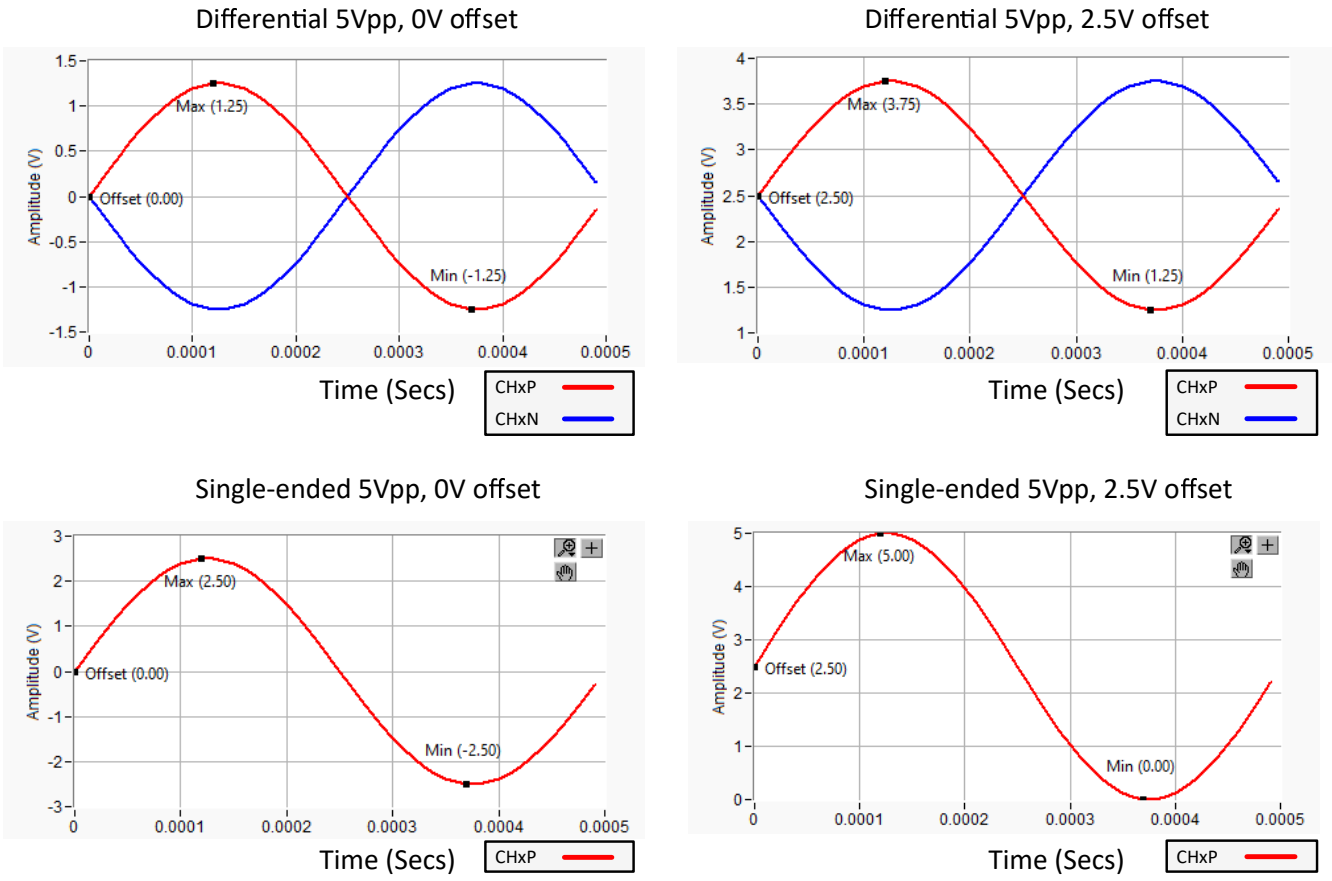


Figure 2-1. Maximum input signal range (Vref = 2.5V)

Copyright © 2024 Texas Instruments Incorporated

2.2 Power Requirements

The ADS127L18EVM requires an external power source. A standard lab supply capable of providing a single +6V, 500mA output connected to J7, screw terminals GND and +Vin can be used. Another option is to use an AC Power adapter (SMI18-5.9-V-P5 or equivalent) connected to barrel connector J6. Either of these power supply options support the default unipolar operation of the ADS127L18EVM.

Optionally, an additional -6V, 500mA source can be connect to the -Vin screw terminal of J7 if full bipolar operation of the ADS127L18EVM is required. In bipolar power operation, move jumper JP2 to the -2.5V:AVSS position. Figure 2-2 shows the details of the power connection options.

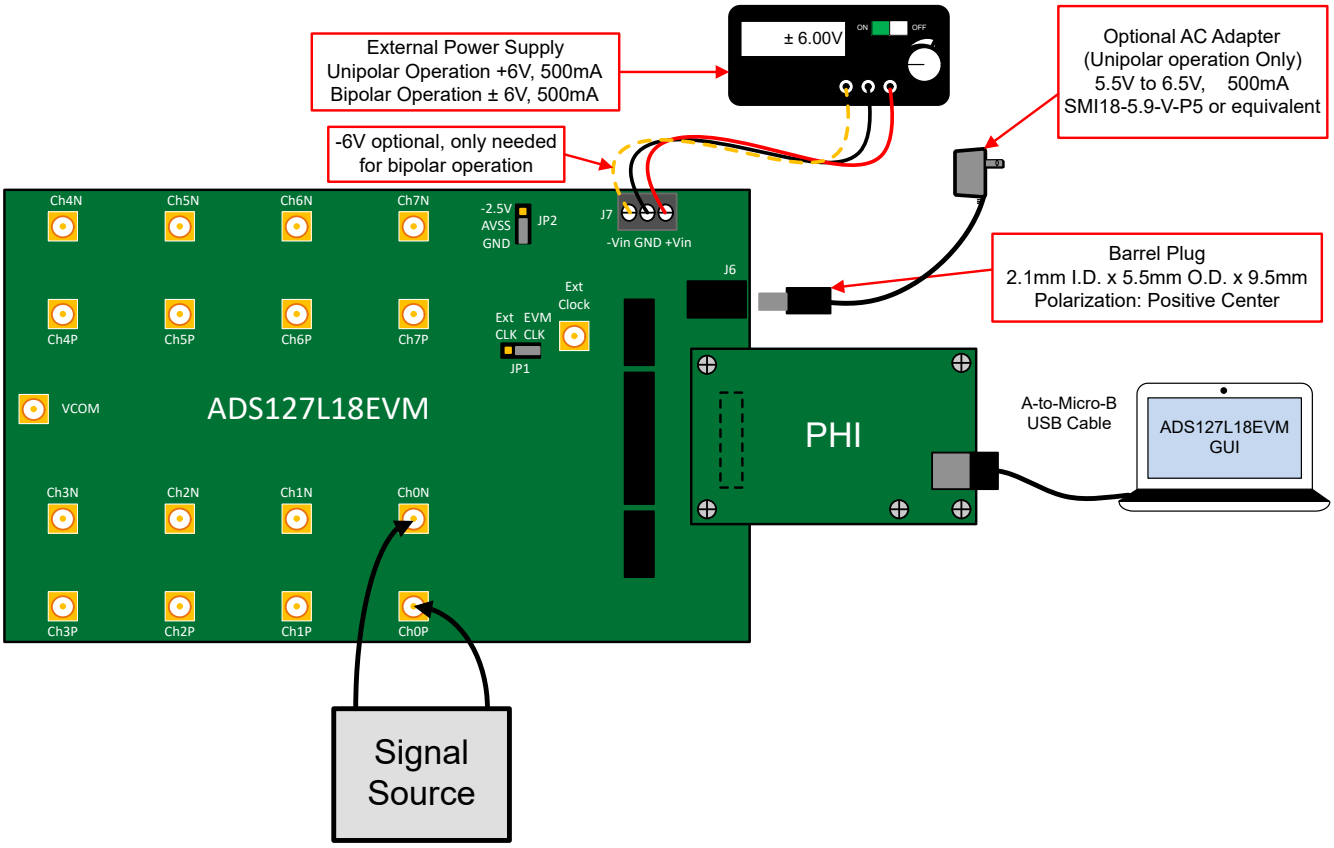


Figure 2-2. Power Connections

Copyright © 2024 Texas Instruments Incorporated

2.3 ADC Connections and Decoupling

Figure 2-3 shows all connections to the ADS127L18 data converter (U1). Each power supply connection has a 10µF decoupling capacitor. Make sure these capacitors are physically close to the device and have a good connection to the GND plane. The supply connections also have a series 0Ω resistor. The purpose of this component is to facilitate current measurement for the ADC. Each digital pin has a 10Ω series resistor. These resistors smooth the edges of the digital signals to provide minimal overshoot and ringing. Also, each digital pin has a 100kΩ pull-up or pull-down resistor. These resistors are installed to minimize connections to an FPGA development board. Although not strictly required, these components can be included in the final design to improve digital signal integrity.

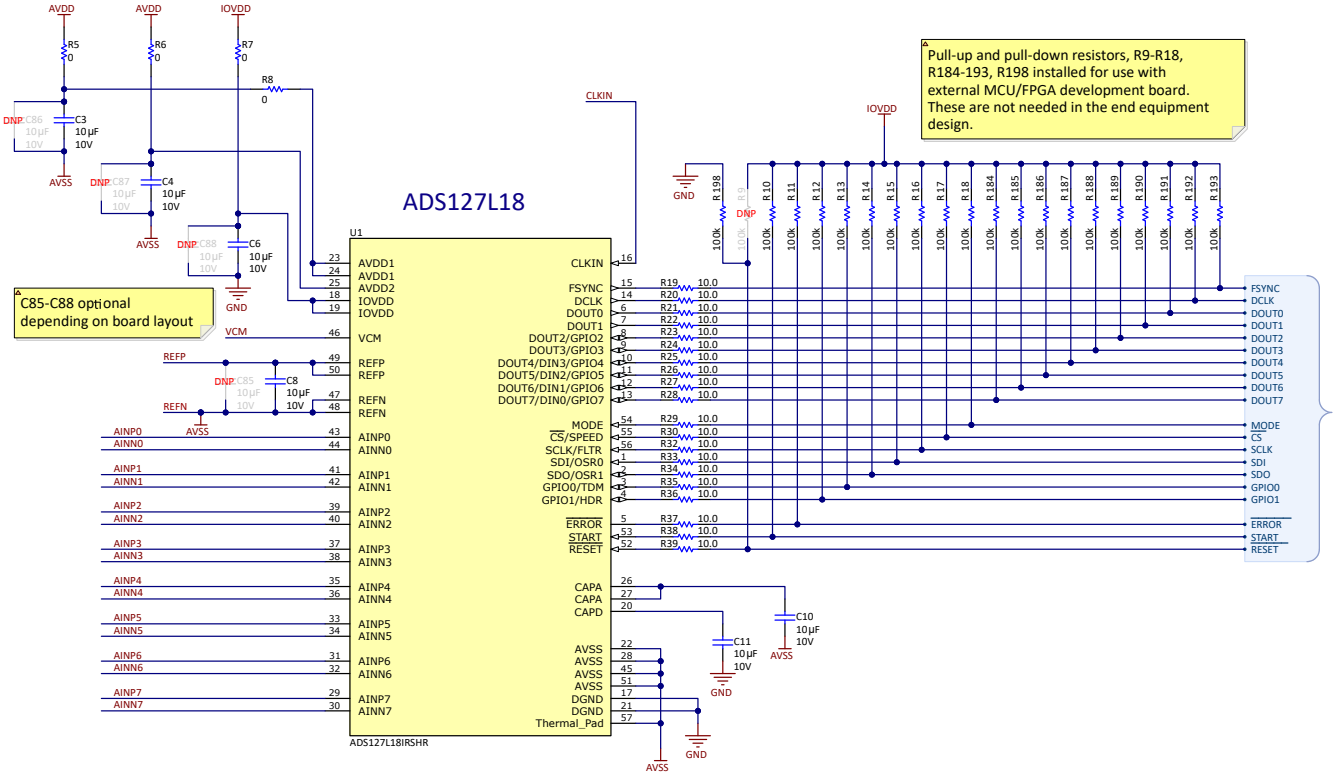


Figure 2-3. ADS127L18 Connections and Decoupling

Copyright © 2024 Texas Instruments Incorporated

2.4 ADC Input Amplifiers

Figure 2-4 shows the fully differential amplifier circuit (THS4551) that drives each of the ADC input channels 0 through 7. All input channel configurations are identical but only channel 0 is shown. The input signal applied to J11 (Ch0P) and J9 (Ch0N) must be a low-distortion differential signal. The common-mode output for the amplifier is controlled by pin 7 on U10 (VOCM). The common-mode signal is set by the data converter (pin 46, VCM). The output of the amplifier connects to an RC filter that connects to the ADC input (R84, R88, C40, C38, and C41). The amplified configuration has several do-not-populate (DNP) components. These components provide flexibility, but are not required for good performance. The amplifier power supplies are connected to the AVDD and AVSS supplies that are also used for the ADC.

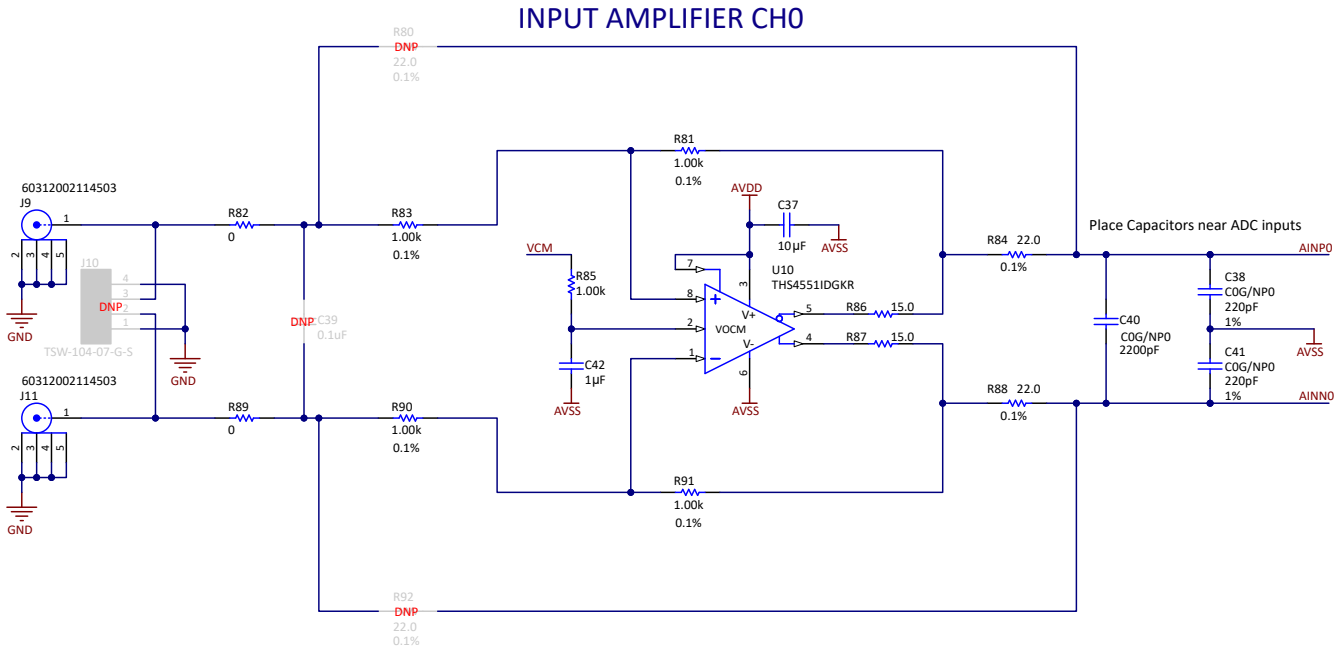


Figure 2-4. ADC Input Amplifier

Copyright © 2024 Texas Instruments Incorporated

2.5 VCOM Buffer

The circuit shown in Figure 2-5 buffers the VCM signal from the ADC and connects this signal to the J8 SMA connector. This process is useful if the VCOM signal must be connected to an external piece of test equipment to set the common-mode voltage. A common use case is to connect this signal to the Audio Precision SYS-2722 to set the signal generator's common-mode output. This circuit is not required in the end application and is only used for testing purposes.

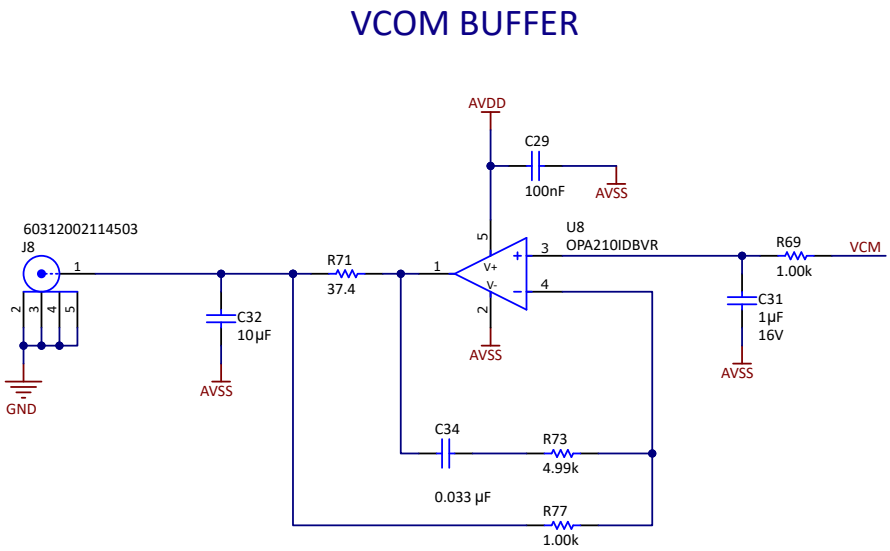


Figure 2-5. VCOM Buffer

2.6 Voltage Reference

Figure 2-6 shows the REF6225 and REF7040 configuration. By default, the REF6225 is connected to the ADS127L18 through the 0Ω resistor R62. The REF6225 includes an integrated wide bandwidth buffer that is capable of driving the switched-capacitor input to the ADS127L18 without the need for an additional buffer. The REF6225 is sufficient to meet the ADS127L18 data sheet specifications for dynamic performance.

The REF7040 is not populated, but can be added to the board if needed. The REF7040 can be configured to directly drive the ADS127L18 reference input by removing resistor R62 and populating resistor R63. This option provides good DC performance, but AC performance is not the best. For best AC and DC performance using the REF7040, the external reference buffer can be used. Please refer to Section 2.7 for more details.

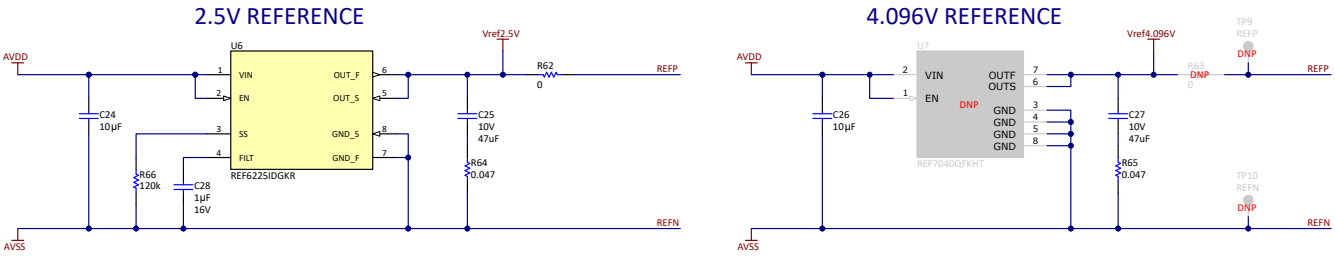


Figure 2-6. Onboard Voltage Reference

Copyright © 2024 Texas Instruments Incorporated

2.7 Reference Buffer

Figure 2-7 shows the onboard reference buffer. The OPA211 amplifier U9 was selected for low voltage offset, low offset drift, and low noise. The amplifier topology is designed to drive capacitive loads. For information on this topology, see the Op Amp Stability Videos in TI Precision Labs. The default connection for the reference buffer input is the REF7040 reference output through resistor R76. To connect the reference buffer output to the ADS127L18 input, populate resistor R75 and remove resistors R62 and R63.

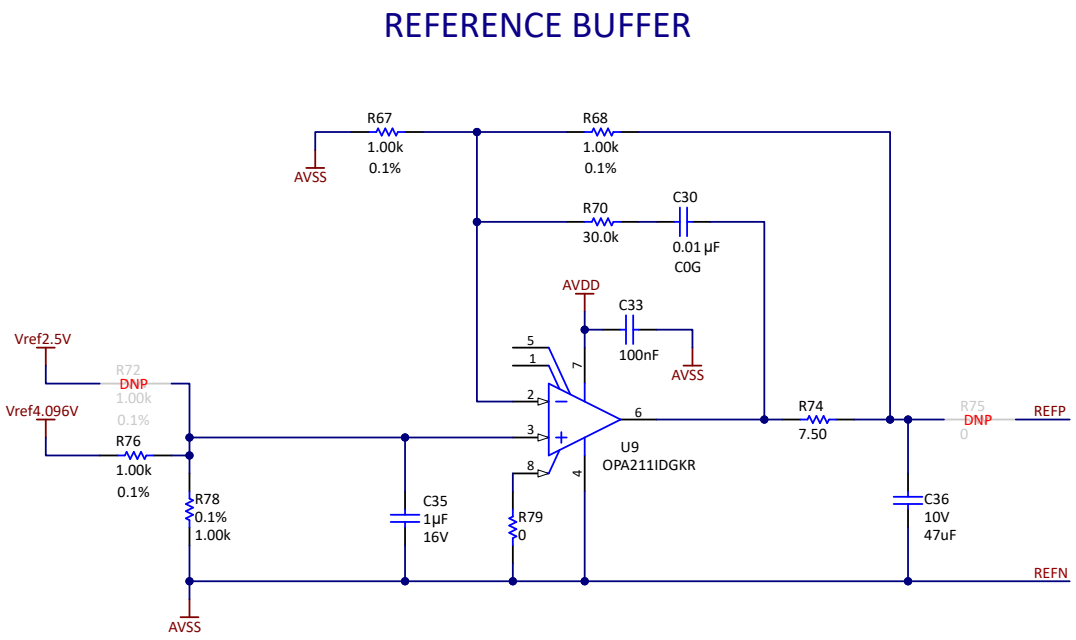


Figure 2-7. Reference Buffer

Copyright © 2024 Texas Instruments Incorporated

2.8 Clock Tree

Figure 2-8 shows the different clock options for the ADS127L18EVM that are selected by jumper JP1. The default setting for JP1 is the 2-3 position (EVM CLK), which enables the local 32.768MHz oscillator (Y1) on the ADS127L18EVM board. This clock is routed to the clock input of the ADS127L18 to support all speed modes. Moving JP1 to the 1-2 position (EXT CLK) allows an external clock supplied on the SMA connector (J2). Use a CMOS square-wave signal with an amplitude equal to 1.8V (IOVDD) and a frequency within the specified range of the ADS127L18.

CAUTION

The maximum operating voltage level for the clock input (J2) is 1.95V. Exceeding this voltage level or applying a clock input before the ADS127L18EVM has been powered-up can cause permanent damage to the ADS127L18.

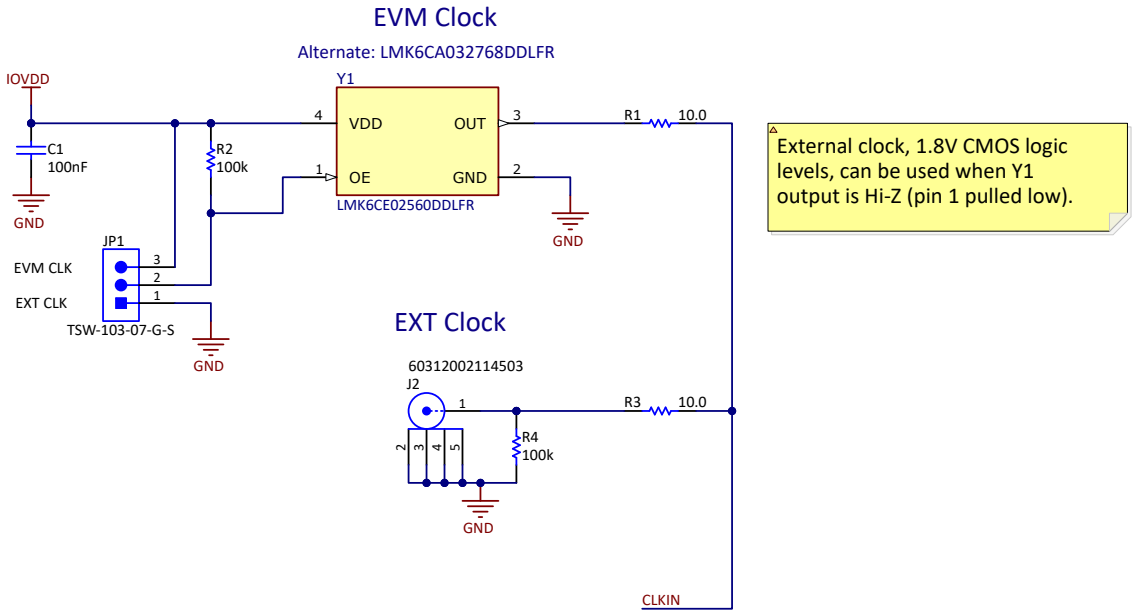


Figure 2-8. Clock Tree

Copyright © 2024 Texas Instruments Incorporated

2.9 Serial Interface

Figure 2-9 shows the digital connections between the ADS127L18EVM and the PHI. The ADS127L18 ADC uses SPI serial communication in mode 1 (CPOL = 0, CPHA = 1) to configure the internal registers and a Frame-Sync Data Port for conversion data. Because the serial clock (SCLK) frequency and data clock (DCLK) frequency can be as fast as 32.768MHz, the ADS127L18EVM offers 10Ω resistors between the digital signals to aid with signal integrity. Typically, in high-speed SPI and Frame-Sync communication, fast signal edges can cause overshoot; these 10Ω resistors slow down the signal edges to minimize signal overshoot. Headers J3, J4, and J5 provides test points to measure the digital signals or to connect the ADS127L18EVM to an FPGA development board.

CAUTION

The maximum operating voltage level for the digital signals on headers J3, J4, and J5 is 1.95V. Exceeding this voltage level or applying a digital signal before the ADS127L18EVM has been powered-up can cause permanent damage to the ADS127L18.

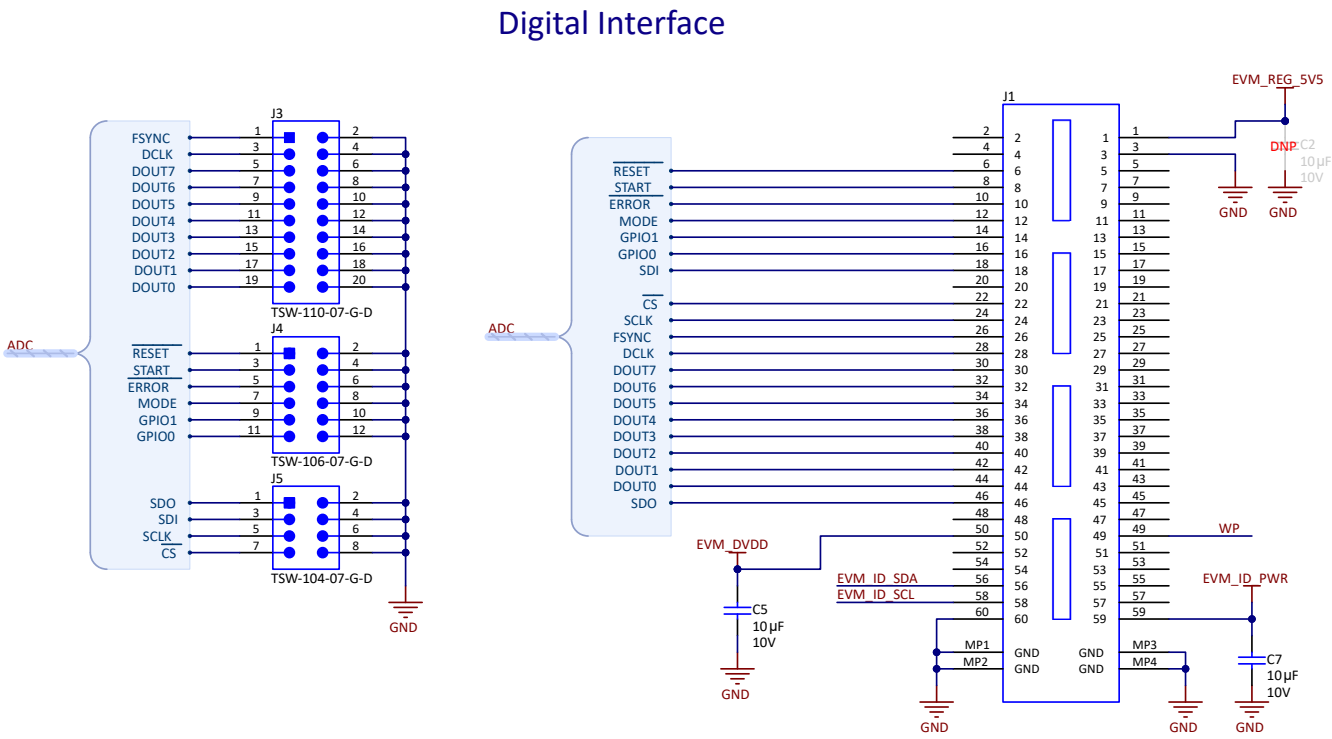


Figure 2-9. Connections to Digital Signals on PHI and Test Points

Copyright © 2024 Texas Instruments Incorporated

2.10 EEPROM

The circuit shown in Figure 2-10 is used with the EVM controller (PHI) for EVM identification only. The EEPROM communicates with the PHI over an I2C bus and is not shared with the ADS127L18. This circuit is not required by the ADS127L18 for operation and is powered down when not used with the PHI.

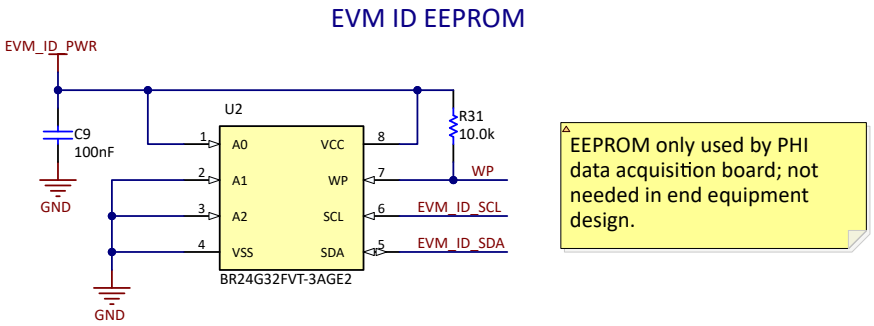


Figure 2-10. EEPROM for EVM ID

2.11 Power Supplies

Figure 2-11 shows the connection options for the external power supply that is required for normal EVM operation.

The EVM supports two different power configurations: unipolar, where the ADS127L18 AVDD supply is set to 5V, and AVSS is connected to GND; and bipolar operation, where AVDD is set to +2.5V and AVSS is set to -2.5V. Please refer to Section 2.2 for more details.

In unipolar operation mode, a single external supply voltage can be used. Either an external lab supply set to +6V can be connected to screw terminal J7, pin 1 (+6V) and pin 2 (GND), or an external power adapter can be connected to barrel connector J6.

In bipolar operation mode, a dual output lab supply must be used. The external lab supply must be set to +6V, -6V and connected to screw terminal J7, pin 1 (+6V), pin 2 (GND), and pin 3 (-6V).

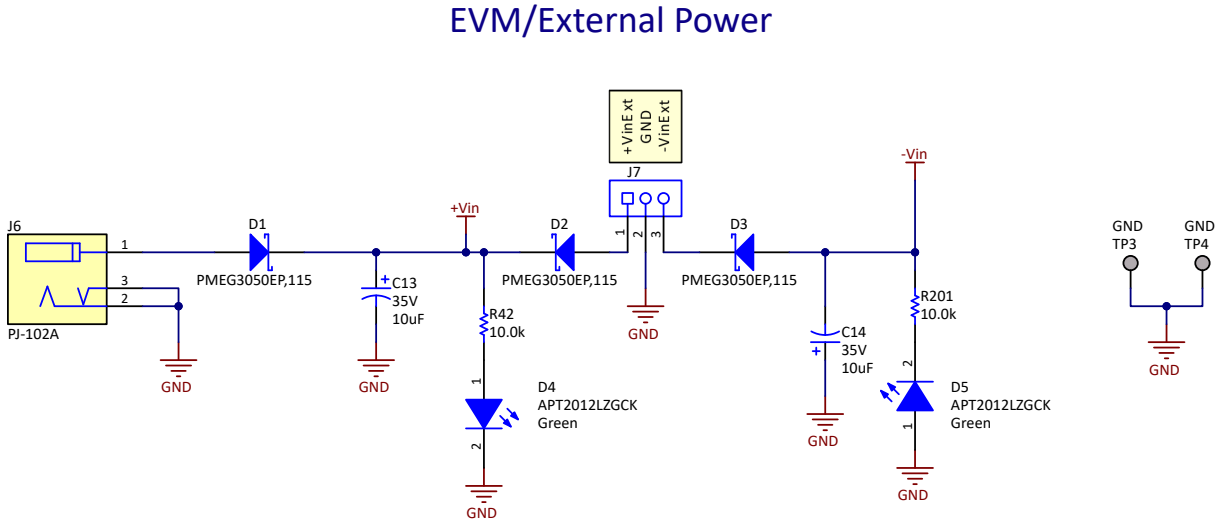


Figure 2-11. External Power Supply Connections

Copyright © 2024 Texas Instruments Incorporated

2.12 Low Dropout Regulator (LDO)

Figure 2-12 shows how the ADS127L18 AVDD, AVSS, and IOVDD supplies are generated. Power is provided by an external supply on either J7 or J6; refer to Section 2.11 and Figure 2-11 for more details. AVDD and IOVDD are regulated to 5V and 1.8V, respectively, using low-noise TPS7A47 LDOs. The 5V LDO output is used for the AVDD connections and can be reprogrammed to different output voltages using R44, R45, R46, R47, R48, R49 and R50. The 1.8V LDO is used for IOVDD and can be reprogrammed from 1.7V to 1.9V only.

An additional LDO generates –2.5V for AVSS using the low-noise TPS7A30 LDO. This LDO is only supplied by external power on J7. By default, AVSS is connected to GND with a shunt on jumper JP2, position 1-2. If AVSS is set to –2.5V for bipolar operation, connect an external negative supply to J7 and move the shunt on jumper JP2 to position 2-3. In this configuration, the voltage level for AVDD does not need to be changed. The 5V LDO is referenced to AVSS, so setting AVSS = -2.5V also changes the AVDD supply to 2.5V (with respect to GND).

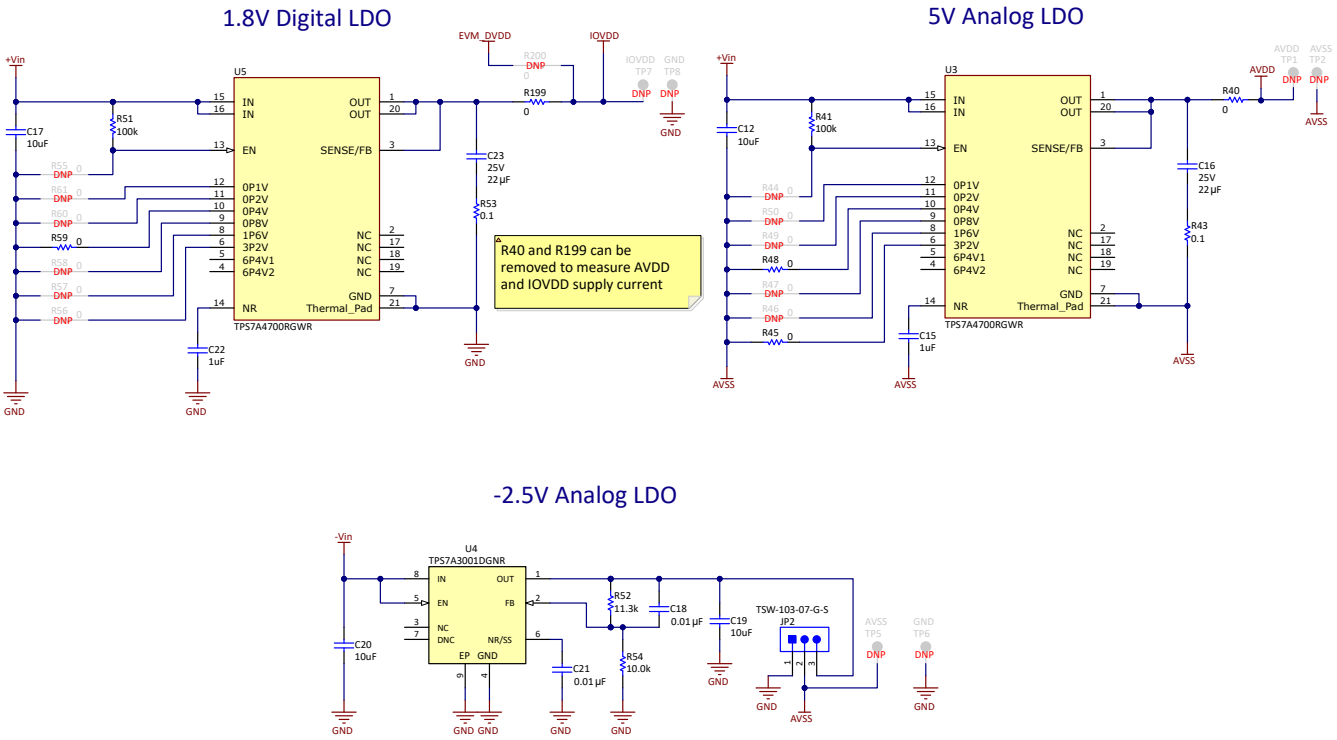


Figure 2-12. LDO Regulators 5V, 1.8V, -2.5V

Copyright © 2024 Texas Instruments Incorporated

3 Software

3.1 Software Description

The ADS127L18EVM-PDK-GUI software suite includes graphical tools for data capture, full ADS127L18 register configuration, time domain analysis, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file for post-processing.

3.2 ADS127L18 EVM Software Installation

Download the latest version of the EVM GUI installer from the Tools and Software folder of the ADS127L18EVM and run the GUI installer to install the EVM GUI software on your computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message can possibly appear or the installer.exe file can be deleted.

As shown in Figure 3-1, accept the license agreement and follow the on-screen instructions to complete the installation. If the LabVIEW™ run-time engine has not already been installed, then a prompt shows to accept this license agreement and to reboot the computer to complete installation.

Copyright © 2024 Texas Instruments Incorporated

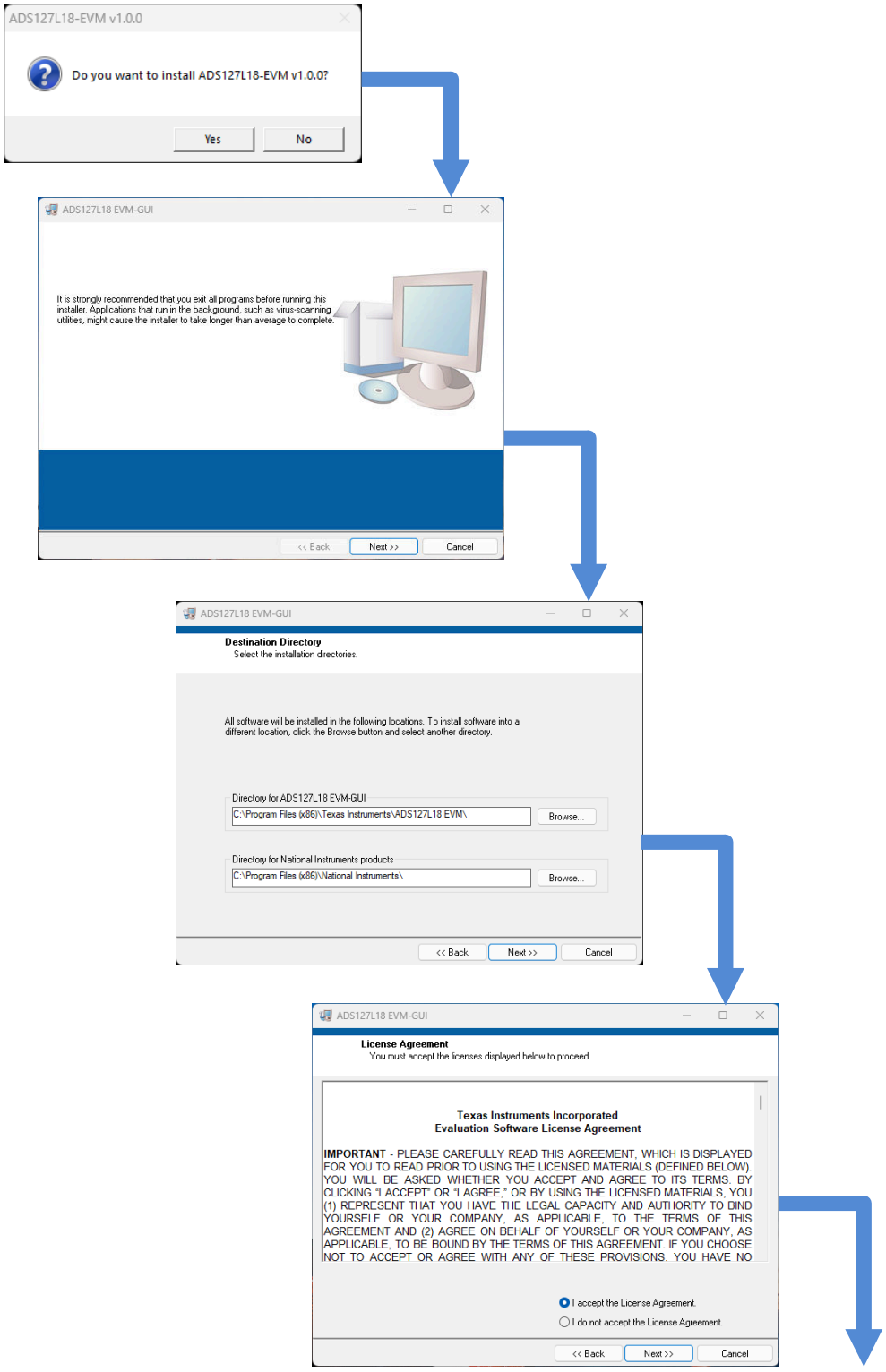


Figure 3-1. Software Installation and Prompts (1)

Copyright © 2024 Texas Instruments Incorporated

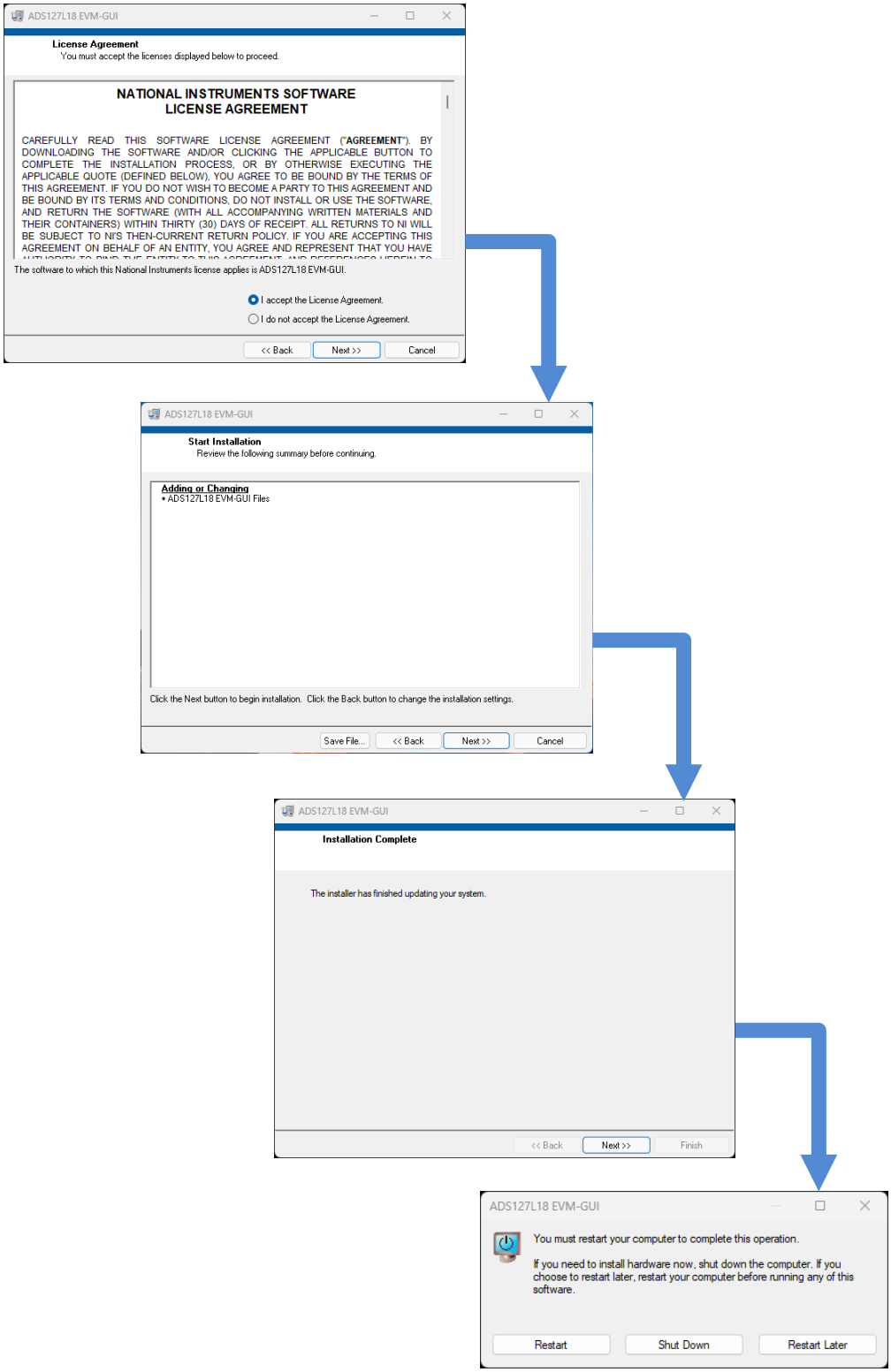


Figure 3-2. Software Installation and Prompts (2)

Copyright © 2024 Texas Instruments Incorporated

4 Implementation Results

4.1 EVM Operation

4.1.1 Evaluation Setup

Connect the EVM as shown in Figure 4-1 after installing the software:

1. Physically connect P2 of the PHI to J1 of the ADS127L18 EVM. Install the included screws to provide a robust connection.
2. Connect an external +6V, 0.5A lab supply to J7 or connect an AC power adapter rated for 6V, 0.5A to J6 such as SMI18-5.9-V-P5 or equivalent.
3. Connect the USB connector on the PHI to the computer.
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
   b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC; Figure 4-1 shows the resulting LED indicators.
4. Start the software GUI as shown in Figure 4-2. Notice that the LEDs blink slowly when the FPGA firmware is loaded on the PHI. This loading takes a few seconds.
5. Connect the differential signal generator. The full scale input range is ±2.5V differential and a common mode from 0V to 2.5V. A common input signal applied is a 4.8VPP signal. This signal is adjusted just below the full-scale range to avoid clipping.

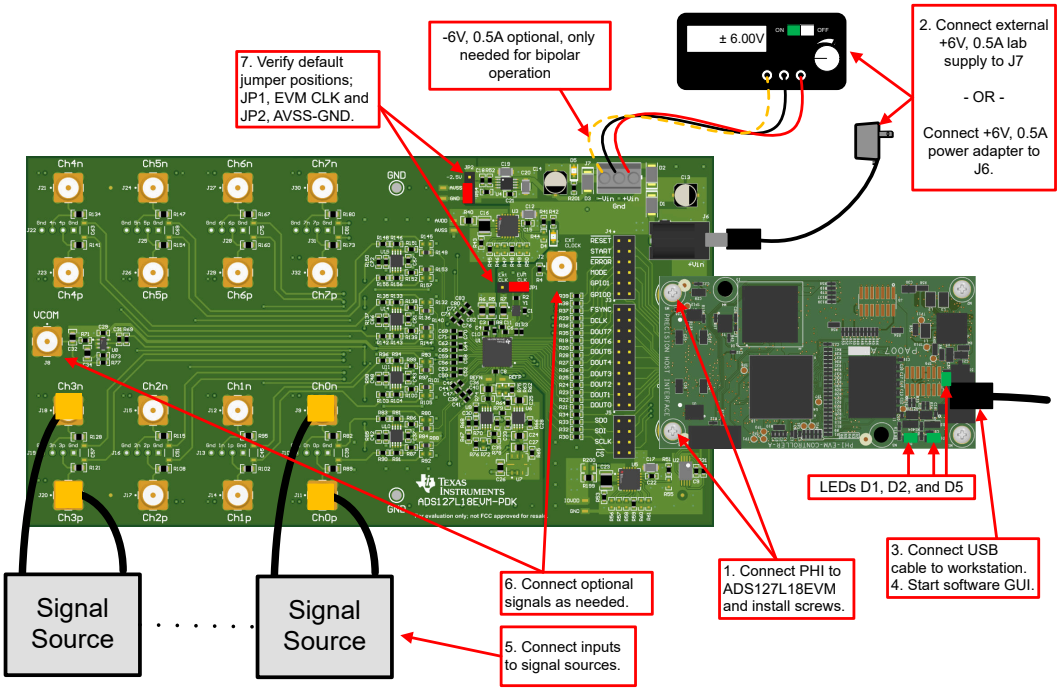


Figure 4-1. Connecting the Hardware to the ADS127L18EVM

Copyright © 2024 Texas Instruments Incorporated

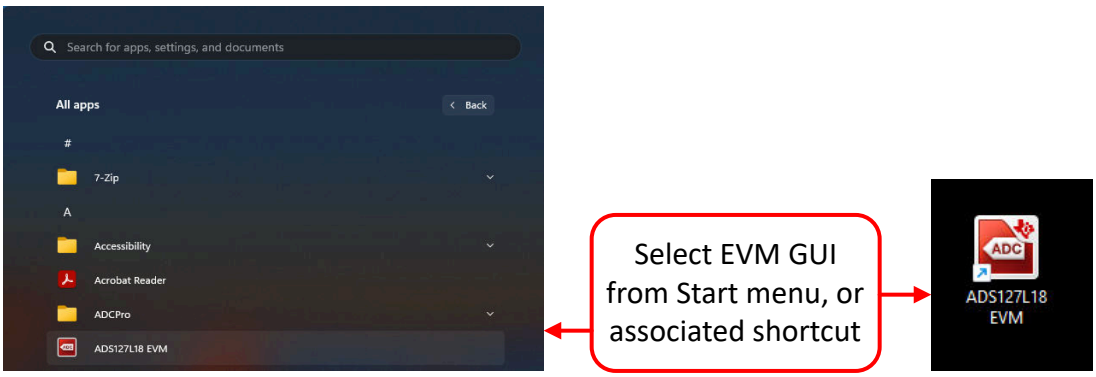


Figure 4-2. Launch the ADS127L18EVM GUI Software

4.1.2 Optional EVM Connections

Figure 4-3 shows optional connections to the power, clock, and VCM. These connections are not required for initial setup of the EVM but can be helpful to configure the EVM more closely to the end application configuration. Review the schematic and hardware sections of this document to understand how these connections are used.

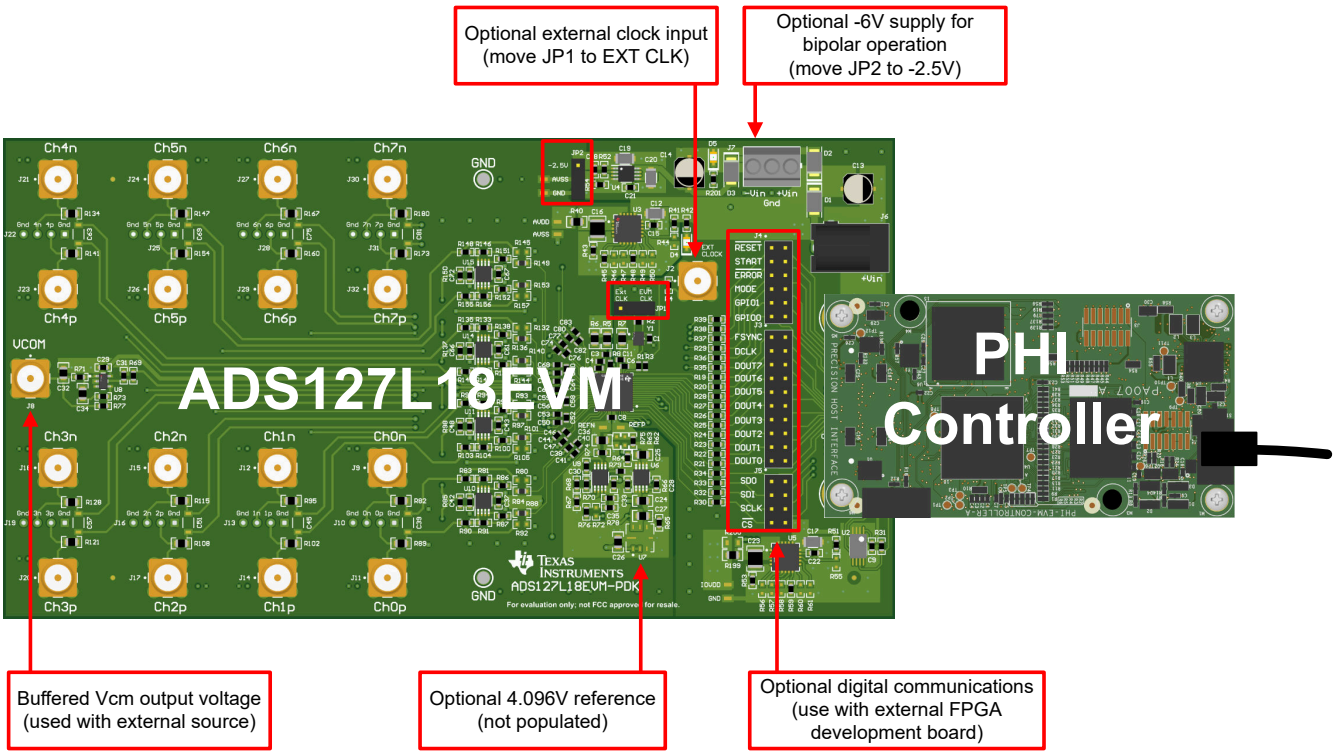


Figure 4-3. Optional EVM Connections

Copyright © 2024 Texas Instruments Incorporated

4.1.3 EVM Register Settings

Figure 4-4 shows the ADC register settings. The registers can be used to set the different device modes (such as filter settings and power settings). This page can be accessed by selecting the Register Configurations under Pages on the left side of the GUI.

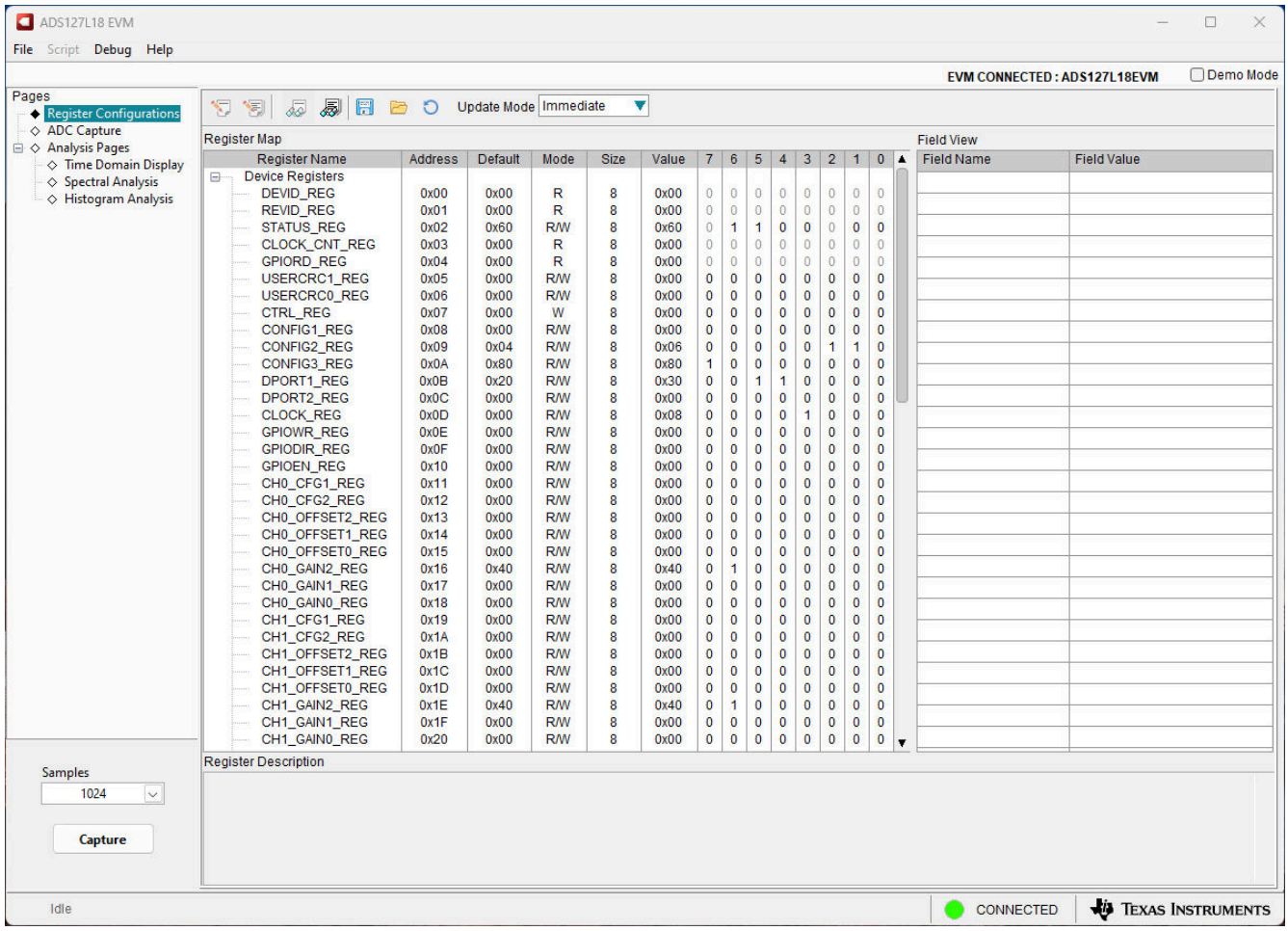


Figure 4-4. EVM Register Configuration

Copyright © 2024 Texas Instruments Incorporated

4.1.4 ADC Capture Settings

The ADC Capture Settings page allows easy configuration of multiple ADC settings and is an alternative method to using the Register Configurations page. There are multiple tabs on the ADC Capture Settings page, including ADC, Clocking, SPI and Data Port, Filter, and Channel. Changing these settings also updates the values on the Register Configuration page. These tabs are discussed in more detail in the following sections.

4.1.4.1 ADC Configuration

Figure 4-5 shows the ADC Configuration tab that allows the user to quickly select the Reference range, enable the Reference buffer, VCM buffer, Auto Standby mode, Average mode, and to adjust the digital IO drive strength. Under the Waveform Settings, the Reference Voltage value can be updated if a different reference voltage is used from the default 2.5V EVM configuration. Please refer to the ADS127L18 data sheet for more details on the function of these settings.

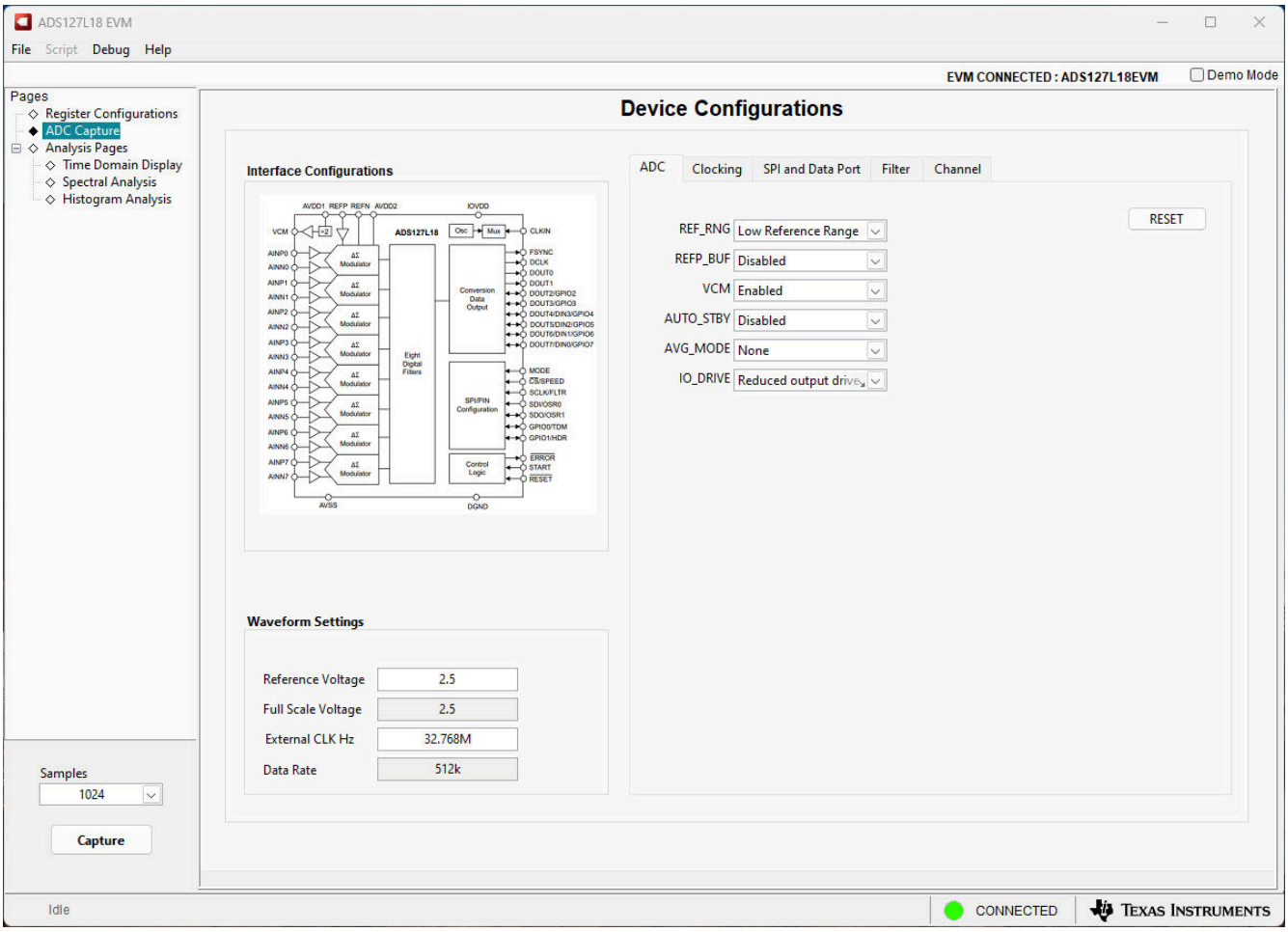


Figure 4-5. ADC Configuration

Copyright © 2024 Texas Instruments Incorporated

4.1.4.2 Clocking Configuration

Figure 4-6 shows the Clocking Configuration tab that allows the user to quickly select the different clock options for both the ADC modulator, data port, and other timing configurations. Under the Waveform Settings, the External Clock value can be updated if a different clock frequency is used from the default 32.768MHz EVM configuration. Updating the External Clock value also updates the calculated Data Rate. Please refer to the ADS127L18 data sheet for more details on the function of these settings.

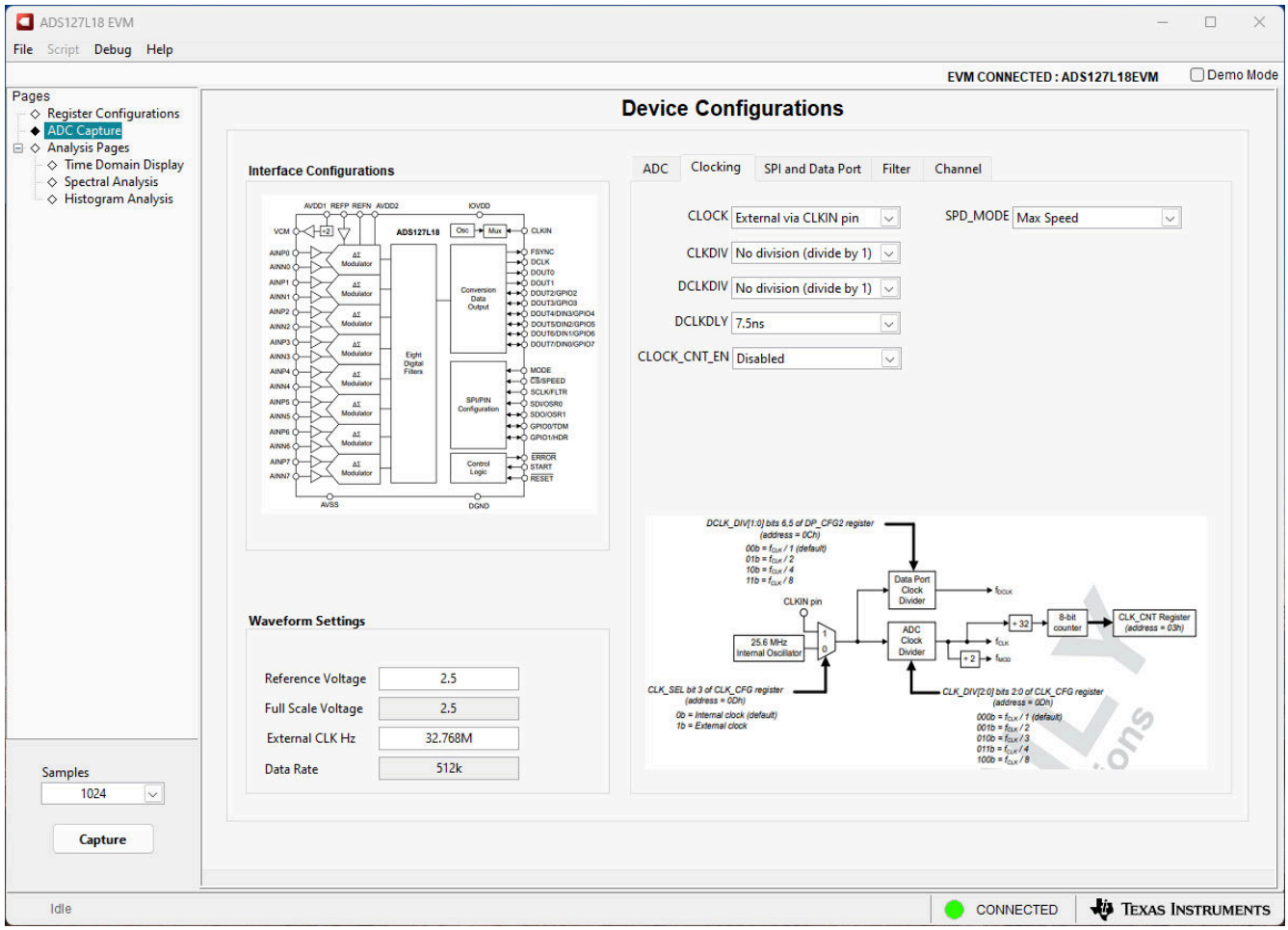


Figure 4-6. Clocking Configuration

Copyright © 2024 Texas Instruments Incorporated

4.1.4.3 SPI and Data Port Configuration

Figure 4-7 shows the SPI and Data Port Configuration tab that allows the user to quickly select the different communication options. The user can enable multiple CRC checks, configure the Data Port to 1, 2, 4, or 8 lanes of data, and multiple other options. The EVM GUI Software only supports the default options for data capture; selecting different configurations can result in the software not working correctly. Please refer to the ADS127L18 data sheet for more details on the function of these settings.

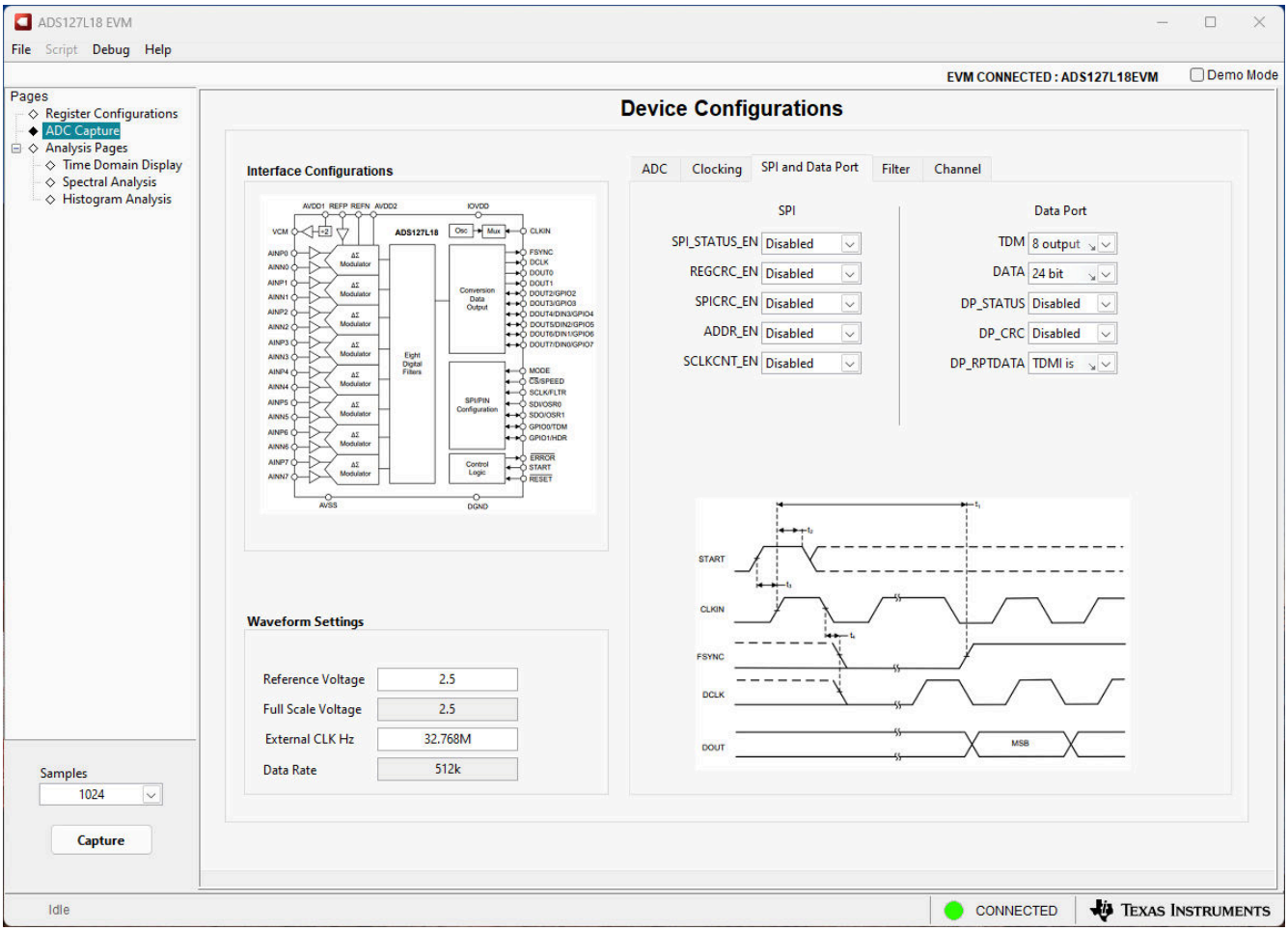


Figure 4-7. SPI and Data Port Configuration

Copyright © 2024 Texas Instruments Incorporated

4.1.4.4 Filter Configuration

Figure 4-8 shows the Filter Configuration tab that allows the user to quickly select the different filter options for each of the 8 channels, including both wideband filters and multiple SINC filter options. Please refer to the ADS127L18 data sheet for more details on the function of these settings.

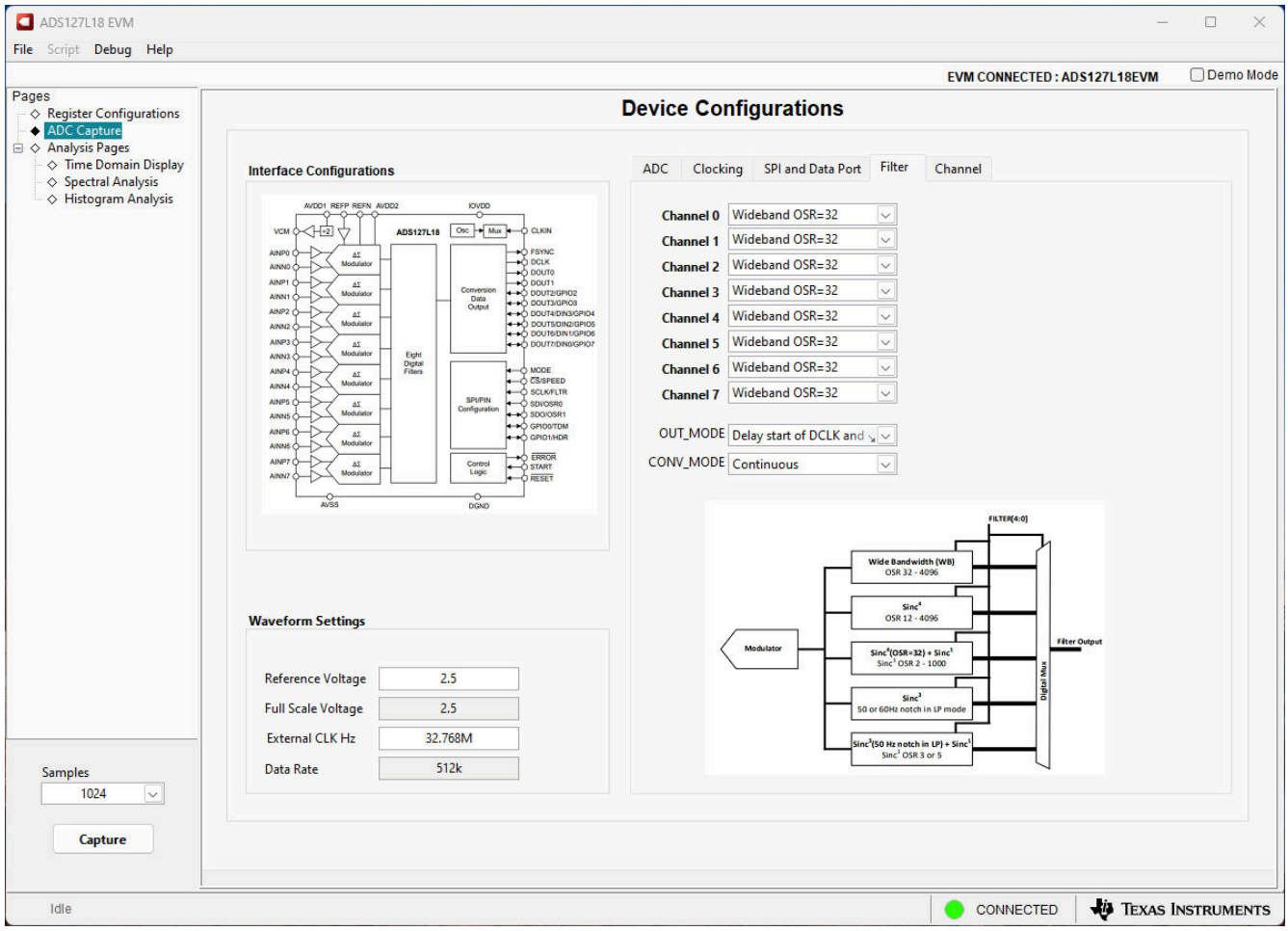


Figure 4-8. Filter Configuration

Copyright © 2024 Texas Instruments Incorporated

4.1.4.5 Channel Configuration

Figure 4-9 shows the Channel Configuration tab that allows the user to quickly select the different options for each of the 8 channels, including input configuration, input buffer enable, input range, and channel power-down. Please refer to the ADS127L18 data sheet for more details on the function of these settings.

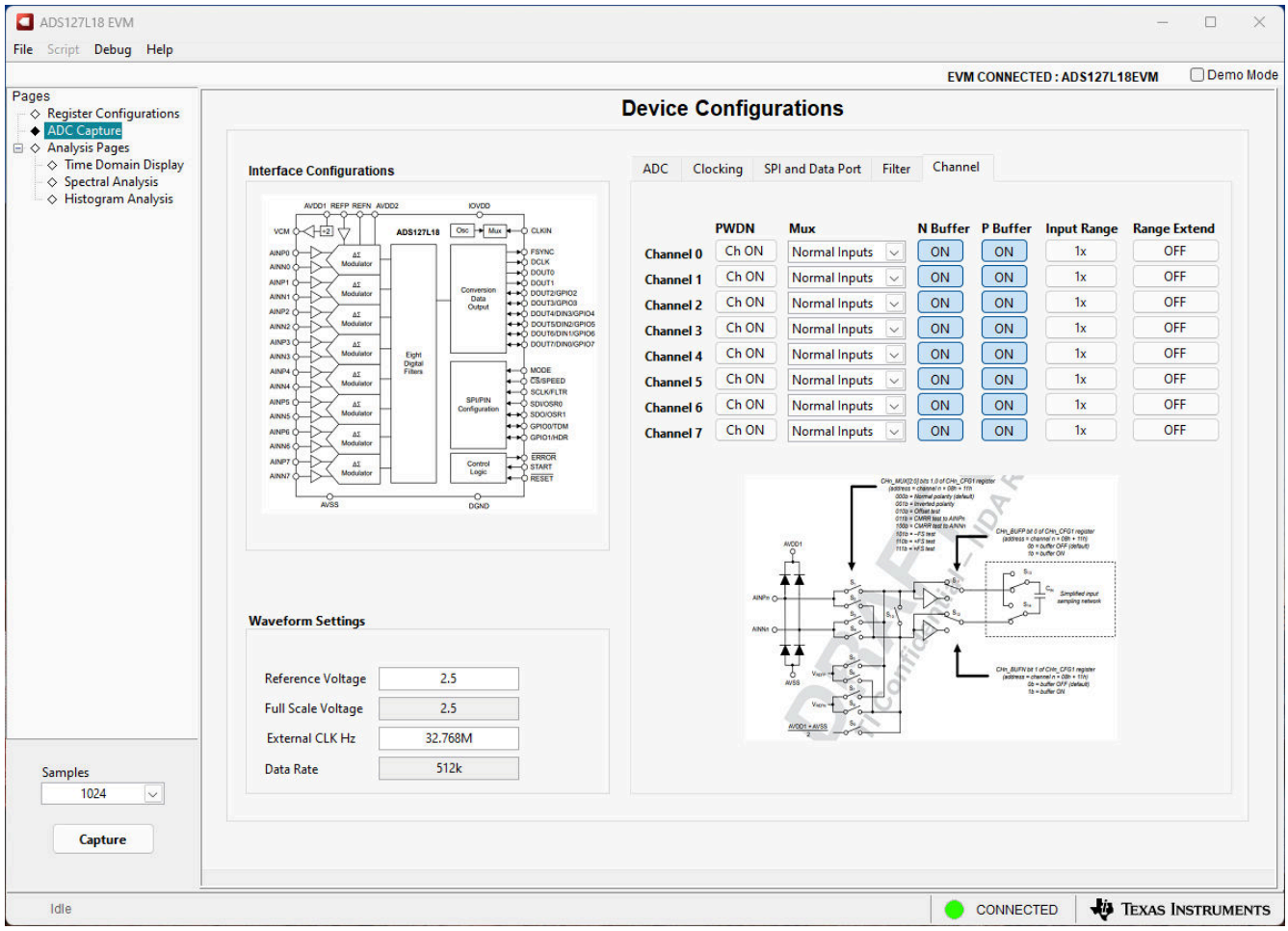


Figure 4-9. Channel Configuration

Copyright © 2024 Texas Instruments Incorporated

4.1.5 Time Domain Display

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior of and debugging any gross problems with the ADC or drive circuits. The user can trigger a capture of the data of the selected number of samples from the ADS127L18EVM, as per the current interface mode settings indicated in Figure 4-10 by using the *Capture* button. The sample indices on the x-axis and the y-axis show the corresponding equivalent analog voltages based on the specified reference voltage. Switching pages to any of the analysis tools described in the subsequent sections causes calculations to be performed on the same set of data.

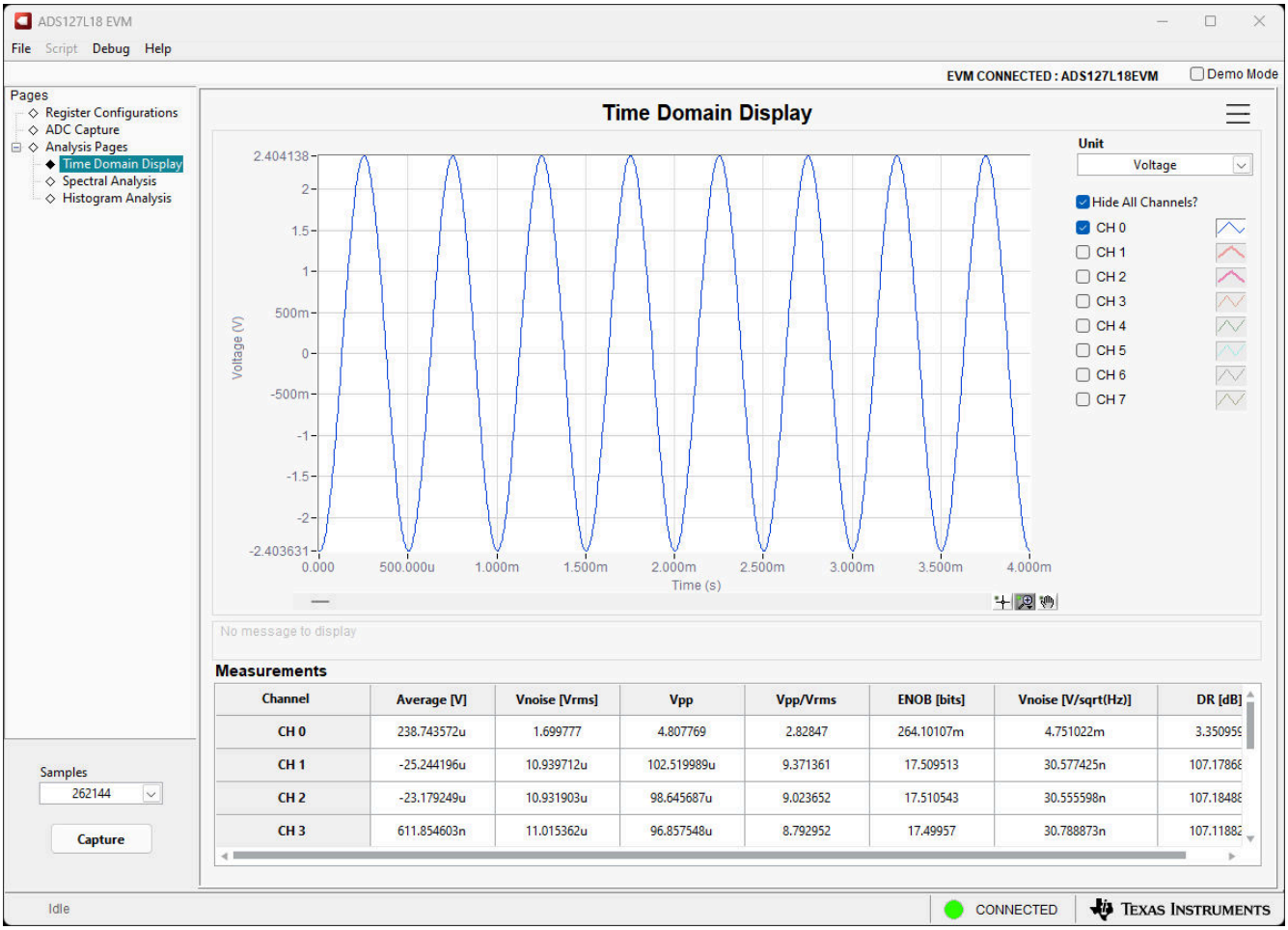


Figure 4-10. Time Domain Display

Copyright © 2024 Texas Instruments Incorporated

4.1.6 Spectral Analysis Display

The spectral analysis tool, shown in Figure 4-11, is intended to evaluate the dynamic performance (SNR, THD, THD+N, SFDR, and Dynamic Range) of the ADS127L18 ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-Term Blackman-Harris window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The *Rectangle* option corresponds to not using a window (or a rectangular window) and is not recommended.

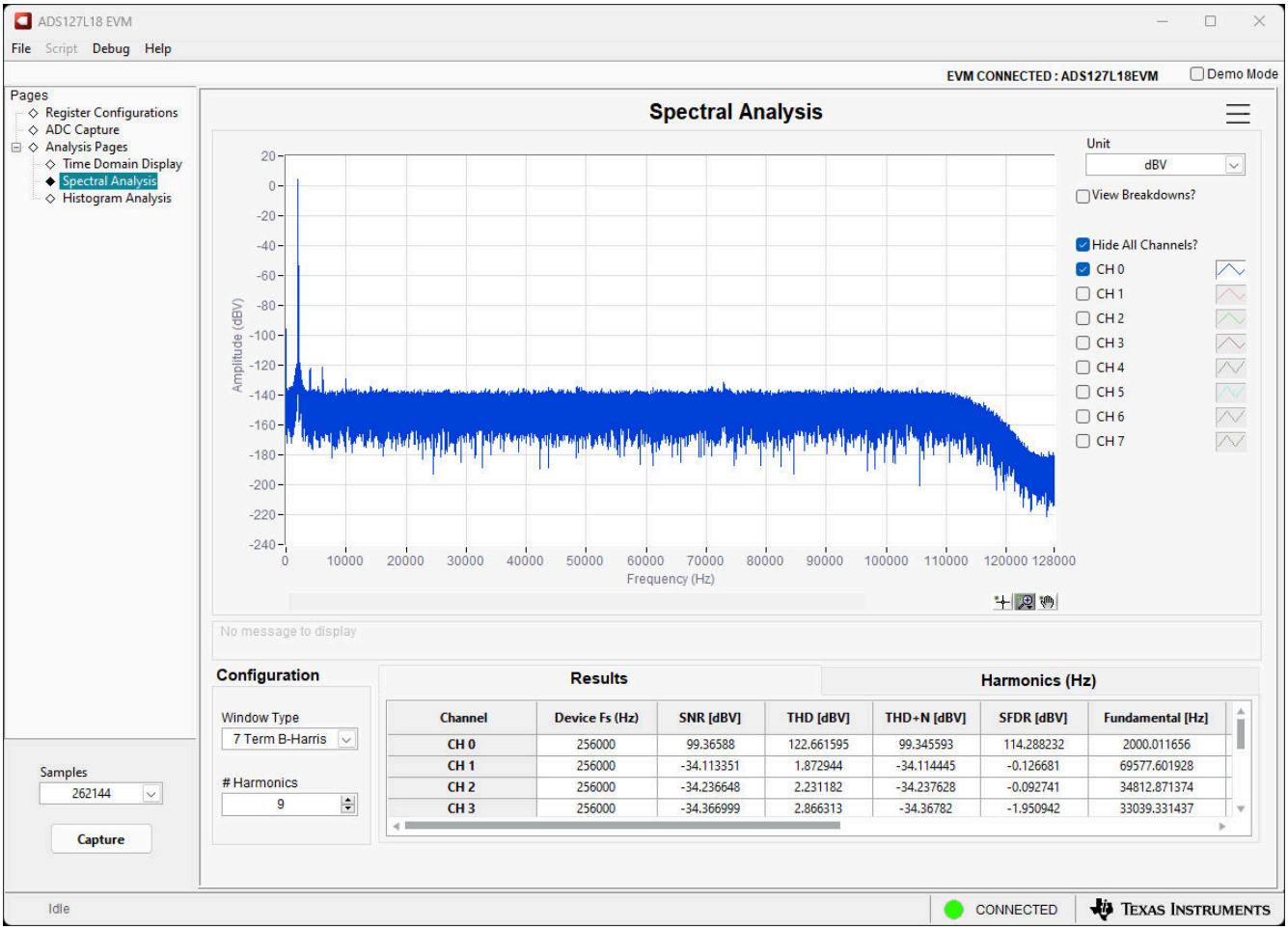


Figure 4-11. Frequency Domain Display

Copyright © 2024 Texas Instruments Incorporated

4.1.7 Histogram Analysis Display

Noise degrades ADC resolution and the histogram tool can be used to estimate effective resolution. The cumulative effect of noise coupling to the ADC output from sources (such as the input drive circuits, reference drive circuit, ADC power supply, and the ADC) is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel. As shown in Figure 4-12, the histogram corresponding to a dc input is displayed on clicking the *Capture* button.

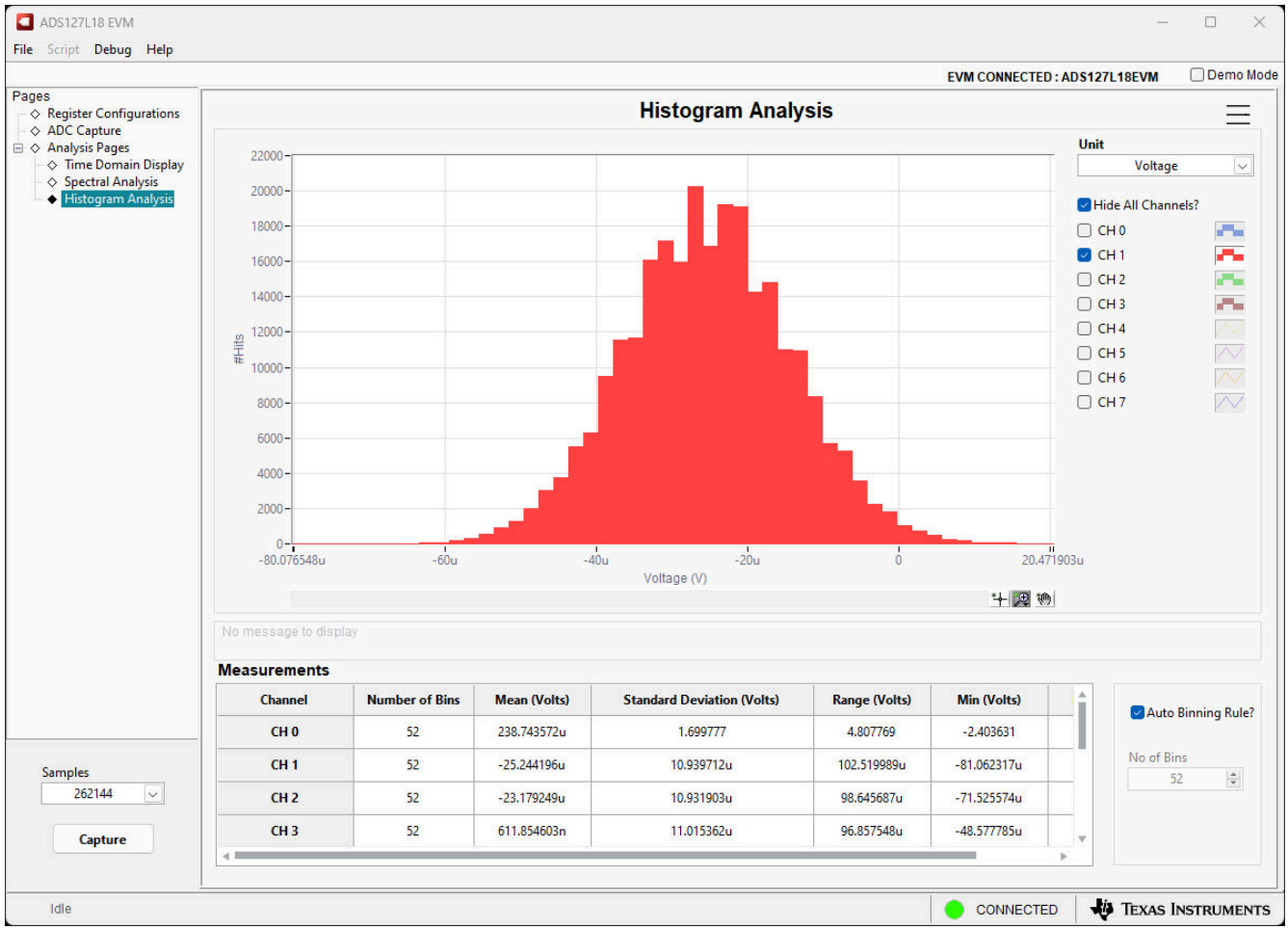


Figure 4-12. Histogram Display

Copyright © 2024 Texas Instruments Incorporated

5 Hardware Design Files

This section contains the ADS127L18EVM bill of materials (BOM), PCB layouts, and schematics.

5.1 Schematics

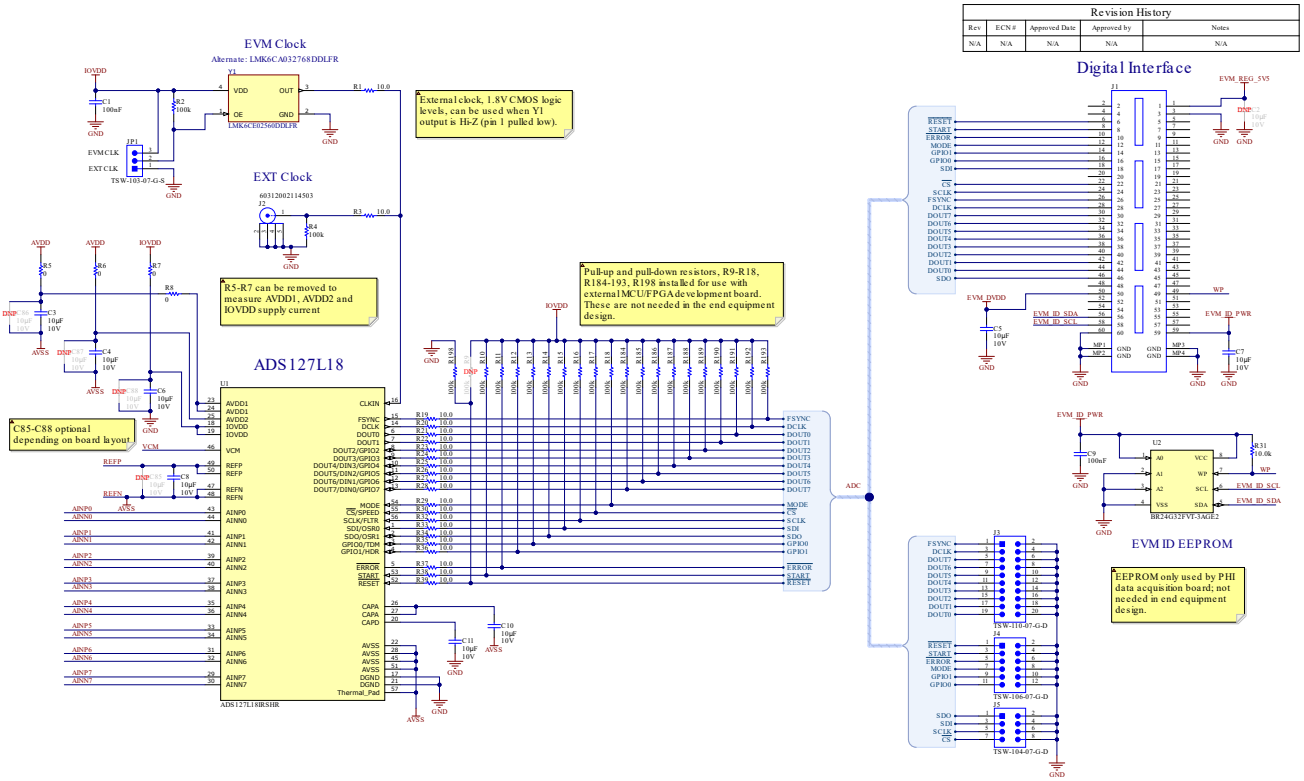


Figure 5-1. ADS127L18EVM ADC Interface and Reference Schematic

Copyright © 2024 Texas Instruments Incorporated

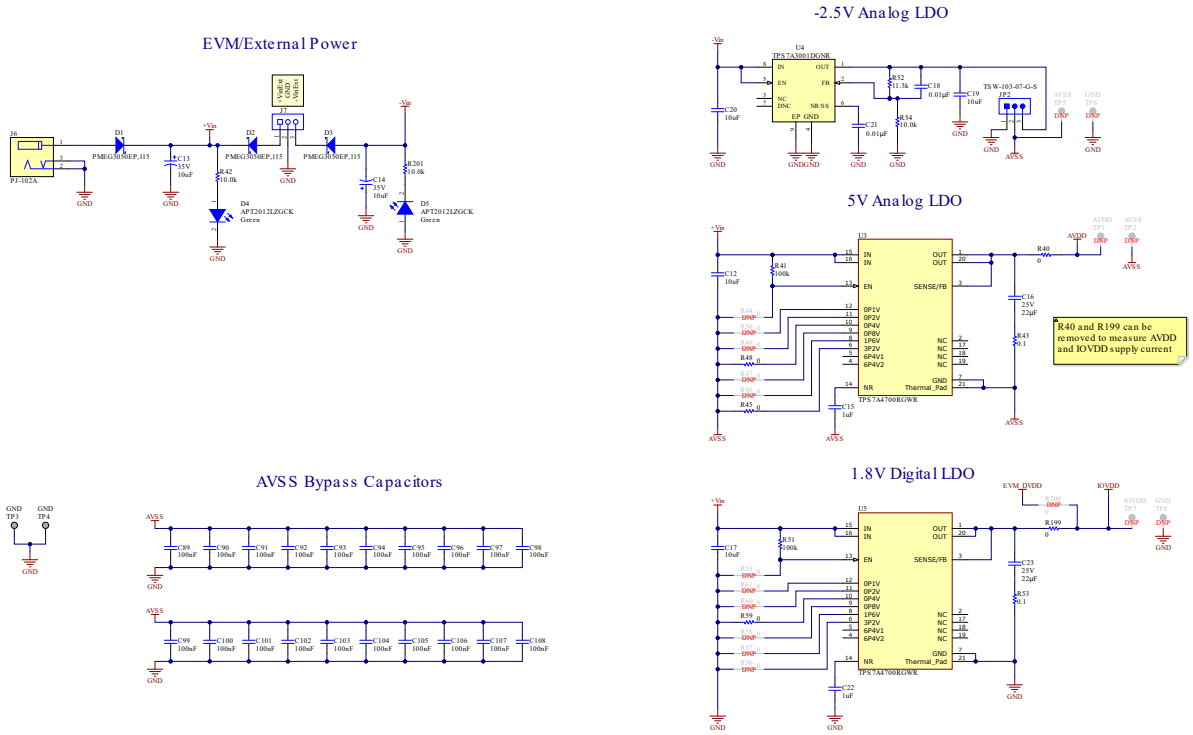


Figure 5-2. ADS127L18EVM External Power Schematic

Copyright © 2024 Texas Instruments Incorporated

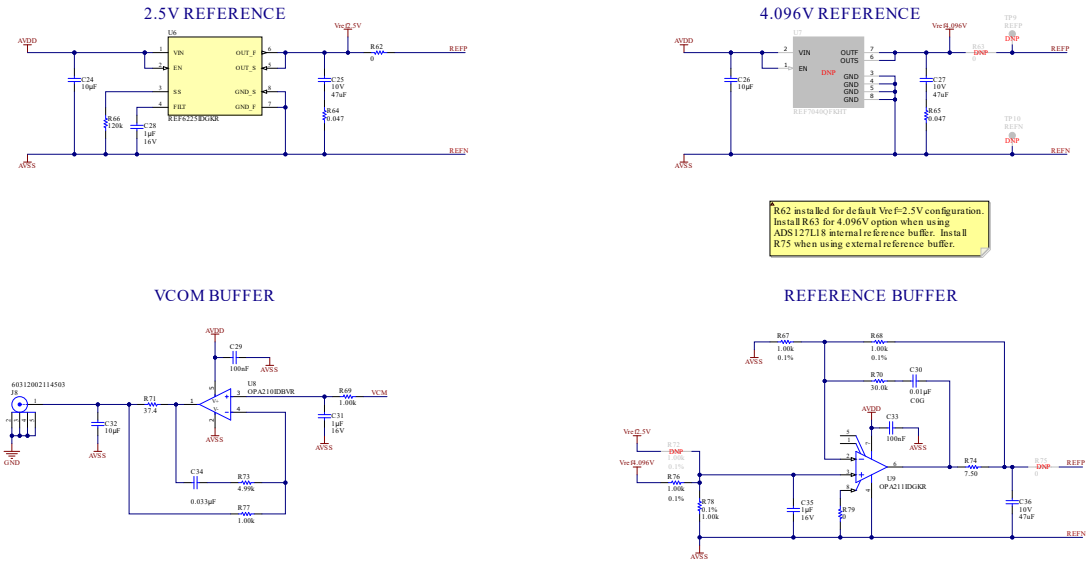


Figure 5-3. ADS127L18EVM Reference and VCOM Buffer Schematic

Copyright © 2024 Texas Instruments Incorporated

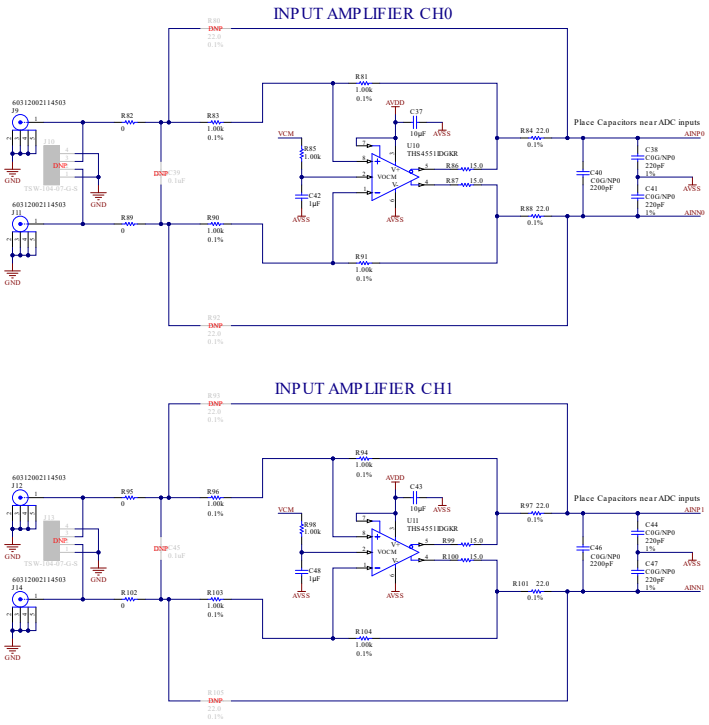


Figure 5-4. ADS127L18EVM Input Channels 0 and 1 Schematic

Copyright © 2024 Texas Instruments Incorporated

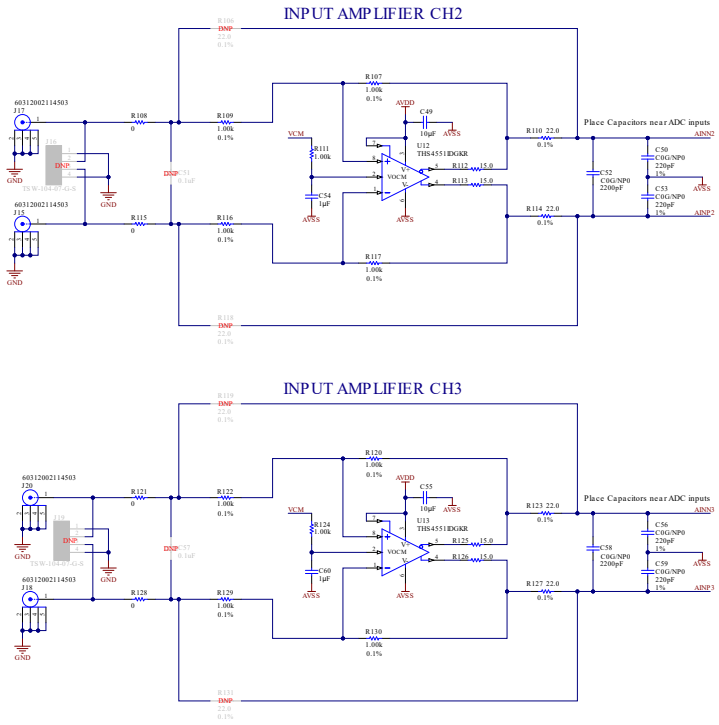


Figure 5-5. ADS127L18EVM Input Channels 2 and 3 Schematic

Copyright © 2024 Texas Instruments Incorporated

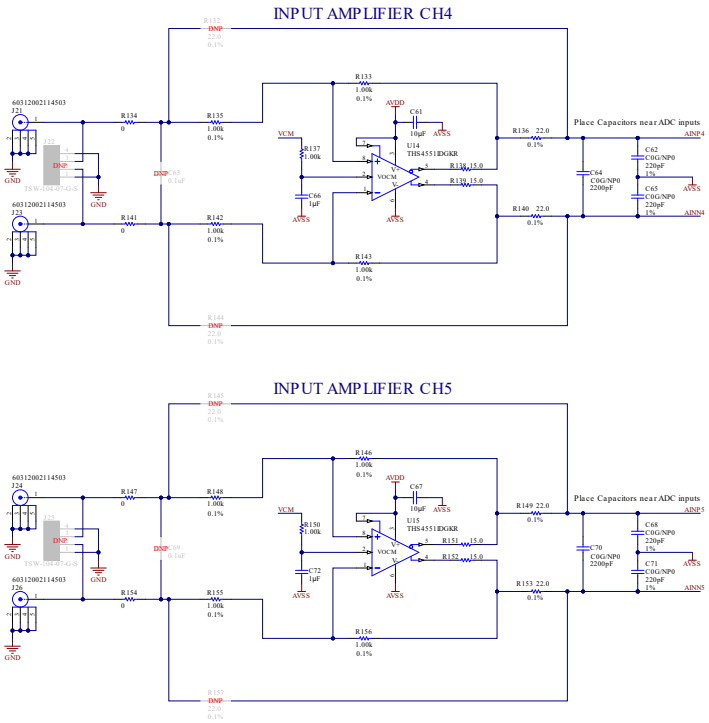


Figure 5-6. ADS127L18EVM Input Channels 4 and 5 Schematic

Copyright © 2024 Texas Instruments Incorporated

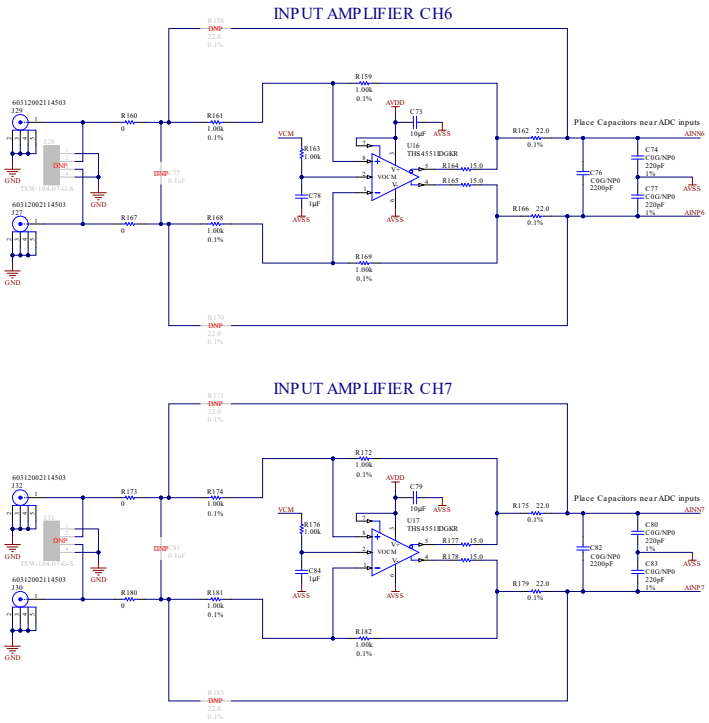


Figure 5-7. ADS127L18EVM Input Channels 6 and 7 Schematic

Copyright © 2024 Texas Instruments Incorporated

5.2 PCB Layouts

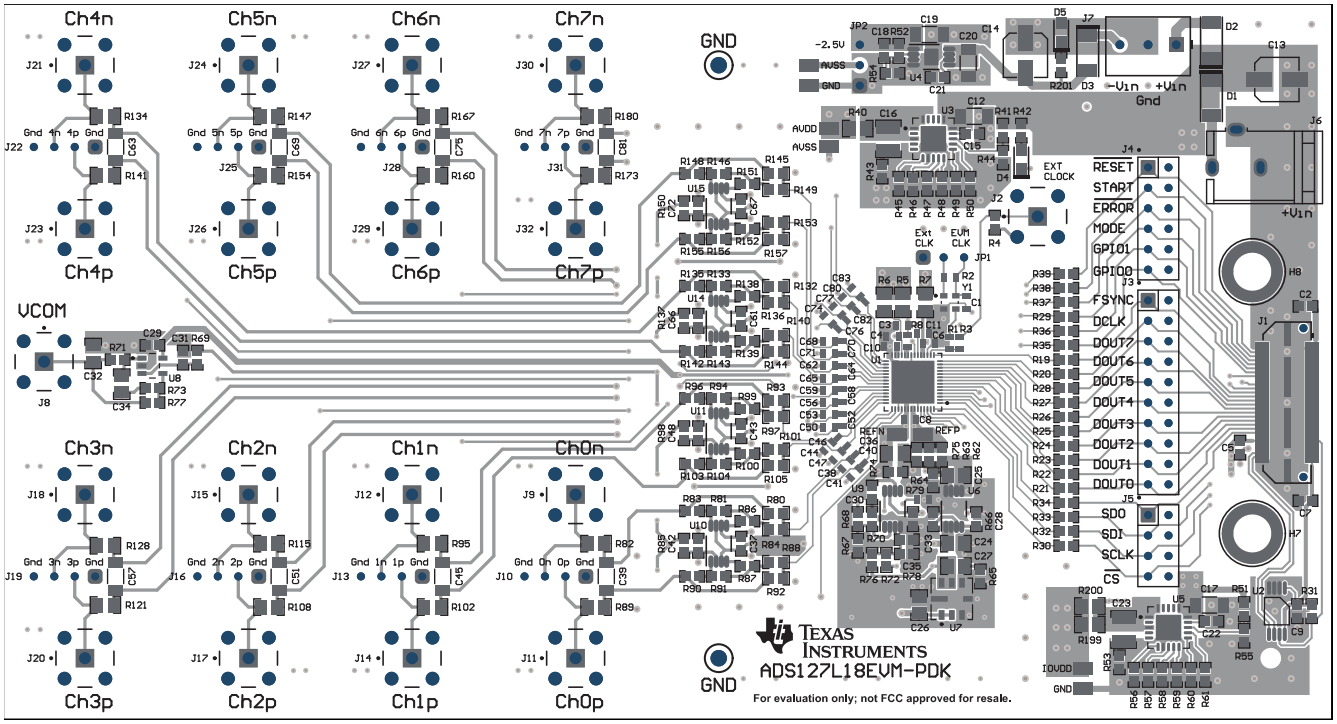


Figure 5-8. PCB Layout for the ADS127L18EVM (Top View)

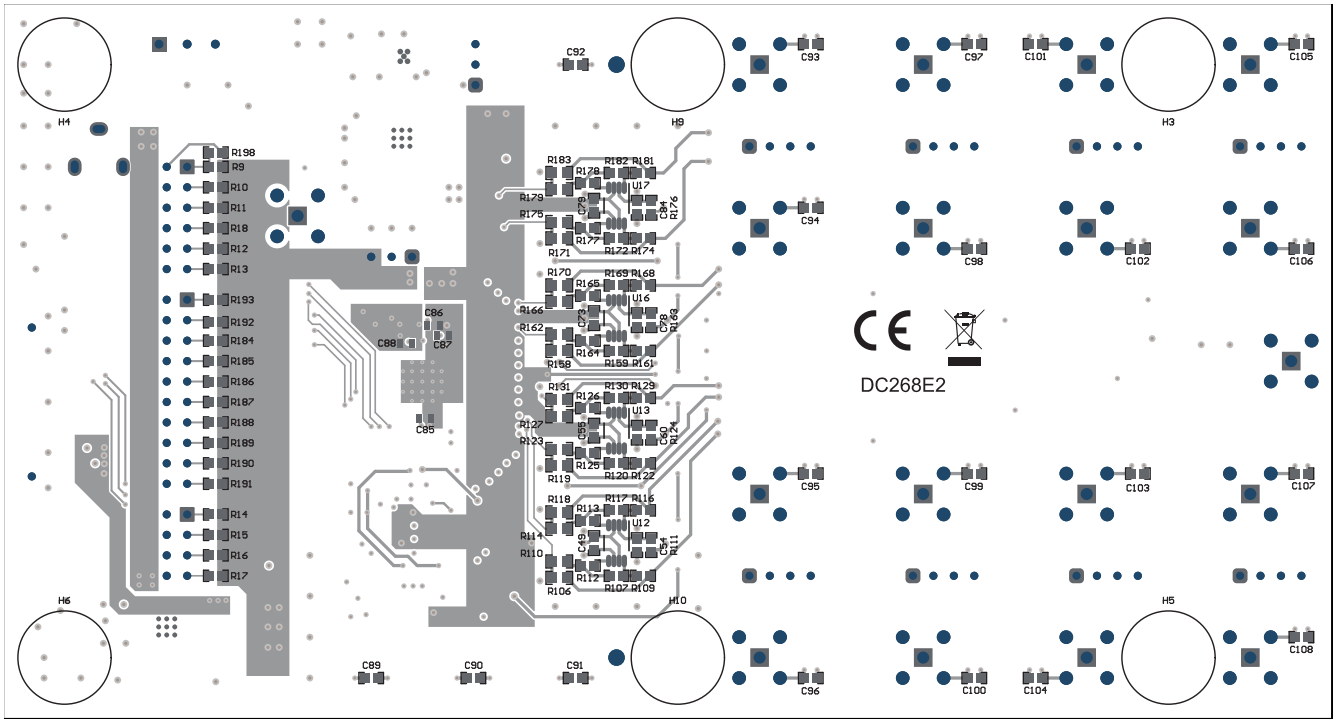


Figure 5-9. PCB Layout for the ADS127L18EVM (Bottom View)

Copyright © 2024 Texas Instruments Incorporated

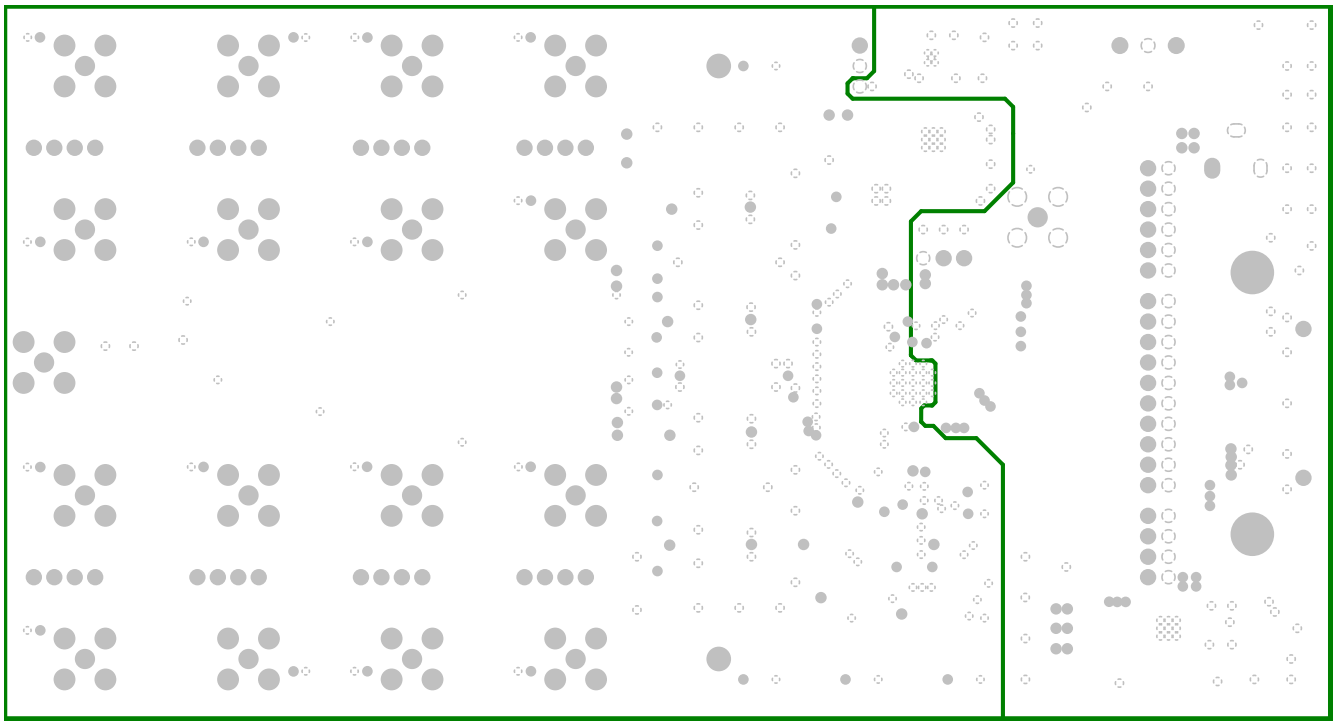


Figure 5-10. PCB Layout (internal AVSS/GND plane 1) for the ADS127L18EVM

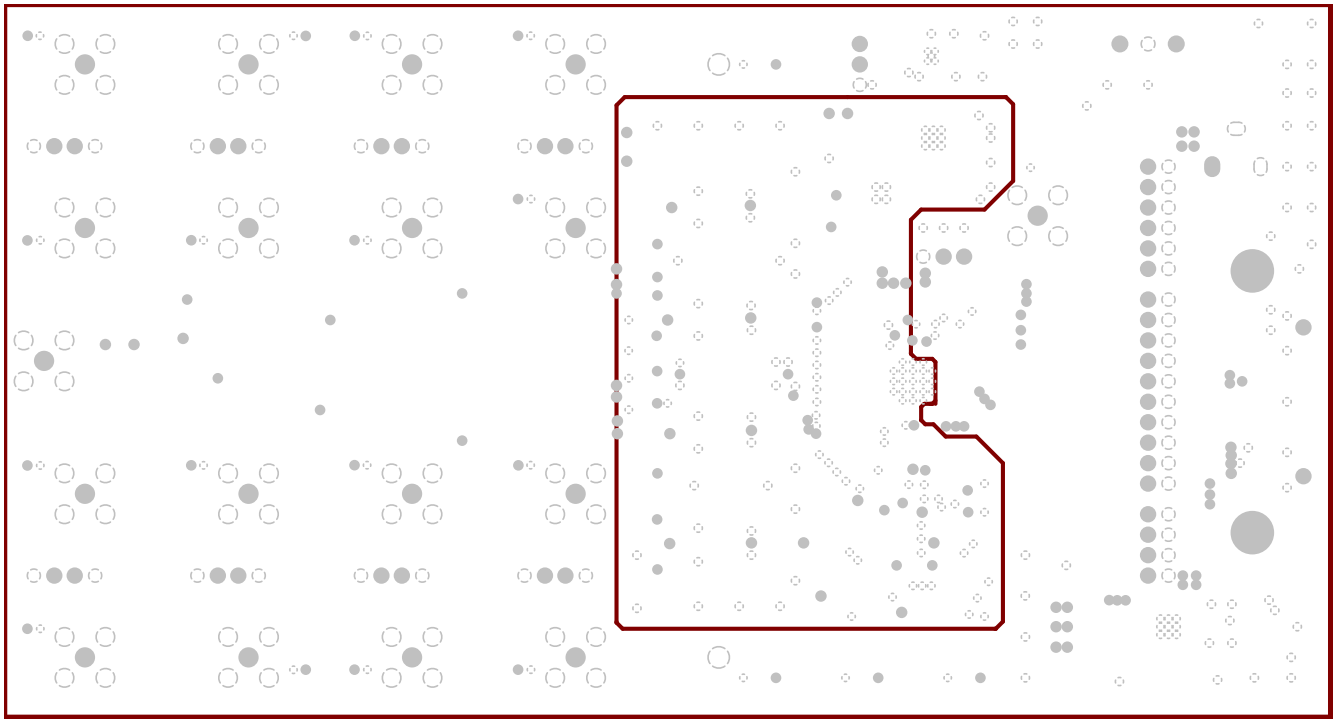


Figure 5-11. PCB Layout (internal AVSS/GND plane 2) for the ADS127L18EVM

Copyright © 2024 Texas Instruments Incorporated

5.3 Bill of Materials (BOM)

Table 5-1. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		DC268	Any
C1, C9, C29, C33, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108	24	0.1uF	CAP, CERM, 0.1uF, 25V, +/- 5%, X7R, 0603	0603	C0603C104J3RACTU	Kemet
C3, C4, C5, C6, C7, C8, C10, C11, C37, C43, C49, C55, C61, C67, C73, C79	16	10uF	CAP, CERM, 10uF, 10V, +/- 20%, X7R, 0603	0603	GRM188Z71A106MA73D	MuRata
C12, C17, C19, C20	4	10uF	CAP, CERM, 10µF, 25V, +/- 10%, X7R, 1206_190	1206_190	C1206C106K3RACTU	Kemet
C13, C14	2	10uF	CAP, AL, 10µF, 35V, +/- 20%, 0.76 ohm, SMD	5x5.8	UUD1V100MCL1GS	Nichicon
C15, C22	2	1uF	CAP, CERM, 1µF, 25V, +/- 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet
C16, C23	2	22uF	CAP, CERM, 22µF, 25V,+/- 10%, X7R, 1210	1210	CL32B226KAJNFNE	Samsung Electro-Mechanics
C18, C21, C30	3	0.01uF	CAP, CERM, 0.01µF, 25V,+/- 1%, C0G/NP0, 0603	0603	C0603C103F3GACTU	Kemet
C24, C26, C32	3	10uF	CAP, CERM, 10µF, 10V,+/- 10%, X7R, 0805	0805	GRM21BR71A106KA73L	MuRata
C25, C27, C36	3	47uF	CAP, CERM, 47µF, 10V, +/- 20%, X5R, 0805	0805	C2012X5R1A476M125AC	TDK
C28, C31, C35, C42, C48, C54, C60, C66, C72, C78, C84	11	1uF	CAP, CERM, 1µF, 16V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1C105K080AC	TDK
C34	1	0.033uF	CAP, CERM, 0.033µF, 50V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0805	0805	CGA4J2C0G1H333J125AA	TDK
C38, C41, C44, C47, C50, C53, C56, C59, C62, C65, C68, C71, C74, C77, C80, C83	16	220pF	CAP, CERM, 220pF, 50V, +/- 1%, C0G/NP0, 0603	0603	06035A221FAT2A	AVX

Copyright © 2024 Texas Instruments Incorporated

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C40, C46, C52, C58, C64, C70, C76, C82	8	2200pF	CAP, CERM, 2200pF, 50V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H222JA01D	MuRata
D1, D2, D3	3	30V	Diode, Schottky, 30V, 5A, SOD-128	SOD-128	PMEG3050EP,115	Nexperia
D4, D5	2	Green	LED, Green, SMD	LED_0805	APT2012LZGCK	Kingbright
H1, H2	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL
H3, H4, H5, H6, H9, H10	6		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
H7, H8	2		ROUND STANDOFF M3 STEEL 5MM	ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik
J1	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A	Samtec
J2, J8, J9, J11, J12, J14, J15, J17, J18, J20, J21, J23, J24, J26, J27, J29, J30, J32	18		SMA Connector Jack, Female Socket 50Ohm Through Hole Solder	CONN_SMA_PTH	6.0312E+13	Wurth Electronics
J3	1		Header, 100mil, 10x2, Gold, TH	10x2 Header	TSW-110-07-G-D	Samtec
J4	1		Header, 100mil, 6x2, Gold, TH	6x2 Header	TSW-106-07-G-D	Samtec
J5	1		Header, 100mil, 4x2, Gold, TH	4x2 Header	TSW-104-07-G-D	Samtec
J6	1		Connector, DC Jack 2.1X5.5 mm, TH	POWER JACK, 14.4x11x9mm	PJ-102A	CUI Inc.
J7	1		Terminal Block, 3.5mm, 3x1, Tin, TH	Terminal Block, 3.5mm, 3x1, TH	393570003	Molex
JP1, JP2	2		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
R1, R3, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R32, R33, R34, R35, R36, R37, R38, R39	22	10	RES, 10.0, 1%, 0.25 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310R0FKEAHP	Vishay-Dale

Copyright © 2024 Texas Instruments Incorporated

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R2, R4, R10, R11, R12, R13, R14, R15, R16, R17, R18, R41, R51, R184, R185, R186, R187, R188, R189, R190, R191, R192, R193, R198	24	100k	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
R5, R6, R7, R40, R82, R89, R95, R102, R108, R115, R121, R128, R134, R141, R147, R154, R160, R167, R173, R180, R199	21	0	RES, 0, 5%, 0.125 W, 0805	0805	RC0805JR-070RL	Yageo America
R8, R45, R48, R59, R62, R79	6	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
R31, R42, R54, R201	4	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R43, R53	2	0.1	RES, 0.1, 1%, 0.1 W, AEC-Q200 Grade 1, 0603	0603	ERJ-L03KF10CV	Panasonic
R52	1	11.3k	RES, 11.3 k, 1%, 0.1 W, 0603	0603	RC0603FR-0711K3L	Yageo
R64, R65	2	0.047	RES, 0.047, 1%, 0.1 W, AEC-Q200 Grade 1, 0603	0603	ERJ-L03KF47MV	Panasonic
R66	1	120k	RES, 120 k, 0.1%, 0.1 W, 0603	0603	RG1608P-124-B-T5	Susumu Co Ltd
R67, R68, R76, R78, R81, R83, R90, R91, R94, R96, R103, R104, R107, R109, R116, R117, R120, R122, R129, R130, R133, R135, R142, R143, R146, R148, R155, R156, R159, R161, R168, R169, R172, R174, R181, R182	36	1.00k	RES, 1.00 k, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERA3AEB102V	Panasonic

Copyright © 2024 Texas Instruments Incorporated

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R69, R77, R85, R98, R111, R124, R137, R150, R163, R176	10	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
R70	1	30.0k	RES, 30.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3EKF3002V	Panasonic
R71	1	37.4	RES, 37.4, 1%, 0.1 W, 0603	0603	RC0603FR-0737R4L	Yageo
R73	1	4.99k	RES, 4.99 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06034K99FKEA	Vishay-Dale
R74	1	7.5	RES, 7.50, 1%, 0.1 W, 0603	0603	RC0603FR-077R5L	Yageo
R84, R88, R97, R101, R110, R114, R123, R127, R136, R140, R149, R153, R162, R166, R175, R179	16	22	RES, 22.0, 0.1%, 0.063 W, 0603	0603	CPF0603B22RE1	TE Connectivity
R86, R87, R99, R100, R112, R113, R125, R126, R138, R139, R151, R152, R164, R165, R177, R178	16	15	RES, 15.0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060315R0FKEA	Vishay-Dale
SH-J1, SH-J2	2	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
TP3, TP4	2		Terminal, Turret, TH, Double	Keystone1573-2	1573-2	Keystone
U1	1		512 kSPS, Quad/Octal, Simultaneous Sampling, 24-Bit, Delta-Sigma ADC	VQFN56	ADS127L18IRSHR	Texas Instruments
U2	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm
U3, U5	2		36V, 1A, 4.17-µVRMS, RF low-dropout (LDO) voltage regulator 20-VQFN -40 to 125	VQFN20	TPS7A4700RGWR	Texas Instruments
U4	1		Single Output High PSRR LDO, 200mA, Adjustable -1.18V to -33V Output, -3V to -36V Input, with Ultra-Low Noise, 8-pin MSOP (DGN), -40 to 125 degC, Green (RoHS & no Sb/Br)	DGN0008D	TPS7A3001DGNR	Texas Instruments

Copyright © 2024 Texas Instruments Incorporated

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
U6	1		High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	DGK0008A	REF6225IDGKR	Texas Instruments
U8	1		2.2nV/√Hz, low-power, 36V operational amplifier 5-SOT-23 -40 to 125	SOT23-5	OPA210IDBVR	Texas Instruments
U9	1		1.1nV/rtHz Noise, Low-Power, Precision Operational Amplifier, DGK0008A (VSSOP-8)	DGK0008A	OPA211IDGKR	Texas Instruments
U10, U11, U12, U13, U14, U15, U16, U17	8		Low Noise, Precision, 150MHz, Fully Differential Amplifier, DGK0008A (VSSOP-8)	DGK0008A	THS4551IDGKR	Texas Instruments
Y1	1		High-Performance BAW Oscillator 25.6MHz, 1.8V LVCMOS Output	VSON4	LMK6CE02560DDLFR	Texas Instruments

Copyright © 2024 Texas Instruments Incorporated

6 Additional Information

6.1 Trademarks

LabVIEW™ is a trademark of National Instruments.
Windows® and Microsoft® are registered trademarks of Microsoft Corporation.
All trademarks are the property of their respective owners.

7 Related Documentation

7.1 Supplemental Content

Table 7-1 shows the related documentation from Texas Instruments.

Table 7-1. Related Documentation

Document	Literature Number
ADS127L18 product data sheet	SBASAM0
PSI EVM User's Guide	SBAU289

Copyright © 2024 Texas Instruments Incorporated

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated