EVM User's Guide: ADS1278V2EVM-PDK

ADS1278EVM-PDK Evaluation Module

Description

The ADS1278 evaluation module (EVM) is a platform for evaluating the performance of the ADS1278, which is a 24-bit, 8-channel simultaneous-sampling delta-sigma (ΔΣ) analog-to-digital converter (ADC). The ADS1278 combines high-precision industrial measurement with excellent dc and ac specifications, providing a usable signal bandwidth of up to 90% of the Nyquist rate with less than 0.005dB of passband ripple. The ADS1278 EVM eases the evaluation of the device with hardware, software, and computer connectivity through the universal serial bus (USB) interface.

Get Started

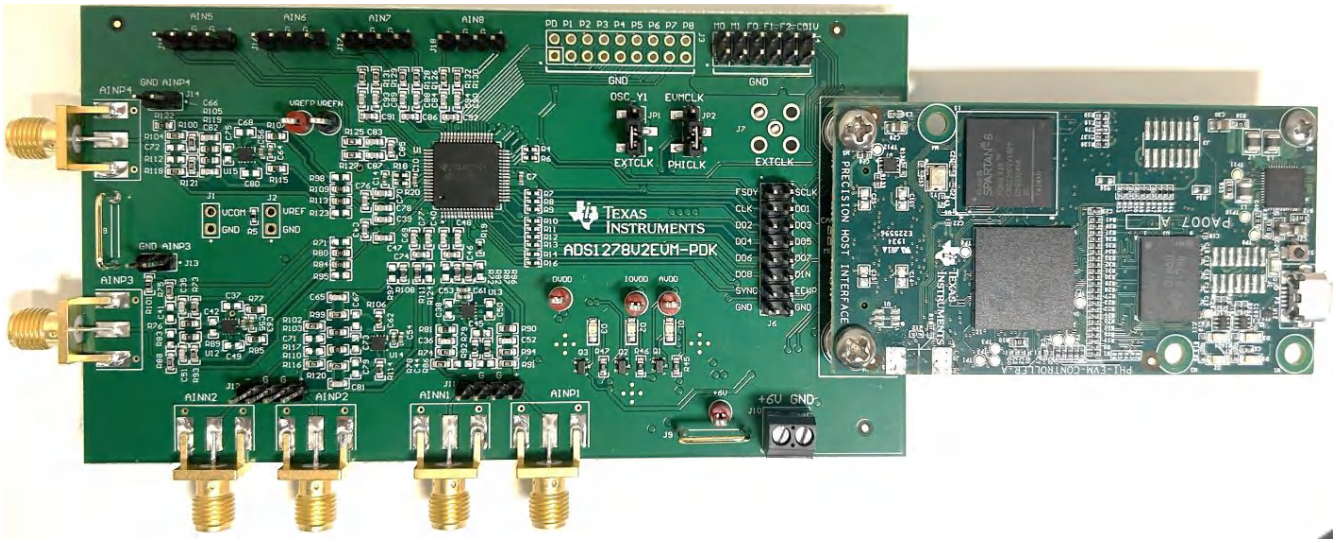
1. Order the EVM from ti.com.
2. Download the latest software from ADS1278EVM-PDK.
3. Launch the ADS1278 EVM GUI from the start menu.
4. Power the ADS1278 EVM from a 6V supply.
5. Connect the ADS1278 EVM to the PHI controller board and connect the PHI board to the computer running the ADS1278 EVM GUI.

Features

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS1278
- The PHI controller provides a convenient communication interface to the ADS1278 over USB 2.0 (or higher) for digital input and output
- Easy-to-use evaluation software for 64-bit Microsoft® Windows® 10 operating system
- The software suite includes graphical tools for data capture, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file for post-processing

Applications

- Vibration/modal analysis
- Multi-channel data acquisition
- Acoustics/dynamic strain gauges
- Pressure sensors



1 Evaluation Module Overview

1.1 Introduction

The ADS1278EVM-PDK is a platform for evaluating the performance of the ADS1278, a 24-bit, 8-channel, simultaneous sampling delta-sigma ADC. The evaluation kit includes the ADS1278 EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over the USB for data capture and analysis. The ADS1278 EVM board includes the ADS1278 and all the peripheral analog circuits and components required to evaluate the performance of the ADS1278. The PHI board provides a communication interface from the ADS1278 EVM to the computer through a USB port.

This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS1278 EVM.

Note

The ADS1278 EVM and software can also support the 4-channel ADS1274 device. However, the user must manually remove the ADS1278 and install the ADS1274. See Section 5.2 for the location of the ADS1278 on the EVM. The ADS1274 is not discussed further in this document.

1.2 Kit Contents

The ADS1278EVM-PDK includes the following components, as shown in Figure 1-1.

1. The PHI controller board.
2. The ADS1278 EVM board which includes the ADS1278 and peripheral circuitry required for device operation and communication with the PHI board.
3. An A-to-Micro-B USB cable for communication between the PHI board and the EVM GUI.
4. The EVM GUI, which can be found online in the EVM tool folder.

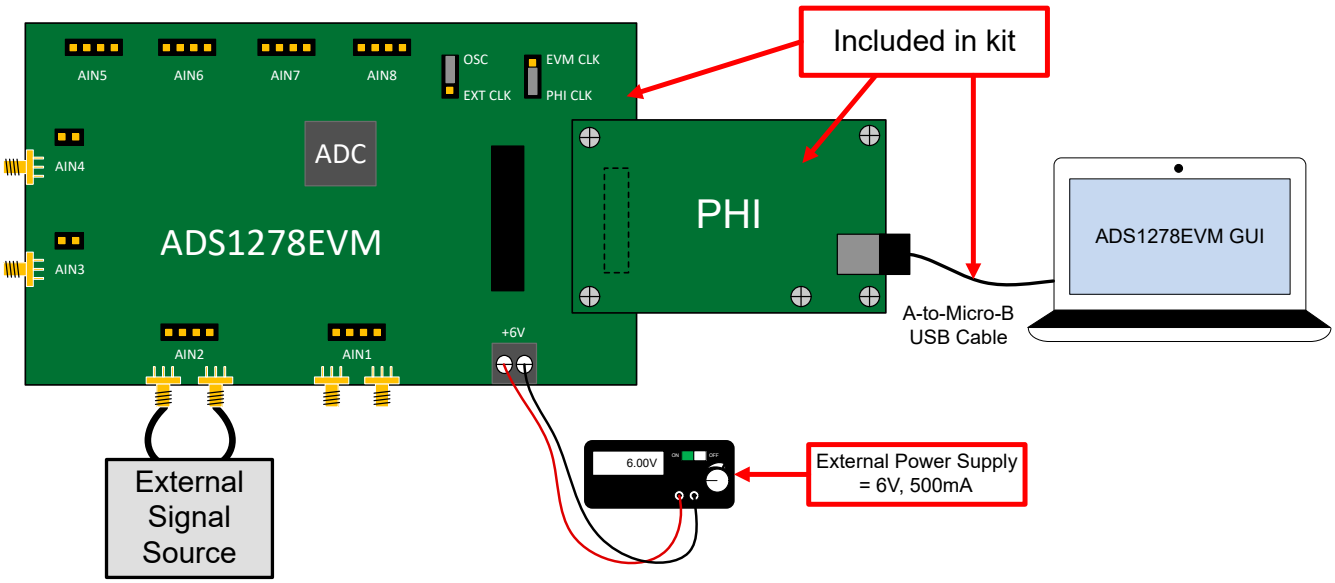


Figure 1-1. System Connection for Evaluation

1.3 Specification

The ADS1278EVM-PDK requires an external 6V power source to power three ultra-low noise TPS7A4700 low-dropout (LDO) linear regulators that supply the ADS1278 voltage rails. The EVM supports the use of an external clock, as well as setting the MODE, FORMAT, and CLKDIV pins with jumpers.

The EVM can also be configured by populating and depopulating the appropriate pin headers and zero-ohm jumper resistors to manually measure or set the Vcm, Vref, and shutdown pins of the ADS1278 EVM.

Control and monitoring of the communications between the EVM and the PHI controller board is provided using the pin header test points. Likewise, monitoring the analog input signals and power supply rails is supported using the test points built into the board.

The operating conditions listed in Table 1-1 must be observed when using the ADS1278EVM.

Table 1-1. Operating Conditions

PARAMETER	CONDITIONS	VALUE
Temperature	Recommended operating free-air temperature range, T_A	15°C to 35°C
Power supply input range	Voltage input range for J10 (+6V supply)	+5.5V to +6.5V
	Supply current range $\|I_S\|$	300mA ≤ $\|I_S\|$ ≤ 500mA
Analog input voltage range	Absolute input voltage versus GND for CH1-CH8 inputs	0V to +5V
Maximum VCOM current	Recommended max current from J1 (optional VCOM output pins)	30mA
EXT clock frequency	High-speed mode	0.1 to 37MHz
	Other modes	0.1 to 27MHz
Digital logic input levels	Recommended digital voltage high level (V_{IH})	0.7 IOVDD ≤ V_{IH} ≤ IOVDD
	Recommended digital voltage low level (V_{IL})	0.3 IOVDD ≥ V_{IL} ≥ GND
ADS1278 AVDD Voltage range	Voltage supplied to ADS1278 AVDD pins from onboard regulator or external source	+4.75V to +5.25V
ADS1278 IOVDD voltage range	Voltage supplied to ADS1278 IOVDD pins from onboard regulator or external source	+1.65V to +3.6V
ADS1278 DVDD voltage range	Voltage supplied to ADS1278 DVDD pin from onboard regulator or external source	+1.65V to +1.95V
ADS1278 VREF voltage range	Voltage supplied to J2 (optional VREF input)	+0.5V to +3.1V

1.4 Device Information

The ADS1278 is a 24-bit, 8-channel, simultaneous sampling delta-sigma ADC with data rates up to 144 kilosamples per second, as shown in Figure 1-2.

Traditionally, industrial delta-sigma ADCs offering good drift performance use digital filters with large pass-band droop. As a result, these delta-sigma ADCs have limited signal bandwidth and are the best choice for low-frequency measurements. High-resolution ADCs in audio applications offer larger usable bandwidths, but the offset and drift specifications are significantly weaker than respective industrial counterparts. The ADS1278 combines these types of converters, allowing high-precision industrial measurement with excellent dc and ac specifications.

The high-order, chopper-stabilized modulator achieves very low drift with low in-band noise. The onboard decimation filter suppresses modulator and signal out-of-band noise. This ADC provides a usable signal bandwidth up to 90% of the Nyquist rate with less than 0.005dB of passband ripple.

Four operating modes allow for optimization of speed, resolution, and power. All operations are controlled directly by pins; there are no registers to program. The device is fully specified over the extended industrial range (–40°C to +105°C) and is available in an HTQFP-64 PowerPAD™ package.

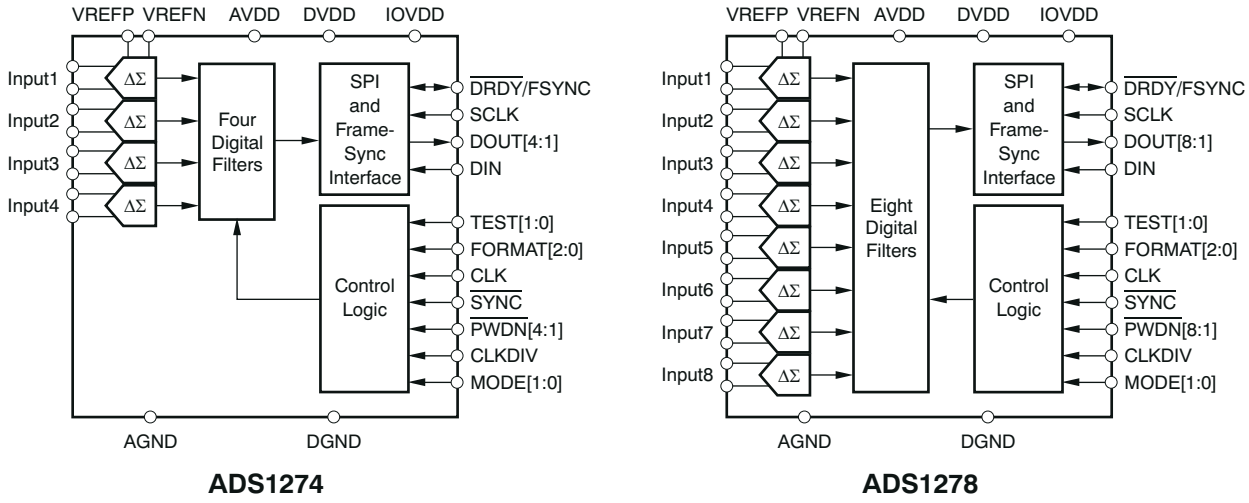


Figure 1-2. ADS1274 and ADS1278 Block Diagram

2 Hardware

The ADS1278 EVM is designed for easy interfacing with analog input sources. This section covers the details of the front-end circuit, including jumper configuration for different input test signals and board connectors for signal sources.

2.1 EVM Analog Input Options

The ADS1278 EVM board offers different analog input circuits, including Differential SMA Inputs (Section 2.1.1), Single-Ended SMA Inputs (Section 2.1.2), and Differential Input Pins (Section 2.1.3).

2.1.1 Differential SMA Inputs

For best performance, connect differential analog input signals through the SMA connectors on channels 1 and 2, as shown in Figure 2-1. Alternatively, headers are provided to directly connect inputs for dc measurements, or where best ac performance is not needed. A possibility is to use the fully-differential SMA inputs as single-ended inputs. Connect the single-ended input to either the AINP or AINN SMA connector, then use the supplied shunt to connect the unused input to GND via the header. The input driver circuits use the THS4551 fully-differential amplifier in a low pass, unity-gain configuration with an additional single-pole RC filter at the output. Multiple passive components around the amplifier are intentionally left uninstalled to give users the flexibility to customize the input drive circuit for specific application.

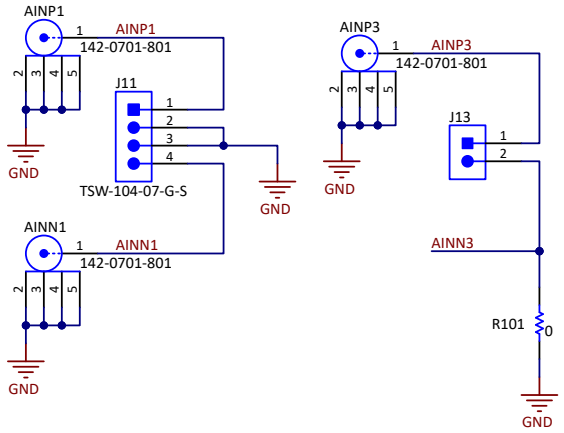


Figure 2-1. SMA Input Connections

2.1.2 Single-Ended SMA Inputs

Connect single-ended input signals through the SMA connectors on channels 3 and 4 . These channels also feature headers that can be used to short the inputs to ground using shunt connectors. The input driver circuits are identical to the ones used in the fully differential SMA input circuits on channels 1 and 2 except the negative inputs are grounded as shown in Figure 2-1.

2.1.3 Differential Input Pins

Connect differential input signals directly to the ADC on channels 5-8 using the input headers. These channels are connected to the device pins though a small charge bucket filter to counteract the effects of the inrush current on the device. Similar to Section 2.1.1, apply single-ended signals to these headers by grounding one of the input pins. Figure 2-2 shows an example of the undriven input pin headers and associated charge bucket circuitry for channel 5.

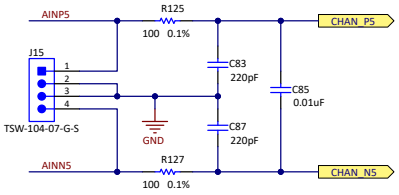


Figure 2-2. Unbuffered Input Connections

2.2 Power Supplies

The ADS1278 EVM requires a 6V input through the J10 terminal block and typically draws less than 500mA of current. Three low-noise TPS7A4700 low dropout (LDO) voltage regulators (U9-U11) provide the three voltage rails used by the ADS1278 and the external circuitry. By default, AVDD is configured for 5V, IOVDD is configured for 3.3V, and DVDD is configured for 1.8V. DVDD can be configured to 2.1V for up to 37MHz operation in high-speed mode by installing zero-ohm resistors at locations R69 and R70.

Each voltage rail also features an indicator LED and a test point for convenient verification of power supply functionality.

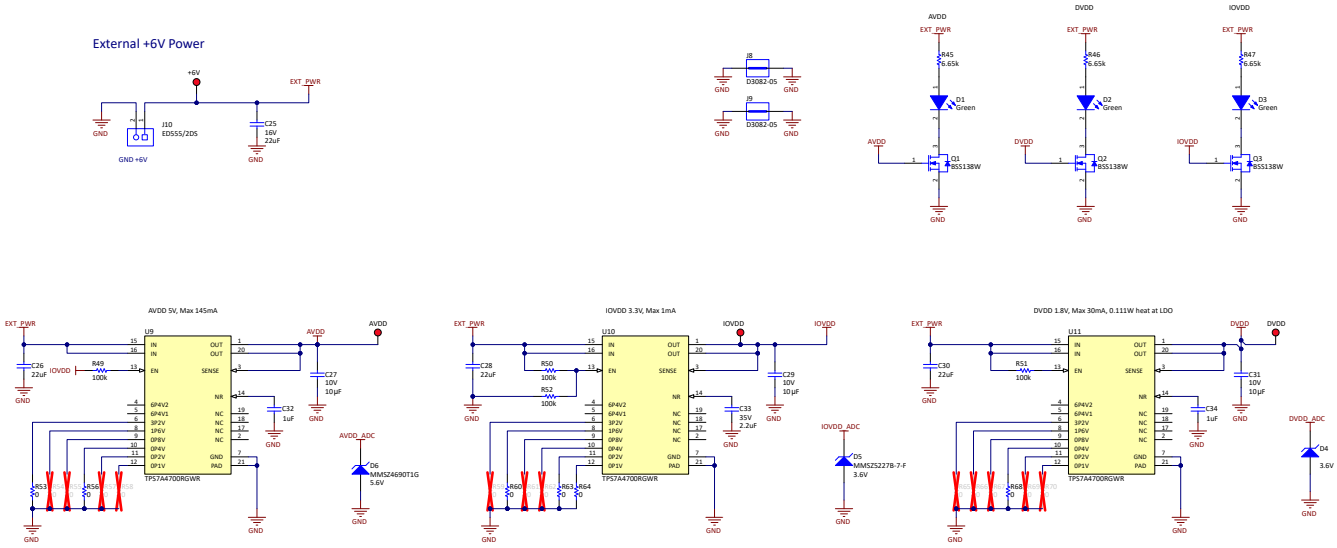


Figure 2-3. Power Supply Circuitry

2.3 ADC Connections and Decoupling

The circuit shown in Figure 2-4 shows all connections to the ADS1278 (U1). Each analog power supply connection has a 100nF decoupling capacitor and each power supply has a 10µF decoupling capacitor. These capacitors are physically close to the device and have a good connection to the GND plane. Also, each digital input has a 50Ω series resistor. These resistors smooth the edges of the digital signals so that the signals have minimal overshoot and ringing. Although not strictly required, these components can be included in final designs to improve digital signal integrity.

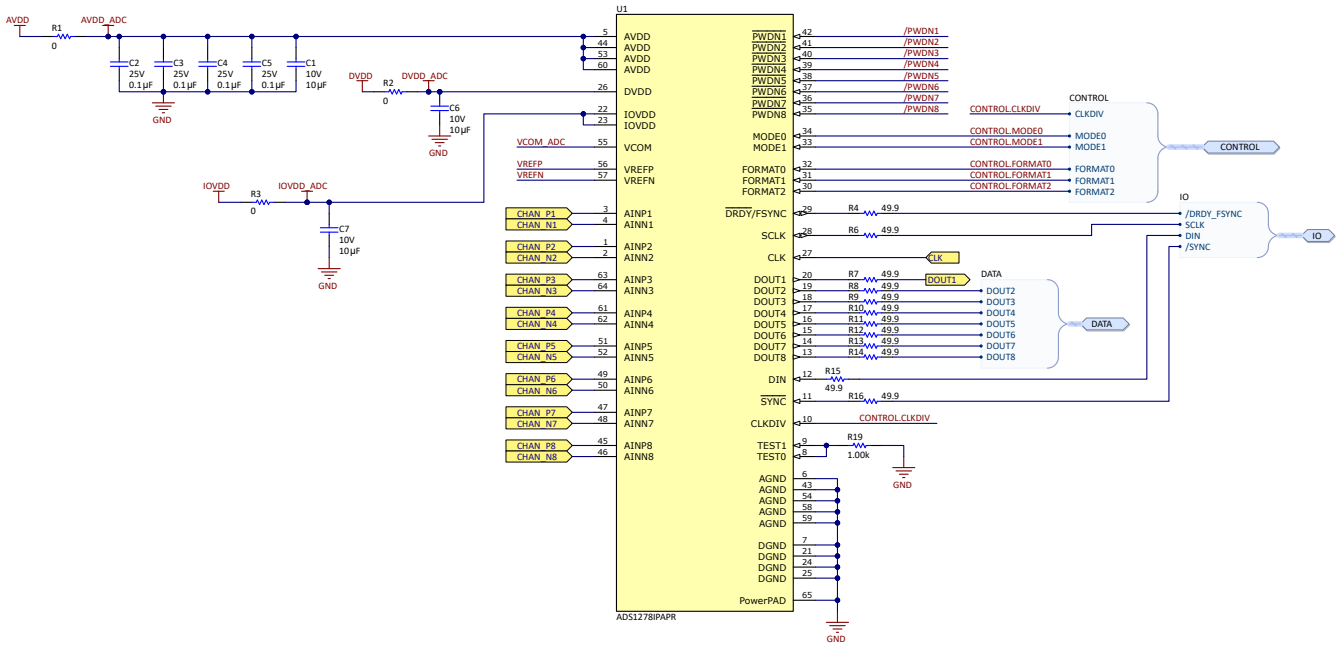


Figure 2-4. ADS1278 Connections and Decoupling

2.4 ADC Input Amplifiers

Figure 2-5 shows the fully differential amplifier (THS4551) circuit used to drive the ADC. The input applied to AINP and AINN must be a low-distortion differential signal. Pin 7 on U13 (VOCM) controls the common-mode output for the amplifier, and is set by the ADS1278 VCOM output (pin 55). The feedback network includes a low pass filter (R74, R78, R94, R91, C36, and C52). The amplifier output connects to an RC filter that connects to the ADC input (R37, R43, C30, C26, and C32). The amplified configuration has several do-not-populate (DNP) components that provide flexibility, but are not required for good performance. The amplifier power supplies are connected by default to the AVDD and GND supplies that are also used for the ADC.

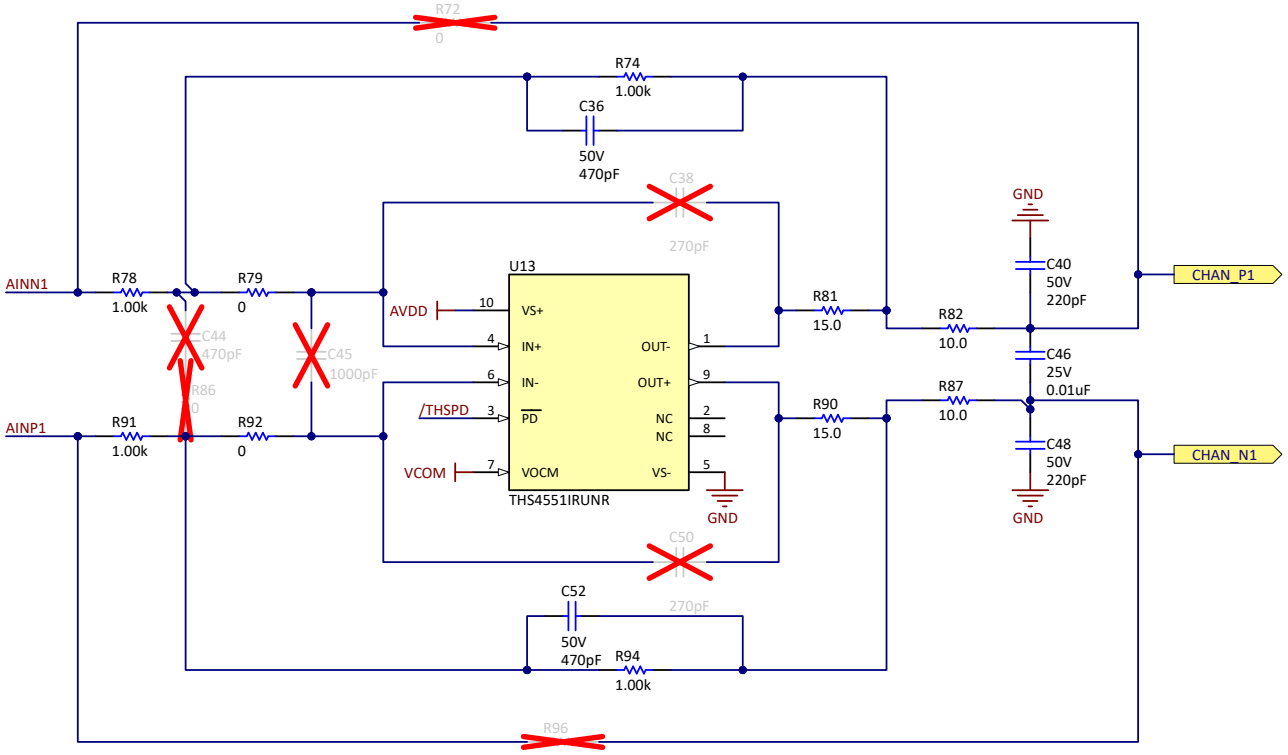


Figure 2-5. Input Drive Amplifier Circuit

2.5 VCOM Buffer

Figure 2-6 shows the buffer circuit for the ADC VCOM signal. The output of the VCOM buffer connects to the VOCM signal of the input driver amplifiers. The J1 VCOM header pins (depopulated by default) can also be used to provide an alternate source for VCOM by depopulating resistor R5. Jumper J1 can also be used to connect the VCOM signal to an external piece of test equipment to set the common-mode voltage. A common use case is to connect this signal to the Audio Precision SYS-2722 to set the signal generator's common-mode output.

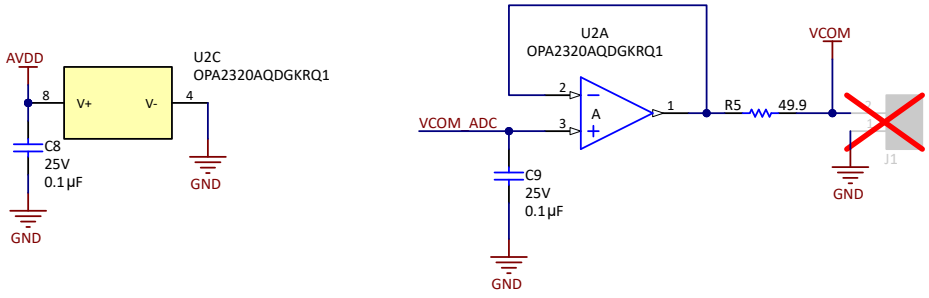


Figure 2-6. VCOM Buffer Circuit

2.6 Voltage Reference

Figure 2-7 shows the REF5025 configuration. The OPA2320 buffer circuit drives the ADS1278 reference input pins. The reference voltage can optionally be provided through the J2 VREFext header pins (depopulated by default) by depopulating jumper resistor R22. Create a low pass filter by replacing the components connecting the buffer to the ADS1278 (R18, C10, R20). Use test points VREFP and VREFN to read back the reference voltage provided to the filter.

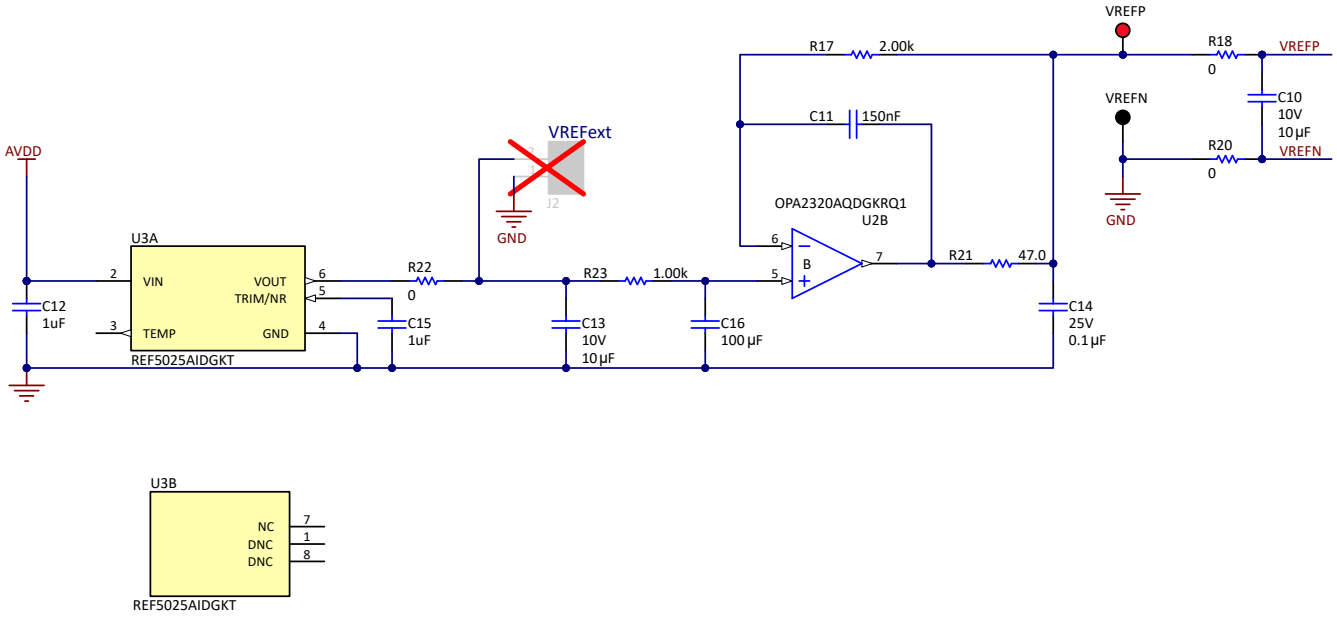


Figure 2-7. Reference Voltage Circuit

2.7 Clock Tree

The onboard PLL of the PHI controller board provides the default clock for the ADS1278 EVM. This clock is configurable for arbitrary frequencies using the *Clock Settings* dialogue in the GUI as described in Section 4.2. The ADS1278 EVM can also be configured to use an onboard hardware oscillator or an external clock. Figure 2-8 shows the different on-board clock options for the ADS1278 EVM.

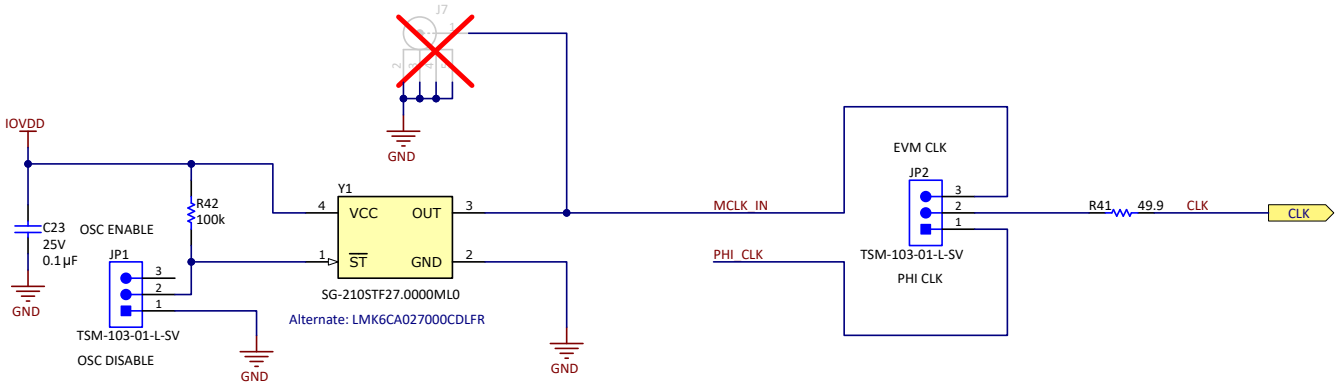


Figure 2-8. Clock Source Circuit

When jumper JP2 is in the default position (1-2), the CLK pin on the ADS1278 is routed to the PHI clock output. Change the shunt on jumper JP2 to position 2-3 if the ADS1278 EVM is used with the onboard clocking options. Moving jumper JP1 to position 1-2 disables the local 27MHz oscillator (Y1) on the ADS1278 EVM, allowing an external clock supplied on the SMA connector (J7).

To use an external clock source, apply a CMOS square-wave signal with an amplitude equal to IOVDD (3.3V) and a frequency within the specified range of the ADS1278. Additionally, the appropriate clock frequencies must be programmed into the *Clock Settings* dialogue in the GUI to verify the communication speed is correct.

Note

Writing the same frequency repeatedly to the onboard PLL of the PHI controller sometimes causes the PLL to become *stuck* at that frequency. To prevent this, the GUI software prevents repeated writes of the same frequency to the PLL. However, the PLL has a limited frequency resolution and repeated writes to different frequencies can cause the PLL to become *stuck* if the entered frequencies are coerced to the same frequency. If this occurs, then disconnect and reconnect the GUI to reset the PLL.

2.8 Digital Interfaces

As noted in Section 1.1, the EVM interfaces with the PHI and communicates with the computer over the USB. The PHI communicates with two devices on the EVM: the ADS1278 (over SPI or frame-sync) and the EEPROM (over I2C). The EEPROM comes preprogrammed with the information required to configure and initialize the ADS1278 platform. When the hardware is initialized, the EEPROM is no longer used. The ADS1278 uses SPI serial communication in mode 1 (CPOL = 0, CPHA = 1) or frame-sync mode. Header J6, shown in Figure 2-9, provides test points to measure the digital signals. The configuration inputs, which are configurable by the PHI interface by default but can also be configured by placing jumpers on J3 and J4, are also shown in Figure 2-9.

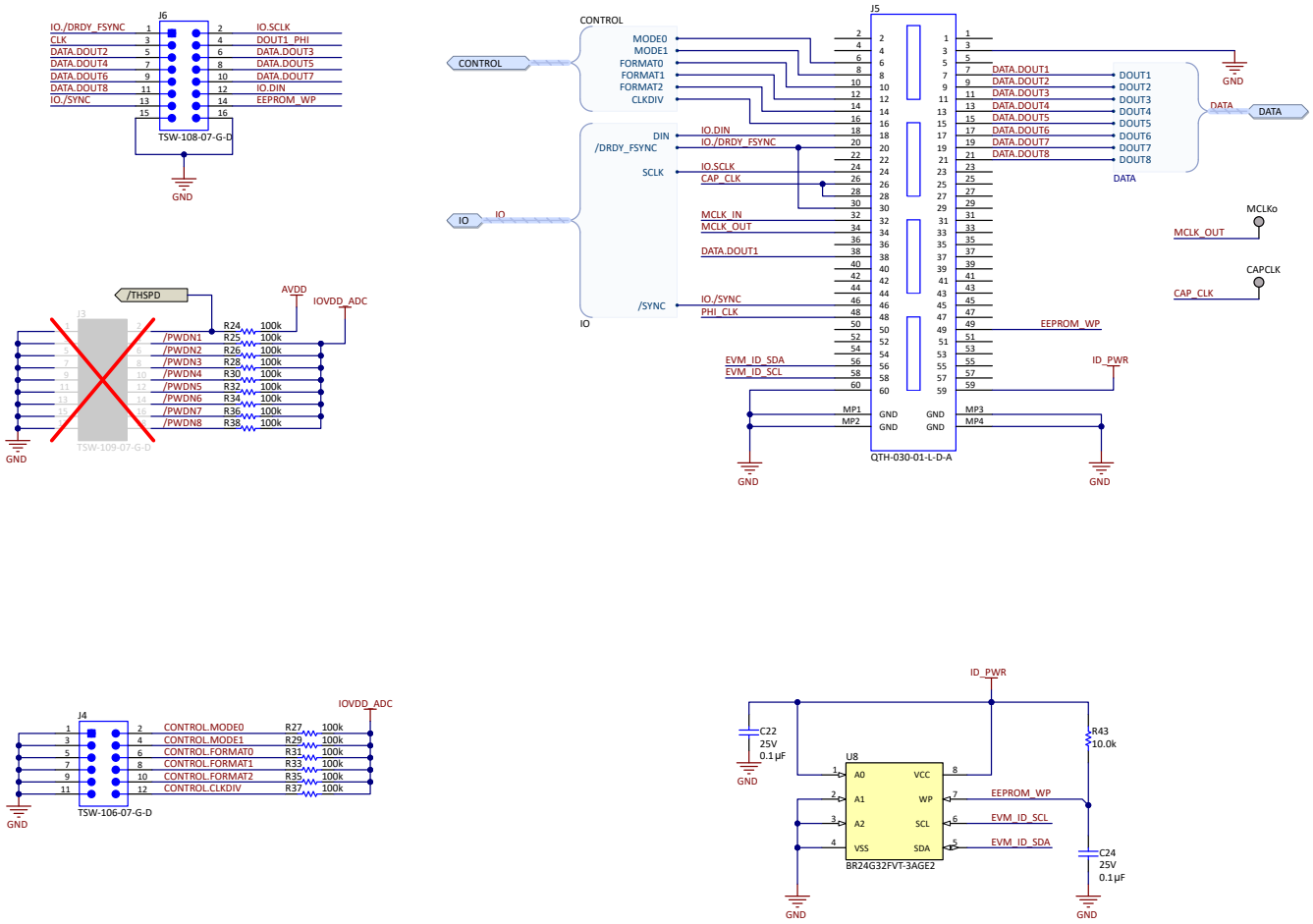


Figure 2-9. Digital Interface Connections

2.9 Using the ADS1278EVM With an External Controller

The ADS1278EVM is designed for easy connection to an external controller. This design enables the user to test application code and firmware on the ADS1278 without having to develop a custom PCB. This section describes the specific connections required to use the ADS1278EVM with an external controller. Figure 2-10 shows the location of various headers and terminal blocks described in this section.

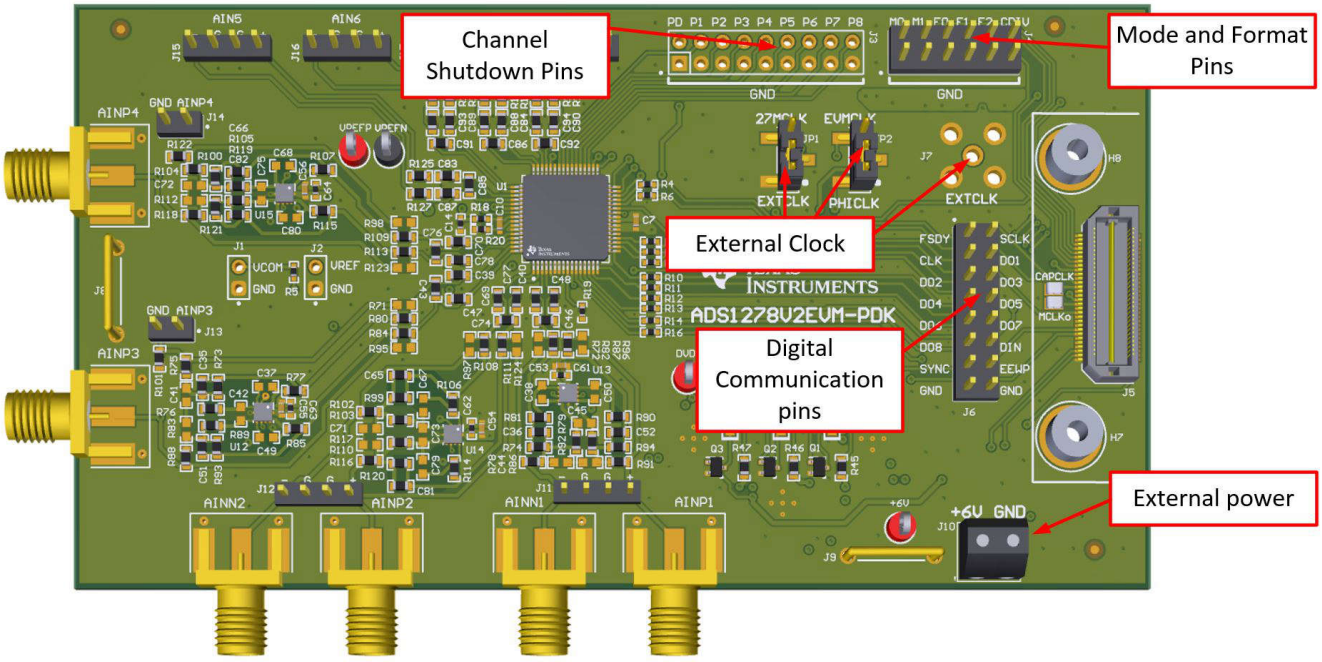


Figure 2-10. Connecting an External Controller to the ADS1278EVM

First, complete the following steps to prepare the ADS1278EVM board for use with an external controller:

1. Remove the PHI board if still connected to the EVM.
2. Provide +6V and ground (GND) to terminal block J10 from an external bench supply. Make sure the external controller also connects to GND on the EVM.
3. See Section 2.7 to connect an external clock to the ADS1278EVM. Alternatively, use the 27MHz oscillator included with the EVM by:
   a. Moving jumper JP1 to pins 2-3 (OSC_Y1) to enable the oscillator
   b. Moving jumper JP2 to pins 2-3 (EVMCLK) to select the oscillator
4. Install jumpers on header J4 to configure the ADC. For example, install jumpers on MODE0, MODE1, FORMAT0, FORMAT1, and FORMAT2, while leaving CLKDIV open (high). These selections configure the ADC for high-speed mode, SPI interface, and dynamic TDM DOUT mode. See the ADS1278 data sheet for more information regarding the different modes of ADC operation.

Finally, make the following connections to enable digital communication between the ADS1278EVM and the external controller:

1. Connect POCI (peripheral out, controller in) from the controller to the DOUT1 pin on header J6 on the EVM.
2. Connect SCLK from the controller to the SCLK pin on header J6 on the EVM.
3. Connect the DIN pin on header J6 on the EVM to GND, do not leave floating.
4. Connect an I/O pin from the controller to the $\overline{\text{SYNC}}$ pin on header J6 on the EVM. This connection is needed for robust power-up reset. Alternatively, tie the $\overline{\text{SYNC}}$ pin to IOVDD for test purposes.
5. Connect an I/O pin from the controller to the $\overline{\text{DRDY}}$ pin on header J6 on the EVM. $\overline{\text{DRDY}}$ is an output from the ADC, indicating when new data are ready to be clocked out of the ADC. As shown in Figure 2-11, the user-defined data collection routine monitors this pin (polling or interrupt) and only transfers data after a falling edge.

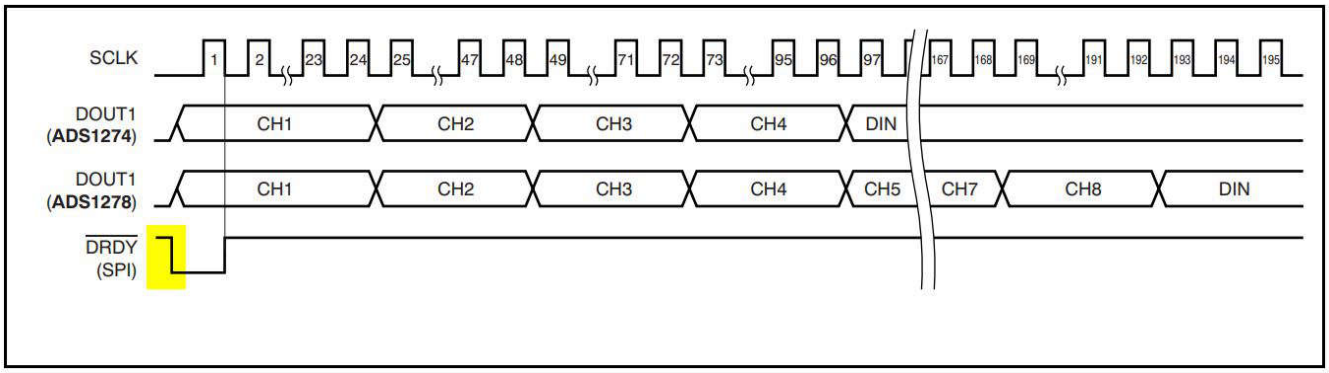


Figure 2-11. ADS1278 $\overline{\text{DRDY}}$ Pin Behavior

3 Software

3.1 ADS1278EVM Software Installation

Download the latest version of the EVM GUI installer from the Tools and Software folder of the ADS1278 EVM and run the GUI installer to install the EVM GUI software on your computer.

> **CAUTION**
> Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message can appear or the installer.exe file can be deleted.

As shown in Figure 3-1, accept the license agreements and follow the on-screen instructions to complete the installation.

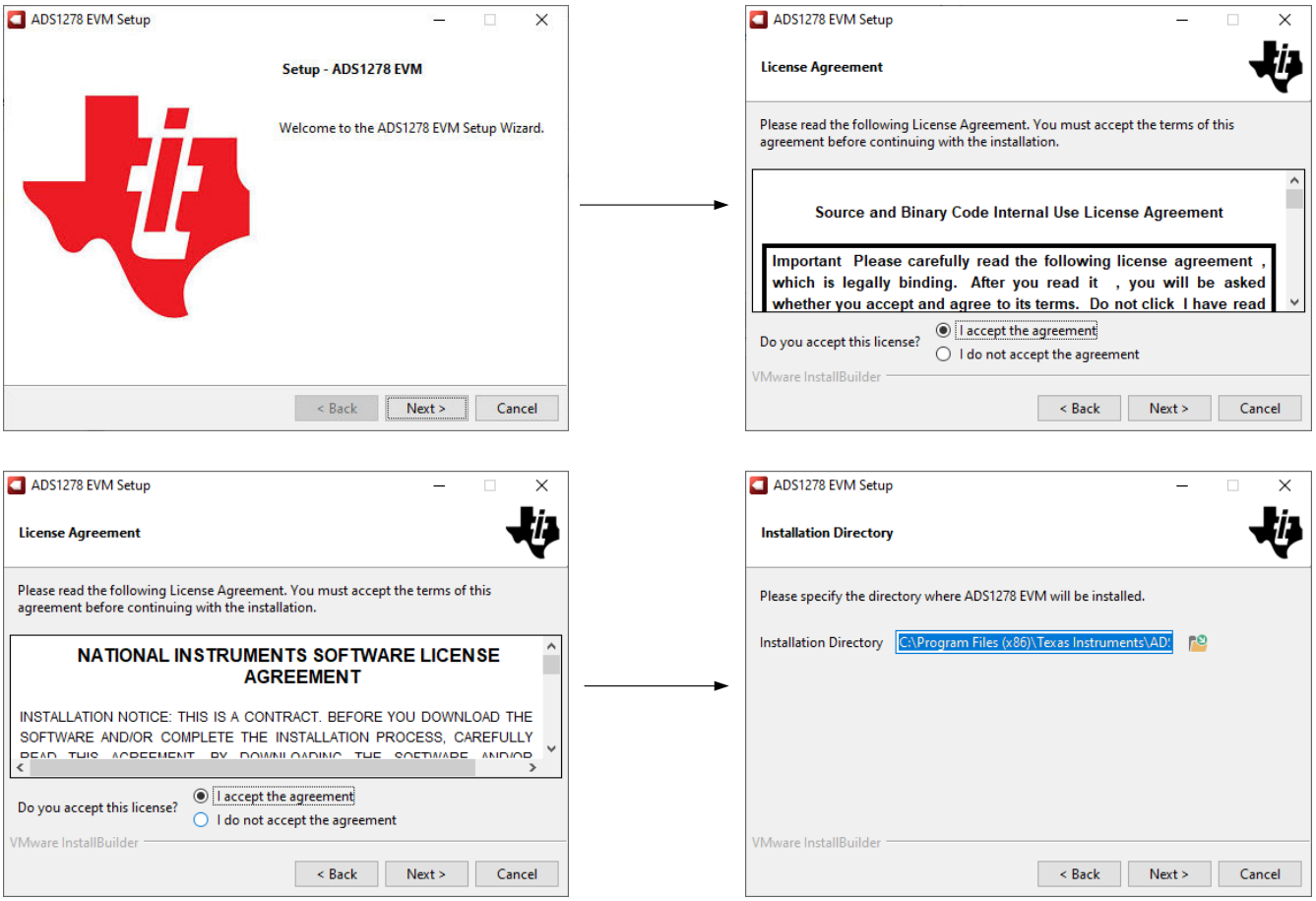


Figure 3-1. GUI Installation Prompts

As a part of the ADS1278 EVM GUI installation, install the Device Driver as shown in Figure 3-2. Click *Next* to proceed.

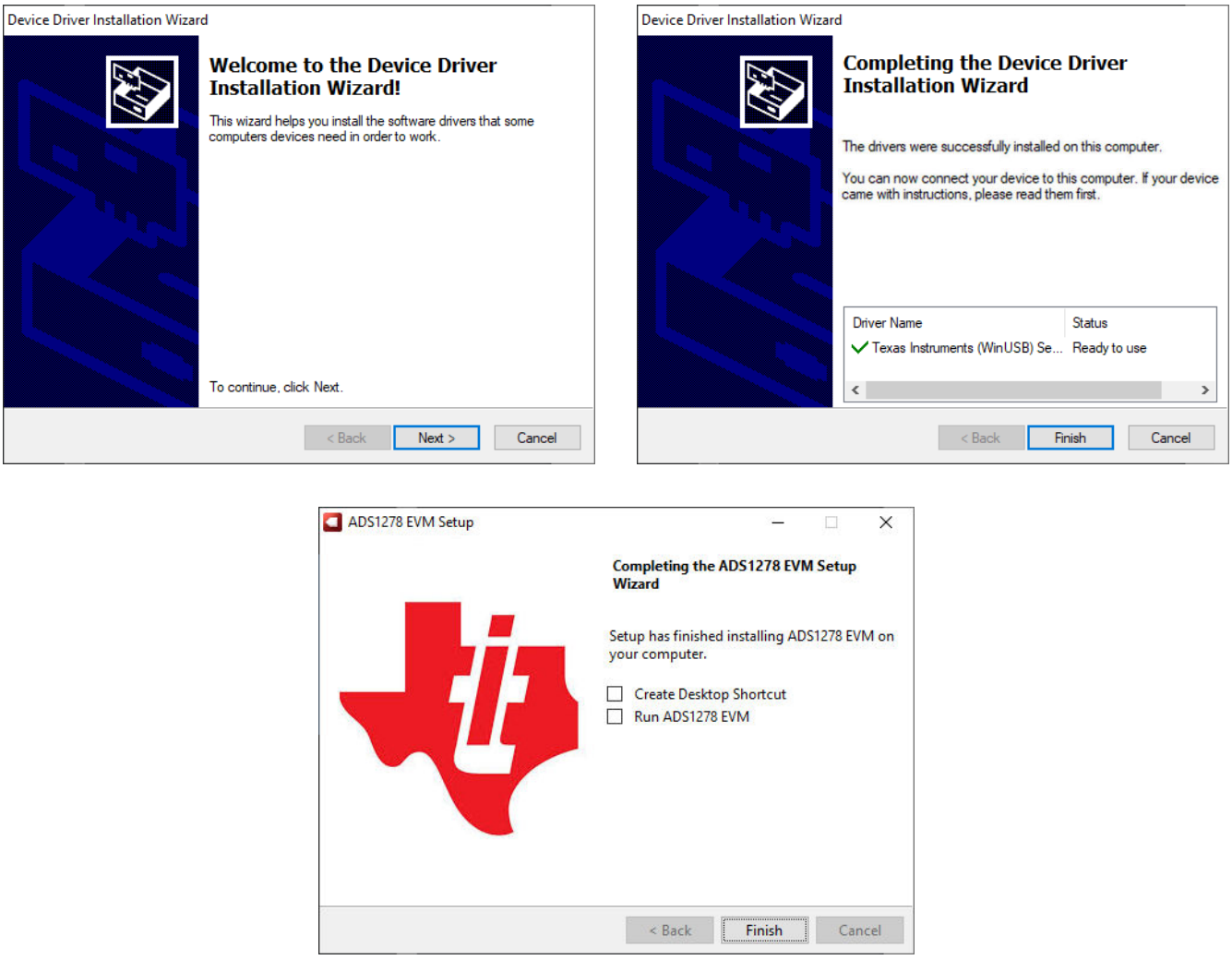


Figure 3-2. Device Driver Installation Prompts

The ADS1278 EVM requires the LabVIEW™ run-time engine and can prompt for the installation of this software if the LabVIEW run-time engine is not already installed, as shown in Figure 3-3.

Figure 3-3. LabVIEW Runtime Installation Prompts

4 Implementation Results

4.1 Hardware Connections

Connect the EVM as shown in Figure 4-1 after installing the software:

1. Physically connect P2 of the PHI to J5 of the ADS1278 EVM.
2. Install the screws to provide a robust connection. Connect the USB on the PHI to the computer.
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
   b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC.
3. Power the ADS1278 EVM through the J10 terminal with 6V.
4. Start the software GUI. Notice that the LEDs on the PHI blink slowly when the FPGA firmware is loaded on the PHI. Loading takes a few seconds.
5. Connect the signal generator. The input range is 0V to 5V. A common input is a 4.9V_{PP} signal with a 2.5V offset. This signal is adjusted just below the full-scale range to avoid clipping.

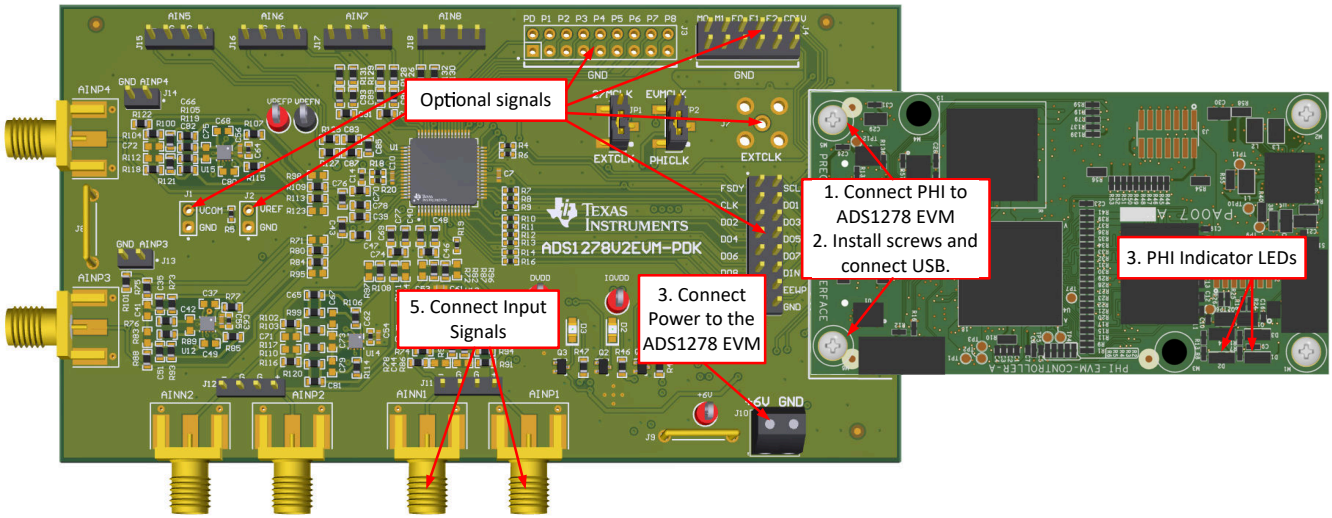


Figure 4-1. Hardware Connections

4.2 GUI Settings for ADC Control

Figure 4-2 shows that the EVM global controls are located on the left-hand side of the GUI. These controls include the number of samples, clock frequencies, sampling rate, and other important parameters. In the upper left-hand side of the GUI is the *Pages* tree, which allows access to the other key pages in the GUI.

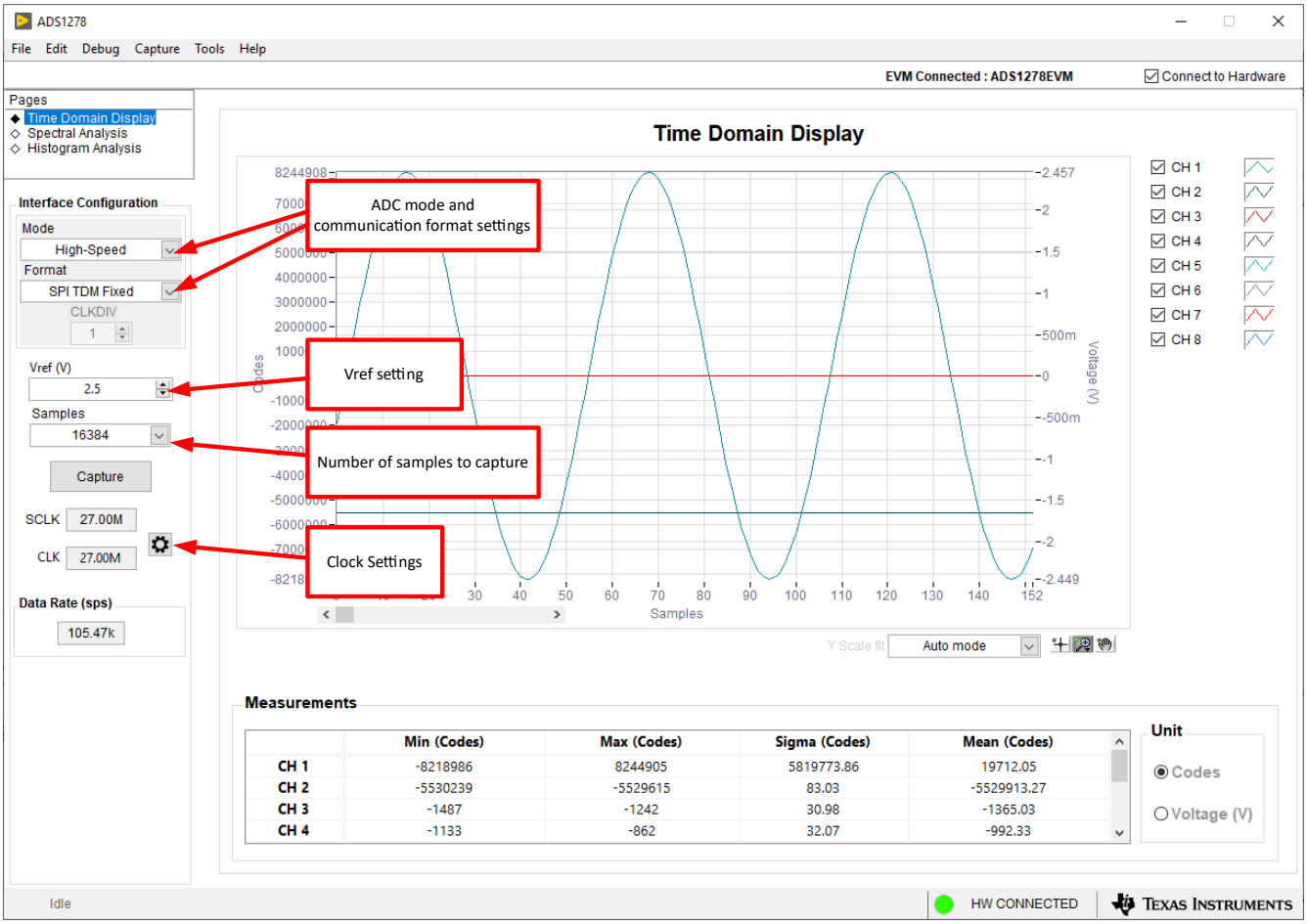


Figure 4-2. EVM Settings

4.3 Time Domain Display

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits. The user can capture the selected number of samples from the ADS1278 EVM by using the *Capture* button. The sample indices are on the x-axis and two y-axes show the corresponding output codes and the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the analysis tools described in the subsequent sections causes calculations to be performed on the same set of data.

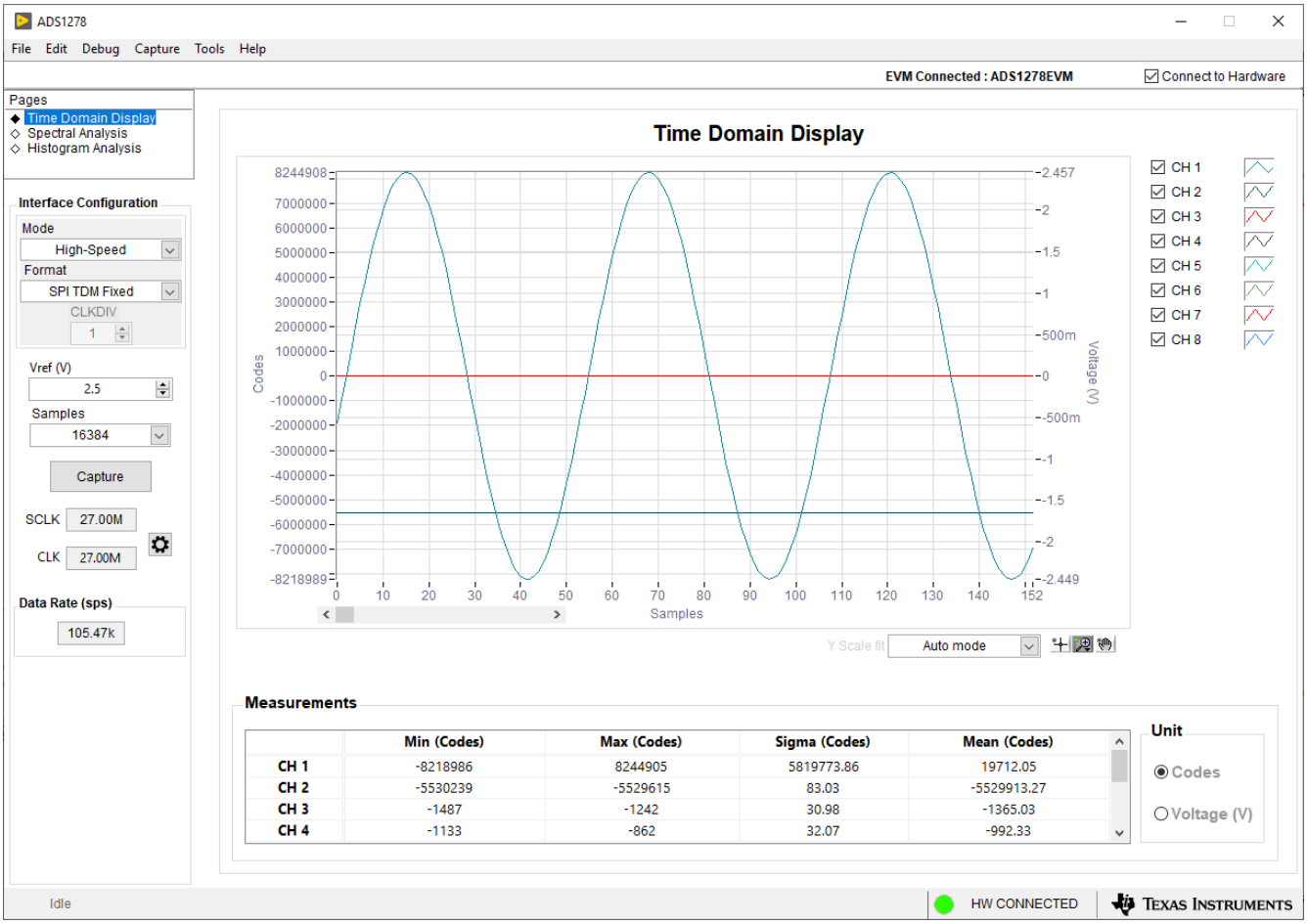


Figure 4-3. Time Domain Display

4.4 Frequency Domain Display

The spectral analysis tool shown in Figure 4-4 is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS1278 ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-Term Blackman-Harris window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The *None* option corresponds to not using a window (or a rectangular window) and is not recommended.

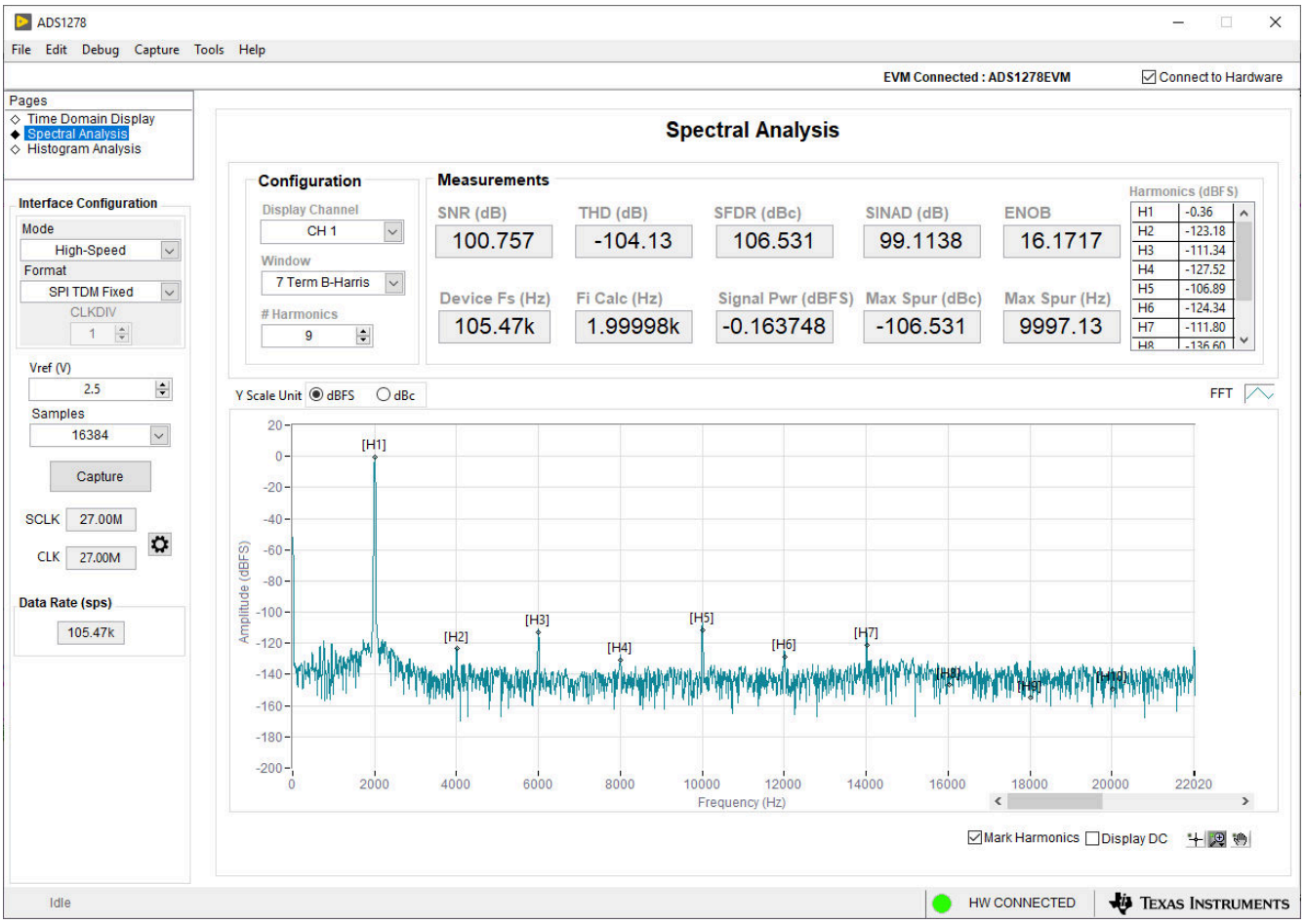


Figure 4-4. Frequency Domain Display

4.5 Histogram Display

Noise degrades ADC resolution and the histogram tool can be used to estimate effective resolution, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a dc signal. The cumulative effect of noise coupling to the ADC output from sources (such as the input drive circuits, reference drive circuit, ADC power supply, and the ADC) is reflected in the standard deviation of the ADC output code histogram. The histogram is obtained by performing multiple conversions of a dc input applied to a given channel. As shown in Figure 4-5, the histogram corresponding to a dc input is displayed on clicking the *Capture* button.

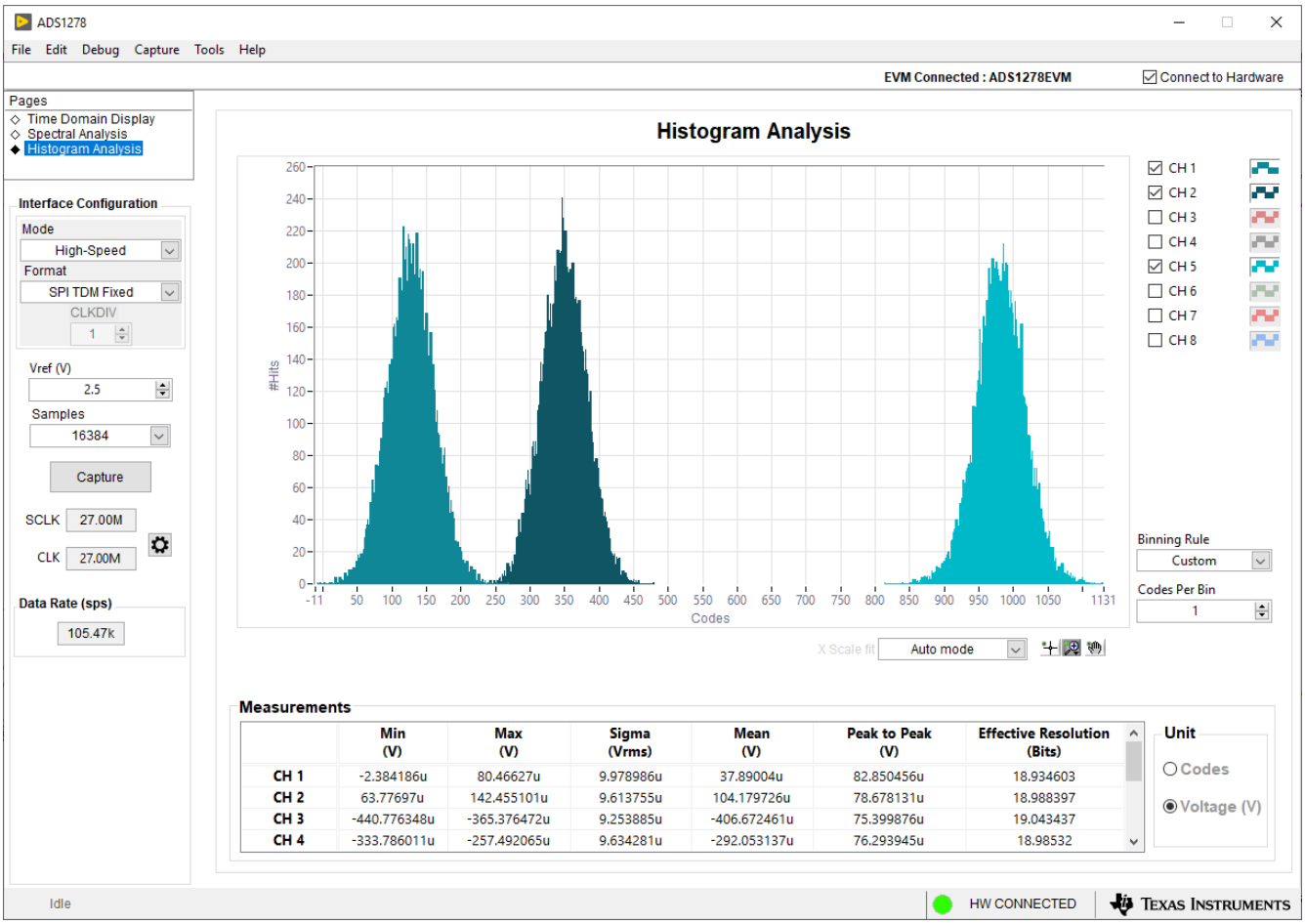


Figure 4-5. Histogram Display

5 Hardware Design Files

This section contains the ADS1278 EVM schematics, and PCB layout, and bill of materials (BOM)

5.1 Schematics

This section shows the schematics for the ADS1278 EVM.

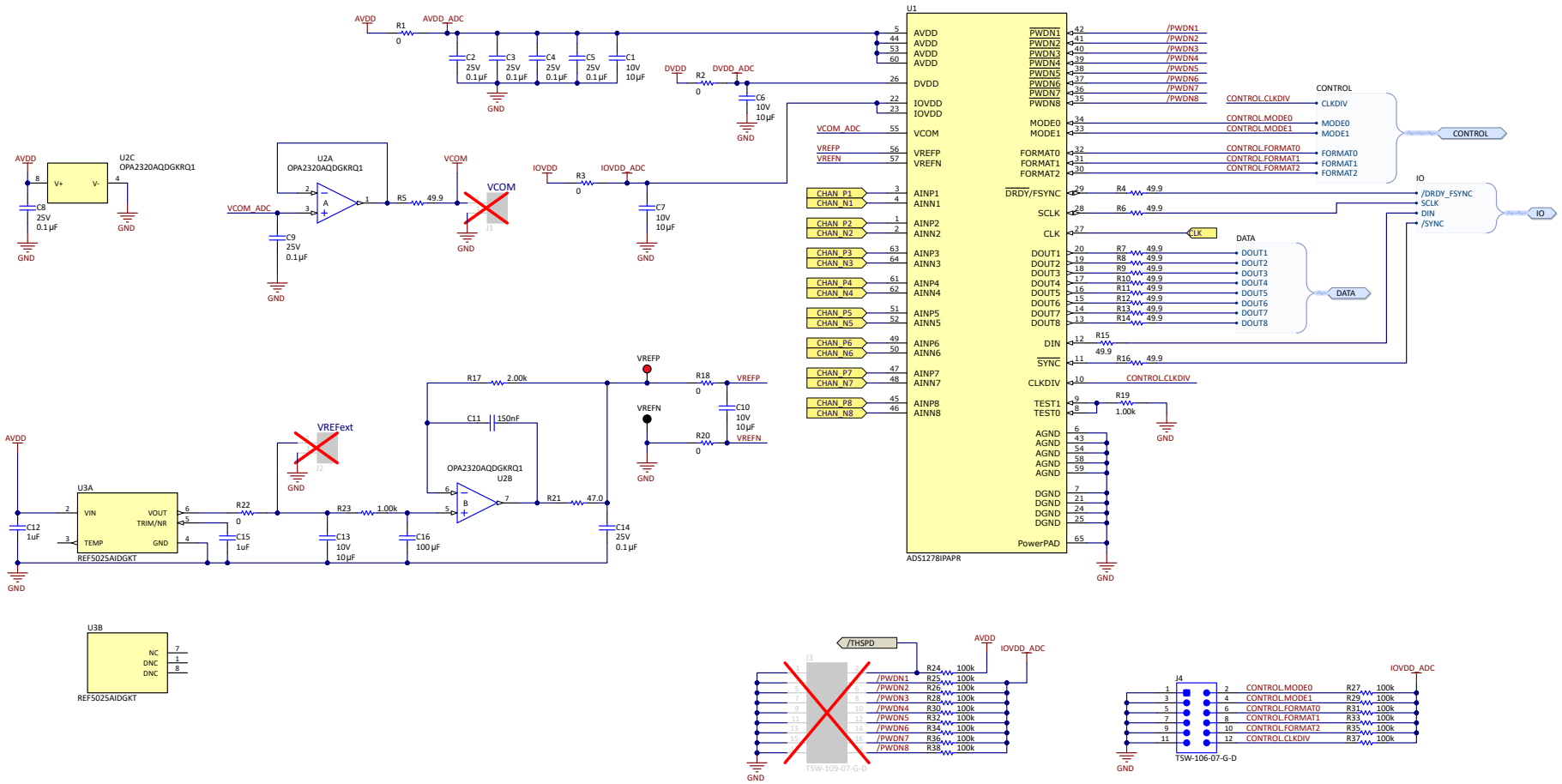


Figure 5-1. ADS1278 Connections Schematic

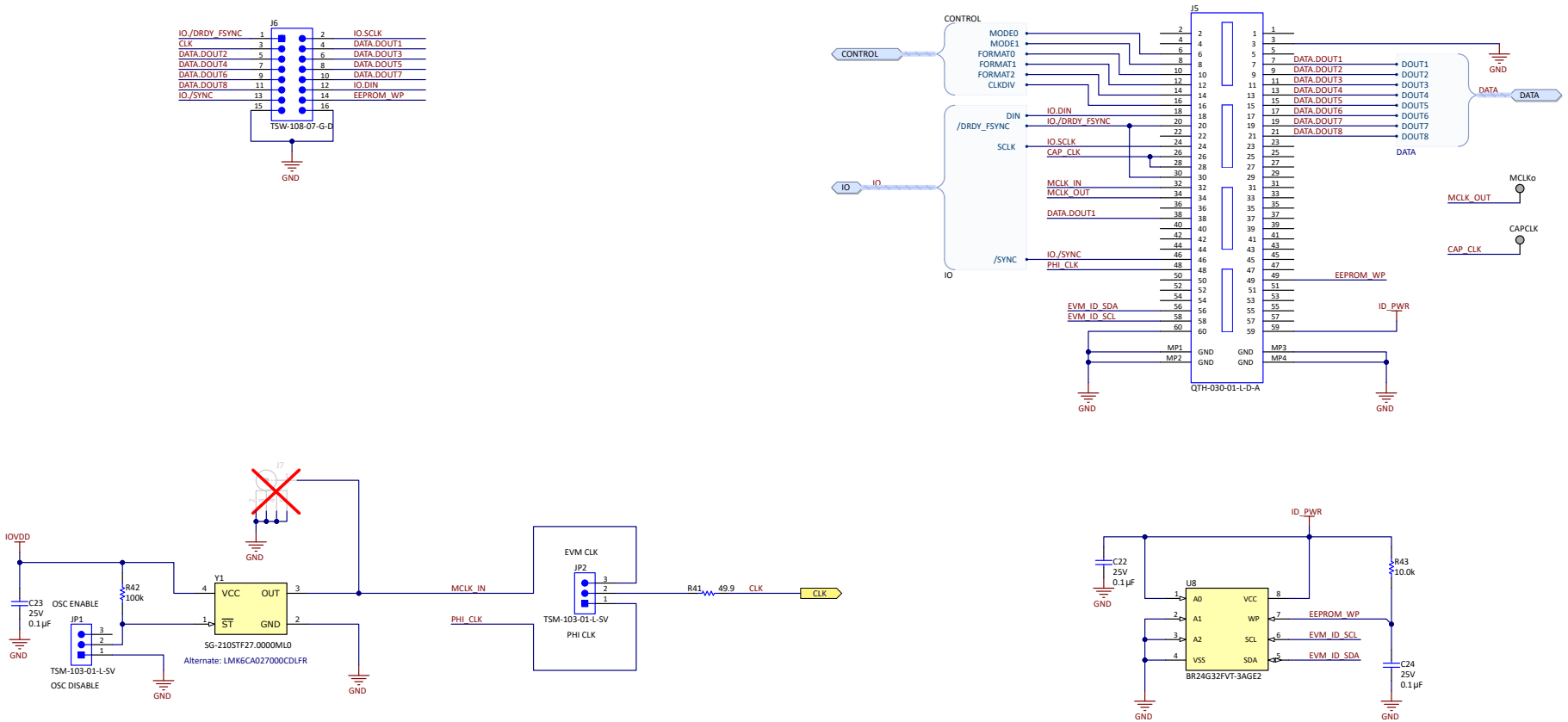


Figure 5-2. ADS1278 EVM Digital Connections Schematic

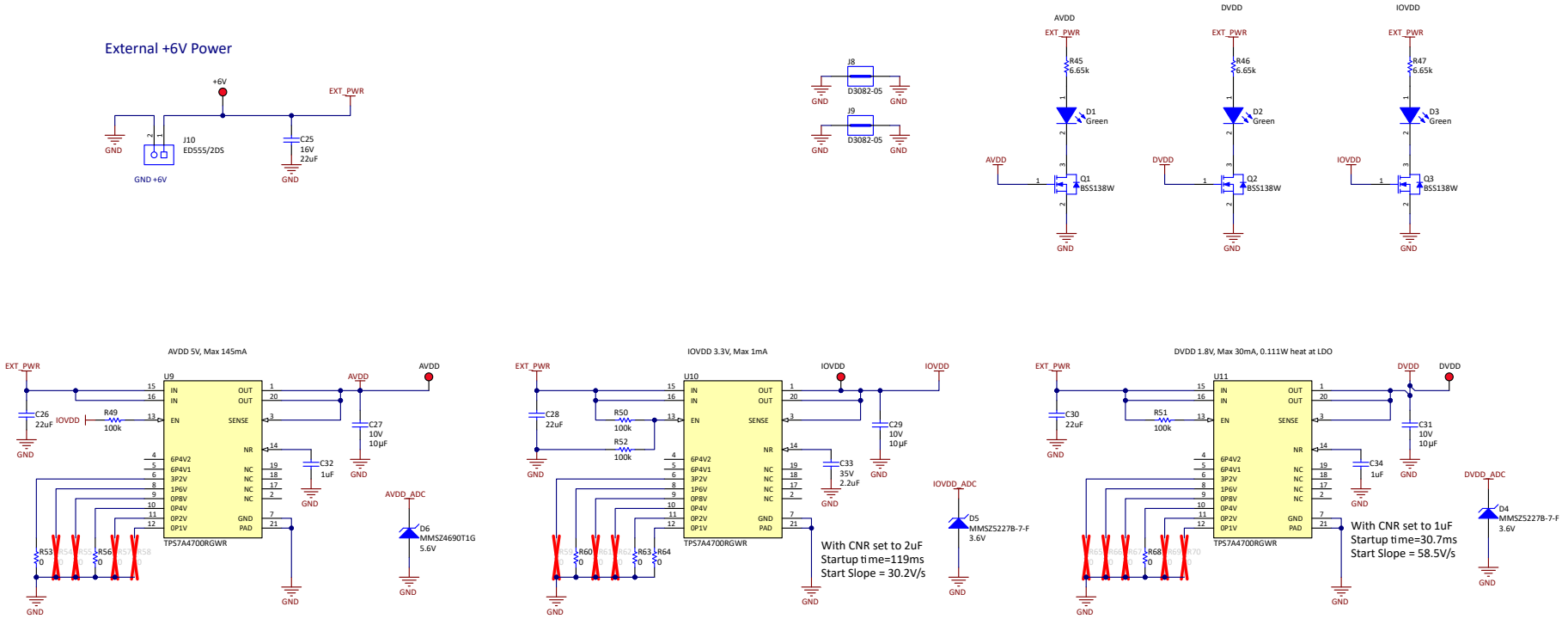


Figure 5-3. Power Supplies Schematic

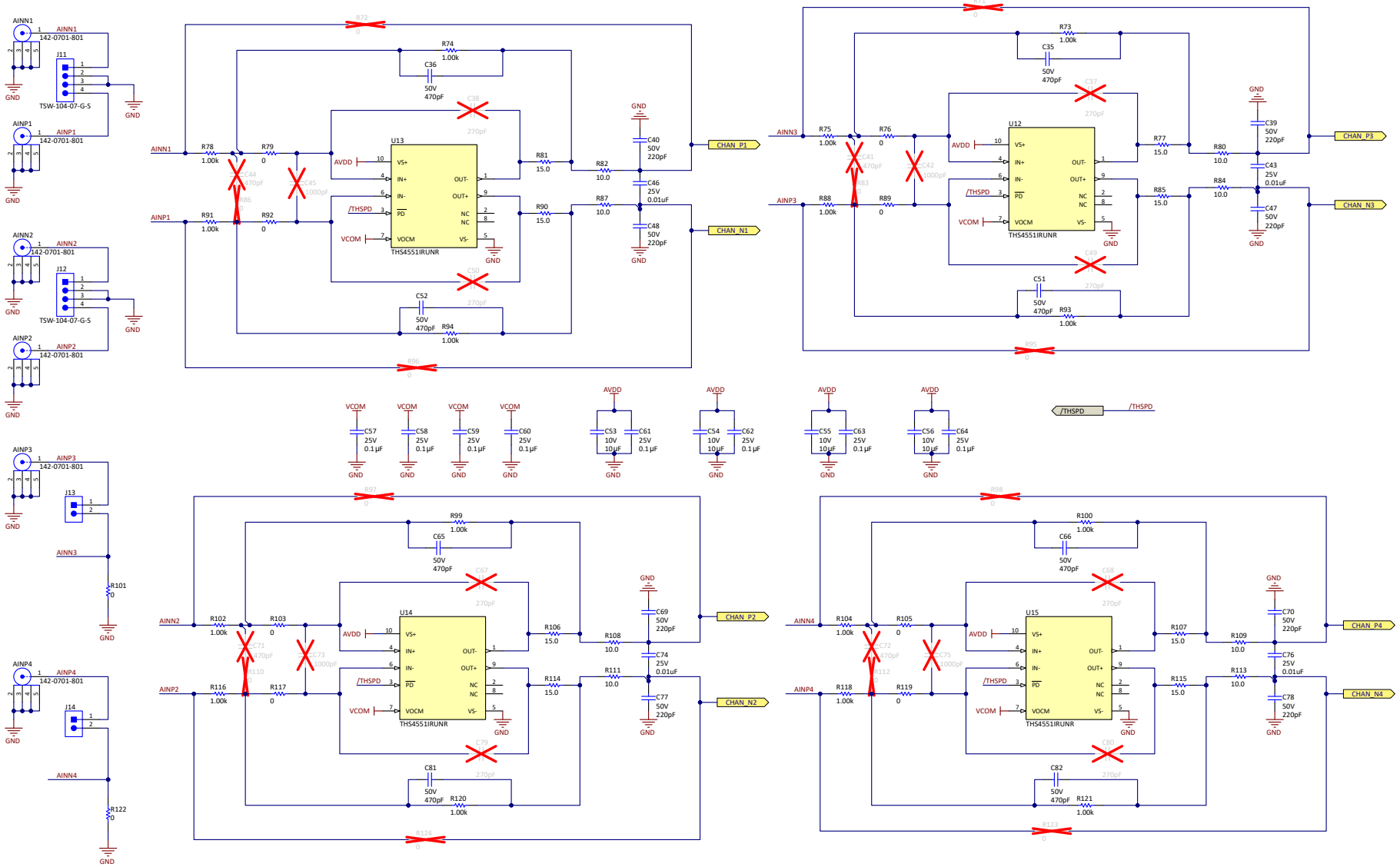


Figure 5-4. Driven Input Circuitry Schematic

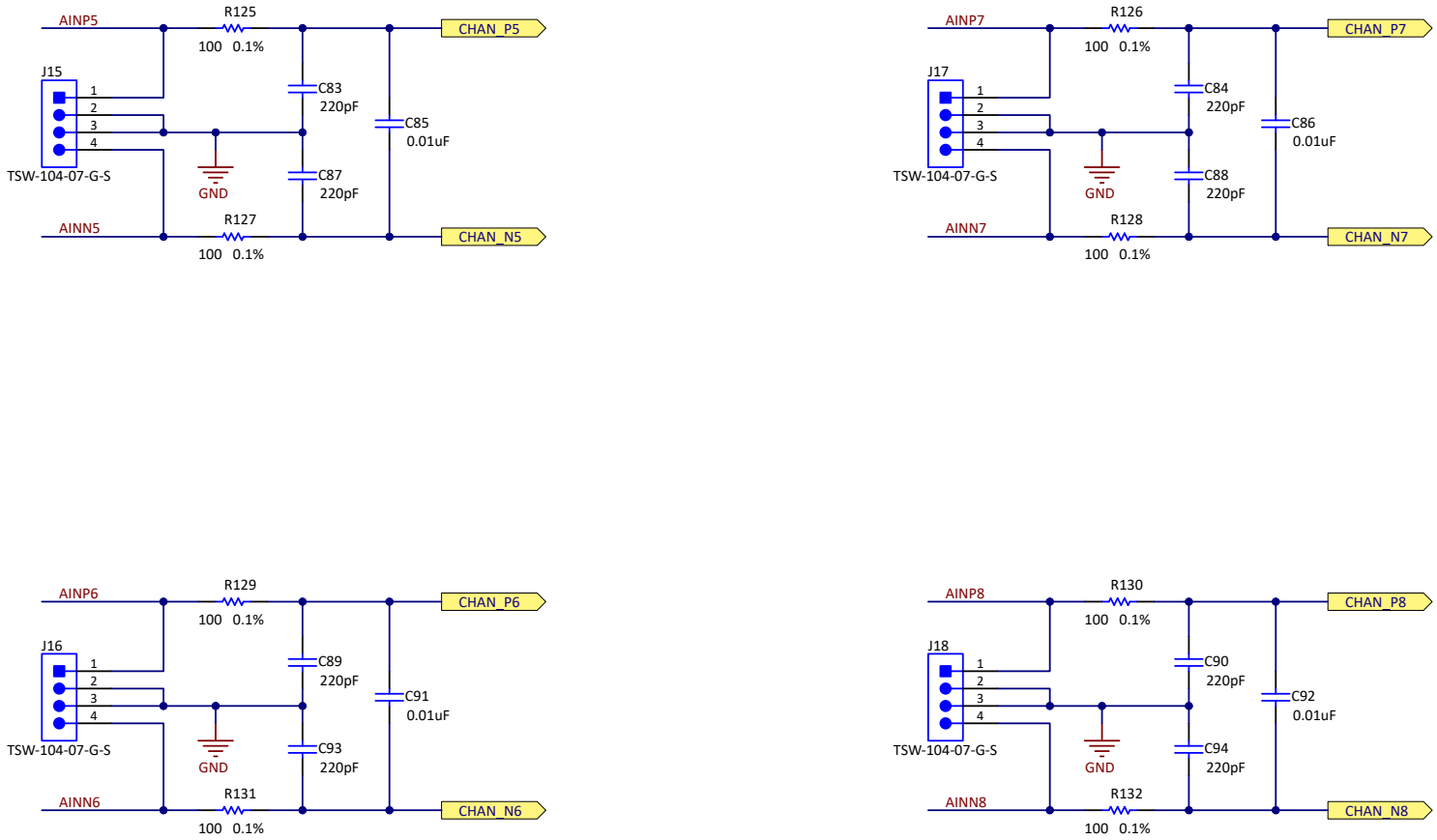


Figure 5-5. Undriven Input Circuitry Schematic

5.2 PCB Layouts

Figure 5-6 through Figure 5-11 show the PCB layouts for the ADS1278 EVM.

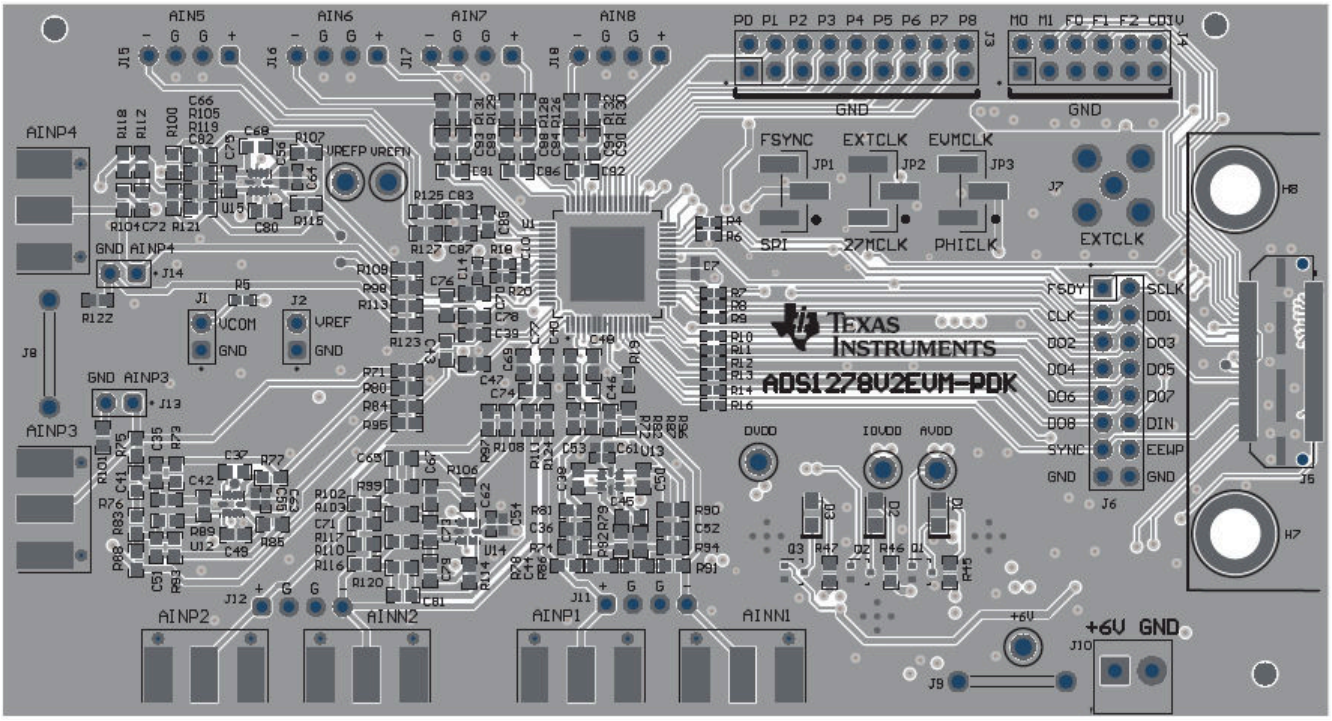


Figure 5-6. Top Side Composite Layout

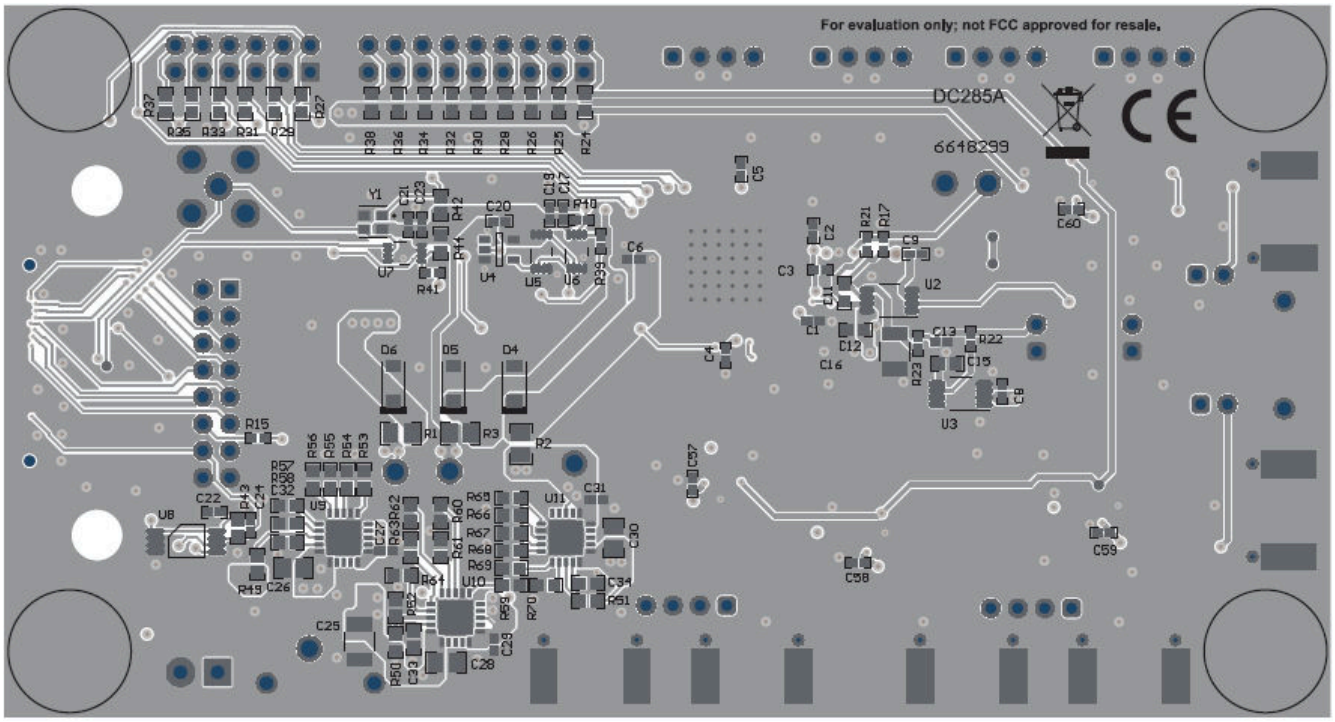


Figure 5-7. Bottom Side Composite Layout

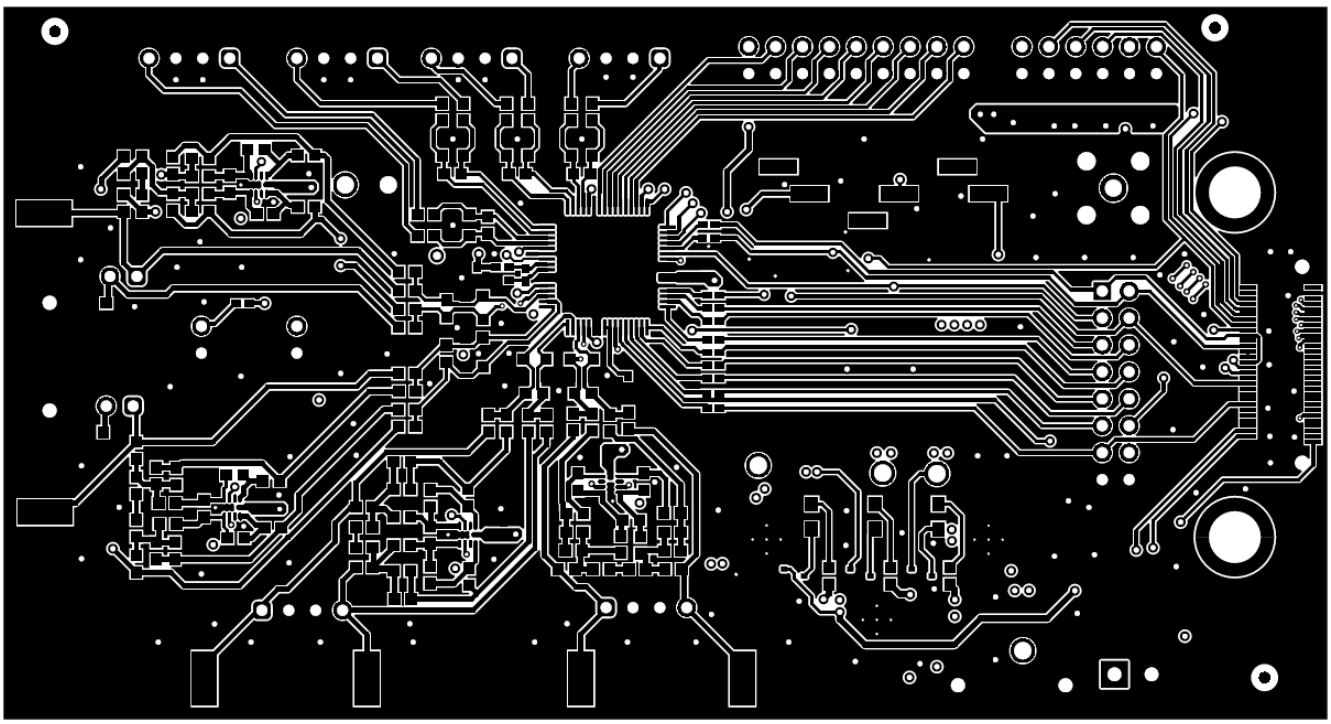


Figure 5-8. Top Signal Layer Layout

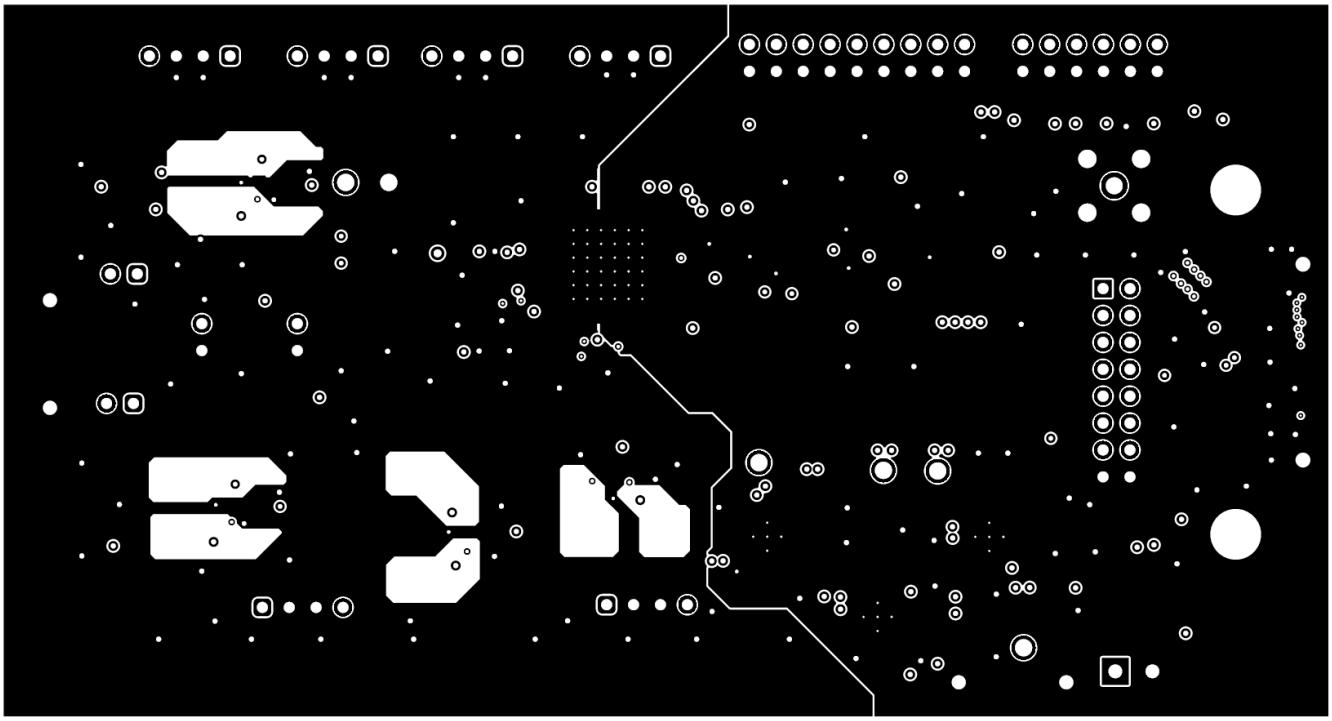


Figure 5-9. Ground Layer Layout

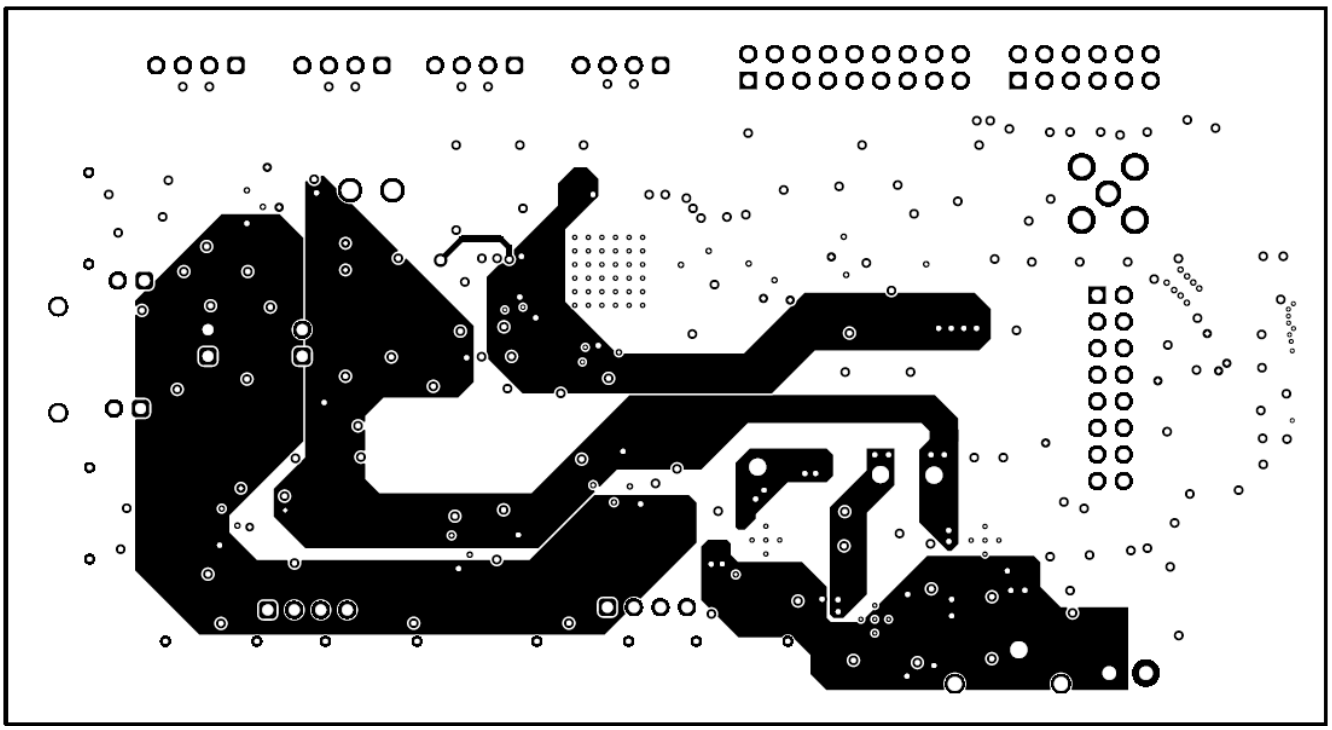


Figure 5-10. Power Layer Layout

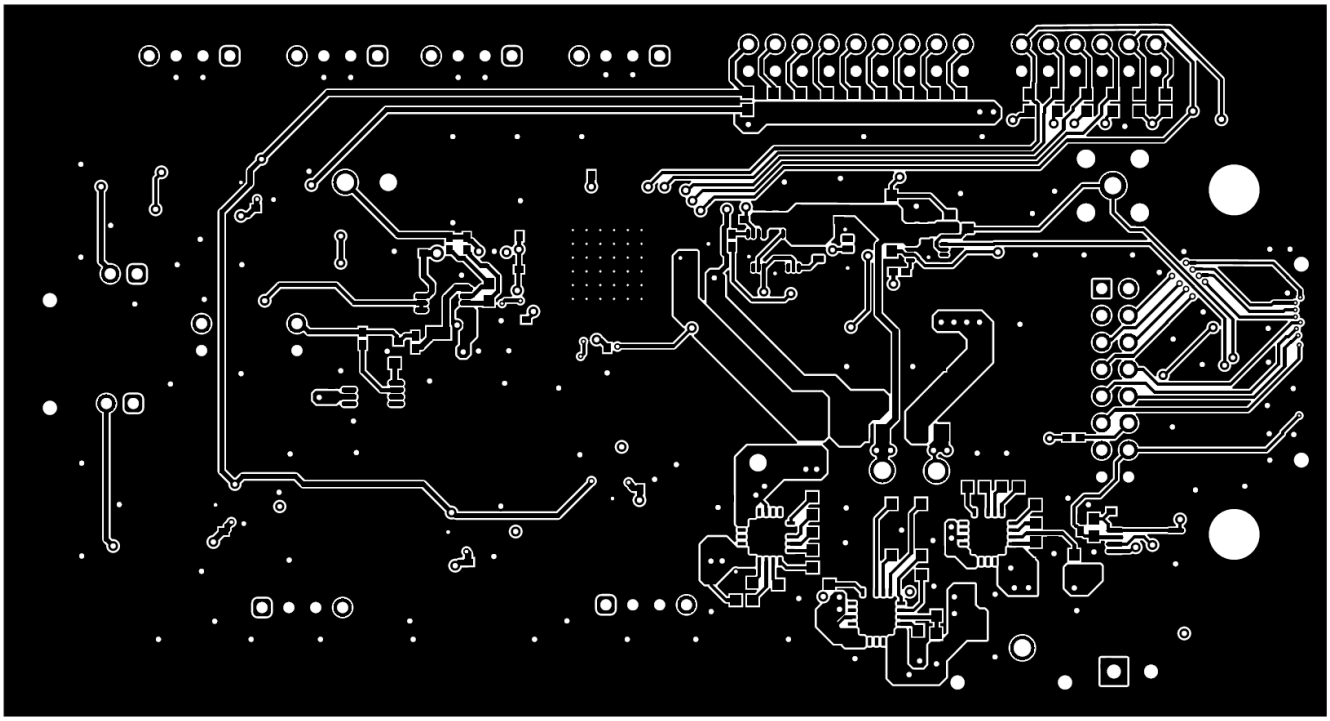


Figure 5-11. Bottom Signal Layer Layout

5.3 Bill of Materials (BOM)

Table 5-1 lists the bill of materials (BOM) for the ADS1278 EVM

Table 5-1. ADS1278EVM Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		DC285	Any
+6V, AVDD, DVDD, IOVDD, VREFP	5		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone Electronics
AINN1, AINN2, AINP1, AINP2, AINP3, AINP4	6		Connector, End launch SMA, 50 ohm, SMT	End Launch SMA	142-0701-801	Cinch Connectivity
C1, C6, C7, C10, C13, C27, C29, C31, C53, C54, C55, C56	12	10uF	CAP, CERM, 10µF, 10V,+/- 20%, X5R, 0402	0402	CL05A106MP8NUB8	Samsung Electro-Mechanics
C2, C3, C4, C5, C8, C9, C14, C22, C23, C24, C57, C58, C59, C60, C61, C62, C63, C64	18	0.1uF	CAP, CERM, 0.1µF, 25V,+/- 10%, X7R, 0402	0402	CC0402KRX7R8BB104	Yageo
C11	1	0.15uF	CAP, CERM, 0.15µF, 25V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	C0603X154K3RAC7867	Kemet
C12, C15, C32, C34	4	1uF	CAP, CERM, 1uF, 35V, +/- 10%, X5R, 0603	0603	GMK107BJ105KA-T	Taiyo Yuden
C16	1	100uF	CAP, CERM, 100µF, 10V,+/- 20%, X5R, 1210	1210	CL32A107MPVNNNE	Samsung
C25	1	22uF	CAP, CERM, 22uF, 16V, +/- 10%, X7R, 1210	1210	GCM32ER71C226KE19L	MuRata
C26, C28, C30	3	22uF	CAP, CERM, 22uF, 35V, +/- 20%, X5R, 0805	0805	C2012X5R1V226M125AC	TDK
C33	1	2.2uF	CAP, CERM, 2.2uF, 35V, +/- 10%, X5R, 0603	0603	C1608X5R1V225K080AC	TDK
C35, C36, C51, C52, C65, C66, C81, C82	8	470pF	CAP, CERM, 470pF, 50V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H471JA01D	MuRata
C39, C40, C47, C48, C69, C70, C77, C78, C83, C84, C87, C88, C89, C90, C93, C94	16	220pF	CAP, CERM, 220pF, 50V, +/- 5%, C0G/NP0, 0603	0603	C0603C221J5GACTU	Kemet
C43, C46, C74, C76, C85, C86, C91, C92	8	0.01uF	CAP, CERM, 0.01uF, 25V, +/- 5%, C0G/NP0, 0603	0603	C0603H103J3GACTU	Kemet
CAPCLK, MCLKo	2		Test Point, SMT	Test Point, SMT	S2751-46R	Harwin

Table 5-1. ADS1278EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
D1, D2, D3	3	Green	LED, Green, SMD	LED_0805	APT2012LZGCK	Kingbright
D4, D5	2	3.6V	Diode, Zener, 3.6V, 500mW, SOD-123	SOD-123	MMSZ5227B-7-F	Diodes Inc.
D6	1	5.6V	Diode, Zener, 5.6V, 500mW, SOD-123	SOD-123	MMSZ4690T1G	ON Semiconductor
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
H5, H6	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL
H7, H8	2		ROUND STANDOFF M3 STEEL 5MM	ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik
J4	1		Header, 100mil, 6x2, Gold, TH	6x2 Header	TSW-106-07-G-D	Samtec
J5	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A	Samtec
J6	1		Header, 100mil, 8x2, Gold, TH	8x2 Header	TSW-108-07-G-D	Samtec
J8, J9	2		1mm Uninsulated Shorting Plug, 10.16mm spacing, TH	Shorting Plug, 10.16mm spacing, TH	D3082-05	Harwin
J10	1		Terminal Block, 3.5mm Pitch, 2x1, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
J11, J12, J15, J16, J17, J18	6		Header, 100mil, 4x1, Gold, TH	4x1 Header	TSW-104-07-G-S	Samtec
J13, J14	2		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
JP1, JP2	2		Header, 100mil, 3x1, Gold, SMT	Samtec_TSM-103-01-X-SV	TSM-103-01-L-SV	Samtec
Q1, Q2, Q3	3	50V	MOSFET, N-CH, 50V, 0.21A, SOT-323	SOT-323	BSS138W	Fairchild Semiconductor
R1, R2, R3	3	0	RES, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6GEY0R00V	Panasonic
R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R41	14	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF49R9X	Panasonic
R17	1	2.00k	RES, 2.00 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K00FKED	Vishay-Dale
R18, R20, R22	3	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale
R19, R23	2	1.00k	RES, 1.00 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K00FKED	Vishay-Dale

Table 5-1. ADS1278EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R21	1	47.0	RES, 47.0, 1%, 0.063 W, 0402	0402	RK73H1ETTP47R0F	KOA Speer
R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R42	16	100k	RES, 100 k, 5%, 0.1 W, 0603	0603	CRCW0603100KJNEAC	Vishay-Dale
R43	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R45, R46, R47	3	6.65k	RES, 6.65 k, 1%, 0.1 W, 0603	0603	RC0603FR-076K65L	Yageo
R49, R50, R51, R52	4	100k	RES, 100 k, 1%, 0.1 W, 0603	0603	RC0603FR-07100KL	Yageo
R53, R56, R60, R63, R64, R68	6	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
R73, R74, R75, R78, R88, R91, R93, R94, R99, R100, R102, R104, R116, R118, R120, R121	16	1.00k	RES, 1.00 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD071KL	Yageo America
R76, R79, R89, R92, R103, R105, R117, R119	8	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603ZT0R00	Stackpole Electronics Inc
R77, R81, R85, R90, R106, R107, R114, R115	8	15.0	RES, 15.0, 0.1%, 0.1 W, 0603	0603	RT0603BRD0715RL	Yageo America
R80, R82, R84, R87, R108, R109, R111, R113	8	10.0	RES, 10.0, 0.1%, 0.1 W, 0603	0603	CRT0603-BY-10R0ELF	Bourns
R101, R122	2	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R125, R126, R127, R128, R129, R130, R131, R132	8	100	RES, 100, 0.1%, 0.1 W, 0603	0603	RT0603BRD07100RL	Yageo America
SH-J1, SH-J2	2	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
U1	1		Octal, Simultaneous Sampling, 24-Bit Analog-to-Digital Converters	HTQFP64	ADS1278IPAPR	Texas Instruments
U2	1		Automotive Qualified Precision, Zero-Crossover, 20MHz, 0.9pA Ib, RRIO, CMOS Operational Amplifier, DGK0008A (VSSOP-8)	DGK0008A	OPA2320AQDGKRQ1	Texas Instruments

Table 5-1. ADS1278EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
U3	1		3µVpp/V Noise, 3ppm/°C Drift Precision Series Voltage Reference, DGK0008A (VSSOP-8)	DGK0008A	REF5025AIDGKT	Texas Instruments
U8	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm
U9, U10, U11	3		36V, 1A, 4.17µVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)	RGW0020A	TPS7A4700RGWR	Texas Instruments
U12, U13, U14, U15	4		Low Noise, Precision, 150MHz, Fully Differential Amplifier, RUN0010A (WQFN-10)	RUN0010A	THS4551IRUNR	Texas Instruments
VREFN	1		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone Electronics
Y1	1		27MHz XO (Standard) CMOS Oscillator 1.6V ~ 3.6V Standby (Power Down) 4-SMD, No Lead	SMT_XTAL_2MM5_2MM	SG-210STF27.0000ML0	Epson
C37, C38, C49, C50, C67, C68, C79, C80	0	270pF	CAP, CERM, 270pF, 50V, +/- 5%, C0G/NP0, 0603	0603	06035A271JAT2A	AVX
C41, C44, C71, C72	0	470pF	CAP, CERM, 470pF, 50V, +/- 5%, C0G/NP0, 0603	0603	06035A471JAT2A	AVX
C42, C45, C73, C75	0	1000pF	CAP, CERM, 1000pF, 50V, +/- 5%, C0G/NP0, 0603	0603	C0603C102J5GACTU	Kemet
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J1, J2	0		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
J3	0		Header, 100mil, 9x2, Gold, TH	9x2 Header	TSW-109-07-G-D	Samtec
J7	0		Connector, SMA, TH	SMA	142-0701-201	Cinch Connectivity
R54, R55, R57, R58, R59, R61, R62, R65, R66, R67, R69, R70	0	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
R71, R72, R83, R86, R95, R96, R97, R98, R110, R112, R123, R124	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06030000Z0EA	Vishay-Dale

6 Additional Information

6.1 Trademarks

PowerPAD™ and LabVIEW™ are trademarks of Texas Instruments.
Microsoft® and Windows® are registered trademarks of Microsoft Corporation.
All trademarks are the property of their respective owners.

7 References

- Texas Instruments, Quad/Octal, Simultaneous Sampling, 24-Bit Analog-to-Digital Converters data sheet

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2024) to Revision B (February 2025)	Page
• Added *Using the ADS1278EVM With an External Controller* section	12
• Deleted *Optional EVM Configuration* section	18

Changes from Revision * (January 2024) to Revision A (February 2024)	Page
• Added *Operating Conditions* table	3

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

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東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

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