

Single-supply, high-input voltage, full-wave rectifier circuit



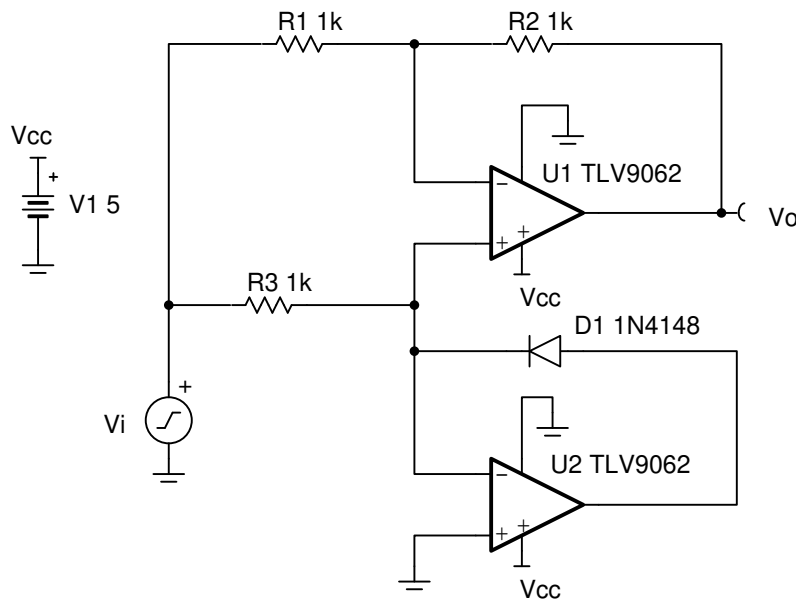
Amplifiers

Design Goals

| Input | Output | Frequency | Supply | |
|------------|------------|-----------|----------|----------|
| V_{iMax} | V_{oMax} | f_{Max} | V_{cc} | V_{ee} |
| 9Vpp | 4.5Vpp | 50kHz | 5V | 0V |

Design Description

This single-supply precision full-wave rectifier is optimized for high-input voltages. When $V_i > 0V$, D_1 is reverse biased and the top part of the circuit, U1, is activated resulting in a circuit with a gain of $1V/V$. When $V_i < 0V$, D_1 is forward biased and the bottom part of the circuit, U2, is activated resulting in an inverting amplifier circuit with a gain of $-1V/V$.

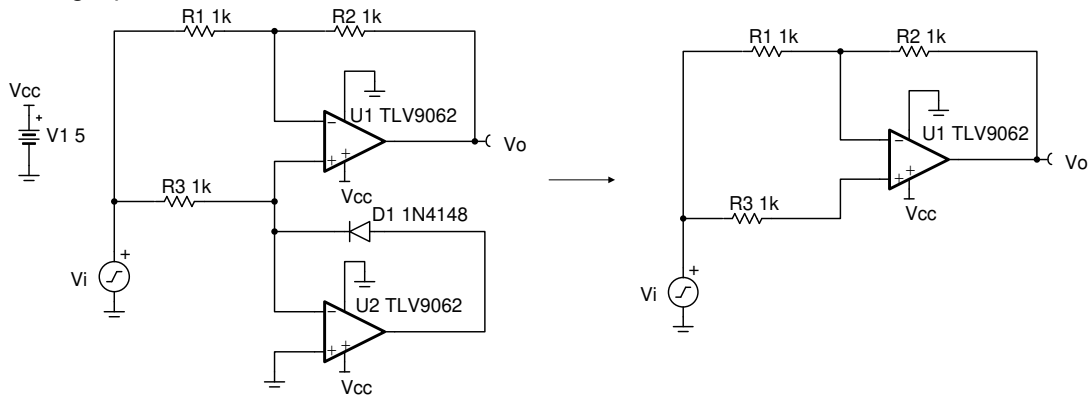


Design Notes

1. Observe common-mode and output swing limitations of op amps.
2. R_3 should be sized small enough that the leakage current from D_1 does not cause errors for positive input cycles while ensuring the op amp can drive the load.
3. Use a fast switching diode for D_1 .
4. Resistor tolerance determines the gain error of the circuit.
5. Use a negative charge pump (such as the [LM7705](#)) for output swing requirements to GND to maintain linearity for output signals near 0V. For additional information. see [Single-supply, low-input voltage, full-wave rectifier circuit](#).
6. For more information on op amp linear operating region, stability, capacitive load drive, driving ADCs, and bandwidth please see the [Design References](#) section.

Design Steps

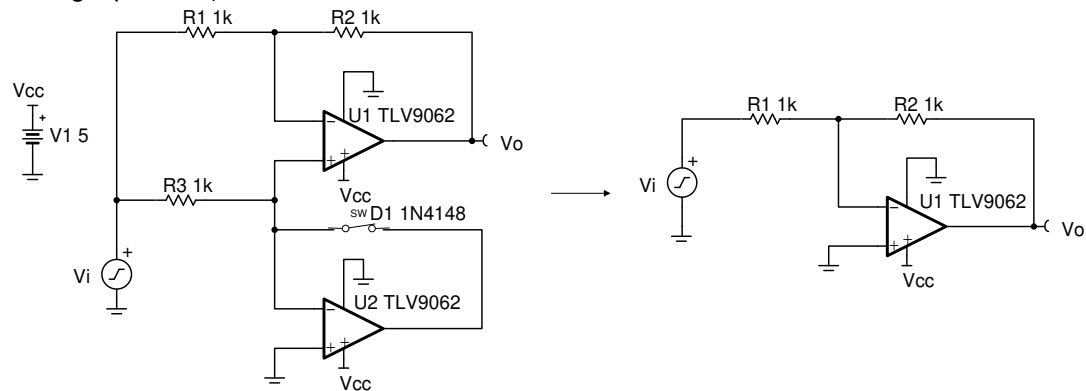
1. Circuit analysis for positive input signals. D_1 is reverse-biased disconnecting the output of U_2 from the non-inverting input of U_1 .



$$\frac{V_o}{V_i} = \left(-\frac{R_2}{R_1}\right) + \left(1 + \frac{R_2}{R_1}\right) = 1$$

$$V_o = V_i$$

2. Circuit analysis for negative input signals. D_1 is forward biased, which connects the output of U_2 to the non-inverting input of U_1 , which is GND.



$$\frac{V_o}{V_i} = \left(-\frac{R_2}{R_1}\right) = -1$$

$$V_o = -V_i$$

3. Select R_1 , R_2 , and R_3 .

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}$$

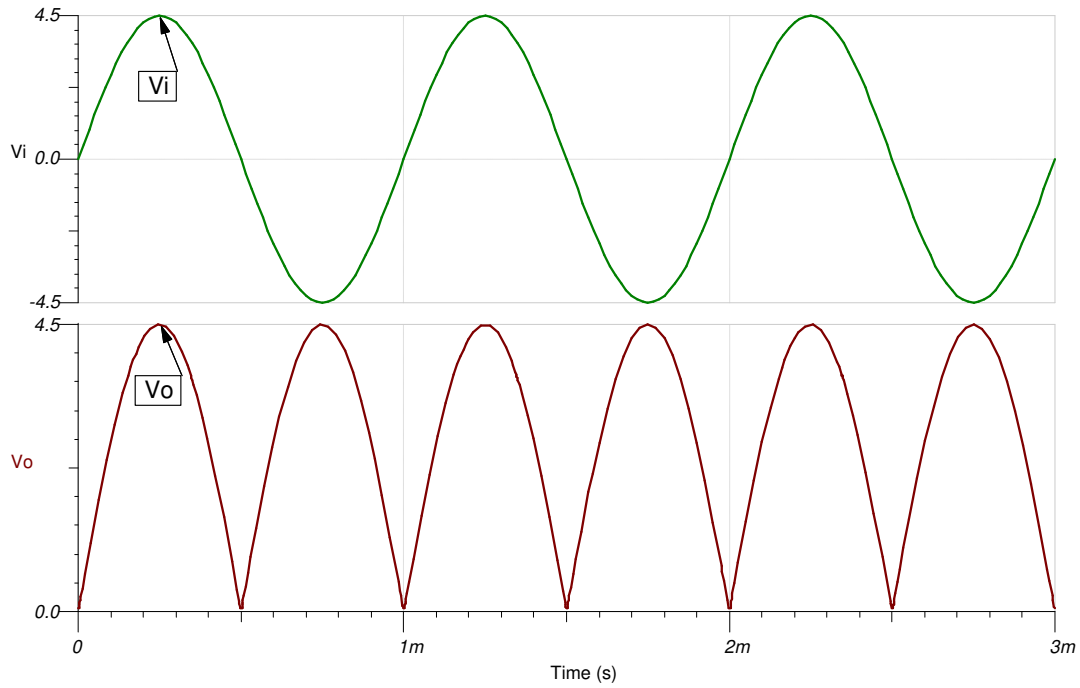
$$\text{If } R_2 = R_1 \text{ then } V_o = -V_i$$

$$\text{Set } R_1 = R_2 = R_3 = 1\text{k}\Omega$$

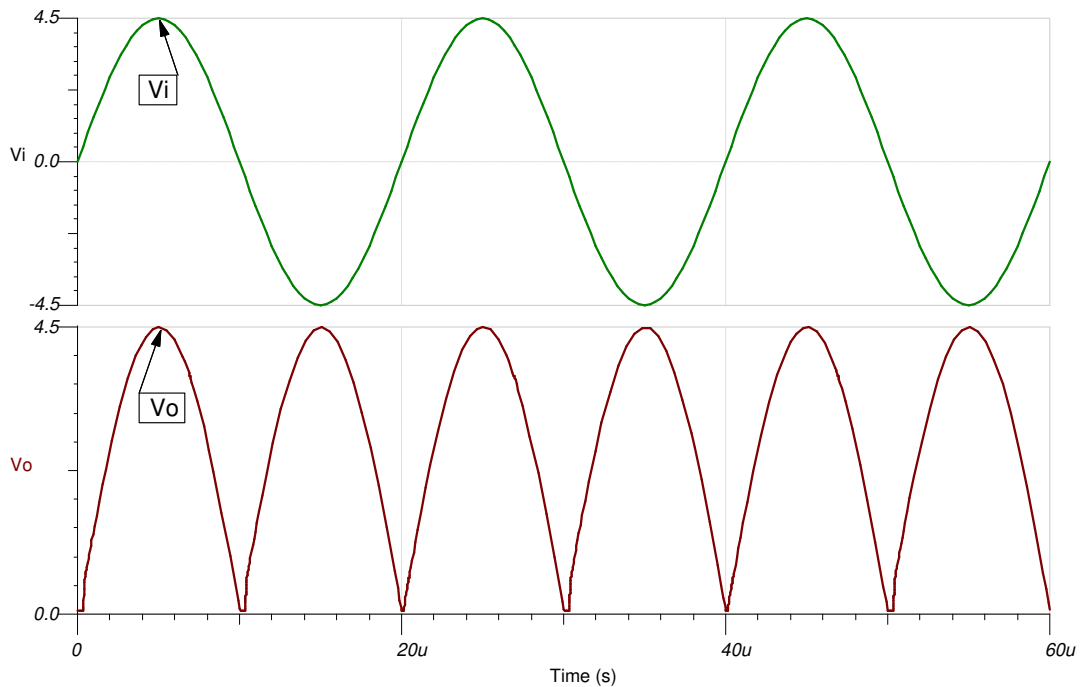
Design Simulations

Transient Simulation Results

A 1-kHz, 9-V_{pp} sine wave yields a 4.5-V_{pp} output sine wave.



A 50-kHz, 9-V_{pp} sine wave yields a 4.5-V_{pp} output sine wave.



Design References

1. See [Analog Engineer's Circuit Cookbooks](#) for the comprehensive TI circuit library.
2. SPICE Simulation File [SBOC529](#).
3. [TI Precision Labs](#)
4. See the [Single-Supply Low-Input Voltage Optimized Precision Full-Wave Rectifier Reference Design](#).

Design Featured Op Amp

| TLV9062 | |
|--|---------------|
| V_{SS} | 1.8V to 5.5V |
| V_{inCM} | Rail-to-rail |
| V_{out} | Rail-to-rail |
| V_{os} | 0.30mV |
| I_q | 538 μ A |
| I_b | 0.5pA |
| UGBW | 10MHz |
| SR | 6.5V/ μ s |
| #Channels | 1, 2, 4 |
| www.ti.com/product/TLV9062 | |

Design Alternate Op Amps

| | OPA322 | OPA350 |
|------------------|--|--|
| V_{SS} | 1.8V to 5.5V | 2.7V to 5.5V |
| V_{inCM} | Rail-to-rail | Rail-to-rail |
| V_{out} | Rail-to-rail | Rail-to-rail |
| V_{os} | 2mV | 0.15mV |
| I_q | 1.9mA | 5.2mA |
| I_b | 10pA | 0.5pA |
| UGBW | 20MHz | 38MHz |
| SR | 10V/ μ s | 22V/ μ s |
| #Channels | 1, 2, 4 | 1, 2, 4 |
| | www.ti.com/product/OPA322 | www.ti.com/product/OPA350 |

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