Application Note

Amplifier Input Common-Mode and Output-Swing Limitations

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ABSTRACT

This application note explains the cause of amplifier input and output limitations, focusing mainly on CMOS input and output stage topologies. We also discuss common design pitfalls associated with input and output range limitations, and offer simple solutions which can be implemented to resolve situations where an amplifier is taken outside of its linear operating range.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Single N-FET or P-FET vs Complimentary N-P-FET Input Stage Limitations

The common-mode voltage range of an amplifier is the range of usable input voltages allowing for linear operation. Depending on the input stage topology, amplifiers may have common mode input range (V_{CM}) which may be limited relative to one or both supply rails; best case scenario is achieved when input voltage range extends slightly beyond both supply rails (rail-to-rail operation). Limitations in the V_{CM} range come from operating voltages needed to bias the transistors in the input stage, and to ensure operation within a linear range (saturation range for MOSFET or active range for bipolar transistors). We'll illustrate these limitations for MOSFET amplifier input stages. Figure 1-1 shows a simplified representation of an N-channel MOSFET input stage. The stage consists of a current source (single NMOS, Q3, shown for simplicity), a differential pair with input voltage applied to the gate of each transistor, and an active load PMOS current mirror, Q4 and Q5. The NMOS differential pair has an input common mode voltage limitation with respect to the negative rail, $-V_s$. Performing Kirchhoff's voltage walk from $-V_s$ to V_{in+}, we have:

$$V_{in\pm\,(min)} = -V_s + V_{sat}(Q_3) + V_{gs}(Q_1,Q_2) \quad (1)$$

$$V_{in\pm\,(min)} = -V_s + 0.1\ V + 0.9\ V$$

$$V_{in\pm\,(min)} = -V_s + 1\ V$$

Therefore, the N-channel MOSFET V_{CM} range is limited to $-V_s$ by a certain voltage as detailed in Equation 1. Note that we make some important assumptions, namely that V_{sat} of both NMOS and PMOS transistors are perfectly matched and equal to 0.1V (a typical value). Similarly, we assume that V_{gs} for both NMOS and PMOS transistors are equal and have a value of 0.9V, a typical value to turn on the transistors. With these assumptions in mind, we can say that this simplified NMOS input stage allows input common mode voltage range operation about 1 V from V_s. Performing Kirchhoff's walk from the opposite end, $+V_s$ to $V_{in\pm}$, we get:

$$V_{in\pm\,(max)} = +V_s - V_{ds}(Q_5,Q_4) - V_{ds}(Q_1,Q_2) + V_{gs}(Q_1,Q_2) \quad (2)$$

$$V_{in\pm\,(max)} = +V_s - V_{gs}(Q_4,Q_5) - V_{sat}(Q_1,Q_2) + V_{gs}(Q_1,Q_2)$$

$$V_{in\pm\,(max)} = +V_s - 0.9\ V - 0.1\ V + 0.9\ V$$

$$V_{in\pm\,(max)} = +V_s - 0.1\ V$$

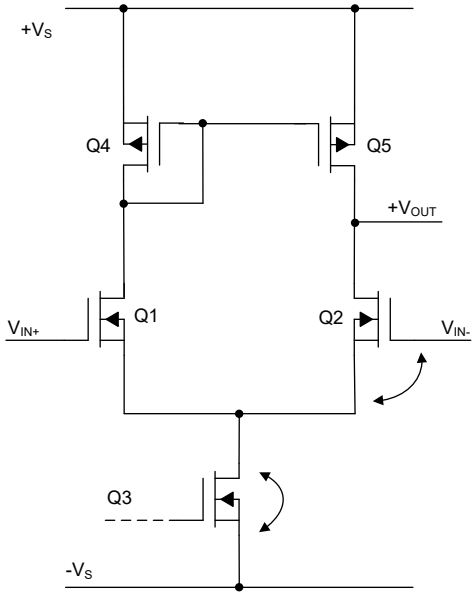

Figure 1-1. Simplified Representation of an N-Channel MOSFET Input Stage

Given that V_{gs} typically exceeds V_{ds} for a MOSFET at the edge saturation (V_{sat} at a minimum, V_{gs} at a maximum), the maximum V_{CM} comes within V_{sat}, or 100 mV, of the positive rail, $+V_s$.

Conversely, the P-channel MOSFET input stage is limited on the positive side, usually on the order of 1 V from positive rail, $+V_s$. On the negative side, the common mode voltage range of a P-MOSFET can come within V_{sata}, or 100 mV from the negative rail,$-V_s$.

To avoid the limitations of the single differential pair input stage, a complimentary N-channel and P-channel MOSFET (CMOS) input stage design can be used. This design uses two input differential pairs (an N-channel MOSFET pair and a P-channel MOSFET pair), a current steering scheme, and a double-folded cacose summing the two input signals (Figure 1-2). V_{set} is a voltage source used to control the functionality of the diverting transistor Q_8. For common mode voltage below $+V_s - V_{set}$, Q_8 is off, and the drain current (I_d) from Q_5 (current source) flows straight through the P-channel differential pair (Q_1 and Q_2). The double-folded cascode allows the drains of Q1 and Q2 to be biased down to V_{sat} above $-V_s$, resulting in V_{CM} swing below the negative rail. This allows the V_{CM} to extend a certain voltage, ΔV_P, below the negative rail. Similarly, for common mode voltage above $+V_s - V_{set}$ Q_8 is on, and I_d is steered from the P-channel pair to the N-channel pair via the current mirror (Q_6 and Q_7). The V_{CM} range can therefore exceed the positive rail, $+V_s$, by a certain voltage, ΔV_N. To sum it up, this gives an op-amp with this input stage topology a rail-to-rail V_{CM} range as detailed in Equation 3.

$$+V_s + \Delta V_N > V_{CM} > -V_s - \Delta V_P \quad (3)$$

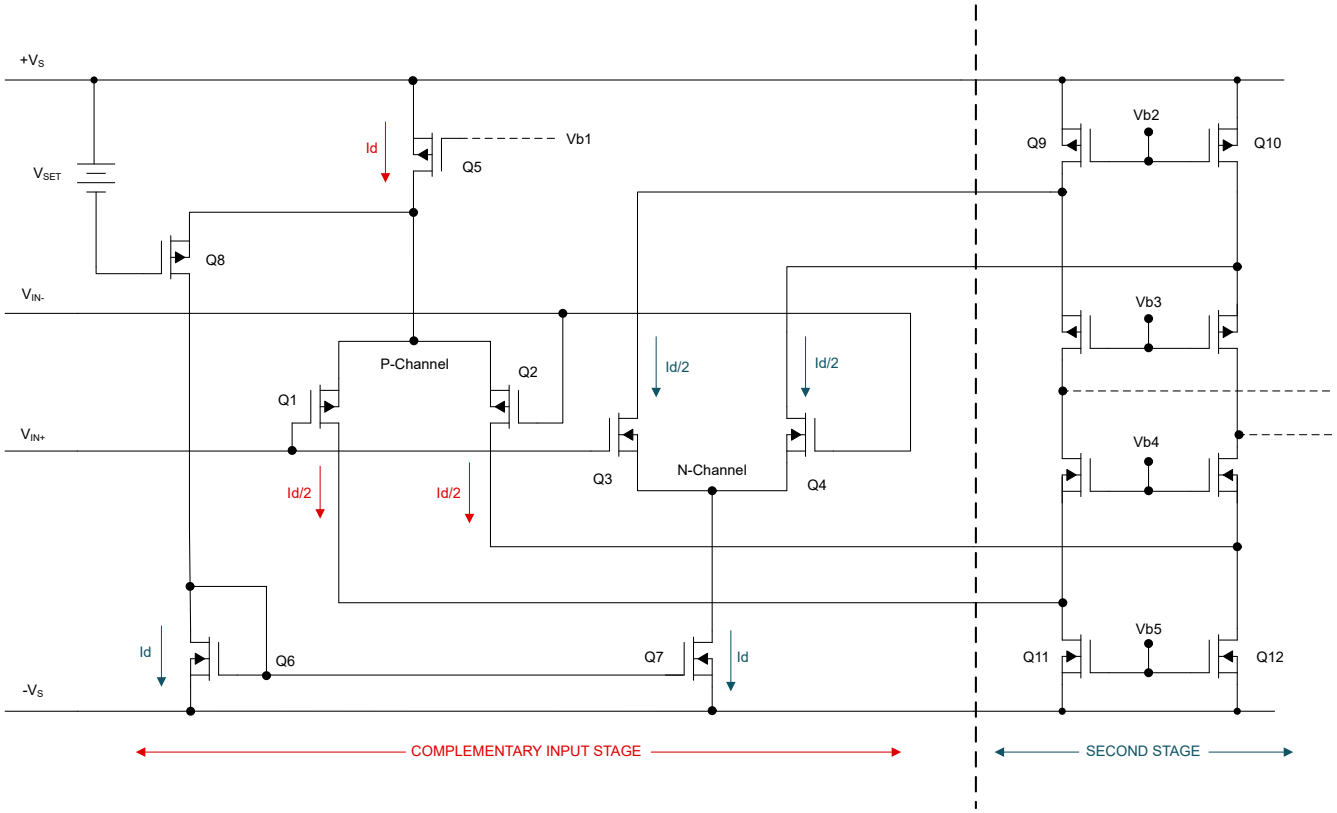

Figure 1-2. Simplified Representation of a Complementary N-P-FET Input Stage

Now that we understand the rail-to-rail operation of a complementary input stage, we more elaborately address ΔV_N and ΔV_P. Looking deeper into the complementary input stage amplifier in Figure 1-2, we can see that the rail-to-rail input performance is dependent on the second stage. Using Kirchhoff's voltage law from the positive rail down to the input, similar to the one performed previously on Figure 1-1.

$$V_{in\pm\,(max)} = +V_s - V_{sat}(Q_9,Q_{10}) - V_{ds}(Q_3,Q_4) + V_{gs}(Q_3,Q_4) \quad (4)$$

$$V_{in\pm\,(max)} = +V_s - 0.1\ V - 0.1\ V + 0.9\ V$$

$$V_{in\pm\,(max)} = +V_s + 0.7\ V$$

We can see from Equation 4 above that the complimentary input stage amplifier has input common mode range 0.7 V above the positive rail. We can find the common mode input voltage range to the negative rail by performing the same procedure.

$$V_{in\pm\,(min)} = -V_s + V_{sat}(Q_{11},Q_{12}) + V_{sat}(Q_1,Q_2) - V_{gs}(Q_1,Q_2) \quad (5)$$

$$V_{in\pm\,(min)} = -V_s + 0.1\ V + 0.1\ V - 0.9\ V$$

$$V_{in\pm\,(min)} = -V_s - 0.7\ V$$

From Equation 4 and Equation 5 we find that the common mode input voltage range extends beyond the positive and negative rail typically by about 0.7 V, which is represented by the aforementioned terms ΔV_N and ΔV_P. In data sheets, you will notice that most rail-to-rail amplifiers are specified up to 0.1 V (not 0.7 V) beyond the supplies. This is due to the protection diodes between the input and each rail.

2 Example 1: Output Swing Limitation from V_{CM} in an Op-Amp for Low Side Current Sense

As an example, let's assume that we are working with OPA391 operational amplifier, which we have in a gain of 100 V/V, powered with a 5.0-V single supply. Let's say we want to measure current between 0 and 50 A, and we choose a 1-mΩ shunt resistor. This means we will see differential input in the range of 0 to 50 A × 1 mΩ = 50 mV. The minimum V_{CM} value for OPA391 is 0.1V below ground, so our input conditions are in agreement with the data sheet requirements. However, OPA391 A_{OL} output conditions are specified in the range of $–V_s$ + 0.1 V < V_{out} < $+V_s$ – 0.1 V. Therefore, between 0 and 0.1 V and 4.9 V to 5 V of output the op-amp may encounter some non-linearity, which is undesirable. We can solve the issue quite easily:

- We can level-shift the input common mode up by 1 mV (which is amplified by the closed loop gain), or level shift $-V_s$ down by 100 mV. Level shifting the input can be achieved through a simple voltage divider circuit, or providing headroom for the output can be accomplished by providing a small negative rail. If no negative rail is present in the system, a negative charge pump like the LM7705 solves that problem in a single IC. In either case, it will put V_{out} at least 100 mV above $–V_s$ under 0 current condition, which resolves the output swing issue on the low end. Take note that either solution also exceeds the maximum linear operating range on the high end, which is in violation of the output voltage swing specifications. We can solve that issue by decreasing the gain of the circuit or the value of the shunt resistor slightly to bring $V_{out\ (max)}$ at or below $+V_s$ – 100 mV.

While the complementary input stage described offers an excellent solution to the input common mode problem, it is important to keep in mind that the transition between each pair will generate a change in the input offset voltage of the amplifier, also known as input crossover distortion. The transition can be eliminated by keeping both pairs conducting at all times, but this is often avoided because of the excessive power dissipation required. The input crossover distortion can be circumvented more elegantly by using a zero-crossover amplifier (*Zero-crossover Amplifiers: Features and Benefits* tech note). These amplifiers use a single transistor pair and an integrated charge pump to push the internal voltage supply enough beyond the nominal value to remain in linear operation.

3 Bipolar and CMOS Output Stage Topologies and Output Swing Limitations

The output swing range of an amplifier is the range of output voltages allowing for linear amplifier operation. As with V_{CM}, the output swing (V_{out}) limitations are related to operating voltages of transistors in the output stage. Depending on the application and topology, V_{out} may be more or less limited relative to the rails, regardless whether they are single, dual, or asymmetric. Perfect rail-to-rail performance does not exist in practice, although some of the complimentary MOSFET designs come fairly close.

Many applications require V_{out} swing to only one rail, typically the negative rail. The earliest op-amp output stages accomplished this by having an NPN emitter-follower configuration with a resistive pull-down (Figure 3-1 A). A pull-down resistor to the negative rail allows the output to approach the negative rail, but this greatly limits the sinking current and results in slow output response. A similar design (bipolar or MOSFET) utilized NPN/NMOS current sources in place of the pull-down resistor, offering higher gain and *near* to-negative-rail output swing (Figure 3-1 B).

With the advent of modern complimentary bipolar processes, better matched, high speed PNP and NPN transistors became available. As a result, the complimentary emitter-follower output stage (Figure 3-1 C) was developed with its most significant advantage being low output impedance. The major drawback of this topology is its limited output swing, typically on the order of 1V or more to the rail due to transistor operating voltages in the stage. Specifically, the minimal forward-bias voltage across the PNP current source (V_{FB-P}), and the base-emitter voltage (V_{BE-N}) limit swing to positive rail, whereas the V_{FB-N} of the NPN current source and the V_{BE-P} limit swing to negative rail. Full output voltage swing of the complimentary bipolar output stage is thus:

$$+V_s - V_{sat\ (npn)} - V_{be\ (pnp)} > V_{out} > -V_s + V_{sat\ (pnp)} + V_{be\ (npn)} \quad (6)$$

More recent complimentary common-emitter or common-source output stages (Figure 3-1 D and Figure 3-1 E), allow the op-amp output swing much closer to rail, but both of these stages have fairly high output impedance. For the bipolar version of this stage, the output swing limitation to each rail comes from $V_{ce,\ (sat)}$, or the minimal collector-emitter voltage needed to keep each transistor operating in the linear region. The typical V_{sat} for a bipolar transistor is 300mV at 25ºC and changes by roughly -2mV per each ºC increase in temperature.

$$-V_s + V_{sat} < V_{out} < +V_s - V_{sat} \quad (7)$$

We can perform a similar analysis to the MOSFET version of this stage, illustrated in Figure 3-1 (E). The output swing limitation comes from the MOSFET *on-resistance* (R_{on}) while in the triode region, which causes an output voltage range limitation relative to the rail equal to $I_d \times R_{on}$. In essence, in the non-linear operating region, the MOSFET acts as a small resistor and produces a voltage drop. Under unloaded conditions, $I_d = I_q$, the limitation caused by the voltage drop is on the order of 5 mV to 50mV, which is considered *almost* truly rail-to rail performance.

$$-V_s + I_d \times R_{on} > V_{out} > +V_s + I_d \times R_{on} \quad (8)$$

Keep in mind, that under normal operation I_d is equal to the quiescent current of the output transistors, I_q, plus the load current. In other words, the output swing will decrease as the load current increases. A plot illustrating this effect is included in data sheets – look for the output voltage swing vs output current plot (often known as a claw curve). Operate within the range of the curves to remain in linear operation

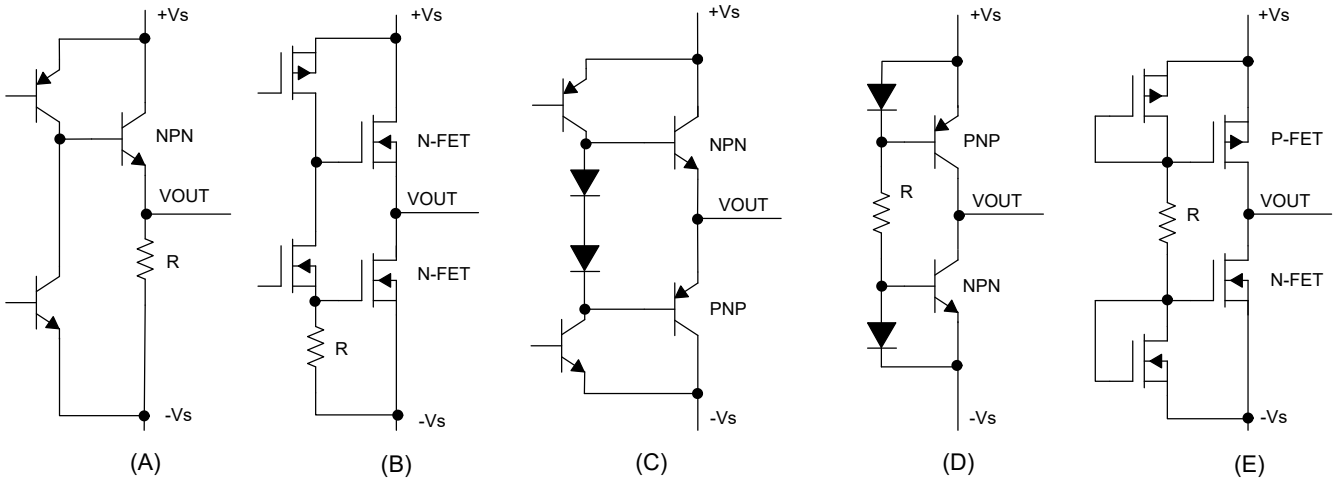

Figure 3-1. Common Output Stage Topologies

4 Example 2: Output Swing Limitations With Instrumentation Amplifiers

Let’s go back to our current shunt example, but this time the INA326 device is used in a gain of 100 V/V, and we power with a 5-V supply. Let's say we want to measure current between 1 A and 50 A, and we choose a 1mΩ shunt resistor. This means we will see a minimum of 1 A × 1 mΩ × 100 V/V = 100 mV on the output. The swing-to-GND of the INA326 is $-V_S$ + 0.02 V, so an expected minimum output of 100 mV is acceptable. However, at 50 A current, the output voltage would be 50 A × 1mΩ × 100V/V = 5 V. The swing to rail spec is $+V_S$ – 75mV, worst case, and 5 V exceeds that.

So, what we can do to improve the circuit?

1. Increase supply by at least 75 mV over 5 V (thus, increasing the output swing of the amplifier). This isn't usually an option in designs as power supplies are generally fixed at common values like 1.8 V, 2.5 V, 3.3 V, 5 V, and so forth. Also, the variation (minimum) of the supply needs to be considered, and has to always exceed 5.075 V to ensure linear operation.
2. Lower the gain. Setting a lower gain value would result in a lower maximum expected output voltage, keeping the amplifier within the linear mode of operation, at the expense of lower measurement resolution.
3. Choose a smaller shunt resistor. Reducing the value of the shunt resistor will decrease input signal and subsequently the output signal. Switching from 1 mΩ to 0.5 mΩ would keep the output well within the permissible range, at the expense of measurement resolution.
4. Choose a different amplifier with more suitable supply voltage specifications. For instance, the INA823 has a swing-to-positive supply spec of $+V_S$ – 150 mV, thus switching from the INA326 to the INA823 by itself would not resolve the output swing issue. However, the INA823 can support power supply voltages up to 36 V, so if the supply voltage was increased to the next higher available rail, this would ensure output remains within the linear range of the amplifier (this solution is applicable to op-amps as well).

5 Summary

In board-level design, it is important to recognize amplifier input and output stage limitations. Different amplifier input and output stage topologies offer different operating common mode voltage and output swing voltage ranges, respectively. Single supply mode of operation sometimes offers challenges with respect to keeping V_{CM} within the linear operating range on the low end. Choosing a device with V_{CM} range extending below ground or using a negative charge pump to lower the negative supply below ground can help resolve such issues. Conversely, having an expected output voltage value beyond the data sheet output swing specified limits will degrade output accuracy and should be avoided. If selecting an amplifier with a closer to-rail output swing is not an option, then parameters such as the gain of the circuit and supply voltage range can be adjusted to overcome output swing limitations.

Table 5-1. New Device Recommendations

Device	Description
OPA391	Micro-power (24 µA), ultra-low bias (0.8 pA), e-Trim™ rail-to-rail op-amp
OPA392	Wide-bandwidth (13 MHz), ultra-low bias (0.8 pA), precision (10 µV), e-Trim™ rail-to-rail op amp
OPA3S328	Wide bandwidth (40 MHz), low bias (10 pA), zero-crossover dual op amp with integrated switches in a tiny package
INA819	Low power (350 µA), low noise (8 nV/√Hz), precision (35 µV), 36-V super-beta input instrumentation amplifier available in tiny package Low power (350 µA), precision instrumentation amp with ±60-V overvoltage protection (gain pins 2, 3)
INA849	Low power (350 µA), low noise (8 nV/√Hz), precision (35 µV), 36-V super-beta input instrumentation amplifier with +/-60V overvoltage protection available in tiny package
INA823	Low power (180µA), precision (100µV), wide supply range (2.7-36 V) instrumentation amplifier with below ground input range (150 mV) and +/-60V overvoltage protection

6 References

- Texas Instruments, Op amps with complementary-pair input stages: What are the design trade-offs? Analog Design Journal
- Texas Instruments, Linear operating region of two-op-amp instrumentation amplifiers with gain stages Analog Design Journal
- Texas Instruments, Measuring the linear operating region of instrumentation amplifiers Analog Design Journal
- Instrumentation amplifier V_{CM} vs. V_{OUT} plots: Part 1
- Instrumentation amplifier V_{CM} vs. V_{OUT} plots: Part 2
- Instrumentation amplifier V_{CM} vs. V_{OUT} plots: Part 3

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