Application Note

Optimizing Dual Feedback Compensation in the OPA593 With a Current Booster for 1µF Capacitive Loads in ATE Applications

Raymond Zhang

ABSTRACT

Since the introduction of the OPA593, the power operational amplifier (PA) has gained traction in the test and measurement sector. Specifically designed for Automated Test Equipment (ATE) applications, the OPA593 can drive output voltages up to 80V and output currents up to ±250mA, all within a compact 4mm × 4mm WSON package. The OPA593 operates across the full industrial temperature range of -40°C to 125°C, providing exceptional DC precision and robust output current limiting features that cater to diverse design requirements in ATE applications.

This application note demonstrates how to compensate for the OPA593 PA and current booster configuration, enabling output driving currents up to ±1A. Additionally, the document explains the implementation of the op amp's dual feedback compensation techniques when driving capacitive loads of up to 1µF, making sure of adequate phase margin, stabilizing loop gains through AC analysis, and achieving fast step time responses in ATE applications.

Table of Contents

Trademarks

1 Introduction

The OPA593 is a high-voltage, high-output-current power amplifier (PA) that operates on an 85V single supply or a ±42.5V dual-supply configuration, with the capability to source or sink current up to ±250mA. This article focuses on dual-supply rail configurations, favored for their programmable and flexible precision voltage regulator setups commonly used in automated test equipment (ATE) applications. While the OPA593 meets the output voltage requirements for most power voltage regulator applications, OPA593 does not provide sufficient current drive in certain scenarios. In such cases, combining the OPA593 with a current booster topology can enhance the current drive capabilities while maintaining the amplifier's overall operating voltage range, bandwidth, accuracy, and responsiveness to timing requirements.

In practice, a large capacitive load is often connected to the output of a power amplifier stage. Capacitive loads serve several purposes, including decoupling, filtering high-frequency noise, reducing voltage spikes, stabilizing transient responses, and improving output voltage regulation at the device under test (DUT). However, adding capacitive loads can introduce undesirable phase lag, potentially leading to loop instability in the power amplifier's feedback system.

Driving large capacitive loads presents significant design challenges for engineers, particularly in compensating for stability issues. This application note addresses these challenges when using the OPA593 with a Darlington current booster configuration. The document also explores the trade-offs associated with this technique, especially when driving capacitive loads up to 1µF.

Figure 1-1 and Table 1-1 present the schematic discussed in this application note, which aims to meet (or exceed) the design requirements.

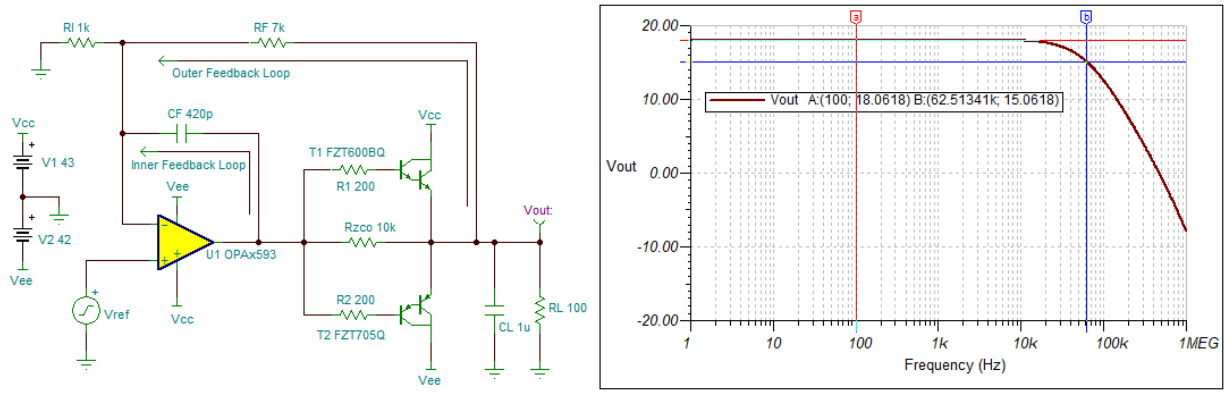

Figure 1-1. The OPA593 With a Current Booster Circuit Drives 1µF Capacitive Load, C_L

Table 1-1. ATE Design Requirements for OPA593 + Current Booster

Design Parameters	Composite Amplifier's Voltage Regulator Specifications
Input voltage range	Input swing up to ±5V_{dc}
Output voltage range	Output swing up to ±40V_{dc}
Output current range	OPA593 with current booster, driving up to ±1A_{dc}
Output impedance	R_L ≥ 40Ω
Closed-loop gains	8V/V
Open-loop output impedance	Open loop output impedance, Z_o < approximately 1Ω
Capacitive load	Low ESR (20mΩ), 1µF ceramic capacitive load and DUT
Effective bandwidth	Approximately 50kHz, cutoff frequency at the –3dB point
Step time behavior	Output rising/falling edge step-time response <100µs
Output voltage accuracy	Approximately 0.05% or better across full scale

2 Current Booster, Push-Pull Topology Output Characteristics

The current booster's open-loop output impedance and frequency response are among the key parameters in selecting a driver for ATE applications. The following criteria are summarized.

Table 2-1. Current Booster Driver Selection Criteria

No	Current Booster Driver Selection Guide
1	Low and consistent open-loop output impedance, with Z_o variation over frequency in a given application.
2	Low distortion and high slew rate: Minimize crossover distortion while optimizing voltage biasing.
3	Meet source or sink current requirements for driving large capacitive and resistive loads.
4	Capability to withstand high power dissipation and effectively manage thermal stress under worst-case conditions.
5	Maximizing output voltage swing headroom relative to programmable power supply voltage rails.
6	Inclusion of output overvoltage and overcurrent protection features: overload, short-circuit, and current limiting.

Line items 1 through 3 in Table 2-1 regarding the current booster are addressed in Sections 2 and 3 of the article.

2.1 Open-Loop Output Impedance

In this design, the current booster is configured as a complementary push-pull Darlington topology with unity gain buffering. Figure 2-1 and Figure 2-2 demonstrate that the open-loop output impedance is regulated by a small bias voltage applied to the bases of the transistors. Forward biasing the base-emitter junction of the NPN transistor (T1) allows the booster to source positive voltage and current, while forward biasing the PNP transistor (T2) enables it to sink negative voltage and current. The bias voltage directly affects the open-loop output impedance; higher bias levels result in lower output impedance, as shown in Equation 1.

$$r_o \approx \frac{V_A}{I_C} \rightarrow Z_{CE} = \frac{r_{op} \times r_{on}}{r_{op} + r_{on}} \rightarrow Z_{CBO} = Z_{CE} \parallel R_L \quad (1)$$

Where,

- r_o represents the BJT's output impedance
- V_A refers to the Early voltage
- I_C denotes the bipolar collector current
- r_{op} represents the NPN's open-loop output impedance
- r_{on} represents the PNP's open-loop output impedance
- Z_{CE} represents the parallel output impedance of the complementary Darlington pair
- Z_{CBO} refers to the overall parallel open-loop output impedance

When the NPN transistor (T1) base-emitter junction is forward-biased, the current booster sources positive voltage and current at the output. Figure 2-1 illustrates the open-loop output impedance where the effects of $Z_{CE} \parallel R_L$ are shown to be less than 1Ω.

Conversely, when the emitter-base junction of the PNP transistor (T2) is forward-biased, the current booster sinks negative voltage and current at the output. Figure 2-2 demonstrates the open-loop output impedance, with the $Z_{CE} \parallel R_L$ effects yielding similar results. The combined open-loop output impedance remains consistent across the frequency range up to 1MHz.

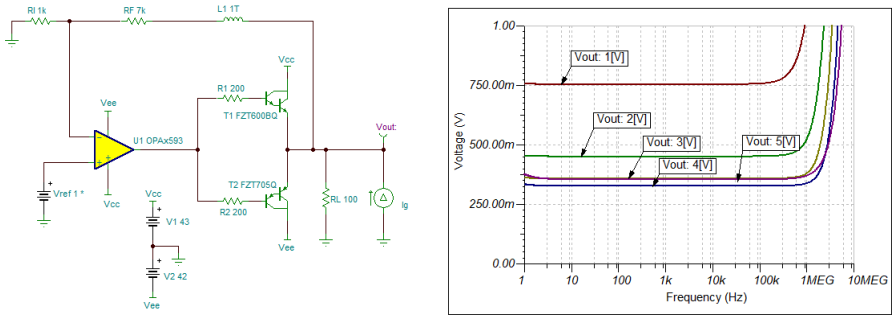

Figure 2-1. Open-Loop Output Impedance (Z_{CBO}) with T1 Forward Biased

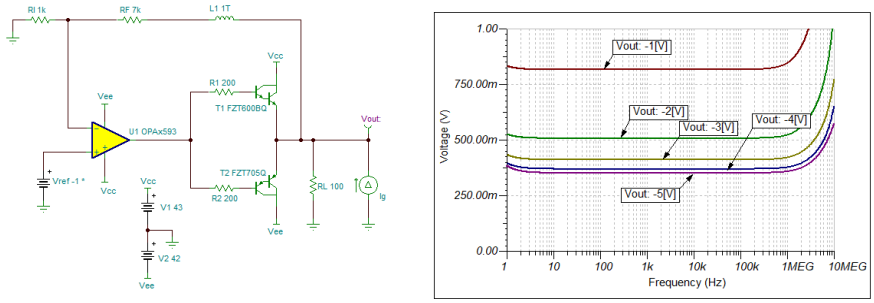

Figure 2-2. Open-Loop Output Impedance (Z_{CBO}) with T2 Forward Biased

The BJT transistor's forward biased voltage directly affects the open-loop output impedance; higher bias voltages lead to lower output impedance. The open-loop output impedance of the push-pull complementary BJT driver is primarily influenced by the output resistances (r_o) of the NPN (r_{op}) and PNP (r_{on}) transistors, as well as the load resistance (R_L). The open-loop output impedance of the Darlington current booster operates in parallel with R_L, as illustrated in Equation 1.

3 Various Current Booster Configurations

Various current booster pairs are designed for this application, with "C" indicating complementary pairs in which power transistors must be matched for ATE applications. Options include discrete CMOSFET, CBJT, or CIGBT, as well as integrated open-loop buffers (for example, BUF634A, LME49600) and power amplifiers utilized as unity gain buffers (for example, OPA593, OPA544). Table 3-1 compares the advantages and disadvantages of CMOSFET and CBJT current boosters, emphasizing key trade-offs and differences. Choosing the correct current booster requires understanding these variations and the implications for performance and cost.

3.1 Complementary MOSFET versus BJT Current Booster Comparisons

Table 3-1 compares the pros and cons of CMOSFET and CBJT current drivers, which are two of the most popular and cost-effective options. Although detailed comparisons are not provided in this section, note that there are significant differences and trade-offs that need to be considered when selecting current boosters for a specific application.

Table 3-1. Pros and Cons Comparisons Between CMOSFET and CBJT in Current Booster Applications

No.	Complementary MOSFET (CMOSFET) Output Stage	Complementary BJT (CBJT) Output Stage
1	Faster switching on and off speeds, possible in MHz, wider BW	Slower switching speeds, possible in the 100s kHz range, lower BW
2	High input impedance, lower standby power dissipation	Low input impedance, higher standby power dissipation
3	Slightly higher intrinsic output impedance, if normalized in theory	Lower intrinsic output impedance in theory
4	V_{DS} interface exhibits PTC over temperature	I_{CE} interface exhibits NTC over temperature
5	Less prone to classical second breakdown, requires device protections	Comparable to MOSFET devices, require device protections
6	Lower transconductance, g_m- Lower voltage gain per stage	Higher transconductance, g_m- higher voltage gain per stage
7	Better power dissipation, better thermal stability and performance, simpler thermal management	Higher power dissipation, prone to thermal runaway, requires more thermal management circuitry

Table 3-1. Pros and Cons Comparisons Between CMOSFET and CBJT in Current Booster Applications (continued)

No.	Complementary MOSFET (CMOSFET) Output Stage	Complementary BJT (CBJT) Output Stage
8	Requires a higher V_{GS} threshold voltage to turn on	Lower V_{BE} voltage, requires approximately 0.65V forward biased voltage to turn on
9	As V_{GS} increases, the conductivity of drain-source increases	As I_{BE} increases, the conductivity of collector-emitter increases
10	Designed for wider voltage and high current power applications	Designed for high current gain applications
11	Operates in the triode or linear region; voltage-controlled current-source	Operates in the active region; current-controlled current-source
12	Slightly higher costs than BJT devices	Generally lower costs than MOSFET devices
13	pA to nA DC input bias current at the gate	µA to mA DC input bias current at the base
14	Lower current density per unit area	Higher current density per unit area
15	Better for high power linear regulator, and higher headroom	Better linearity, simpler to control, and lower headroom

4 Stabilizing a Design for Power Amplifier Driving 1µF Capacitive Load (C_L)

To effectively understand dual feedback compensation (DFC) techniques and make sure of loop stability, recognize the interactions between resistive and capacitive loads, as well as the open-loop output impedance of the power amplifier. Proper management of the placement of poles and zeros within a feedback system is vital for achieving stability and performance.

Using a power amplifier (PA) Spice model, such as the one provided by the Tina simulator, can streamline the analysis and enhance comprehension of the DFC approach. This model mimics the performance characteristics of the OPA593 with the current booster composite amplifier, offering a clear framework for understanding the DFC technique. The emulated Spice model emphasizes the key interactions among compensated components, including the output resistive load (R_L), capacitive load (C_L), feedback resistors (R_F, R_I), and the op-amp's open-loop output impedance (Z_o), as shown in Figure 4-1.

Table 4-1summarizes the op-amp behaviors of the emulated Spice model for the OPA593 + current booster composite amplifier. Table 4-2 outlines the design requirements for the power amplifier, which is intended to drive 1µF capacitive and resistive loads with an output current rated up to ±1A_{dc}.

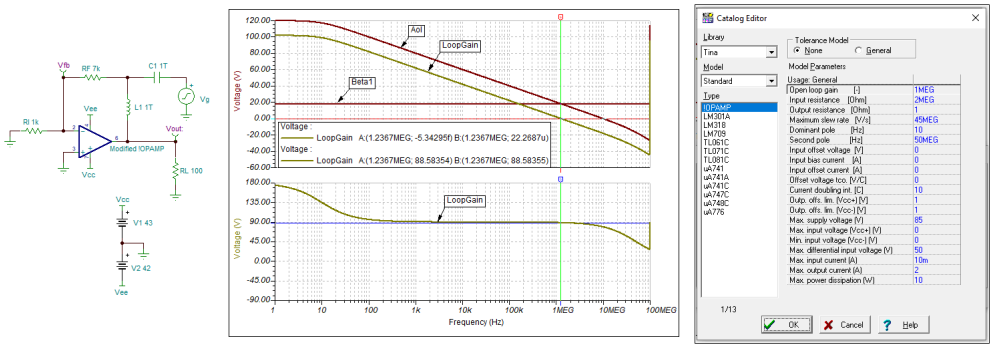

Figure 4-1. Emulated Power Amp Drives a Resistive Load - Open-Loop AC Stability Analysis

Table 4-1. Key Parameters of the Emulated Power Amplifier

Design Parameters	Modified PA Specification
Open-loop gain	1 × 10^6V/V or 120dB
Dominated pole	10Hz
Open-loop output impedance	1Ω
Maximum output current	2A
Power amplifier's second poles	50MHz

4.1 Op-Amp Driving Resistive Load

In the simulator, an ideal power amplifier is modified to demonstrate the DFC compensation technique. Table 4-1 summarizes the key parameters of this modified power amplifier (PA). The simulation results in Figure 4-1 validate the model's behavior and confirm its consistency with the SPICE model. The unity gain bandwidth calculated from the gain bandwidth product (GBP) is approximately 1.2MHz, while the phase margin is approximately 88.6°.

Table 4-2. Emulated PA Design Requirements for Driving 1µF Capacitive Load

Design Parameters	Design Specification
ATE design requirements	High accuracy, programmable voltage regulators
Input voltage range	Input swing up to ±5V_{dc}
Output voltage range	Output swing up to ±40V_{dc}
Output current range	Driving current up to ±1A_{dc}
Output resistive load	$R_L \geq 40\Omega$
Closed-loop gains	8V/V
Output impedance	Low open-loop output impedance, Z_o = 1Ω across all frequencies

Table 4-2. Emulated PA Design Requirements for Driving 1µF Capacitive Load (continued)

Design Parameters	Design Specification
Output capacitive load	Low ESR (20mΩ), 1µF ceramic capacitive load and DUT
Effective bandwidth	Approximately 50kHz, cutoff frequency at the –3dB point
Step time behavior	Output rising-and-falling edge step-time response <100µs
Power regulation	Output voltage accuracy: approximately 0.05% or better at full scale

4.2 Op-Amp Driving Capacitive Load and Challenges

In automated test equipment (ATE) applications, the output stage of a power amplifier frequently interfaces with substantial capacitive loads. Driving large capacitive loads (for example, 1µF) presents challenges due to an additional pole introduced within the op-amp's unity-gain bandwidth (UGBW). This extra pole (f_{p2}), described in Equation 2 can destabilize the op-amp's loop gain and reduce the phase margin in the closed loop within the UGBW.

No op-amp can drive large capacitive loads while making sure of stability without appropriate feedback loop compensation. The term "large capacitive load" is relative and varies based on several factors, including the op-amp's open-loop output impedance, load resistance, load capacitance, and unity-gain bandwidth (f_{unity}). Typically, op-amps can drive capacitive loads ranging from 10pF to 100pF without requiring external compensation. Op-amps with low open-loop output impedance can drive higher capacitive loads, up to 1nF, while still maintaining adequate phase margin without additional compensation. However, capacitive loads exceeding 1nF are generally considered "large" and can lead to issues such as oscillation, making compensation essential for preserving loop stability.

$$f_{p2} = \frac{1}{2\pi(Z_O \parallel R_L)C_L} \quad (2)$$

While some op-amps can drive capacitive loads up to 1nF, others can become unstable. This distinction depends on the op-amp's open-loop output impedance, the interaction with the capacitive load (C_L), and the location of the extra pole (f_{p2}) relative to unity-gain bandwidth (UGBW). These factors collectively determine an op-amp's ability to drive capacitive loads effectively. Table 4-3 summarizes the stability of an op-amp when driving capacitive loads under various scenarios.

Table 4-3. Op-Amp Closed-Loop Behaviors Related to an Additional Pole (f_{p2}) and UGBW

Op-Amp Closed-Loop Stability Assessment		C_L Load Example
Stable	f_{p2} is more than 2 octaves beyond the UGBW of the op-amp	10pF to 100pF load (typical)
Unstable	f_{p2} is within the UGBW of the op-amp, leading to instability	Large capacitive load (C_L> 1nF)
Unity Gain Unstable	f_{p2} coincides exactly with the UGBW	f_{p2} = UGBW
Conditionally Stable	f_{p2} is within 1 octave beyond the UGBW	Uncertain stability behaviors

In summary, the stability of an op-amp driving capacitive loads is influenced by the relationship between the second pole (f_{p2}) and the UGBW. If f_{p2} is far beyond the UGBW, the system remains stable. However, if f_{p2} is within or near the UGBW, the op-amp can become unstable or conditionally stable.

The phase margin, obtained from open-loop AC analysis, is a quantitative measure to evaluate the stability of an op-amp in a closed-loop feedback configuration. Phase margin predicts whether the system can remain stable, oscillate, or exhibit uncertain behavior, especially when driving capacitive loads. A phase margin of at least 45° is generally required to make sure of stable operation according to open-loop AC stability analysis.

4.3 Open-Loop AC Stability Analysis - Compensating C_L Effects Using DFC

How to adequately compensate capacitive loads in op-amps is well documented in the *Precision Lab Series: Op Amps*. This video series provides an overview of theories, simulations, examples and application notes.

One technique covered is the Dual Feedback Compensation (DFC) method, commonly used to compensate for complex loads in op-amps. However, detailed information on this technique is limited, particularly concerning current booster configurations like the OPA593 combined with a current booster driver.

The DFC technique mitigates the effects of capacitive loads, as demonstrated in Figure 4-2. This method involves placing an isolation resistor in series with the op-amp's output or within the feedback path. The combination of the op-amp's output impedance (Z_o + R_{iso}) with the capacitive load (C_L) introduces an additional pole (f_{p2}), derived from Equation 4.

To estimate R_{iso}, use the provided equation and select the nearest standard resistor value. In this example, the gain bandwidth product is defined at 10MHz, with a gain of 8V/V. The op-amp's closed-loop dominant pole (f_{dom}, 10MHz/8) is calculated to be 1.25MHz. The emulated op-amp's open-loop output impedance, Z_o, is modeled at 1Ω across all frequencies, and R_{iso} is determined to be 356.8mΩ, approximately 357mΩ, as calculated from Equation 3.

$$R_{iso} \approx \sqrt{\frac{Z_o}{2\pi C_L f_{dom}}} \quad \left(\text{if } C_L > 10nF\right) \tag{3}$$

The open-loop AC loop analysis focuses on determining the UGBW, loop gain, phase margins and other small signal stability parameters, as shown in Figure 4-2. Next, the compensated op-amp configuration is simulated to verify the circuit's closed-loop stability. This verification is achieved by applying a small step transient signal at the op-amp input during closed-loop operation. Making sure of the stability of an op-amp driving a complex load requires at least two simulation steps. The loop-stability iteration process optimizes the compensation between open-loop AC characteristics and closed-loop feedback responses. Without the proper step sequence, the op-amp's closed-loop behavior is undetermined, and output oscillatory behavior can manifest, as the uncompensated op-amp demonstrated in Figure 4-3.

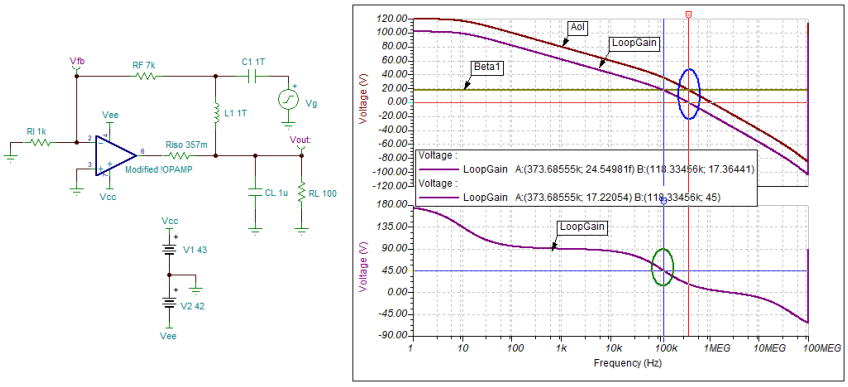

Figure 4-2. Open-Loop AC Analysis of an Uncompensated Op-amp With R_{iso}

$$f_{p2} = \frac{1}{2\pi((Z_o + R_{iso}) \parallel R_L)C_L} \approx \frac{1}{2\pi(Z_o \parallel R_L)C_L} \quad \left(\text{if } R_{iso} \ll Z_o\right) \tag{4}$$

When an op-amp feedback system drives a capacitive load, understanding the interaction between the open-loop output impedance and the load capacitance is crucial. The emulated power amplifier's open-loop output impedance, Z_o, is defined at 1Ω across all frequencies.

When driving 1µF capacitive load, a newly generated pole is calculated to be approximately 118kHz, as presented in Equation 4. Without the capacitive load, the unity gain bandwidth, f_{unity}, was simulated at 1.25MHz with a phase margin of 88.6°, as shown in Figure 4-1. Introducing the capacitive load causes f_{unity} to decrease, reducing the op-amp's roll-off slope from -20dB/decade to -40dB/decade, and the UGBW from 1.25MHz to approximately 374kHz. This additional pole reduces the phase margin from 88.6° to 17.4°, limiting the overall bandwidth of the system.

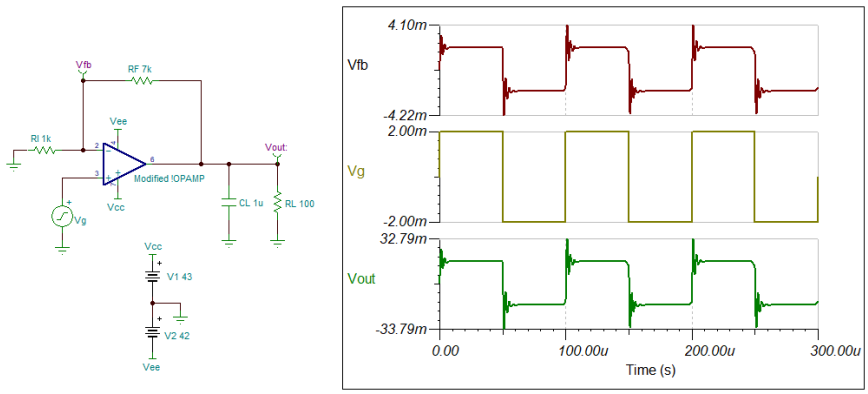

Figure 4-3. Uncompensated Op-Amp Driving 1µF Load - Unstable

To stabilize the feedback loop in Figure 4-2, set the additional f_{p2} pole frequency approximately 1 to 2 octaves lower than the simulated 374kHz. With the effective bandwidth defined at 50kHz in Table 4-2, we assign this value to f_{DFC_BW} and calculate C_F using Equation 5, estimating the result to be approximately 455pF. A standard capacitor value of 420pF is selected, as shown in Figure 4-4.

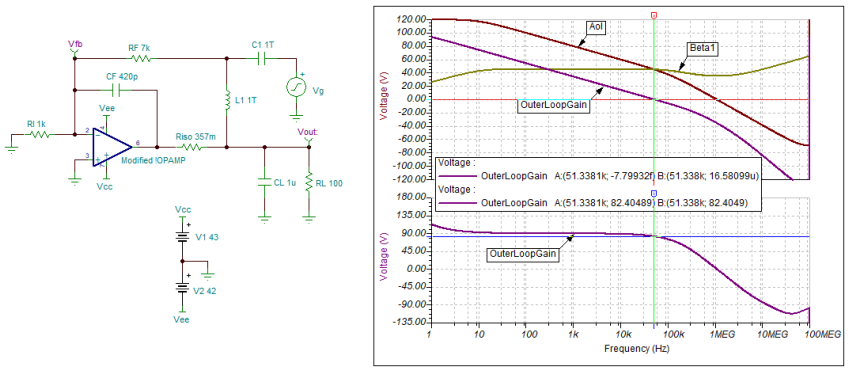

Figure 4-4. Outer Feedback Loop Compensation Bode Plot Driving (Z_o + R_{iso})‖R_L *and* C_L

The effective bandwidth of the DFC technique refers to the frequency range in which the op-amp achieves the desired gains and performance. In a dual feedback compensation topology, the op-amp bandwidth is not determined by the gain bandwidth product (GBP); instead, the effective bandwidth is primarily influenced by external compensation components, such as R_{iso}, R_F and C_F, as illustrated in Figure 4-5 and described in Equation 5. The compensation of the outer pole in the feedback loop, represented as approximately $1/sR_FC_F$, defines the effective bandwidth (f_{DFC_BW}) of the DFC configuration.

$$f_{DFC\_BW} = \frac{1}{2\pi(R_F + R_{iso})C_F} \approx \frac{1}{2\pi R_F \times C_F} \text{ (if } R_{iso} \ll R_F\text{)} \quad (5)$$

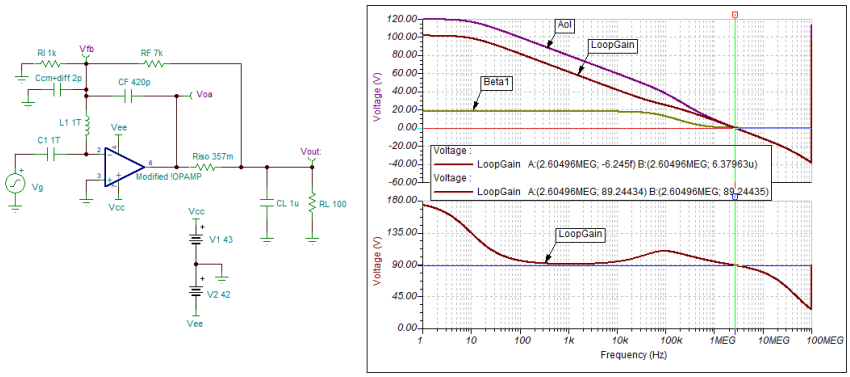

Figure 4-5. DFC Overall Open-Loop AC Analysis: 2.6MHz UGBW and Phase Margin 89°

4.4 Closed-Loop Stability Response - Small Signal Step Transient Analysis

The small-signal step transient simulation plot confirms that the DFC is stable in the closed loop, as shown in Figure 4-6. There is no output overshoot, and the design meets the timing requirements outlined in Table 4-2.

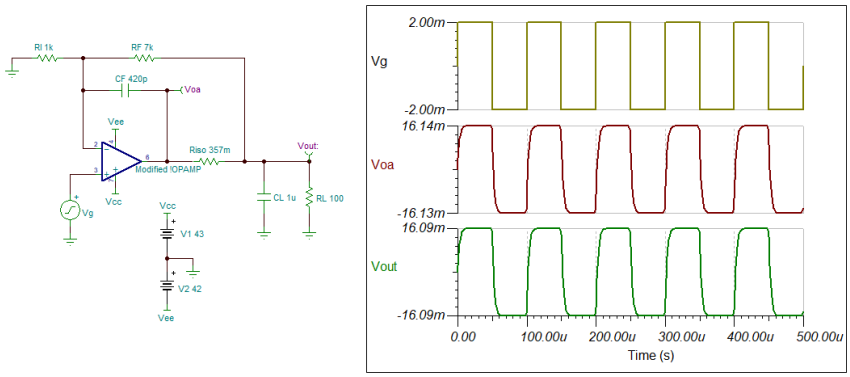

Figure 4-6. The Compensated Closed-Loop Response: Step Transient Analysis in Driving 1µF Load

The final validation step in the simulation involves a frequency sweep of the OPA593 with the current booster and analyzing the gain responses, as shown in Figure 4-7. If the AC gains increase with frequency near the -3dB point, it typically suggests that two poles are too closely spaced or overlapped. This phenomenon is discussed in the next section.

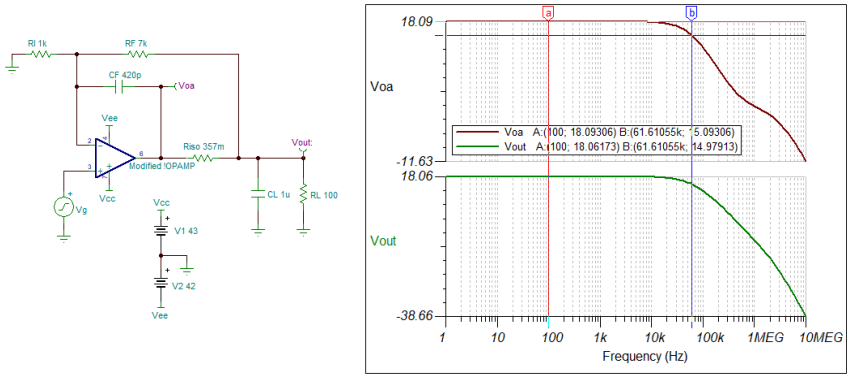

Figure 4-7. AC Frequency Sweep of the Emulated PA Driving 1µF Load

4.5 Effects of R_{iso} on Frequency Response in Dual Feedback Compensation

The DFC technique for compensating capacitive loads is complex. One challenge in optimizing DFC is that the effective bandwidth often exhibits gain peaking or Q effects in the AC frequency response. Gain peaking or a high Q factor indicates that more than one pole is present within the UGBW, a phenomenon characteristic of the DFC method, as illustrated in Figure 4-8. Gain peaking occurs when poles are closely spaced or overlapped within the closed feedback loop, resulting in resonant responses that elevate gains. This effect is observable only when the feedback loop is closed, whether in the time or frequency domain.

In the op-amp compensated for 1µF capacitive load, as depicted in Figure 4-8, the resistance R_{iso} values are progressively increased from 100mΩ, 500mΩ, 1Ω, and 5Ω. The selection of R_{iso} is relative to the op-amp's open-loop output impedance, defined at 1Ω across all frequencies in the emulated Spice model. As R_{iso} increases, the additional pole f_{p2} shifts toward lower frequencies, as described by Equation 4. This pole shift contributes to gain peaking in the frequency response when the newly emerged pole moves closer to the dominant pole, f_{DFC_BW} defined in the DFC loop. Gain peaking occurs when these two poles overlap or come too close together, as shown in Figure 4-8.

To optimize the value of R_{iso} in the DFC technique and eliminate guesswork, Equation 3 is used to calculate R_{iso}, based on the following *Determine Optimal Isolation Resistance for Driving Capacitive Load*, application note. The R_{iso} value must be significantly lower than both Zo and R_F parameters. A larger R_{iso} value can adversely affect the gain peaking or quality factor (Q) of the compensation loop, potentially altering the circuit's stability and effective bandwidth.

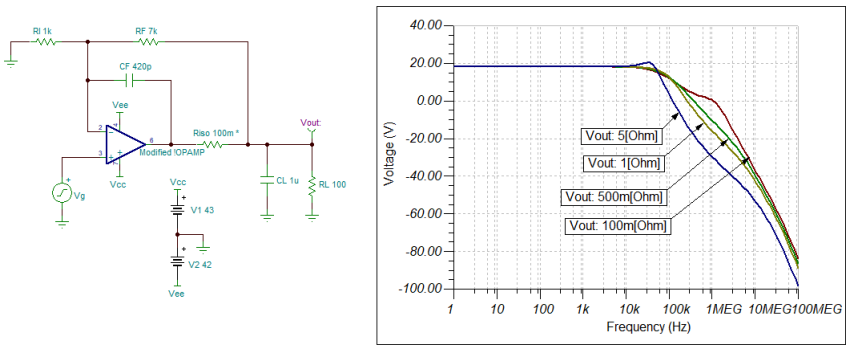

Figure 4-8. Effect of R_{iso} of the Compensated Op-Amp Driving 1µF Capacitive Load

4.6 Summary of the DFC Technique

The DFC technique utilizes two distinct feedback paths to improve overall loop stability: a low-frequency feedback path and a high-frequency feedback path, as shown in Figure 1-1. The low-frequency feedback path serves as the outer feedback loop, establishing nominal gains and bandwidth based on the op-amp's dominant pole, defined by f_{DFC_BW} in Equation 5.

Conversely, the high-frequency feedback path serves as the inner feedback loop, operating at a higher bandwidth than the outer loop. These dual feedback loops interact, where the UGBW of the inner feedback loop resembles a pole in relation to the UGBW of the outer loop. This interaction affects both bandwidth and phase levels, impacting the overall stability of the system.

The DFC procedures are summarized in Table 4-4, along with some of the simulated parameters used in the article.

Table 4-4. Summary: The DFC Procedures for Stabilizing Capacitive Load

Summary of Dual Feedback Compensation Technique	
a	Determine R_{iso} in Equation 3 for DFC compensation
b	Perform an open-loop AC stability analysis to assess gain and phase, as illustrated in Figure 4-4.This step identifies the UGBW and the adequate phase margin from the point of perturbation injection in the outer feedback loop.
c	After stabilizing the outer feedback loop, verify the inner feedback loop, which reflects the overall loop-gain of the compensation scheme, as shown in Figure 4-5. Both feedback loops must be stable to make sure of the stability of the capacitive loads.
d	Verify the closed-loop behavior of the compensated op-amp, as illustrated in Figure 4-6, by applying a small signal step transient to the input. This can provide essential insights into the system's performance, bandwidth, and stability in the time domain.
e	Perform an AC frequency sweep in the closed-loop configuration to validate the gain response across frequencies, as shown in Figure 4-7. The AC gain cannot exhibit any peaking in the frequency domain, and the effective bandwidth of the frequency sweep must align with the design requirements.
f	The loop stability iteration can be necessary for optimization, as loop stability balances open-loop AC stability analysis with closed-loop response in both the time and frequency domains. This makes sure that the simulated behaviors align with the stability and design criteria.
g	Finally, the overall performance can be validated through real-world applications by conducting bench testing.

- The feedback resistor R_F is chosen based on the requirement of ±40V_{dc} and ±10mA, resulting in a minimum resistance of 4kΩ, as 10mA is the input current at the OPA593's absolute maximum rating. For simulation, a 7kΩ resistor was used. However, in real-world ATE applications, an R_F value closer to 14kΩ is recommended to make sure of additional limiting current within the design margin.
- In the OPA593, asymmetric power supply rails of +43V_{dc} and -42V_{dc} are used. During simulation, the output voltage swing was ±2V below the supply rails. In practical applications, ±42.5V_{dc} needs to suffice to achieve an output of ±40.0V_{dc}. To reduce heat dissipation, it is crucial to minimize the voltage difference between the supply rails and the output.

5 Stabilizing the OPA593 and Darlington Current Booster for 1µF Capacitive Load

The design approach using the OPA593 with a Darlington current booster topology for driving 1µF capacitive load follows the dual feedback compensation (DFC) process designed for the emulated power amplifier, shown in Figure 4-5. A key difference is that the current booster effectively acts as the isolation resistor (R_{iso}) in the designed emulated PA example. While the OPA593 maintains an output impedance of approximately 228Ω from 1kHz to 1MHz, this is not designed for driving large capacitive loads using the compensation technique outlined in Table 4-4, where alternative DFC compensation techniques are more appropriate.

The design requirements for the OPA593 and the current booster configuration are detailed in Table 1-1 at the beginning of the article. Integrating the OPA593 with a Darlington current booster creates a composite amplifier with low open-loop output impedance. This composite amplifier benefits from the OPA593's performance attributes—such as high input voltage handling, high slew rate, current limiting, and Enable or Disable functionality. These features make the OPA593 capable of driving large capacitive loads and meeting high current demands in ATE applications, provided that the feedback network is properly compensated.

In the current booster configuration shown in Figure 5-1, simulations reveal that the unity gain bandwidth, f_{unity} of the OPA593 combined with the Darlington current booster remains consistent, with a measured f_{unity} of approximately 1.4MHz and a phase margin of 79°. When the gain bandwidth product is applied, the simulation results closely match those of the emulated power amplifier depicted in Figure 4-1. This suggests that the closed-loop of the composite amplifier needs to exhibit similar behaviors as the emulated power amplifier.

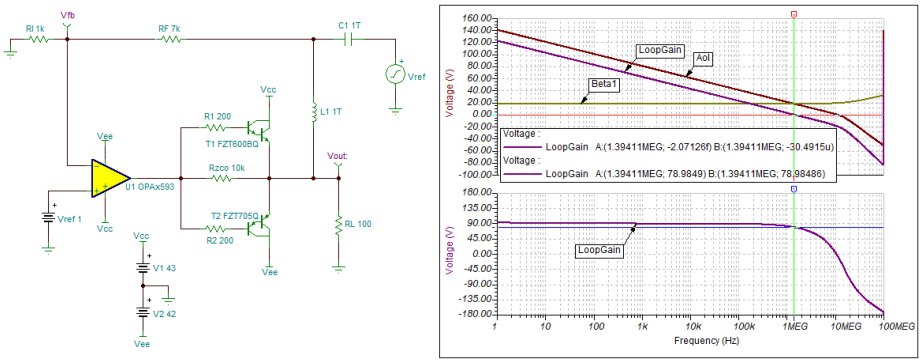

Figure 5-1. OPA593 + Current Booster Driving Resistive Load with V_{REF} = 1V_{dc}

5.1 Open-Loop AC Stability Analysis - Composite Op-Amp Driving 1µF C_L

When a capacitive load of C_L = 1µF is introduced at the output of the current booster stage, a second pole, f_{p2}, is estimated to occur at approximately 320kHz, as determined by Equation 4. This pole falls within the UGBW, measured at 549kHz, resulting in significant phase lag and reducing the phase margin from 79° to –19.4°, as illustrated in Figure 5-2. Consequently, the combination of the OPA593 and the current booster becomes unstable when driving 1µF capacitive load in the closed-loop configuration.

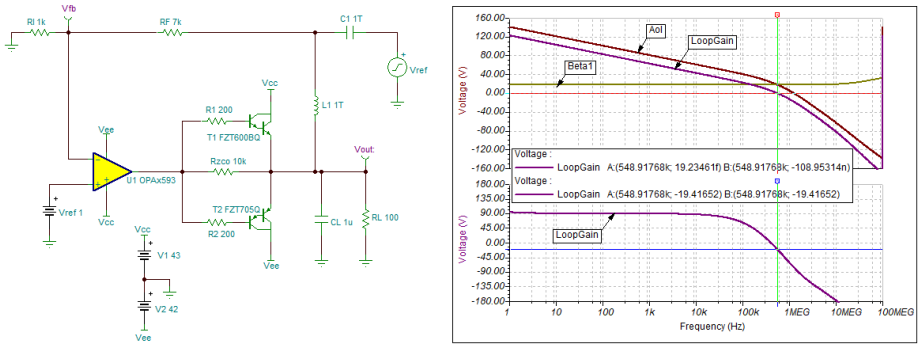

Figure 5-2. OPA593 + Current Booster's Outer Feedback Loop AC Analysis - Driving 1µF (C_L)‖100Ω (R_L)

To stabilize the outer feedback loop, it is crucial to account for the additional pole, f_{p2}, at approximately 320kHz, arising from the interaction between Z_{CBO} (~0.5Ω) and C_L. A common technique in DFC is to reduce the outer loop-gain by incorporating a compensation capacitor, C_F. This capacitor ensures that the outer loop's UGBW is at least 1-2 octaves below f_{p2}. A conservative guideline recommends setting the outer loop's UGBW two octaves below f_{p2}, translating to less than 100kHz, to maintain stability within the multiple feedback loop compensation scheme. While larger values of C_F can improve overall DFC stability, they also significantly limit the circuit's effective bandwidth, creating a trade-off that designers must carefully evaluate based on application requirements. Other DFC methods, primarily involving pole-zero cancellation, can also effectively address the pole that appears at the outer feedback loop's UGBW. However, detailed compensation procedures are beyond the scope of this application note.

According to the design requirements outlined in Table 1-1 and Equation 5, the target cutoff frequency, $f_{DFC\_CB\_BW}$, is defined at approximately 50kHz. To achieve this specification, the compensation capacitor, C_F is calculated to be around 455pF. The closest standard value, $C_F \approx$ 420pF, is then chosen. As shown in Figure 5-3, the simulated outer feedback loop's UGBW is measured at 50.8kHz, with a phase margin of approximately 76°, based on the open-loop AC analysis. Consequently, the outer feedback loop is expected to remain stable during closed-loop operation, as indicated by the perturbation injection analysis.

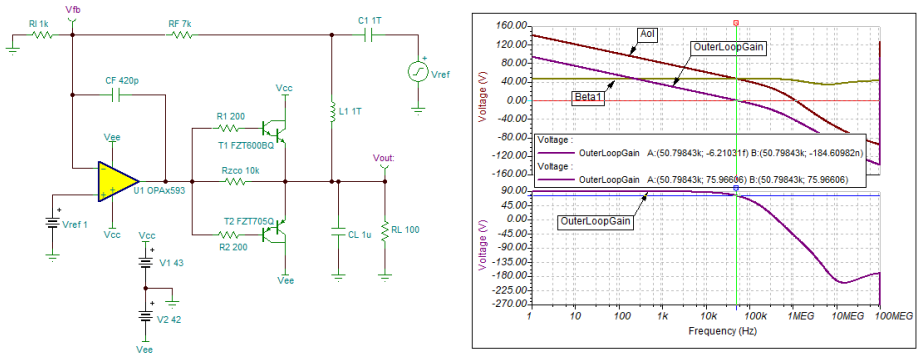

Figure 5-3. OPA593 + Current Booster Composite Amplifier's Outer Feedback Loop Stability

As mentioned in the Summary of Section 4, the DFC technique utilizes dual feedback loop compensation. In Figure 5-3, we examined the AC stability of the outer feedback loop. Now, we can analyze the inner feedback loop, which is responsible for high-frequency compensation. This inner loop is crucial for determining overall AC loop stability, and can be simplified as the Loop-Gain of the DFC technique. Figure 5-3 shows the AC loop gain stability analysis, and the compensation approach is detailed in the *Precision Lab Series: Op Amp.*

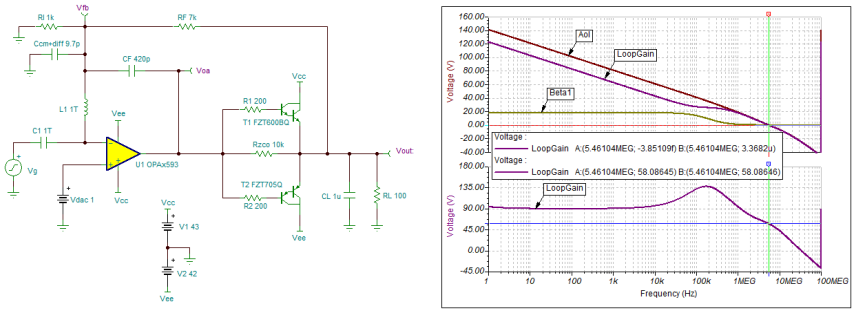

Figure 5-4. Open-loop AC Analysis in DFC shows a Phase Margin of 58° at the UGBW

From the AC stability analysis in Figure 5-4, the unity gain bandwidth of the loop gain is measured at 5.46MHz with a phase margin of approximately 58°, indicating that the overall DFC loop is stable.

5.2 Closed-Loop Stability Response - Composite Op-Amp's Step Transient Analysis

To assess the closed-loop behavior of the compensated OPA593 in the current booster configuration, a small signal step transient analysis was performed, as shown in Figure 5-5. The closed-loop transient response reveals no overshoot or oscillation, indicating a sufficient phase margin and effective compensation applied to the inner and outer feedback loops.

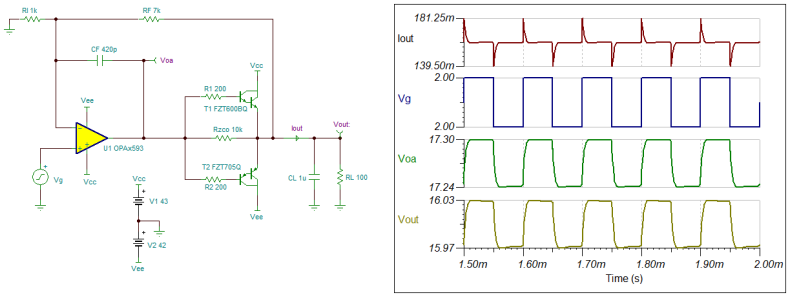

Figure 5-5. Compensated Composite Amplifier - Step Transient Response in Time Domain

Like the emulated power amplifier in Section 4, gain peaking or Q effects can be more pronounced in actual op-amp simulations. Each op-amp design contains numerous hidden poles and zeros. While these high frequency

poles and zeros typically do not interfere with single feedback loop compensation within the UGBW, the DFC compensation methods can be an exception, particularly when managing multiple feedback loops. Thus, it is crucial to examine the AC frequency response behavior, to verify sweep frequency response in ATE applications, as shown in Figure 5-6.

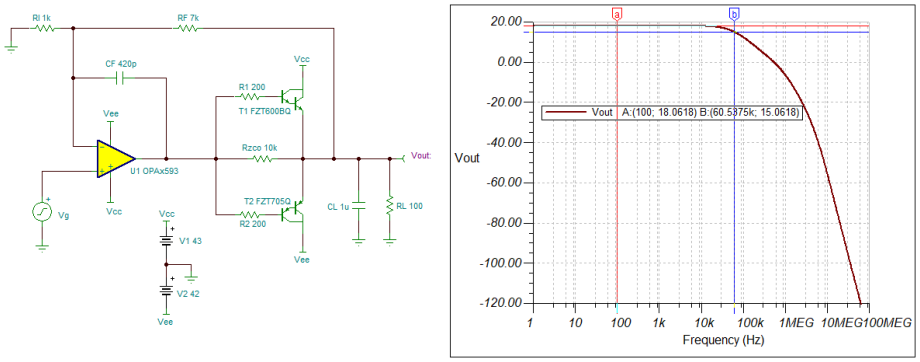

Figure 5-6. OPA593 and Current Booster's Effective Bandwidth: AC Sweep in Frequency Domain

6 Composite Amplifier's Effective BW and Step Time Response

Note the importance to clarify the concepts of op-amp bandwidth and step timing response in ATE applications, as engineers often confuse these terms.

An op-amp's effective bandwidth is derived from AC small-signal analysis in a linear model, which describes how quickly the amplifier can respond to small-signal changes at both the input and output while maintaining a relatively constant gain. This model defines the frequency range in which the amplifier can perform effectively in a specific closed-loop configuration. In a closed-loop feedback system, the op-amp bandwidth is a first-order approximation based on the gain-bandwidth product.

In contrast, an op-amp's step response or timing requirements are associated with the slew rate and the characteristics of the input signal, which are typically evaluated using the large-signal model. For ATE applications, step timing responses are generally very rapid, typically on the order of 10µs from applying the input signal to stabilizing the output setpoint, which are critical design parameters.

When output stages are loaded with capacitive or inductive components, longer time constants are introduced due to these load parameters. Merely increasing the op-amp bandwidth does not resolve the time delay or significantly enhance the step response.

To improve the step response time in ATE applications, output driving stages must provide a higher current rate over a short duration. For larger capacitive loads, achieving a fast output voltage setpoint requires rapid feedback control and a high rate of current change to drive the capacitive load, represented as $C(di/dt)$. In the OPA593 + current booster configuration, the large signal step response time is determined by the slew rate of the OPA593 and the rate of current change in the booster driver (for example, di/dt). Overall performance is also influenced by the compensated op-amp, output voltage swing, settling time, and transient overshoot or undershoot behaviors. Thus, a trade-off must be made between minimizing output current spikes and optimizing step response time in ATE applications.

8 Summary

This article explores the OPA593 in a current booster topology, using the DFC compensation technique to stabilize large capacitive loads in a voltage regulator configuration. The application note provides a comprehensive approach to compensating the power output stage and managing large capacitive loads in ATE applications. By implementing the DFC technique, the design makes sure loop stability for composite amplifiers, improves system bandwidth, and optimizes performance - critical factors for supporting high-current ATE systems.

9 References

- Texas Instruments, *OPA593 85-V, 250-mA Output Current, Precision, Power Op Amp,* data sheet.
- Texas Instruments, *Determine Optimal Isolation Resistance for Driving Capacitive Load*, application note.
- Texas Instruments, *Closed-Loop Analysis of Load-Induced Amplifier Stability Issues Using ZOUT,* application note.
- Texas Instruments, *Stability Analysis of Voltage-Feedback Op Amps*, application note.
- Texas Instruments, *OPA593 Evaluation Module*.
- Texas Instruments, *Precision Lab Series: Op Amps*. training video.
- Texas Instruments, *TINA-TI.*

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265