Application Report
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Spread Spectrum Clocking Using the CDCS502/503

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ABSTRACT

Spread Spectrum Clocking (SSC) is a common way to overcome EMI issues. This application report provides an overall view of the principles behind SSC. It also includes practical considerations about why, when, and how to use the CDCS502 and CDCS503 SSC clock generator. When SSC is included early in the design process, it can reduce the redesign cycle and drastically decrease the cost of new product development.

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1 Introduction to Spread Spectrum Clocking

Due to the periodicity of the digital clock signals, the energy concentrates in one particular frequency and also in its odds harmonics. These levels or energy is radiated and therefore this is where a potential EMI issue arises. Spread spectrum clocking (SSC) is a special way to reduce the radiated emissions of digital clock signals.

SSC is the variation of the frequency of a clock signal in a controlled way. In the frequency domain, the SSC reduces the peak amplitude of a digital clock signal by shifting the frequency. In other words, the energy of the clock is spread. In the time domain, the amplitude of the modulated clock has the same value as the nonmodulated clock. SSC reduces the peak values of the radiation and can help when EMI testing gives problems. Figure 1 shows the results for 0% (blue), ±0.5% (green), ±1%(cyan) and ±2% (red) SSC for the CDCS502. The reduction of the peak amplitude is approximately -8 dB when using ±2% SSC. This reduction in the amplitude is higher when looking at the harmonics, i.e., –13 dB for the seventh harmonic when ±2% SSC is used.

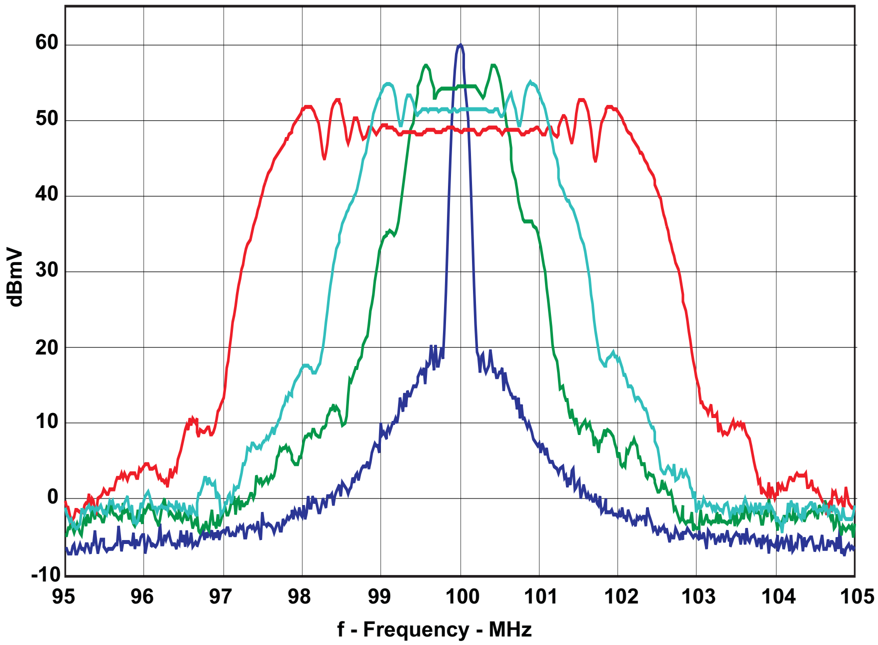

Figure 1. CDCS502 With a 25-MHz Crystal, FS = 1, Fout = 100 MHz, and 0%, ±0.5, ±1%, and ±2% SSC

The most important parameters of spread spectrum clocking are:

- Amount of SSC
- Center or down spread
- SSC profile
- Modulation frequency

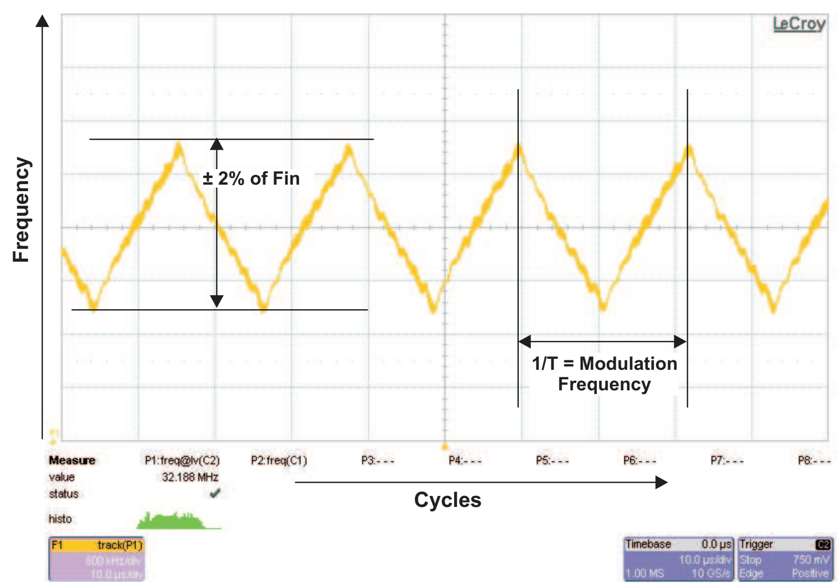

Figure 2. Time Domain of CDCS502 Cycles vs Output Frequency, Fin = Fout = 32 MHz

The amount of SSC finally selected has to meet two requirements.

- Pass EMI testing
- SSC device's jitter has to be within the jitter specifications of the system using the clock signal.

The SSC can be either centered around the output frequency or down spread. Normally, when it is specified using "±", it means that the SSC is centered. When only "–" is used, then it means that it is down spread. For example, if ±1% SSC is selected for a 32-MHz output frequency, it means that the output frequency oscillates between 32.32 MHz (32 MHz + 0.32 MHz) and 31.68 MHz (32 MHz – 0.32 MHz). This means that some clock cycles are above 32 MHz. This can be a problem if the system is already running at its maximum frequency. In this case, use only a down-spread SSC.

SSC profiles can be implemented in several ways. The most common way to design an SSC is using a triangular shape. This is because it is relatively easy to design compared with some more complicated ways, like for example, the Hershey shape (Figure 3). The CDCS502 and CDCS503 use triangular modulation as shown in Figure 2. Figure 3 shows different SSC shapes.

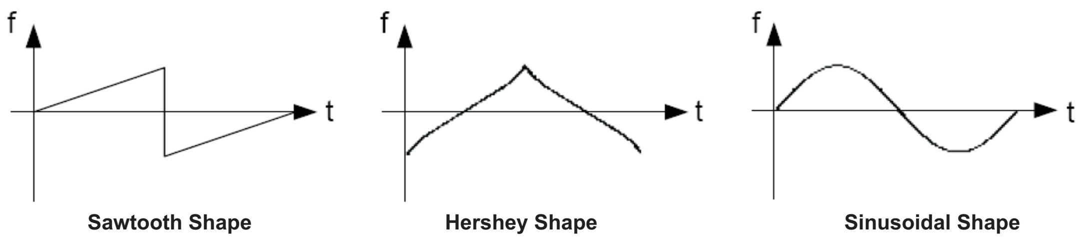

Figure 3. Different SSC Shapes

For the CDCS502 and CDCS503, the modulation frequency is a parameter that is a function of the input frequency. The device is normally designed to force the modulation frequency to be above 30 kHz and below 100 kHz in order to avoid interference in audio applications. Modulation frequency can be either constant or random. It causes the gaps when measuring SSC; this can be seen in the spectrum analyzer.

2 CDCS502/503 and SSC

The CDCS502 and CDCS503 have a triangular modulation profile, as can be seen in Figure 2. For both devices, SSC is centered; the amount of SSC can be configured using pins SSC_SEL0 and SSC_SEL1. Therefore, these two control pins have four SSC spread amount options, 0%, 0.5%, 1%, and 2%.

The modulation frequency (f_{mod}) of the CDCS502/503 depends on f_{IN}. It can be calculated using the following formulas. FS is the status of the Frequency Selection pin.

FS = 0: $f_{mod} = f_{IN} / 708$
FS = 1: $f_{mod} = f_{IN} / 620$

Table 1 and Table 2 show jitter values for the CDCS502 when using a 25-MHz crystal. Table 1 has FS set to LOW, and therefore the output frequency is 25 MHz. Table 2 results were obtained when setting FS to HIGH, and therefore the output is 100 MHz. The values are typical and measured over 10k cycles.

Table 1. CDCS502 Jitter With Fin = 25-MHz Crystal and Fout = 25 MHz

SSC Amount	Cycle-Cycle Jitter (ps)	Period pk-pk Jitter (ps)
0%	36	41
±0.5%	93	512
±1%	117	1001
±2%	195	1990

Table 2. CDCS502 Jitter With Fin = 25-MHz Crystal and Fout = 100 MHz

SSC Amount	Cycle-Cycle Jitter (ps)	Period pk-pk Jitter (ps)
0%	36	41
±0.5%	72	178
±1%	72	292
±2%	78	529

3 Can I Use the CDCS502/503 in My Application?

In order to know if the CDCS502/503 can be used in a given application, the jitter tolerance of the system must be known. For example, in several DSPs, peak-to-peak jitter tolerance is specified as a factor of the period. For example, the TMS320DM6467 Digital Media System-On-Chip specifies maximum period jitter as 0.02UI. Where UI is the period of the input clock. If the frequency is 27 MHz, then UI = 37.037 ns and therefore period jitter is 0.02 × 37.037 ns = 0.740 ns = 740 ps. This limit is within the limits of the CDCS502/503 for 0% and ±0.5% SSC.

Some other applications are only sensitive to cycle-to-cycle jitter. As can be seen in Table 1 and Table 2, this parameter does not increase in the same amount as the period jitter does.

4 Using the CDCS502

Figure 4 shows a typical schematic using the CDCS502. Note that resistors R1, R2, R3, and R4 footprints are available on a printed-circuit board in order to fine tune the amount of SSC when doing EMI testing. The final configuration depends on the jitter tolerance of the device connected to the CDCS502 and the EMI tests results.

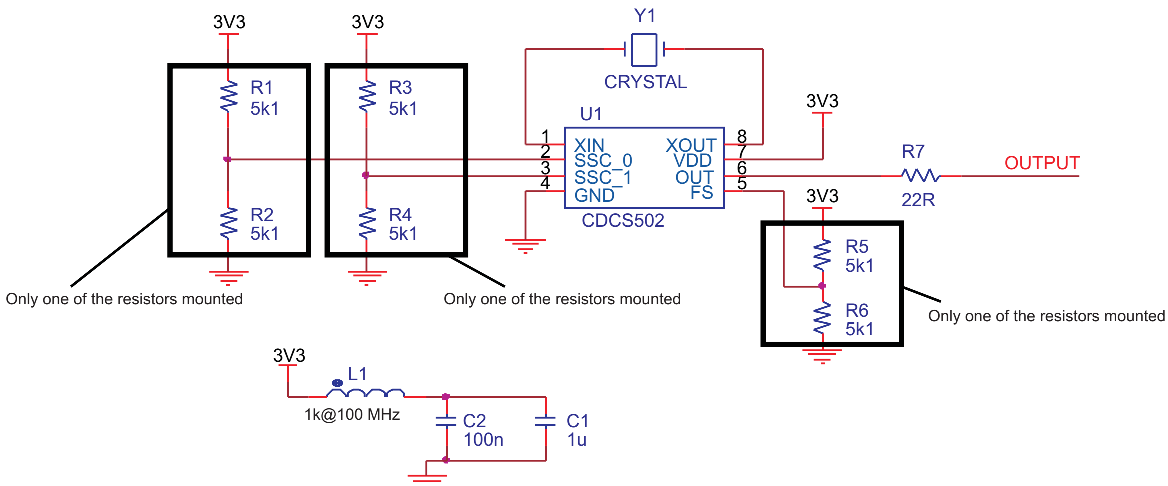

Figure 4. CDCS502 Schematic

Table 3 shows some example values for the schematic shown in Figure 4.

Table 3. Some Example Values for Schematic Shown in Figure 4

R1 or R2 Mounted?	R3 or R4 Mounted?	R5 or R6 Mounted?	Multiplication Factor	SSC
R1	R3	R5	X4	±2%
R1	R3	R5	X4	±2%
R2	R3	R6	X1	±0.5%
R2	R4	R6	X1	±0%

5 Using the CDCS503

Figure 5 shows a typical schematic using the CDCS503. Note that resistors R8, R9, R10, and R11 footprints are available in a printed-circuit board in order to fine tune the amount of SSC when doing EMI testing. The final configuration depends on the jitter tolerance of the device connected to the CDCS503 and the EMI tests results.

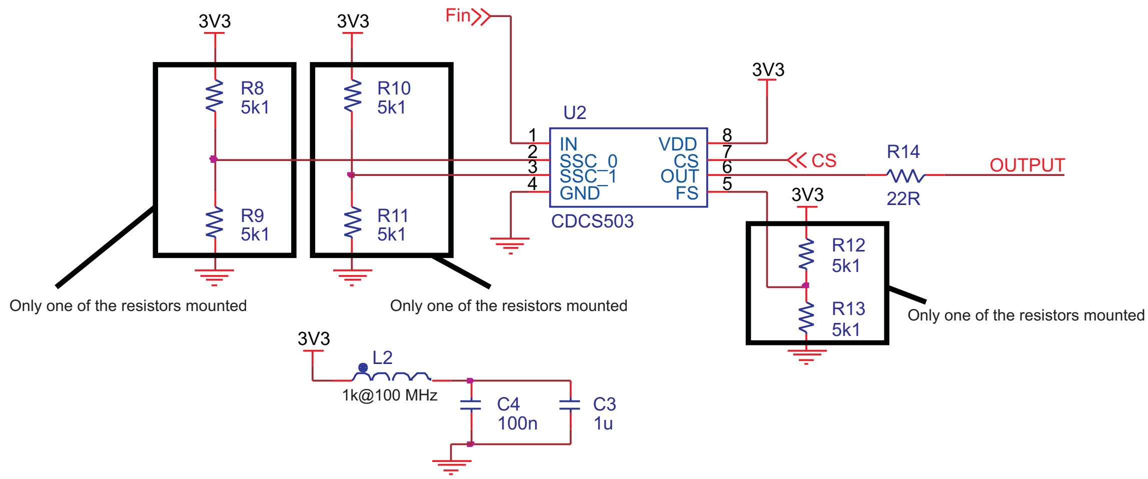

Figure 5. CDCS503 Schematic

6 Conclusions

Spread Spectrum Clocking is one of the most common technologies used for overcoming EMI issues. The CDCS502 and CDCS503 can help if used in an early stage of the design phase. The fine tuning of the SSC can be achieved using the control pins of these devices.

Additionally, the CDCS502/503 can work as a clock multiplier (x4) to generate a higher frequency, adding SSC when needed.

7 References

1. *CDCS502, Crystal Oscillator/Clock Generator With Optional SSC*, data sheet (SCAS868)
2. *CDCS503, Clock Buffer/Clock Multiplier With Optional SSC*, data sheet (SCAS872)