Application Report
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General I2C/EEPROM Usage for the CDCE(L)9xx Family

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ABSTRACT

The CDCE(L)9xx family is a family of programmable clock generators. The devices are designed with great flexibility to allow for customized clock solutions. To reach this flexibility the device utilizes two kinds of memory. These are volatile registers for direct access to all device functions as well as non-volatile EEPROM memory for storage and power up.

This note gives a quick overview on the memory organization and way the EEPROM and the registers are working together.

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1 Memory Organization

1.1 Registers

The content of the registers is used to directly influence the behavior of the device. They are the only part of the chip that can be directly accessed from the outside. For this the registers are programmable via an I2C interface.

The registers consist out of two main parts. These parts are the "generic configuration register" and the "PLLx configuration registers". According to the number of PLLs used in the device there are 1 to 4 PLL configuration registers.

This PLL configuration registers contain all the information important for the control a specific PLL as well as the according post dividers, multiplexers and outputs. They occupy the address rooms from 0xn0h to 0xnFh while n is the number of the PLL.

The generic control register contains the controls that are important for the general behavior of the chip independent of the PLL settings. It is located from the addresses 0x00h to 0x06h. Address room 0x07h to 0x0Fh is unused.

Table 1. Generic Control Registers

ADDRESS OFFSET	REGISTER DESCRIPTION
00h	Generic Configuration Register
10h	PLL1 Configuration Register
20h	PLL2 Configuration Register
30h	PLL3 Configuration Register
40h	PLL4 Configuration Register

1.1.1 General Behavior

Every byte written to the registers gets active after the last bit of this byte is written.

Several special bits take care of the behavior of the registers/EEPROM itself.

These bits are: "EE Lock" (byte0x01h bit5),
"EEPIP" (byte 0x01h bit 6) and
"EE Write" (byte 0x6h bit 0).

A detailed explanation of these bits can be found below.

There is no limit in the number of times the registers can be written or read.

1.2 EEPROM

The EEPROM is used to store the information from the registers.

It has no direct connection to the other parts of the device besides the registers. The intention of the EEPROM is to store device settings so they get not lost when the device is powered down. The information stored in the EEPROM is loaded back into the registers on power up.

This organization of the memory enables the device to configure itself in a application where no I2C bus is present. It also enables a quick loading of a standard configuration at power up.

The amount of write and read cycles to the EEPROM is typically greater then 1000.

An internal low frequency clock generator is used to transfer data to the EERPOM. This ensures that the EEPROM can be accessed also if no clock reference (crystal or LVCMOS input) is active.

2 Memory Handling

2.1 General

As already described above, the registers are the part of the memory system able to influence the behavior of the device. For this it is not necessary to write every instruction into the EEPROM. Just the configuration needed at power up should be stored there.

2.2 Special Bits for EEPROM Handling

2.2.1 EE Write Bit

As already mentioned the EEPROM is kind of a storage solution for the register states only.

It can be written too by setting the "EE Write" bit to "1". Just the rising edge of the EEWRITE-bit will trigger the EEPROM write cycle. During this cycle all information stored inside the registers will be transferred into the EEPROM. It is not possible to transmit single bits or bytes only.

The "EE Write" bit is controlling the internal EEPROM clock generator as well.

Note that this bit will not be set back automatically after the EEPROM write cycle is done, but has to be set back manually. Otherwise the EEPROM clock generator will continue running and can impact the performance. Also following EEPROM write cycles will fail due to the lack of a rising edge. Alternatively a power cycle will also reset this bit.

The device will not control I2C operations during the time the EEPROM is written. Because of this it is not recommended to make "write" cycle into the registers during this time. Doing so can result in wrongly set bits in the EEPROM.

Therefore the "EE Write" Bit should be the last bit written in a programming sequence. This is important for a block write operation since although this bit is the last bit in the General Purpose registers it is not the last byte in the whole registers. Depending on the device programmed there might be one to four PLL registers with higher addresses after the general purpose register. For this it might be beneficial to program the PLL settings first if the settings are intended to be stored in the EEPROM.

2.2.2 EE PIP Bit

The "EE PIP" bit contains the status of the EEPROM programming operation. A "1" will show that the EE write sequence is still ongoing while a "0" indicates that the EE write cycle is completed or that there is no EE write cycle ongoing. Although writing to the registers is not recommended during an EEPROM write cycle, read operations are permitted.

2.2.3 EE Lock Bit

The "EE Lock" bit is intended to protect the EEPROM against accidental altering. It will prevent the EEPROM to be written too.

This bit is only active if it is written to the EEPROM. Writing this bit will not disrupt the current EEPROM write cycle.

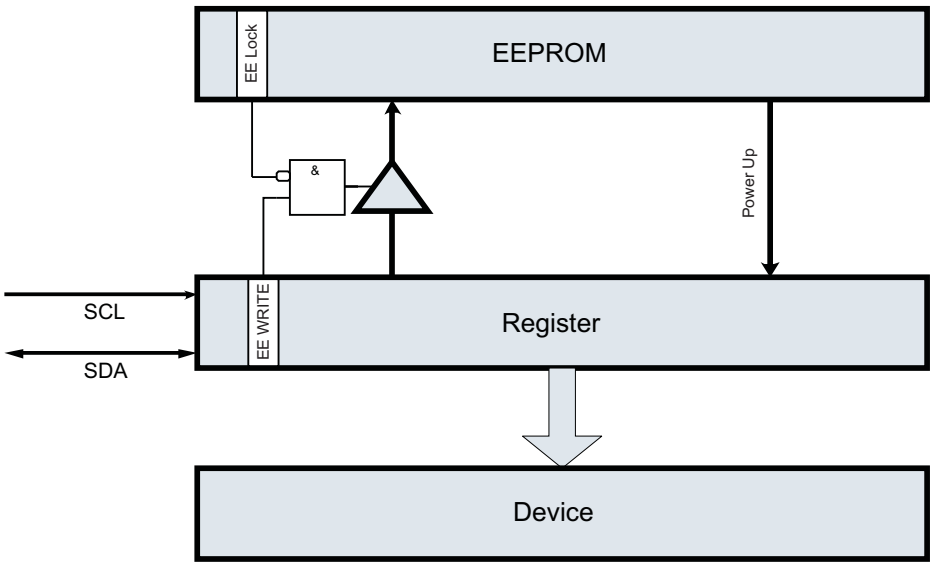

Figure 1. General Organization of the Memory in the CDCE9xx Device Family

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