Texas Instruments

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Product Bulletin

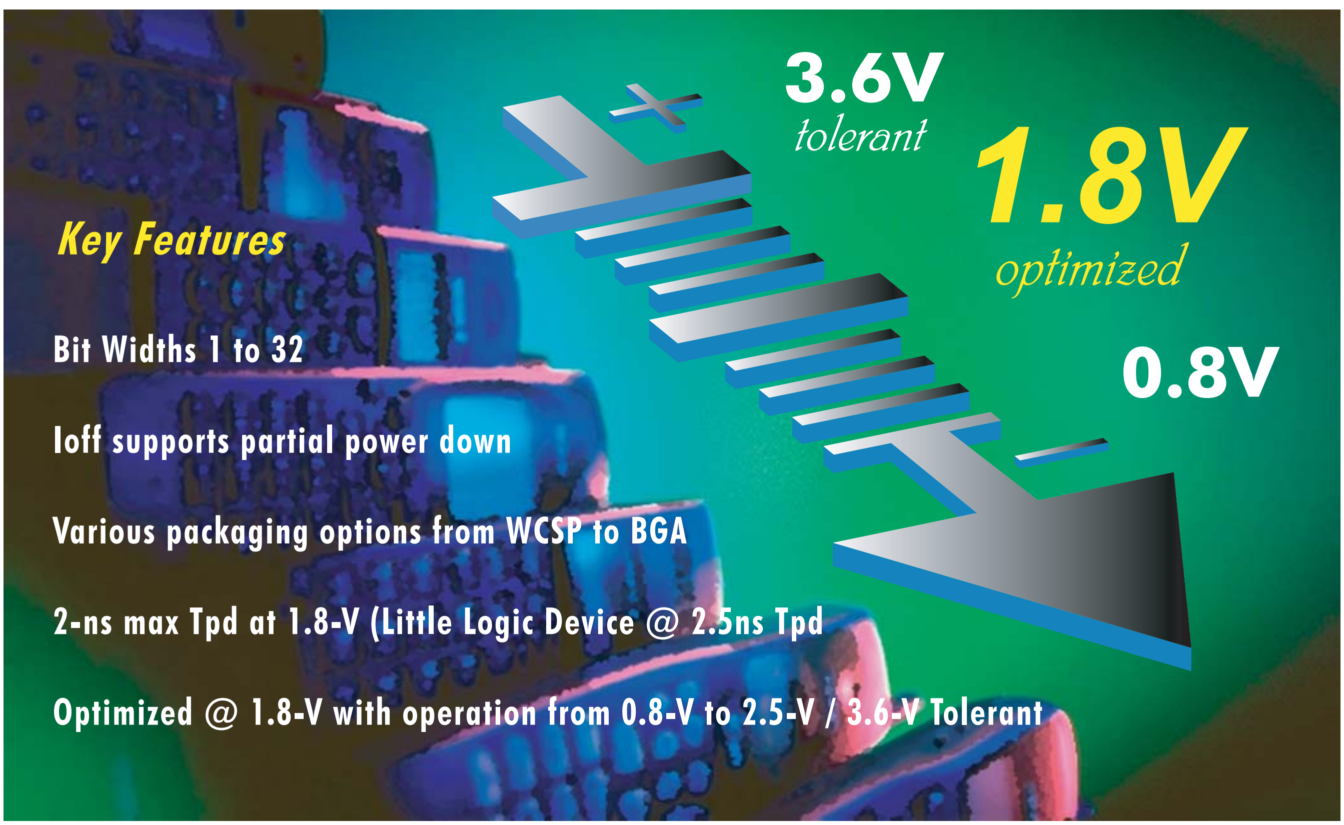
AUC

Advanced Ultra-Low-Voltage CMOS Logic

www.ti.com/sc/AUC

Introduction

AUC (Advanced Ultra-Low-Voltage CMOS Logic) is the industry's first logic family that is optimized for 1.8-V with operation from sub-1V (0.8-V) to 2.5-V and tolerant to 3.6-V. The family meets a variety of demands that have been placed on digital electronic designs, including the move to lower supply voltages, faster speeds, smaller form factors, and lower power consumption without compromising signal integrity. AUC was developed to meet such design parameters for advanced systems such as, telecommunications equipment, high-performance workstations, PCs and networking servers, and consumer electronics. As designers convert the core processors, ASICs, and memories of designs to lower voltages they need the supporting low-voltage logic functions, AUC provides this support.

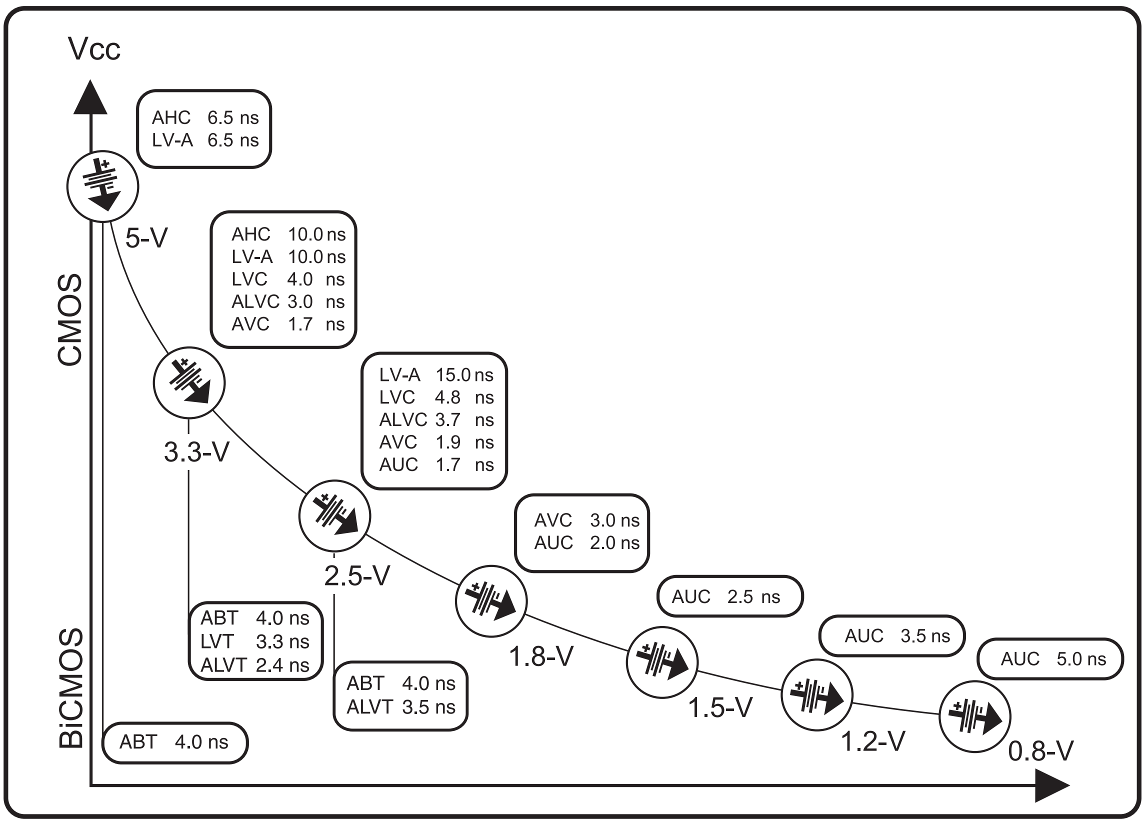


Supply Voltage

The need to move to lower operating voltages is a challenge that many designers are facing today. If working to extend battery life in a portable application or reduce heat dissipation in a constrained operation environment, Texas Instruments has a long-standing history of easing the migration to lower operating system voltages by offering the latest advanced CMOS logic families that meet the demand for such parameters.

Whether it's AHC at 5.0-V, LVC at 3.3-V, or AVC at 2.5-V, TI is committed to be the first to meet the requirement of lower operating voltages. AUC is another logic advancement as designers begin the transition from 5-V, 3.3-V, and 2.5-V systems specification to the next generation, 1.8-V, operating systems.

The AUC family supports mixed-voltage systems due to its operating voltage range of 0.8-V to 2.5-V; And with a voltage tolerance of 3.6-V, AUC is compatible with legacy devices, thus helping to extend the life of a system.



* 16245 Function

The Need for Speed

Another benefit of transitioning to lower system operating voltages is an increase in system needs. With a propagation delay of 2.0ns (max), AUC gives designers the logic component to meet the speed need. AUC has taken the place of AVC as the fastest logic family in its operating voltage range.

AUC

Vcc = 0.8-V	Vcc = 1.2-V	Vcc = 1.5-V	Vcc = 1.8-V	Vcc = 2.5-V	Unit
5 Typ	3.5 Max	2.5 Max	2.0 Max	1.7 Max	ns

AVC

Vcc = 0.8-V	Vcc = 1.2-V	Vcc = 1.5-V	Vcc = 1.8-V	Vcc = 2.5-V	Unit
N/A	3.9 Typ	4.0 Max	3.0 Max	1.9 Max	ns

*16245 Function

These extremely low propagation delays don't come with the signal integrity tradeoffs, that most designers have to make when seeking faster speeds.

Power Consumption

Digital electronics, especially portable and consumer electronics, are migrating to lower voltages in order to consume less power. The return is two-fold. One being that these electronics can make use of smaller battery sizes, thus reducing form factors, while getting the max life of the power supply between charges. The other is reduced heat dissipation in compact designs, such as 1U servers. This reduced heat dissipation simplifies heat removal and decreases the amount of package space needed, saving valuable board real estate in compact designs. AUC enables these low-power, high-performance designs; due in part to the fact that it was specifically designed for optimized operation at 1.8-V with operation to sub-1V levels.

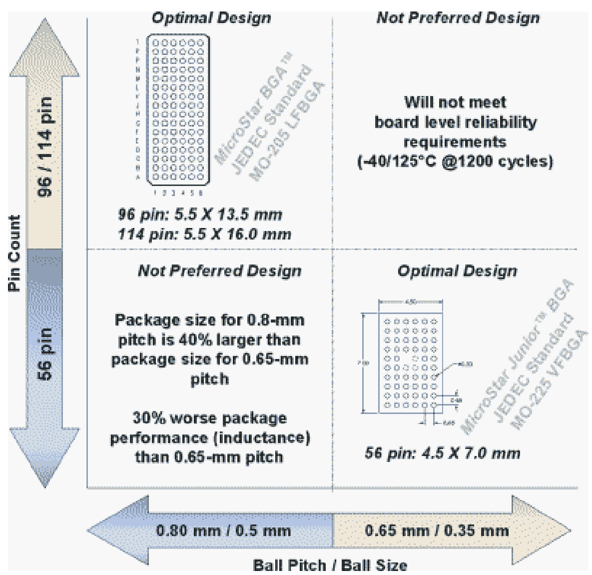
Size

As design form factors continue to shrink and complex board layouts are becoming densely populated, board real estate becomes a key issue. Designers should not have to worry about the footprint of a logic circuit. This is why TI has led the effort in the logic industry to shrink logic-packaging technology. This is shown in the latest Ball Grid Array (BGA) technology and advancements in Wafer Chip Scale Packaging (WCSP), By introducing our latest logic technology, AUC, in space saving packaging advancements, designers will be able to maximize their design resources. Bit Widths of 1 to 32 are provided in the AUC family.

Bit-widths	Little Logic	Gates	Octals	Widebus	Widebus+
Package	YEA	TVSOP	TVSOP	VFBGA	LFBGA
	DCK	TSSOP	TSSOP	TVSOP	
	DBV			TSSOP	
	DCT				
	DCU				

Ball Grid Array

Using TI's 96- and 114-ball MicroStar BGA™ packages, these LFBGA logic products allow increased signal bit width, reduced boards space, and enhanced thermal and electrical performance. The 0.8-mm ball pitch provides improved electrical and thermal characteristics and reduced inductance up to 45 percent compared to TSSOP packages.



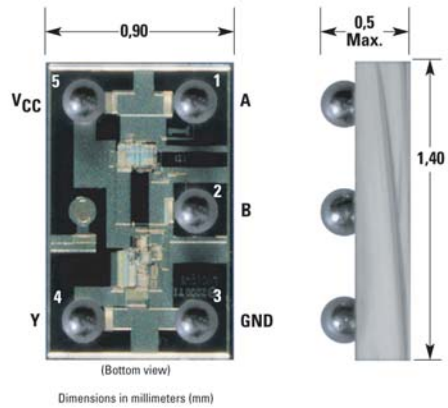
MicroStar Jr. ™

The MicroStar Jr.™, VFBGA package, with a very small 31.5 mm² footprint and a 1mm height, allows designers to reduce their board space in cell phones, personal digital assistance, base stations and networking systems. MicroStar Jr. ™ is 70 to 75 percent smaller than todays TSSOP (thin scale small outline package) logic package. With a ball pitch of 0.65mm, the MicroStar Jr. ™ offers a 30% performance (Inductance) improvement over 56-pin BGA with 0.8mm ball pitch. This is due to shorter wire length/internal traces. The 0.65mm pitch VFBGA offers a 40% space saving over the 0.8mm 56 pin BGA.

WCSP

Driven by applications requiring small circuit board mounting areas, wafer chip scale packaging (WCSP) utilizes the die as the actual package. TI offers both Lead Free WCSP, NanoFree ™ (Designated YZA) and Leaded versions (Designated YEA). With a footprint of 1.26mm, TI's NanoStar ™ is 75% smaller than SC-70 (DCK) and 13% smaller than any other logic package offering in the industry. Besides allowing manufacturers to place more functions in a tighter space WCSP aids in improving system performance with better thermal and electrical characteristics.

Initially, TI will release AUC single gates in the 5 bump WCSP package (YEA/YZA) with dual gates and triple gates being developed in both 8-bump and 6-bump WCSP packages.



Features

Ioff

The inputs and outputs of the AUC family have been designed with all of the reverse-current paths to Vcc blocked. This low Ioff current feature allows the device to remain electrically connected to an active bus during partial power down when Vcc = 0-V, or when the output is in a high performance state. The Ioff feature prevents damage to the device during partial power down.

Bus-Hold

The bus-hold feature holds the last known state of the input and eliminates the need for external resistors on unused or floating input pins. When Vcc = 3.3-V, bus-hold supplies a minimum of +/- 75uA holding current at 0.8-V and 2-V so it does not load down the driving output at valid logic levels. An "H" in the device name indicates bus-hold.

Device Listing

*** AUC Little Logic is alternate sourced by Philips Semiconductor.**
*** AUC WideBusTM, octals, and gates are alternate sourced by Philips and IDT.**

Little Logic Single Gates		
Device	**Description**	**Available**
AUC1G00	Single 2 input NAND Gate	NOW
AUC1G02	Single 2 input NOR Gate	NOW
AUC1G04	Single Inverter	NOW
AUC1GU04	Single Unbuffered Inverter	NOW
AUC1G06	Single Inverter Buffer/Driver with Open Drain Outputs	NOW
AUC1G07	Single Buffer/Driver with Open Drain Outputs	NOW
AUC1G08	Single 2 input AND Gate	NOW
AUC1G14	Single Inverter with Schmitt Trigger Input	NOW

Little Logic Single Gates		
Device	**Description**	**Available**
AUC1G17	Single Buffer with Schmitt Trigger Input	NOW
AUC1G32	Single 2 input OR Gate	NOW
AUC1G66	Single Bilateral Analog Switch	NOW
AUC1G79	Single D Type Flip Flop	Preview
AUC1G80	Single D Type Flip Flop	Preview
AUC1G86	Single 2 input XOR Gate	Preview
AUC1G125	Single Bus Buffer Gate with 3 State Outputs	NOW
AUC1G126	Single Bus Buffer Gate with 3 State Outputs	NOW
AUC1G240	Single Bus Buffer Gate with 3 State Outputs	NOW

Little Logic Dual Gates		
Device	**Description**	**Available**
AUC2G00	Dual 2-input NAND Gate	Preview
AUC2G02	Dual 2-input NOR Gate	Preview
AUC2G04	Dual Inverters	Preview
AUC2GU04	Dual Unbuffered Inverters	Preview
AUC2G06	Dual Inverter Buffer/Drivers with Open-Drain Outputs	Preview
AUC2G07	Dual Buffer/Driver with Open-Drain Outputs	Preview
AUC2G08	Dual 2-input AND Gate	Preview
AUC2G14	Dual Inverters with Schmitt Trigger Input	Preview
AUC2G17	Dual Buffers with Schmitt Trigger Input	Preview
AUC2G32	Dual 2-input OR Gate	Preview
AUC2G34	Dual Buffer Gate	Preview
AUC2G53	Dual Analog Multiplexer/Demultiplexer	Preview
AUC2G66	Dual Bilateral Analog Switch	Preview
AUC2G74	Single Positive Edge Triggered D Type Flip Flop w/ Clear & Preset	Preview
AUC2G86	Dual 2-input Exclusive-OR Gate	Preview
AUC2G125	Dual Bus Buffer Gate with 3-State Outputs	Preview
AUC2G157	Single 2 Line-to-1 Line Data Selector/Multiplexer	Preview
AUC2G241	Dual Buffer/Driver with 3-State Outputs	Preview

Little Logic Triple Gates		
Device	**Description**	**Available**
AUC3G04	Triple Inverter	Preview
AUC3G06	Triple Inverter Buffer/Driver w/ Open Drain Outputs	Preview
AUC3G07	Triple Buffer/Driver w/ Open Drain Outputs	Preview
AUC3G14	Triple Schmitt Trigger Inverter	Preview
AUC3G34	Triple Buffer Gate	Preview

WideBus™		
Device	**Description**	**Available**
AUC16240	16-Bit Buffer/Drivers with 3-State Outputs	Preview
AUC16244	16-Bit Buffer/Drivers with 3-State Outputs	Preview
AUC16245	16-Bit Bus Transceivers with 3-State Outputs	Preview
AUC16373	16-Bit Transparent D-Type Latches with 3-State Outputs	Preview
AUC16374	16-Bit Edge-Triggered D-Type Flip Flops with 3-State Outputs	Preview
AUCH16240	16-Bit Buffer/Drivers with 3-State Outpu	Preview
AUCH16244	16-Bit Buffer/Drivers with 3-State Outputs	Preview
AUCH16245	16-Bit Bus Transceivers with 3-State Outputs	Preview
AUCH16373	16-Bit Transparent D-Type Latches with 3-State Outputs	Preview
AUCH16374	16-Bit Edge-Triggered D-Type Flip Flops with 3-State Outputs	Preview

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Indonesia	001-801-10	-800-800-1450
Korea	001-800-8800-6800	-
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New Zealand	000-911	-800-800-1450
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