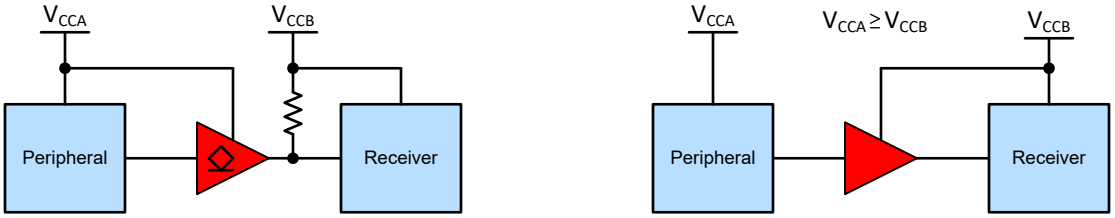
Product Overview

Separate Digital Voltage Nodes

Systems can have multiple digital voltages that are similar in value which need to be separated for optimal performance. For example, an incoming 3.3-V signal may need to communicate with an internally regulated 3.3-V device, and the two may vary separately from 3 V to 3.6 V. In this case, true isolation is not required, however separation of the voltage nodes will prevent issues from the voltage mismatch.



Left: block diagram for open-drain buffer. Right: block diagram for push-pull buffer.

Figure 1. Separate Voltage Nodes Block Diagrams

Design Considerations

- Input thresholds are referenced to the buffer's supply voltage
- Output voltage for open-drain devices can be selected by changing the pull-up resistor supply connection
- Output voltage for push-pull devices is equal to the buffer's supply voltage
- For traces longer than 12 cm (4760 mil) see *Drive Transmission Lines With Logic*
- *[FAQ] How does a slow or floating input affect a CMOS device?*
- *[FAQ] Where do I find maximum power dissipation for a device?*
- Ask a question on our *E2E™ forum*

Recommended Parts

Part Number	AEC-Q100	V_{CC} Range	Channels	Features
SN74LVC1G34		1.65 V – 5.5 V	1	Over-voltage tolerant inputs Partial power down (Ioff) Balanced high-drive CMOS outputs (up to 32 mA)
SN74LVC1G17-Q1	✓	1.65 V – 5.5 V	1	Schmitt-trigger input Over-voltage tolerant input Partial power down (Ioff)
SN74LVC1G07		1.65 V – 5.5 V	1	Open-drain output Over-voltage tolerant input and output Partial power down (Ioff)
SN74LVC1G07-Q1	✓			
SN74LV244A		2 V – 5.5 V	8	Over-voltage tolerant inputs Partial power down (Ioff) Balanced high-drive CMOS outputs (up to 16 mA)
SN74LV244A-Q1	✓			
SN74LVC16244A		1.65 V – 3.6 V	16	Over-voltage tolerant inputs Partial power down (Ioff) Balanced high-drive CMOS outputs (up to 24 mA)
SN74LVC16244A-Q1	✓			

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

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