Application Note

Generate Digital Patterns With TI Programmable Logic Device (TPLD)

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ABSTRACT

Whether it is to generate a test pattern or to initialize logic to a known state, the pattern generator (PGEN) macro-cell within TI Programmable Logic Devices (TPLD) can be configured to generate 1-bit to 16-bit patterns. This application note will discuss how to configure and utilize pattern generators within TPLD.

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Trademarks

1 Configuring the Pattern Generator in TPLD Using InterConnect Studio (ICS)

The pattern generator (PGEN) macro-cell, shown in Figure 1-1, within TPLDs can be configured to generate 1-bit to 16-bit patterns and the reset input polarity can be set to active-low or active-high. The pattern is continually clocked out from most significant bit (MSB) to least significant (LSB) on the rising edge of the CLK input as long as it is not in a reset state. While in the reset state, the output will default to the first bit of the specified pattern.

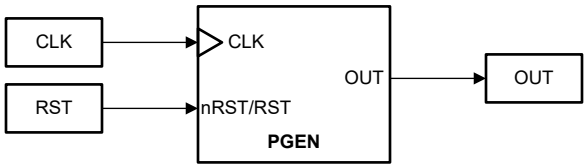

Figure 1-1. Pattern Generator Macro-cell Block Diagram

The circuit configured in InterConnect Studio (ICS), shown in Figure 1-2, generates a 16-bit pattern of *0xD1F2* that is clocked out at 2kHz using the internal oscillator. The pattern can be provided in decimal (0 to 65535) or hexadecimal (0x0000 to 0xFFFF), any bits not specified are defaulted to 0, and is stored in binary from MSB to LSB. Depending on the designated size (*n*), the *n*-bit pattern is clocked out from bit *n*-1 to bit 0, regardless of how many bits are stored in the non-volatile memory.

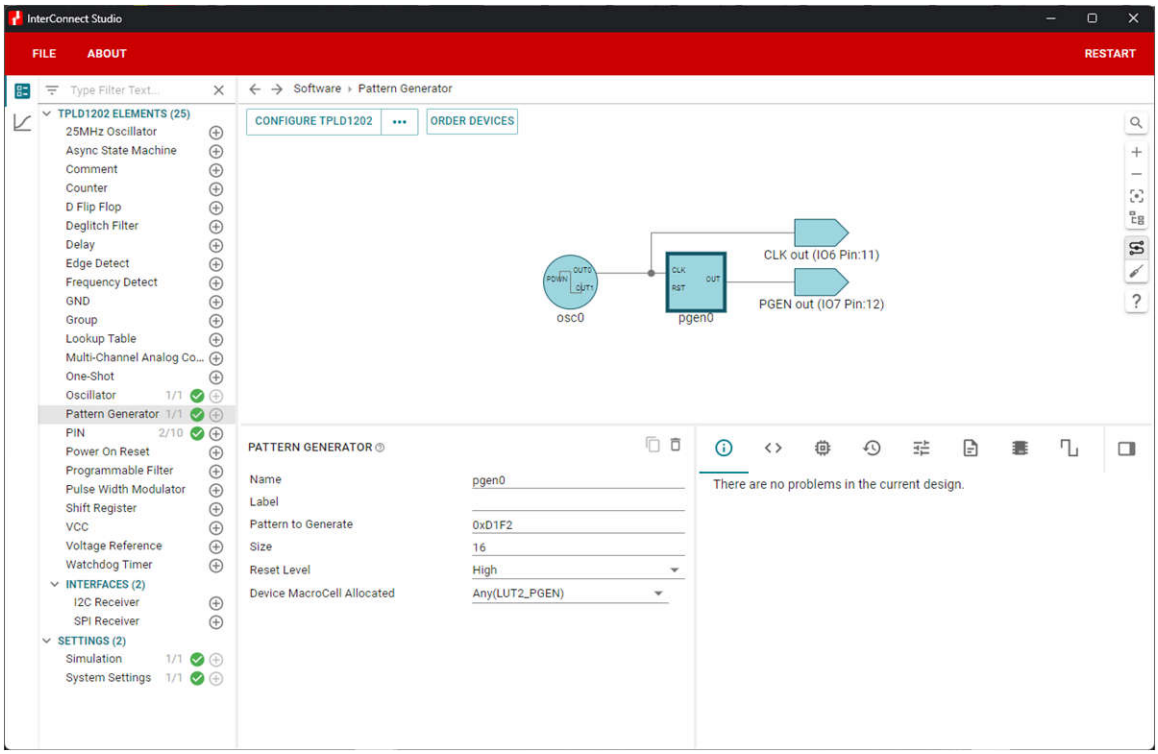

Figure 1-2. Pattern Generator (PGEN) Configuration in ICS

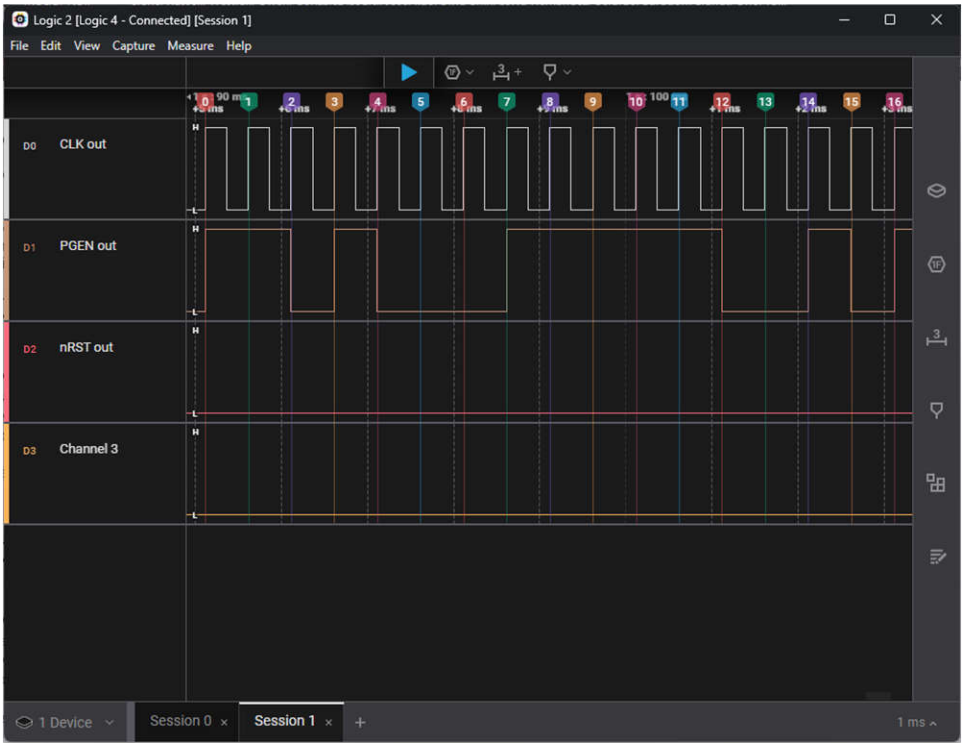

Figure 1-3. Logic Analyzer Capture of Pattern Generator Output

2 Utilizing the Reset Input of the Pattern Generator

A reset signal can be added to the circuit to restart the pattern generator. The PGEN macro-cell defaults to an active-low reset. While in the reset state, the PGEN will continually output the MSB of the specified pattern. After the reset is de-asserted, the pattern will begin to output on the next rising edge of the CLK input. Figure 2-1 shows an example of the PGEN configured to output a 16-bit pattern, 0xD1F2, with an active-high reset. As shown in Figure 2-2, while the RST signal is high, the output of the PGEN remains high since the MSB of the pattern is a 1.

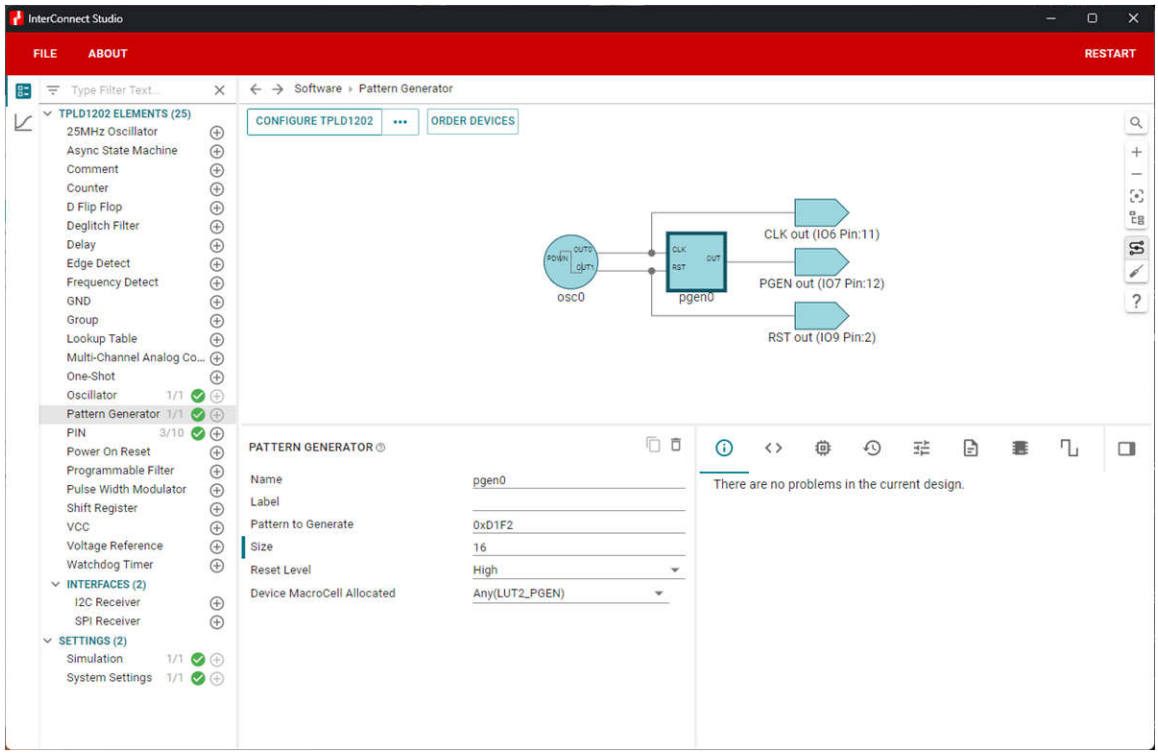

Figure 2-1. PGEN With Reset (16-bit pattern, 0xD1F2) Example Configuration in ICS

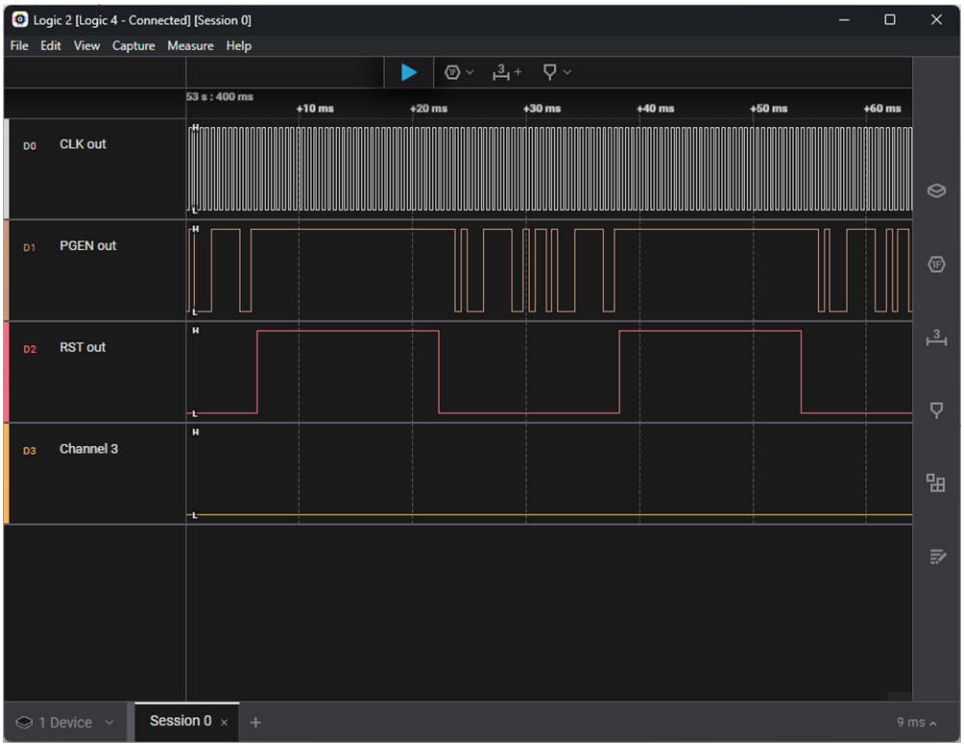

Figure 2-2. Logic Analyzer Capture of PGEN With Reset (16-bit Pattern, 0xD1F2)

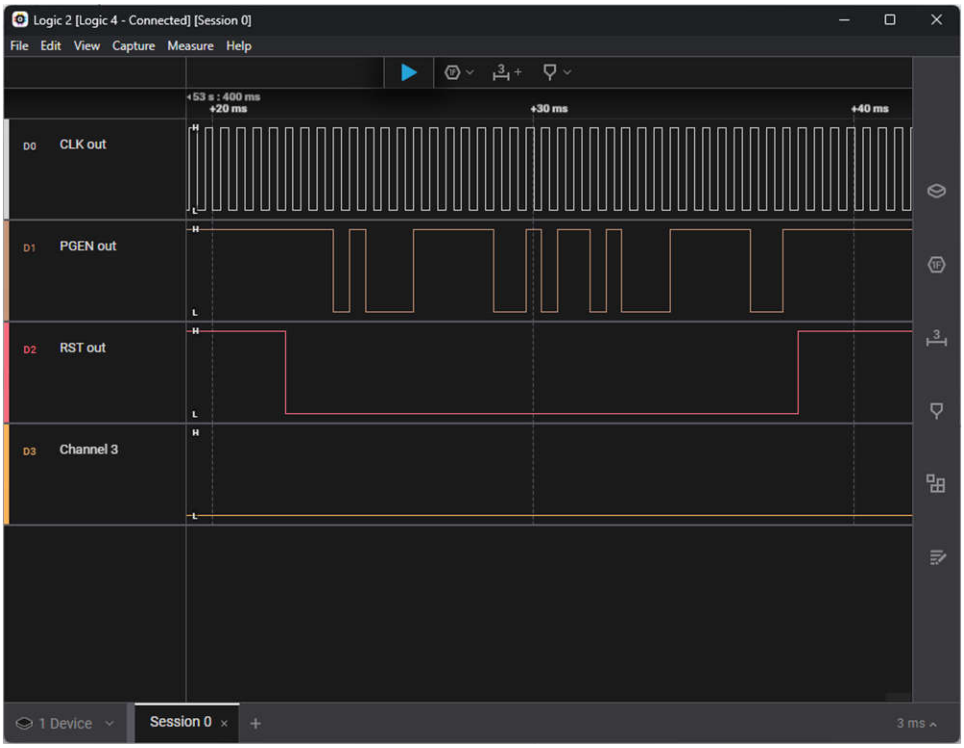

Figure 2-3. Logic Analyzer Capture of PGEN With Reset (16-bit Pattern, 0xD1F2, Zoomed)

3 Generating a Pattern Less Than 16 bits

While the *Pattern to Generate* field will accept any value from 0x0000 to 0xFFFF, only the number of bits specified in the *Size* field will be used for the PGEN output. Figure 3-1 shows an example of a PGEN macro-cell configured with the *Pattern to Generate* 0xD1F2, but with a *Size* of 10, resulting in the lower 10 bits being used and the output pattern of *0x1F2*.

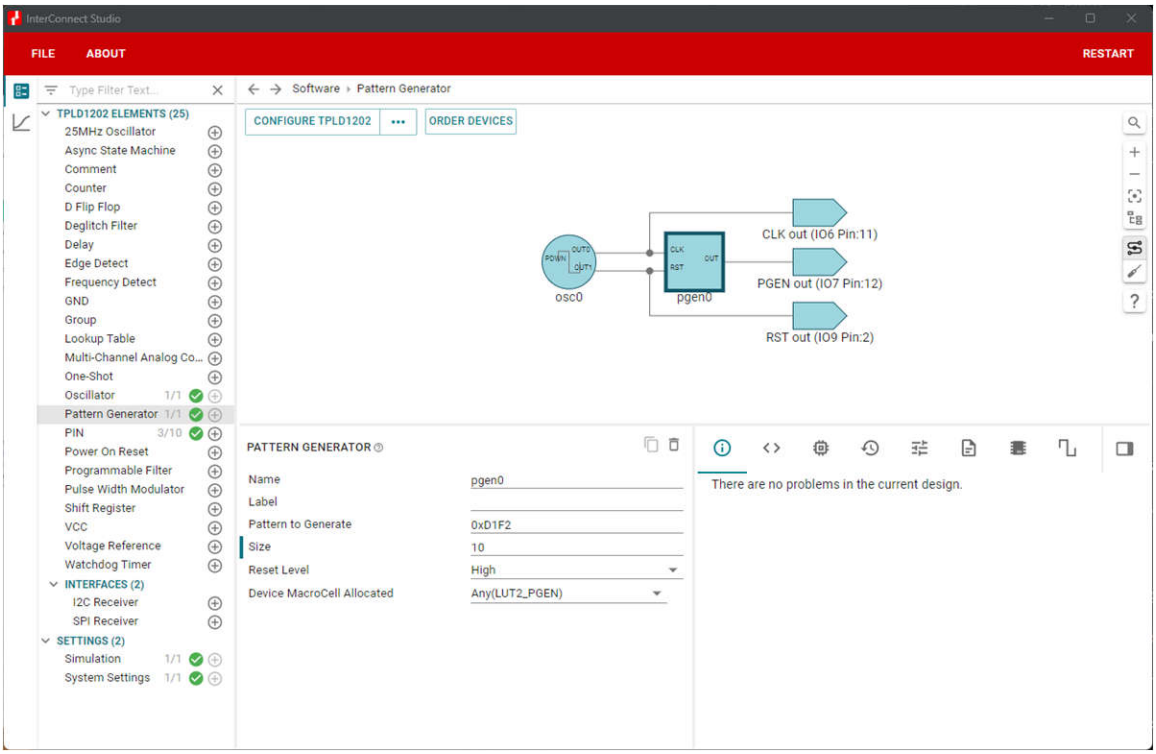

Figure 3-1. PGEN With Reset (10-bit Pattern, 0x1F2) Example Configuration in ICS

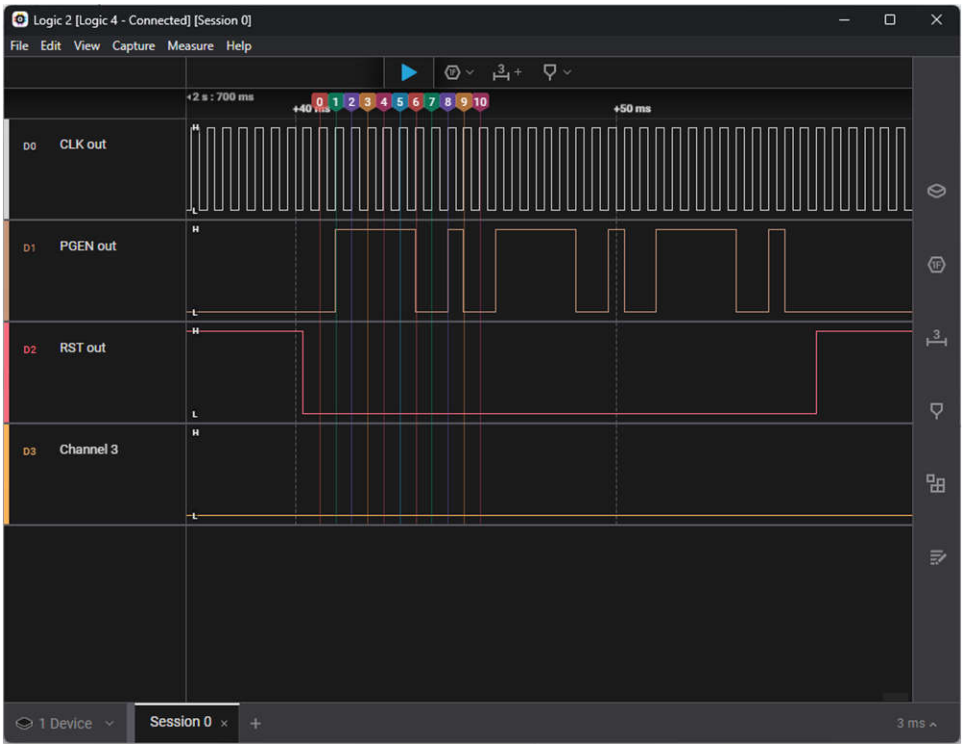

Figure 3-2. Logic Analyzer Capture of PGEN With Reset (10-bit Pattern, 0x1F2)

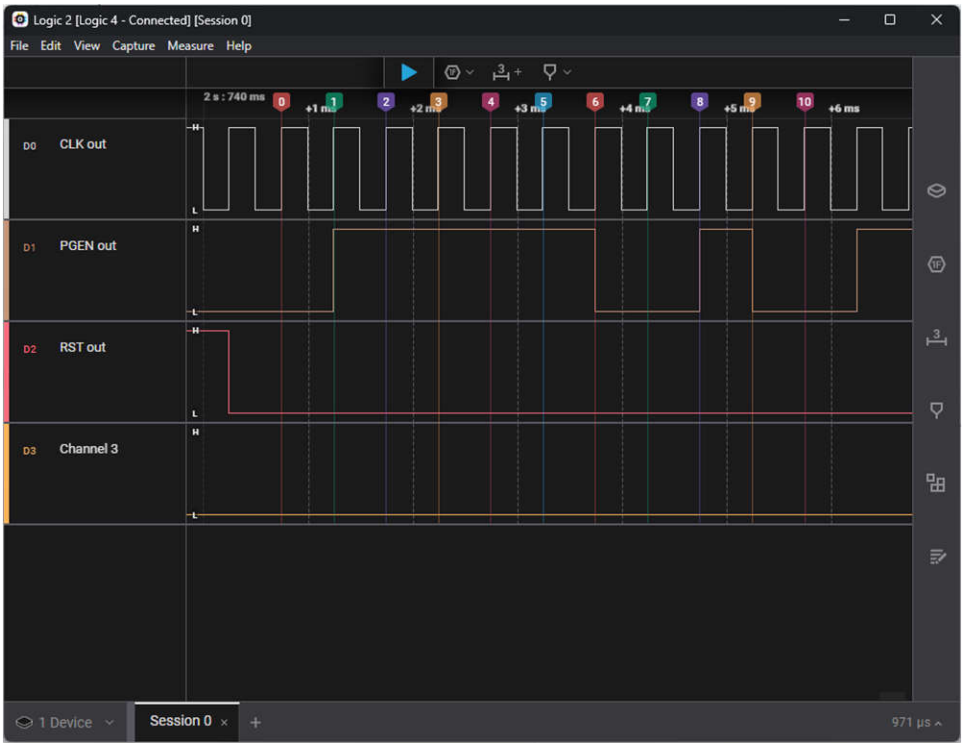

Figure 3-3. Logic Analyzer Capture of PGEN With Reset (10-bit Pattern, 0x1F2, Zoomed)

4 References

- Texas Instruments, TI Programmable Logic Devices

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