Application Brief

Configure a One Shot With TI Programmable Logic Devices

Malcolm Lyn *Interface Logic*

TI programmable logic devices (TPLD) can be configured to behave as monostable multivibrators (also known as one-shots), which, upon receiving an input trigger signal of variable length, output a fixed length pulse signal. The design captured in Figure 1 utilizes the internal oscillator, counter, and lookup table modules in a TPLD device to act as a non-retriggerrable one-shot.

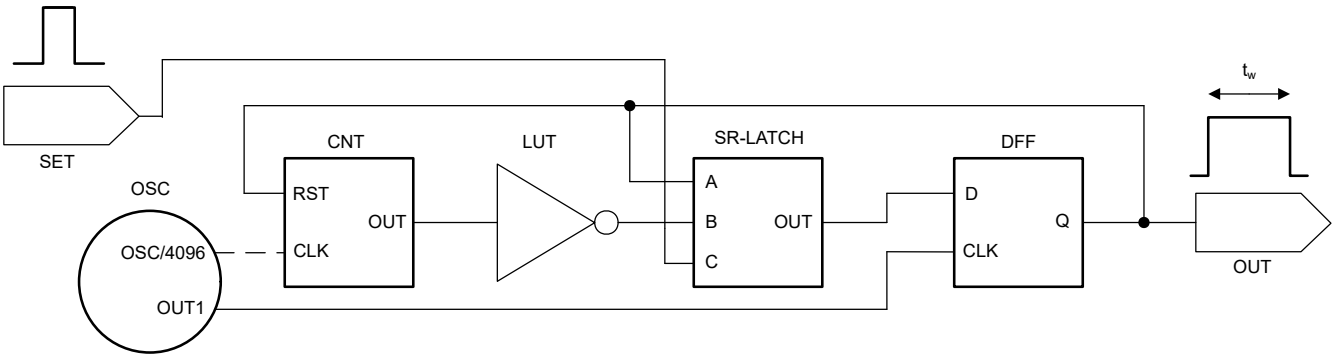

Figure 1. One Shot Schematic

Example Configuration

The 2MHz oscillator is predivided by 8 and outputs a frequency of 250kHz. The counter module (CNT in Figure 1) further divides this frequency by 4096, and thus is driven by a 61Hz signal on the CLK input. The counter module data is set to 255, meaning the counter outputs a high pulse every 255 clock cycles. In this design, the input frequency to the counter module has a period of 1 ÷ 61Hz = 16.4ms, which means the counter pulses high approximately every 4.2s. This means the output pulse width will be approximately 4.2s upon receiving an appropriate input trigger signal.

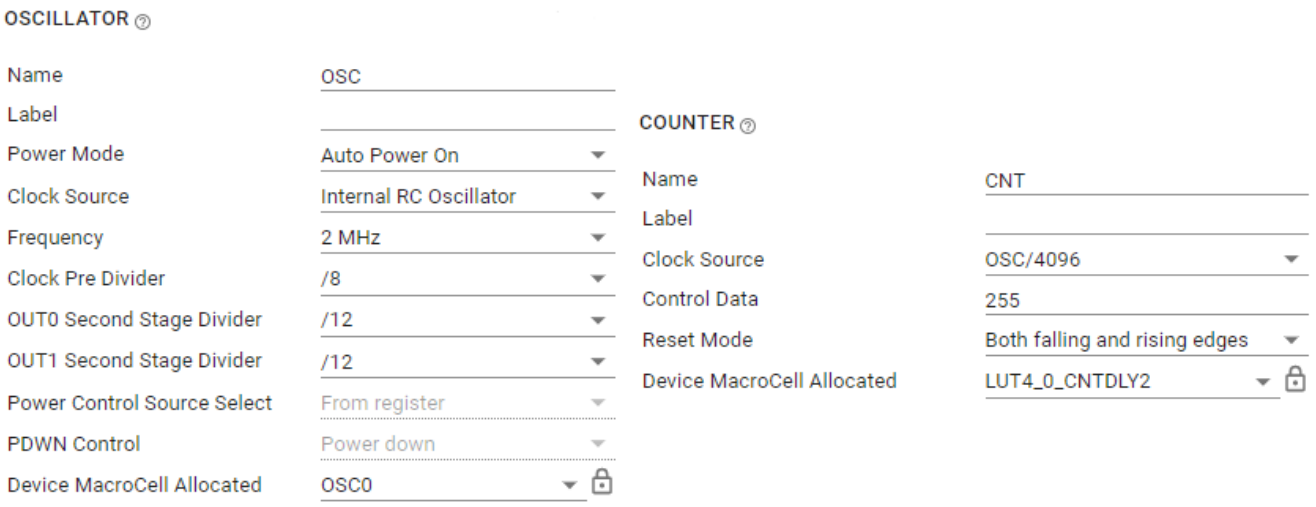

Figure 2. Oscillator and Counter Configurations

The output of the counter module is inverted and connected to a lookup table configured as an SR-Latch. The *C* input of the LUT configured as an SR-Latch is connected to the input pin named *SET* which provides the desired trigger signal. When *SET* pulses high, the SR-Latch outputs high and the DFF latches the input signal and begins outputting the pulse signal. The DFF also resets the counter module so that the counter module has to count all 255 clock cycles from the internal oscillator. Once the counter receives 255 clock cycles from the internal oscillator, the module pulses high, causing the SR-Latch to reset the DFF until the *SET* pin receives another high pulse.

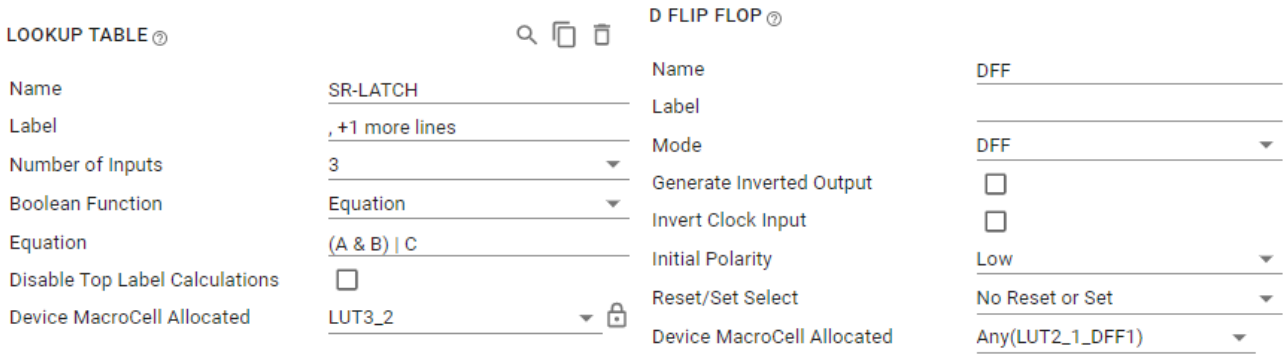

Figure 3. DFF and LUT (SR-Latch) Configurations

Design Considerations

- The output pulse width can be calculated using the equation (counter data × t_{CNT}), where t_{CNT} is equal to the period of the counter CLK input or (1 ÷ counter clock frequency). In the above design, the counter clock frequency was 61Hz and t_{CNT} was 16.4ms
- The input pulse width must be greater than $3t_{CNT}$ to trigger the one-shot, since the counter module pulses high for the next two incoming clock cycles upon reset
- TPLD oscillators have an accuracy of ±5% and the output pulse width can vary considerably from device to device. If precision pulse generation is necessary, consider providing an external clock signal from a crystal oscillator
- If a button or otherwise noisy input signal is being used to trigger the pulse, configure the input pin as a Schmitt trigger input and provide an external RC filter to prevent unwanted pulses from triggering
- Need additional assistance? Ask our engineers a question on the *TI E2E™ logic support forum*.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265