Functional Safety Information

TPS7B86-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the TPS7B86-Q1 (TO-252 and HSOIC packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for a fixed output without PG for reference.

Figure 1-2 shows the device functional block diagram for an adjustable output without PG for reference

Figure 1-3 shows the device functional block diagram for a fixed output with PG for reference

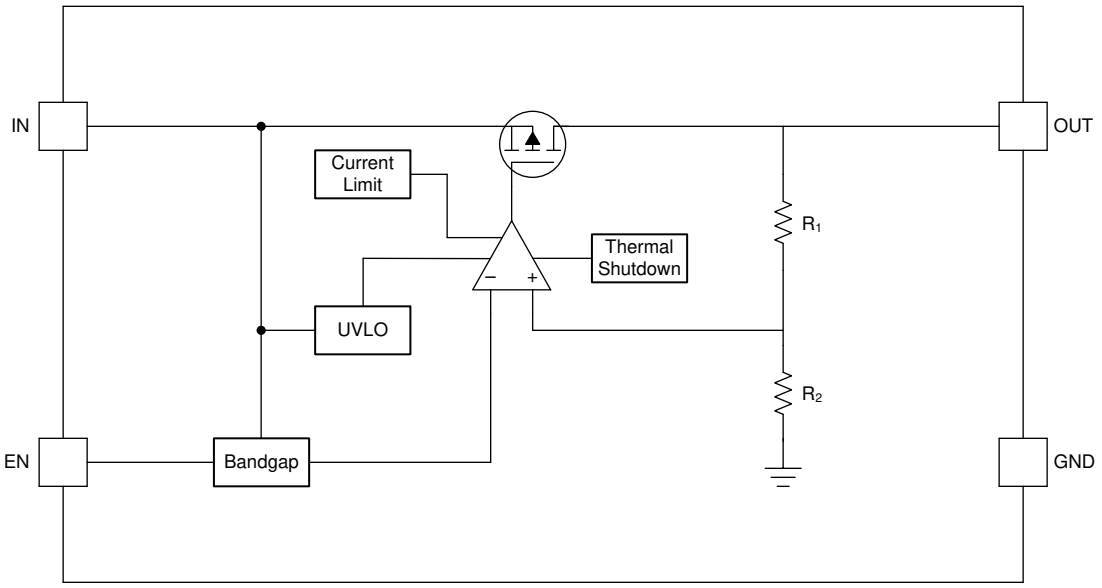

Figure 1-1. TPS7B86-Q1 Fixed Output Without PG

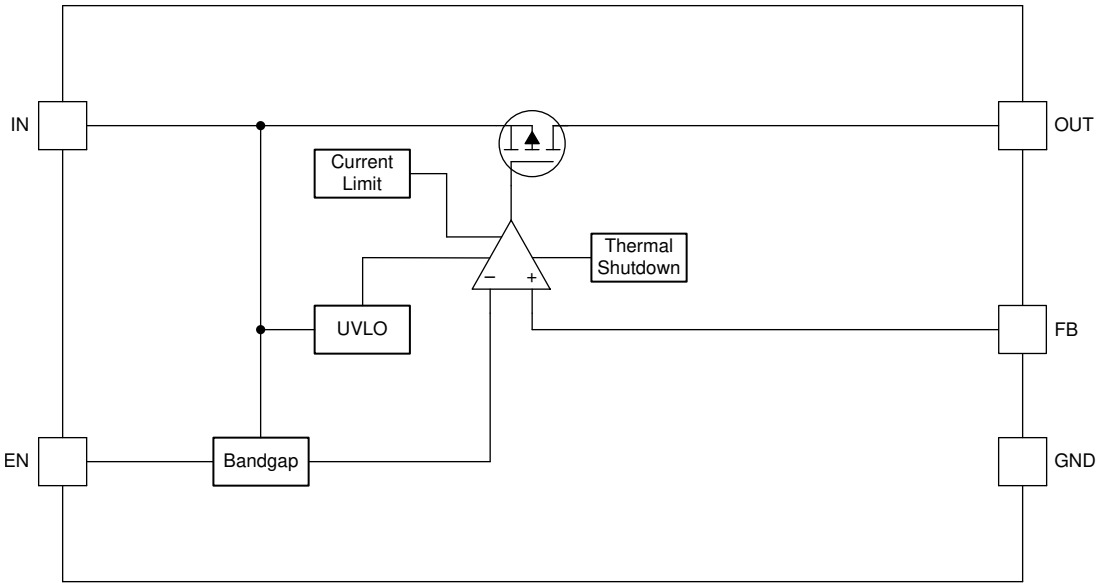

Figure 1-2. TPS7B86-Q1 Adjustable Output Without PG

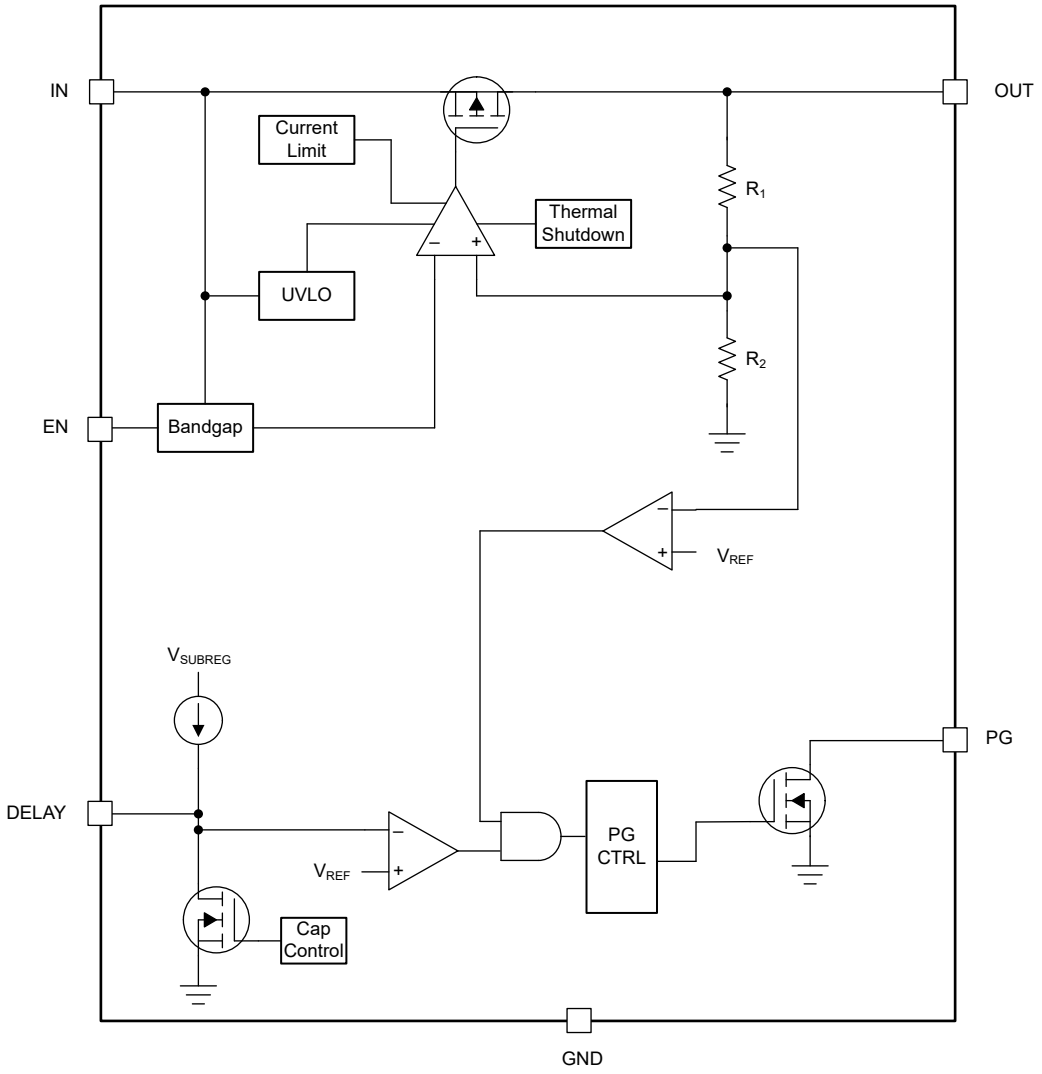

Figure 1-3. TPS7B86-Q1 With PG

The TPS7B86-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 TO-252 Package

This section provides functional safety failure in time (FIT) rates for the TO-252 package of the TPS7B86-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	15
Die FIT rate	4
Package FIT rate	11

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power amplifier and regulator ≤ 1 Watt – (LDO)	40 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 HSOIC Package

This section provides functional safety failure in time (FIT) rates for the HSOIC package of the TPS7B86-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	5
Package FIT rate	8

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power amplifier and regulator ≤ 1 Watt – (LDO)	40 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7B86-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT high (following VIN)	15
VOUT not in specification (voltage or timing)	60
VOUT low (no output)	15
PG false trigger, fails to trigger	5
Short circuit any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7B86-Q1 (TO-252 and HSOIC packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6.)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 TO-252 Package

Figure 4-1 shows the TPS7B86-Q1 pin diagram for the TO-252 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B86-Q1 data sheet.

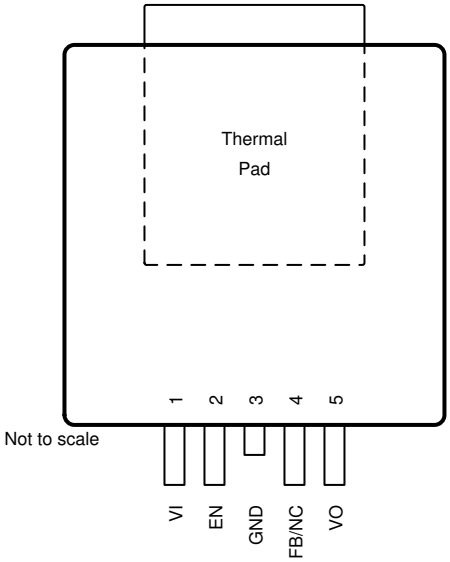

Figure 4-1. Pin Diagram (TO-252 Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to the device. System performance depends on upstream current limiting.	B
EN	2	The device is disabled, resulting in no output voltage.	B
GND	3	No effect. Normal operation.	D
FB/NC	4	(Fixed output.) No effect. Normal operation. (Adjustable output.) Output voltage is input voltage minus dropout voltage because the error amplifier drives the pass transistor gate to the rail.	B/D
OUT	5	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to the device, resulting in no output voltage.	B
EN	2	The enable circuit is in an unknown state. The device can be enabled or disabled.	B
GND	3	There is no current loop for the supply voltage. The device is not operational and does not regulate.	B
FB/NC	4	(Fixed output.) No effect. Normal operation. (Adjustable output.) The error amplifier input is not connected. The output voltage is indeterminate.	B/D
OUT	5	The device output is disconnected from the load.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN	1	EN (pin 2)	The device is always enabled when the input is powered.	B
EN	2	GND (pin 3)	The device is forced off.	B
GND	3	FB/NC (pin 4)	(Fixed output.) No effect. Normal operation. (Adjustable output.) Output voltage is input voltage minus dropout voltage because the error amplifier drives the pass transistor gate to the rail.	B/D
FB/NC	4	OUT (pin 5)	(Fixed output.) No effect. Normal operation. (Adjustable output.) Output voltage is equal to the internal reference voltage.	B/D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No effect. Normal operation.	D
EN	2	The device is always enabled when the input is powered.	B
GND	3	Power is not supplied to the device. System performance depends on upstream current limiting.	B
FB/NC	4	(Fixed output.) No effect. Normal operation. (Adjustable output.) The error amplifier input can be damaged if the input voltage is above 20 V. The output is not at the target voltage.	A/D
OUT	5	Damage is possible if the absolute maximum rating is exceeded (20 V max). Reverse current can destroy the device.	A

4.2 HSOIC Package

Figure 4-2 shows the TPS7B86-Q1 pin diagram for the HSOIC package without PG. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B86-Q1 data sheet.

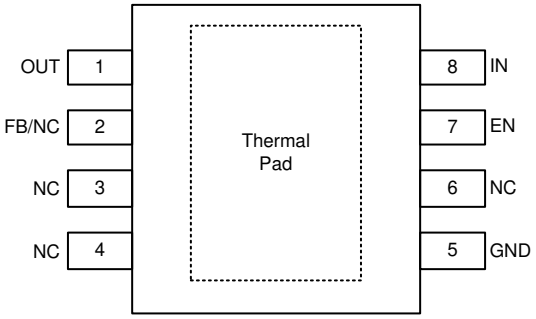

Figure 4-2. Pin Diagram
(HSOIC Package Without PG)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
FB/NC	2	(Fixed output.) No effect. Normal operation. (Adjustable output.) Output voltage is input voltage minus dropout voltage because the error amplifier drives the pass transistor gate to the rail.	B/D
NC	3	No effect. Normal operation.	D
NC	4	No effect. Normal operation.	D
GND	5	No effect. Normal operation.	D
NC	6	No effect. Normal operation.	D
EN	7	The device is disabled, resulting in no output voltage.	B
IN	8	Power is not supplied to the device. System performance depends on upstream current limiting.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device output is disconnected from the load.	B
FB/NC	2	(Fixed output.) No effect. Normal operation. (Adjustable output.) The error amplifier input is not connected. The output voltage is indeterminate.	B/D
NC	3	No effect. Normal operation.	D
NC	4	No effect. Normal operation.	D
GND	5	There is no current loop for the supply voltage. The device is not operational and does not regulate.	B
NC	6	No effect. Normal operation.	D
EN	7	The enable circuit is in an unknown state. The device can be enabled or disabled.	B
IN	8	Power is not supplied to the device, resulting in no output voltage.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	FB/NC (pin 2)	(Fixed output.) No effect. Normal operation. (Adjustable output.) Output voltage is equal to internal reference voltage.	B/D
FB/NC	2	NC (pin 3)	No effect. Normal operation.	D
NC	3	NC (pin 4)	No effect. Normal operation.	D
GND	5	NC (pin 6)	No effect. Normal operation.	D
NC	6	EN (pin 7)	No effect. Normal operation.	D
EN	7	IN (pin 8)	The device is always enabled when the input is powered.	B

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Damage is possible if the absolute maximum rating is exceeded (20 V max). Reverse current can destroy the device.	A
FB/NC	2	(Fixed output.) No effect. Normal operation. (Adjustable output.) The error amplifier input can be damaged. The output is not at the target voltage.	A/D
NC	3	No effect. Normal operation.	D
NC	4	No effect. Normal operation.	D
GND	5	Power is not supplied to the device. System performance depends on upstream current limiting.	B
NC	6	No effect. Normal operation.	D
EN	7	The device is always enabled when the input is powered.	B
IN	8	No effect. Normal operation.	D

4.3 HSOIC Package B Version

Figure 4-3 shows the TPS7B86-Q1 pin diagram for the HSOIC package B version with PG. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B86-Q1 data sheet.

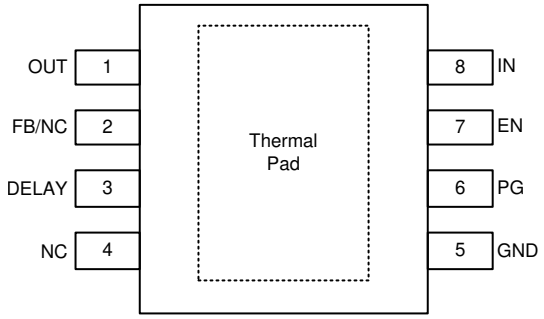

Figure 4-3. Pin Diagram
(HSOIC Package B Version With PG)

Table 4-10. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
FB/NC	2	(Fixed output.) No effect. Normal operation. (Adjustable output.) Output voltage is input voltage minus dropout voltage because the error amplifier drives the pass transistor gate to the rail.	B/D
DELAY	3	Ground current is permanently increased.	C
NC	4	No effect. Normal operation.	D
GND	5	No effect. Normal operation.	D
PG	6	Power-good never asserts when the output voltage is at target, thus potentially effecting power sequencing.	B
EN	7	The device is disabled, resulting in no output voltage.	B
IN	8	Power is not supplied to the device. System performance depends on upstream current limiting.	B

Table 4-11. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device output is disconnected from the load.	B
FB/NC	2	(Fixed output.) No effect. Normal operation. (Adjustable output.) The error amplifier input is not connected. The output voltage is indeterminate.	B/D
DELAY	3	The power-good delay is set to the minimum delay time $t_{(DLY\_FIX)}$.	C
NC	4	No effect. Normal operation.	D
GND	5	There is no current loop for the supply voltage. The device is not operational and does not regulate.	B
PG	6	The power-good signal is not accessible. Power sequencing can be effected.	B
EN	7	The enable circuit is in an unknown state. The device can be enabled or disabled.	B
IN	8	Power is not supplied to the device, resulting in no output voltage.	B

Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	FB/NC (pin 2)	(Fixed output.) No effect. Normal operation. (Adjustable output.) Output voltage is equal to internal reference voltage.	B/D
FB/NC	2	DELAY (pin 3)	(Fixed output.) No effect. Normal operation. (Adjustable output.) PG can possibly never assert and the output voltage can thus be inaccurate.	B/D
DELAY	3	NC (pin 4)	No effect. Normal operation.	D
GND	5	PG (pin 6)	Power-good cannot assert. Power sequencing can be affected.	B
PG	6	EN (pin 7)	Power-good functionality cannot operate correctly. PG can be damaged if the absolute maximum rating (20 V) is violated.	B/A
EN	7	IN (pin 8)	The device is always enabled when the input is powered.	B

Table 4-13. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Damage is possible if the absolute maximum rating is exceeded (20 V max). Reverse current can destroy the device.	A
FB/NC	2	(Fixed output.) No effect. Normal operation. (Adjustable output.) The error amplifier input can be damaged. The output is not at the target voltage.	A/D
DELAY	3	PG can incorrectly assert when the output voltage is not at target. The pin absolute maximum rating (6 V max) can be exceeded and the pin can be damaged.	B/A
NC	4	No effect. Normal operation.	D
GND	5	Power is not supplied to the device. System performance depends on upstream current limiting.	B
PG	6	Power-good functionality cannot operate correctly. PG can be damaged if the absolute maximum rating (20 V) is violated.	B/A
EN	7	The device is always enabled when the input is powered.	B
IN	8	No effect. Normal operation.	D

4.4 HSOIC Package D Version

Figure 4-4 shows the TPS7B86-Q1 pin diagram for the HSOIC package D version with PG. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B86-Q1 data sheet.

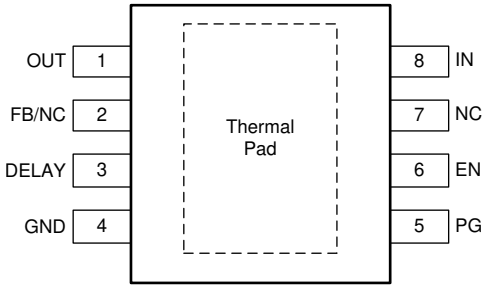

Figure 4-4. Pin Diagram (HSOIC Package D Version With PG)

Table 4-14. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
FB/NC	2	(Fixed output.) No effect. Normal operation. (Adjustable output.) Output voltage is input voltage minus dropout voltage because the error amplifier drives the pass transistor gate to the rail.	B/D
DELAY	3	Ground current is permanently increased.	C
GND	4	No effect. Normal operation.	D
PG	5	Power-good never asserts when the output voltage is at target, thus potentially effecting power sequencing.	B
EN	6	The device is disabled, resulting in no output voltage.	B
NC	7	No effect. Normal operation.	D
IN	8	Power is not supplied to the device. System performance depends on upstream current limiting.	B

Table 4-15. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device output is disconnected from the load.	B
FB/NC	2	(Fixed output.) No effect. Normal operation. (Adjustable output.) The error amplifier input is not connected. The output voltage is indeterminate.	B/D
DELAY	3	The power-good delay is set to the minimum delay time $t_{(DLY\_FIX)}$.	C
GND	4	There is no current loop for the supply voltage. The device is not operational and does not regulate.	B
PG	5	The power-good signal is not accessible. Power sequencing can be effected.	B
EN	6	The enable circuit is in an unknown state. The device can be enabled or disabled.	B
NC	7	No effect. Normal operation.	D
IN	8	Power is not supplied to the device, resulting in no output voltage.	B

Table 4-16. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	FB/NC (pin 2)	(Fixed output.) No effect. Normal operation. (Adjustable output.) The output voltage is equal to the internal reference voltage.	B/D
FB/NC	2	DELAY (pin 3)	(Fixed output.) No effect. Normal operation. (Adjustable output.) PG can possibly never assert and the output voltage can be inaccurate.	B/D
DELAY	3	GND (pin 4)	Ground current is permanently increased.	C
PG	5	EN (pin 6)	Power-good functionality cannot operate correctly. PG can be damaged if the absolute maximum rating (20 V) is violated.	B/A
EN	6	NC (pin 7)	No effect. Normal operation.	D
NC	7	IN (pin 8)	No effect. Normal operation.	D

Table 4-17. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Damage is possible if the absolute maximum rating is exceeded (20 V max). Reverse current can destroy the device.	A
FB/NC	2	(Fixed output.) No effect. Normal operation. (Adjustable output.) The pin absolute maximum rating (20 V max) can be exceeded and the pin can be damaged. The output is not at the target voltage.	A/D
DELAY	3	PG can incorrectly assert when the output voltage is not at target. The pin absolute maximum rating (6 V max) can be exceeded and the pin can be damaged.	A
GND	4	Power is not supplied to the device. System performance depends on upstream current limiting.	B
PG	5	The pin absolute maximum rating (20 V max) can be exceeded and the pin can be damaged.	A
EN	6	The device is always enabled when the input is powered.	B
NC	7	No effect. Normal operation.	D
IN	8	No effect. Normal operation.	D

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