Functional Safety Information

TPS61033-Q1 and TPS610333-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TPS61033-Q1 and TPS610333-Q1 (SOT583 (8) package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagrams for reference.

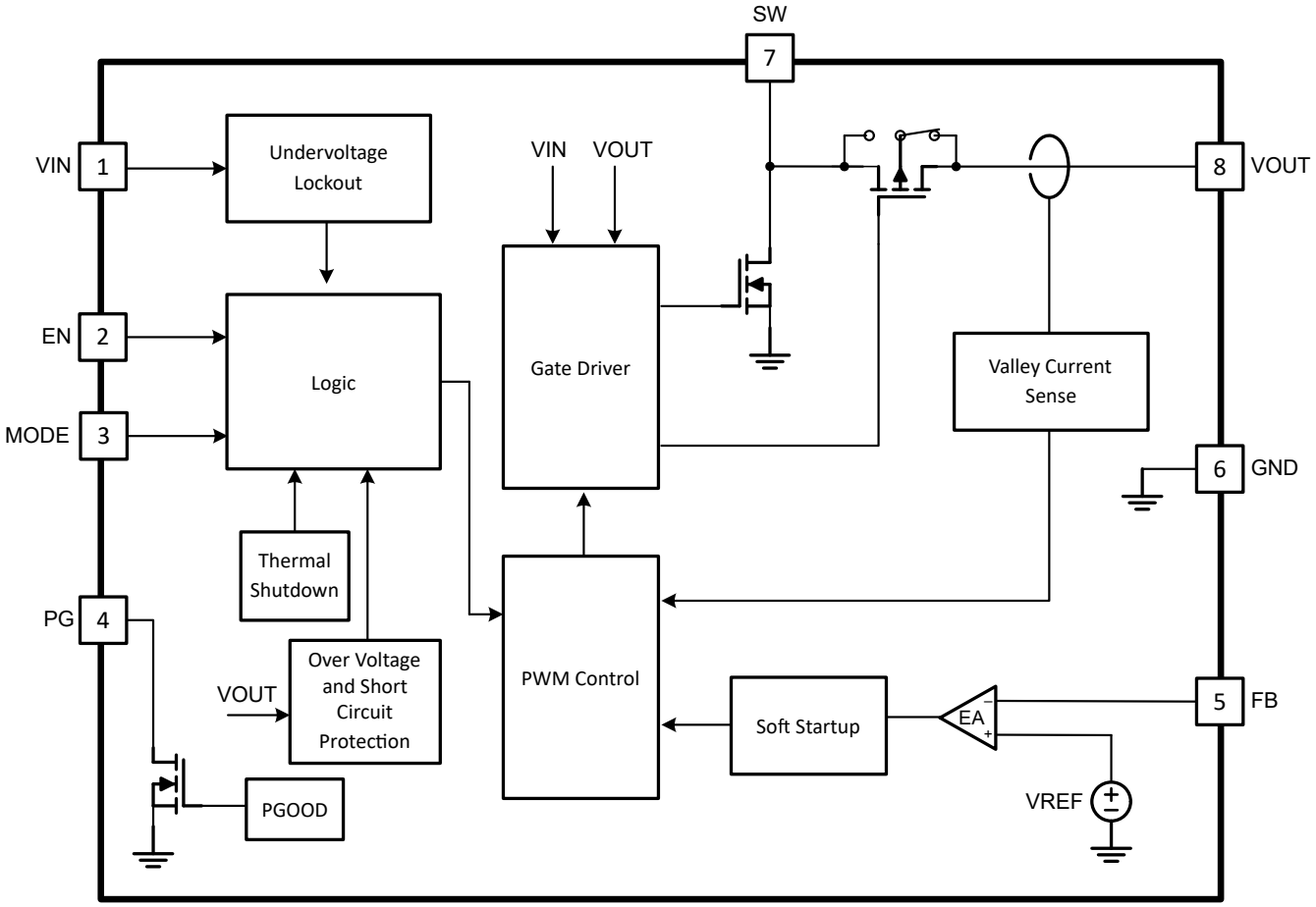

Figure 1-1. TPS61033-Q1 & TPS610333-Q1 Functional Block Diagram

The TPS61033-Q1 and TPS610333-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the TPS61033-Q1 and TPS610333-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	22
Die FIT Rate	20
Package FIT Rate	2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1000 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS61033-Q1 and TPS610333-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VO not in specification voltage or timing	55%
VO No output GND or HIZ	10%
SW FETs stuck on	25%
EN enable fails or false enable	5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS61033-Q1 and TPS610333-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS61033-Q1 and TPS610333-Q1 pin diagrams. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the *TPS61033-Q1 5.5-V 5.5-A 2.4-MHz Fully-Integrated Synchronous Boost Converter, with Output Discharge Function* data sheets.

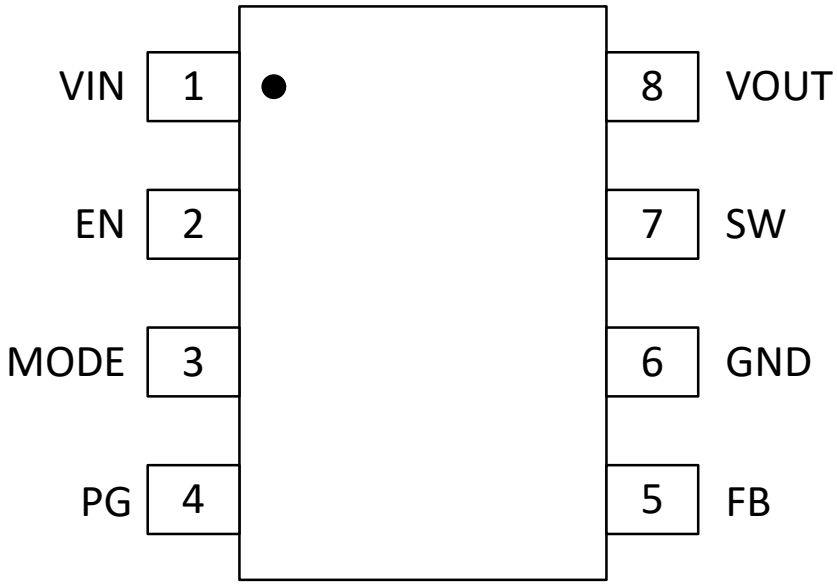

Figure 4-1. TPS61033-Q1 and TPS610333-Q1 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the *Recommended Operating Conditions* and the *Absolute Maximum Ratings* found in the *TPS61033-Q1 5.5-V 5.5-A 2.4-MHz Fully-Integrated Synchronous Boost Converter, with Output Discharge Function* data sheet.
- Configuration as shown in the *Application and Implementation* found in the *TPS61033-Q1 5.5-V 5.5-A 2.4-MHz Fully-Integrated Synchronous Boost Converter, with Output Discharge Function* data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN	1	No output voltage.	B
EN	2	No output voltage.	B
MODE	3	Device remains in auto PFM mode, loss of FPWM functionality.	B
PG	4	Loss of power good indicator functionality.	B
FB	5	If short before start-up, device remains in pre-charge mode, output voltage is not correct.	C
		If short after start-up and load current is low, OVP triggers.	C
		If short after start-up and load current is high, high-side FET is always turning on, output voltage is not correct.	B
GND	6	No effect.	D
SW	7	Possible damage to inductor and pin.	A
VOUT	8	Device is in short-to-ground protection mode, inductor current is limited to approximately 400 mA.	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN	1	No output voltage.	B
EN	2	No output voltage.	B
MODE	3	Device remains in auto PFM mode, loss of FPWM functionality.	B
PG	4	Loss of power good indicator functionality.	B
FB	5	OVP triggers.	B
GND	6	Possible damage to device.	A
SW	7	No output voltage.	B
VOUT	8	Possible damage to device.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN	1	Loss of disable functionality.	B
EN	2	For PFM mode, the device is disabled, no output voltage.	B
		For FPWM mode, loss of disable functionality.	B
MODE	3	For PFM mode, loss of power good functionality.	B
		For FPWM mode, possible damaged to device.	A
PG	4	/	/
FB	5	If short before start-up, device remains in pre-charge mode, output voltage is not correct.	C
		If short after start-up and load current is lower than 1.5A (typ.), OVP triggers.	C
		If short after start-up and load current is higher than 1.5A (typ.), high-side FET is always turning on (similar with pass-through mode), output voltage is not correct.	B
GND	6	Possible damage to inductor and pin.	A
SW	7	Possible damage to device.	A
VOUT	8	/	/

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN	1	No effect.	D
EN	2	Loss of disable functionality.	B
MODE	3	Device remains in FPWM mode, loss of auto PFM functionality.	B
PG	4	Possible damaged to device.	A
FB	5	The output voltage is fixed in 5 V, loss of adjustable output voltage functionality	B
GND	6	No output voltage, power supply is shorted.	B
SW	7	Possible damaged to device.	A
VOUT	8	The output voltage is equal to the supply voltage.	B

5 Revision History

Changes from Revision * (July 2023) to Revision A (November 2023)	Page
• Changed failure mode distribution percentage value from 57.8% to 55% in Table 3-1	4

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