

# LMR43606-Q1 Functional Safety FIT Rate, FMD and Pin FMA



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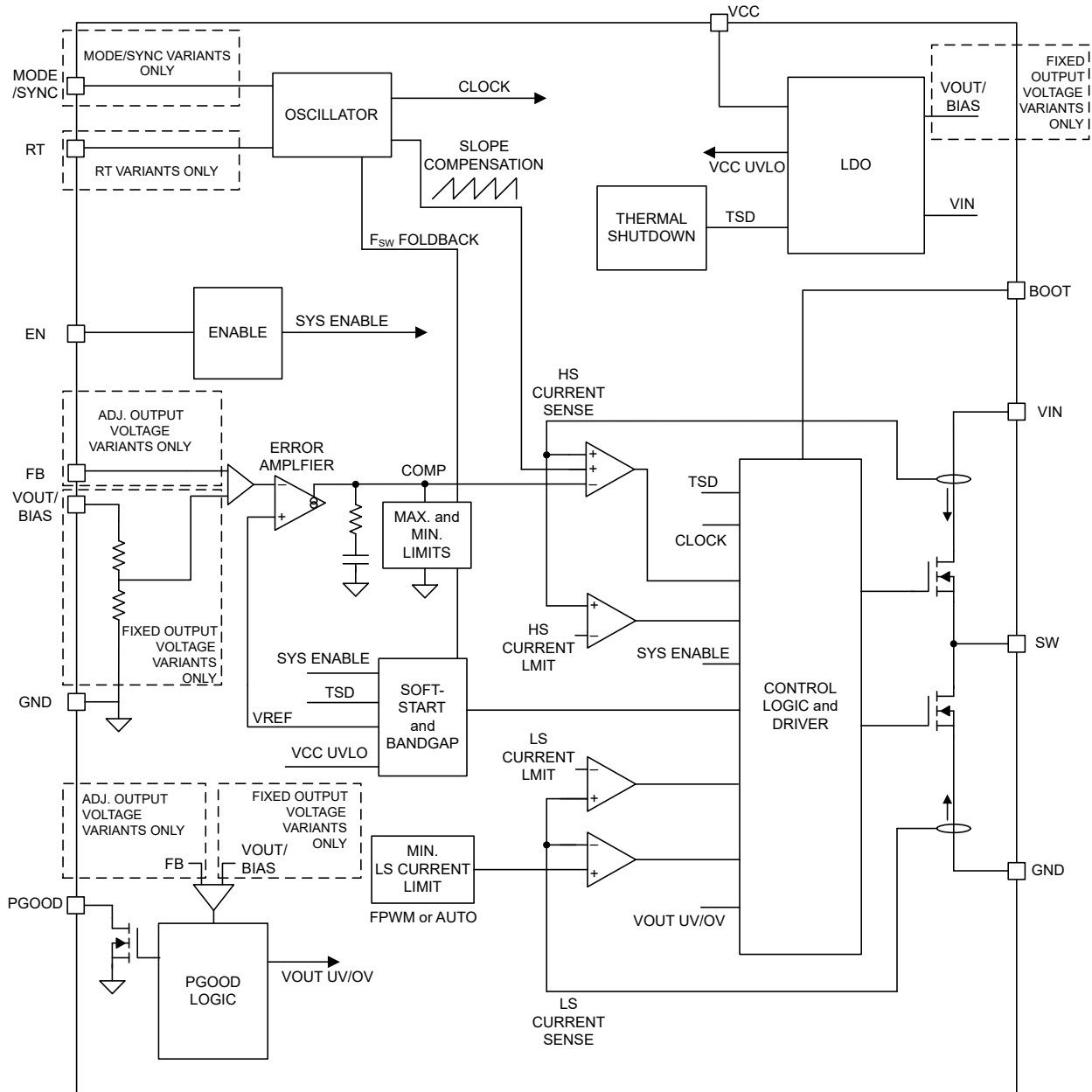
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# 1 Overview

This document contains information for LMR43606-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.



**Figure 1-1. Functional Block Diagram**

LMR43606-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LMR43606-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)
Total Component FIT Rate	7
Die FIT Rate	4
Package FIT Rate	3

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 135 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

Table	Category	Reference FIT Rate	Reference Virtual T <sub>J</sub>
5	CMOS, BICMOS ASICs Analog & Mixed =<50V supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T<sub>J</sub> (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

### 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMR43606-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

Die Failure Modes	Failure Mode Distribution (%)
No Output Voltage	60
Output not in specification - voltage or timing	30
PG false trip or fails to trip	5
Short circuit any two pins	5

The FMD in [Table 3-1](#) excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

## 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LMR43606-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

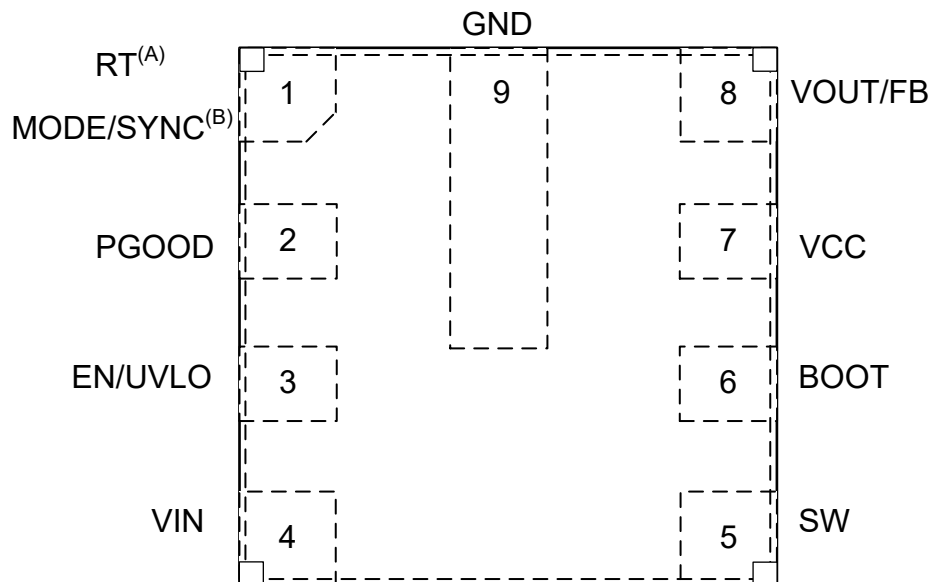
- Pin short-circuited to Ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

**Table 4-1. TI Classification of Failure Effects**

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

[Figure 4-1](#) shows the LMR43606-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LMR43606-Q1 data sheet.



**Figure 4-1. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the [LMR436x0-Q1](#) data sheet is used.

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RT or MODE/ SYNC	1	The switching frequency is 2.2MHz.	D
PGOOD	2	When not in use, this pin can be left grounded (PGOOD is not a valid signal and $V_{OUT}$ is normal).	D
EN/UVLO	3	$V_{OUT} = 0V$ (Enable is off and functionality is halted.)	D
VIN	4	$V_{OUT} = 0V$	B
SW	5	Damage to HSFET	A
BOOT	6	$V_{OUT} = 0V$ . HS does not turn on.	B
VCC	7	$V_{OUT} = 0V$	B
VOU/BIAS or FB	8	When in adjustable output mode, $V_{OUT}$ approaches VIN. When in fixed output mode, $V_{OUT} = 0V$ .	B
GND	9	$V_{OUT}$ is normal.	D

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RT or MODE/ SYNC	1	If it is an RT part, frequency is not defined. If it is a MODE/SYNC part, then the part can go back and forth between FPWM/PFM. The part is up and functional.	C
PGOOD	2	When not in use, this pin can be left open (PGOOD is not a valid signal and $V_{OUT}$ is normal).	D
EN/UVLO	3	Pin cannot be left floating.	B
VIN	4	$V_{OUT} = 0V$	B
SW	5	$V_{OUT} = 0V$	B
BOOT	6	$V_{OUT} = 0$ . HS does not turn on.	B
VCC	7	VCC output is unstable and can increase above 5.5V.	A
VOU/BIAS or FB	8	$V_{OUT}$ approaches VIN.	C
GND	9	$V_{OUT}$ can be abnormal, as reference voltage is not fixed.	C

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
RT or MODE/ SYNC	1	PGOOD	If PGOOD is high, and less than 5.5V, $F_{SW} = 1MHz$ . If PGOOD is low, $F_{SW} = 2.2MHz$ . With PGOOD absolute maximum rating being 20V, RT ESD damages if PG goes to 20V.	A
PGOOD	2	EN/UVLO	If EN/UVLO is greater than 20V, it damages devices connected to the PGOOD pin.	A
EN/UVLO	3	VIN	$V_{OUT}$ is normal (Enable is on and all other blocks work).	D
VIN	4	SW	Damage to LSFET	A
SW	5	BOOT	$V_{OUT} = 0V$ , HS does not turn on and there is no $C_{BOOT}$ .	B
BOOT	6	VCC	Damage occurs and there is a break to the VCC pin.	A
VCC	7	VOU/BIAS or FB	Does not work, but no damage occurs.	B
VOU/BIAS or FB	8	GND	When in adjustable output mode, $V_{OUT}$ approaches VIN. When in fixed output mode, $V_{OUT} = 0V$ .	B
GND	9	RT or MODE/ SYNC	$V_{OUT}$ is normal if the RT/MODE/SYNC pin is low, otherwise not functional.	B

**Table 4-5. Pin FMA for Device Pins Short-Circuited to supply**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RT or MODE/ SYNC	1	If $V_{IN}$ is greater than 5.5V, damage occurs. If $V_{IN} < 5.5V$ , switching frequency is 1MHz.	A
PGOOD	2	If $V_{IN}$ is less than 20V, it damages PGOOD.	A
EN/UVLO	3	$V_{OUT}$ is normal (Enable is on, all other blocks will work).	D
VIN	4	$V_{OUT}$ is normal.	D
SW	5	Damage to LSFET	A
BOOT	6	Damage occurs and BOOT ESD clamp is damaged.	A
VCC	7	If $V_{IN}$ is greater than 5.5V, damage occurs.	A
VOUT/BIAS or FB	8	If $V_{IN}$ is greater than 16V, damage occurs.	A
GND	9	$V_{OUT} = 0V$	B

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