Fact Sheet

Military Semiconductor Products

SM320C80 / SMJ320C80 / 5962-9679101

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NOT RECOMMENDED FOR NEW DESIGNS

Multi-DSP System-On-A-Chip Optimized for Image Processing

HIGHLIGHTS

The SM320C80 is the highest performance military multiprocessor DSP available today. It is a multi-processor system on a single chip. The C80 is optimized for image processing and is also used in military applications as a fixed point and floating point engine. The C80 actually has four 32-bit fixed-point DSPs plus one 32-bit RISC processor with a built-in floating point unit designed and optimized to make real-time image processing a reality. Further chip integration includes 50k Bytes of fast SRAM connected to all five processors through a crossbar switching network, a Transfer Controller to manage data movement, two video controller functions and JTAG/boundary scan functions.

KEY FEATURES/BENEFITS

- Available now in military temperature range and QML versions available
- 2+BOPS (more than 2,000,000,000 RISC-like Operations per second)
- 250 MIPS (250 Million Instructions Per Second)
- 100 MFLOP (100 Million Floating Point Instructions Per Second), IEEE-754
- 400 Mbyte/sec Burst I/O transfer rate through the 64-bit Data Bus
- 32-Bit Fixed-Point DSPs (There are four of these per chip.) (parallel ADSP)
- 32-Bit RISC Master Processor with IEEE-754 Floating Point Unit
- 50 KBytes of on-chip SRAM
- Transfer Controller for cache servicing and data I/O between external and internal SRAM
- Video controller with dual frame timers
- On-chip cache or data RAM is externally accessible via a dynamically sized 64-bit bus
- Extensive Crossbar switch network allows up to 15 on-chip SRAM memory accesses/cycle
- Direct seamless interface to DRAM, SDRAM, SRAM, and VRAM
- JTAG Emulation Interface component allows In-Circuit-Emulation and boundary scan paths via a JTAG/IEEE 1149.1 test access port

DESIGN-IN SUPPORT

TI has the most extensive DSP application support

Product Information Center:	(972) 644-5580 (For general information, availability, etc.)
DSP Developer's Village:	dspvillage.ti.com/docs/dspvillagehome.jhtml
DSP Hotline (Technical questions):	www.ti.com/sc/docs/dsps/hotline/support.htm
Third Parties URL:	www.ti.com/sc/docs/general/dsp/third/index.htm
Military C80 DSP Info:	http://www.ti.com/sc/docs/products/military/processr/320c8x.htm

PACKAGING

GF 305-pin C-PGA (Ceramic Pin Grid Array). This cavity down, heat slug up PGA weighs 41.5 grams. $R_{\theta JC}$ = 0.3°C/W, $R_{\theta JA}$ = 12.6°C/W

HFH 320-lead ceramic quad flat pack with 0.5 mm lead pitch. This cavity up, heat slug down package has a nonconductive tie bar (NCTB) with gold finish leads and weighs 27.1 grams and 32.3 grams with tie-bar. $R_{\theta JC}$= 1.13 °C/W, $R_{\theta JA}$= 26.2 °C/W

$R_{\theta JA}$..... Thermal resistance of a package without a path for heat dissipation. This is specified at a zero linear feet per minute air flow.

$R_{\theta JC}$..... Thermal resistance of a package assuming an infinite path for heat dissipation.

DIE SIZE (Approximate)

525 x 582 mils

TECHNOLOGY

0.5 micron triple level metal EPIC-III™ CMOS (50 MHz) (Vcc=3.3 V)
ESD level: 4 kV

POWER DISSIPATION

Typical: ~3.5 W
Maximum: ~8.25 W VDD x IDD(Max) measured while running non-typical worst case alternating checkerboard memory patterns.

PROCESS/PERFORMANCE OPTIONS All are available now

Device	Package	Speed	DSCC SMD	Processing
SM320C80HFHM50	320-lead C-QFP (NCTB)	50 MHz	n/a	Mil Temperature Range
SMJ320C80HFHM50	320-lead C-QFP (NCTB)	50 MHz	5962-9679101QYC	Full Military QML Processing
SM320C80GFM50	305-pin C-PGA	50 MHz	n/a	Mil Temperature Range
SMJ320C80GFM50	305-pin C-PGA	50 MHz	5962-9679101QXA	Full Military QML Processing

TEST VECTORS

The SM320C80 has ~4,000,000 test vectors. The actual test vectors are TI proprietary information.

ARCHITECTURE

The SM320C80's high performance is achieved through the parallel operation of four 32-bit fixed point DSPs and the high performance 32-bit RISC processor. The processors are fed data from either 50 Kbytes of on-chip SRAM across a crossbar connection network or off-chip memory on a 64-bit data bus. All accesses are controlled by a transfer controller.

INTERNAL MEMORY 25 blocks of 2K x 8 multi-ported SRAM. Each data block can be accessed by any Parallel ADSP.

TRANSFER CONTROLLER All memory accesses are made by the processor through the Transfer Controller TC). Data located in on-chip (memory is accessed across the crossbar through either a local or global bus. Off-chip accesses are made on the 64-bit data bus with a bandwidth of 400 Mbytes/sec.

ARCHITECTURE (continued)

VIDEO CONTROLLERS — Two regions allow the user to simultaneously work with 2 capture regions, 2 display regions, or 1 capture and 1 display region.

PARALLEL PROCESSORS — The Parallel Processors (ADSP) are 32-bit fixed-point DSPs that are optimized for fast pixel processing and DCT transforms used in compression algorithms. Optimizations include: splittable 16 x 16 multiplier, 3-input splittable ALU, ability to perform mixed Boolean and Arithmetic operations in same clock cycle.

NOMENCLATURE

SMJ	320	C80	HFH	M	50
SMJ = QML Process SM = Mil Temp.	DSP Family	Device	Package	Military (-55°C - 125°C) HFH = Ceramic Quad Flat Pack GF = Ceramic Pin Grid Array	Speed = 50 MHz

TOOLS SUPPORT

Part Number	Description
TMDX3240680	C8x XDS510WS Emulator S/W/Debugger
TMDS00510	(PC) XDS510 Emulator Card+Cable
TMDX3240180	(PC) C8x XDS510 Emulator S/W/Debugger
TMDS00510WS	(SUN™) XDS510WS Emulator Box+Cable
TMDS3080002	JTAG Emulator/Cable
TMDX3240080	Emulator Porting Kit
TMDX3260080	(PC) C8x Software Development Board The SDB has its own emulation s/w and hardware. The XDS510 ISA card is NOT needed with the SDB. XDS510 emulation S/W is NOT needed for the SDB.
TMDX3248555-67	(SUN) C8x SPARC™ software tool set includes: C Compiler/Assembler/Linker, Simulator, Source Code examples Register Allocator & Code Compactor are available through TI Web Site
TMDX3248855-07	(PC) C8x software tool set includes: -C Compiler/Assembler/Linker, Register Allocator & Code Compactor

C80 Software or Hardware Name	Detailed Description
PP ALGEBRAIC ASSEMBLER	Converts assembly language to machine language.
MP ASSEMBLER	Converts assembly language to machine language.
PP LINKER	Combines object modules into a single executable object file, performs relocation and resolves external references.
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PP C COMPILER	Translates C source code into PP assembly source code.
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SIMULATOR	Software debugger tool that simulates the operation of the 320C80. Available for SUN SPARC Host only.
More follows	(PP = Parallel Processor, MP = Master Processor)

TOOLS SUPPORT (continued)

XDS-510	Hardware controller card for in-system emulation. XL suffix denotes IBM™ PC compatible card. WS suffix denotes workstation compatible card.
C8x Software Development Board	PCI add-in card providing all necessary hardware and software to acquire audio and video and to develop, benchmark and debug C8x code.
CODE COMPACTOR	Software tool to help developer parallelize C80 code.
REGISTER ALLOCATOR	Software tool to help developer parallelize C80 code.

LITERATURE INFORMATION

Hardware	Literature Number
'C80CD-ROM Complete User's Guide	SPRC001B
'C80 Data Sheet	SGUS025
'C8x Product Bulletin / Brochure	SPRT112B
Master Processor User's Guide	SPRU109A
Parallel Processor User's Guide	SPRU110A
Video Controller User's Guide	SPRU111A

Application Notes	
320C80 to SDRAM Application Note	SPRA055
320C80 to DRAM Application Note	SPRA056
Acoustic Echo Cancellation Algorithm on C80	SPRA063
320C80 Modified Goertzel Algo in DTMF	SPRA066
Vector Maximum Benchmark	SPRA087
Frame Buffer Application Report (VRAM)	SPRA156
Modified Goertzel Algorithm in DTMF	SPRA066
320C8X Fundamental Graphic Algorithms Book	SPRA069

The Fundamental Graphic Algorithms Book includes:

- TMS320C80 3X3 Matrix Multiply
- TMS320C80 4X4 Matrix Multiply
- TMS320C80 Draw Colored Trapezoid Commands
- TMS320C80 Draw Colored Lines
- TMS320C8X PP Integer and FP Math

Development Tools	
C Source Debugger's User's Guide	SPRU107A
Code Generation Tools User's Guide	SPRU108A
Multitasking Executive User's Guide	SPRU112A
PC-Based Tools Product Bulletin	SPRT123A
The TMS320 Third-Party Support Reference Guide	SPRU052C

Designer Notebook Pages www.ti.com/sc/docs/dsps/dnp/pdftoc.htm

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