Application Report
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Using DAC348x with Fault Detection and Auto Output Shut-off Feature

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ABSTRACT

The DAC348x is a family of high-speed, high-dynamic range, multi-channel, 16-bit digital-to-analog converter (DAC) devices. The devices include features such as 2x to 16x interpolation filters, FIFO, quadrature modulation correction circuits, and coarse and fine mixers. All of these features simplify the design of the complex transmitter design.

Moreover, the DAC348x family also includes a flexible set of fault-monitoring circuits that alert for possible malfunctions and shut off the DAC output upon catastrophic events. This application note mainly focuses on the DAC348x family clock and FIFO fault detector and auto shut-off feature. An understanding of the error checking algorithm of the alarms and the appropriate implementation for the system is provided in this report. In addition, the experiment setup procedures, configuration settings, and experiment results are provided for determining set up requirements.

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1 Acronyms

FIFO:	First-In-First-Out memory buffer
NCO:	numerically controlled oscillator
PA:	power amplifier
ISR:	interrupt service routine
DACCLK:	DAC sampling clock. This is the final DAC update rate (F_{DAC})
DATACLK:	clock used to latch the LVDS data input
T_{DTA}:	time delay from DATACLK gone to ALARM is HIGH
T_{DTOS}:	time delay from DATACLK gone to output shut-off
T_{DCA}:	time delay from DACCLK gone to ALARM is HIGH

2 Alarms Usage

The DAC348x family has a flexible set of fault-monitoring circuits that give alerts for possible malfunction scenarios. Refer to the types of alarms in Appendix A. All the alarm events can be accessed either through register config5 or through the ALARM pin with CMOS output. Clock alarms refer to the alarm when either DACCLK or DATACLK has been stopped. FIFO alarms refer to the alarms when there is a collision in the FIFO pointer or a collision event is close.

– *alarm_dacclk_gone*	Occurs when the DACCLK has been stopped
– *alarm_dataclk_gone*	Occurs when the DATACLK has been stopped
– *alarm_fifo_2away*	FIFO write and read pointers are within two addresses of each other
– *alarm_fifo_1away*	FIFO write and read pointers are within one address of each other
– *alarm_fifo_collision*	Write pointer and read pointer are equal to each other

Generally there are two main error checking algorithms in the system logic (that is, FPGA or ASIC): one is interrupt service routine (ISR) and the other is polling. ISR is adopted when the alarm is classified as critical and requires the system processor, like FPGA or ASIC, to quickly respond to the alarm. Once the alarm is triggered, the system will be hardware interrupted to process the alarm event first, perform emergency treatment to protect the whole system immediately, correct the error condition, report to system logic the type of alarm that has occurred, and then clear the alarm, once the error has been fixed.

Prioritize the alarms by masking the less important alarms at config7. The more important alarms will generate a trigger signal for ISR upon an alarm event. These alarms must be unmasked.

Polling is used for minor alarms which may not severely affect the function of the system. The system logic device can check the status of alarm signals from time to time, and when the alarm is set, the system logic device will respond to the alarm event. The end user can decide which error checking algorithm to use based on their end-system requirement. One thing to note is that the alarms have memory to ensure no alarm messages are missed. When an error triggers the alarm, the alarm will not be cleared unless the user writes zero to clear the corresponding alarm, even if the error is settled. Therefore, every time alarm register config5 is read, clear the alarm by writing all zeros.

Figure 1 depicts the FIFO function block diagram. As for transmitter system applications, the alarms for missing DATACLK and DACCLK are critical. For example, for the transmitter system once DATACLK is gone, the FIFO read pointer will cycle through all the previous data, potentially causing high RMS output or significant spurs at the output. Another example is when DACCLK is gone, the output will cease and remain at the last value because the DAC decoder logic can no longer update the value.

In the entire transceiver system, the power amplifier (PA) accounts for most of the build cost. Therefore, protecting the PA from failure is the top priority for most system designers. The PA is fragile to two types of signals: continuous high RMS signal and large transient spurs. Both of these problems could be caused by clock stoppage or FIFO collision.

In order to assist designers with PA protection implementation in their system, the DAC348x family has an automatic shut-off feature which can be adopted in ISR. In order to prevent unexpected DAC outputs from propagating into the transmit signal chain, the clock alarms and alarm_fifo_collision alarms can be set in config2 to shut-off the DAC output automatically, regardless of the state of TXENABLE or sif_txenable. When DATACLK is gone, the DAC will output mid code. When DACCLK is gone, the DAC will output the last data point.

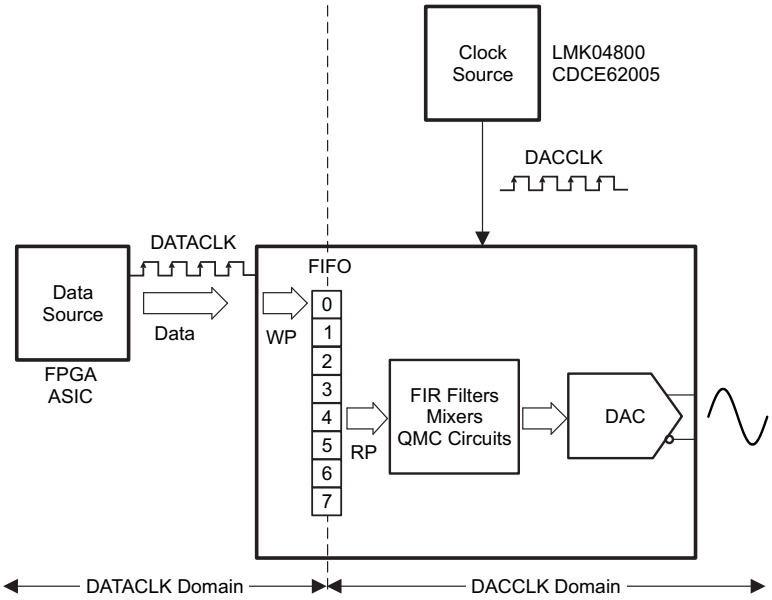

Figure 1. DAC348x Family FIFO Function

2.1 Implementation of the Alarm Monitoring

System setup procedure for the alarm monitoring is as follows:

1. Power up the device using the recommended power-up sequence.
   - Clear all the alarms in config5 by setting them to 0. Due to the memory of the alarm register, some alarms may have been triggered during the transient state of powering up the device. The device may not necessarily have issues at steady state but the alarms need to be cleared to reflect the latest condition.
   - Check for error information and fix the error according to alarm status. Once the system is ready, resynchronize the FIFO and clock divider. Clear up the alarm signal by writing all zeroes in register config5.
   - Prioritize the alarms for ISR based on system requirements. Unmask those alarms that will generate a hardware interrupt through the ALARM pin in config7.
   - Enable automatic DAC shut-off in register config2.
2. In case of a critical alarm event (the alarms are unmasked based on priority), the ALARM pin will trigger the hardware interrupt. If automatic DAC shut-off has been enabled, the DAC outputs will be disabled.
   - Pull TXENABLE or Sif_txenable LOW. This ensures a controlled transmission upon system recovery.
   - Read register config5 to determine which alarm triggered the ALARM pin.
   - Correct the error condition and re-synchronize the FIFO and clock divider.
   - Clear the alarms in config5.
   - Re-read config5 to ensure the alarm event has been corrected.
   - Keep clearing and reading config5 until no error is reported.
   - Pull TXENABLE or Sif_enable HIGH to enable transmission.

2.2 Experiment Setup Procedures

The goal of the experiment is to measure the output shut-off response time when either DATACLK or DACCLK is stopped, respectively.

The devices under test are DAC34H84, DAC3484, and DAC3482. Since interpolation filters and NCO blocks add latency to the digital path, the effect of the output shutoff time versus digital block latency can be observed by providing the test cases of these digital blocks. Therefore, the test variables are interpolation factor and NCO state.

The experiment setup procedure is as follows:

1. Set the DAC sampling rate at 400 MSPS in order to measure the response time more accurately. A wider clock period yields more resolution on time measurement. Set the interpolation rate at 1x, 2x, 4x, 8x, 16x, respectively.
2. Use High Speed Data Capture and Pattern Generation Platform TSW1400 to generate a single tone signal and load the signal pattern to the DAC. The test setup block diagram is shown in Figure 2.

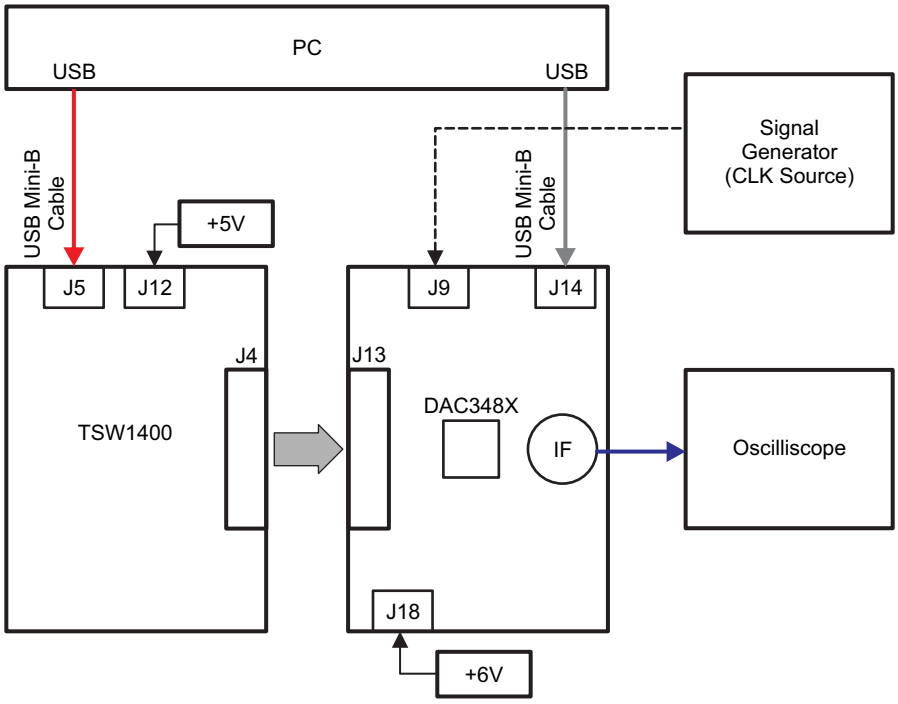

Figure 2. Test Setup Block Diagram for TSW1400 and DAC348x Family

3. Configure the DAC348x family to set interpolation, NCO, and other registers using the GUI. Unmask the DACCLK-gone alarm and DATACLK-gone alarm to generate a hardware interrupt through the ALARM pin in config7. Enable FIFO-collision, DATACLK-gone, and DACCLK-gone automatic DAC shut-off in register config2. In this test, the ALARM output triggers on a low-to-high transition. This can be configured in config0 bit3.

4. Monitor the output ALARM pin, DATACLK and DACCLK using a Tektronix 4-channel, 3-GHz, Digital Oscilloscope. Before testing, calibrate and deskew each probe to minimize the delay difference among the probes. Figure 3 shows the probing parameter of the DAC348x family. In this setup, Channel A is the output of the DAC348x family. To avoid additional energy time constant introduced by the transformer, resistive termination on the DAC output is adopted.

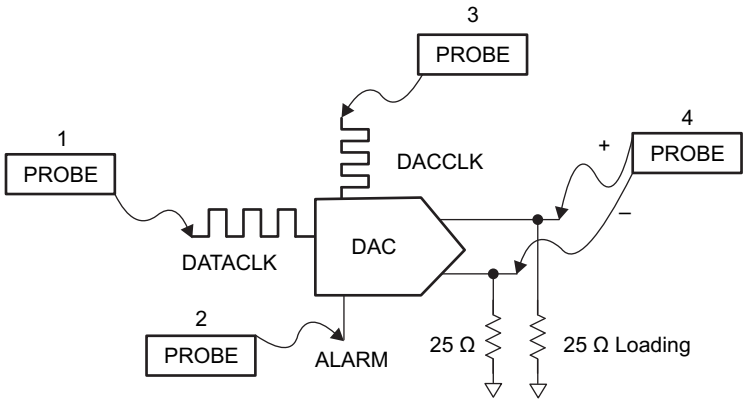

Figure 3. Probing Parameter of the DAC348x Family, DATACLK, DACCLK, Output, and ALARM

5. Select ALARM signal as the trigger signal for the oscilliscope. When testing for missing DATACLK, generate a firmware that the DATACLK can be stopped by pressing the **SW4** button in the TSW1400. When testing for missing DACCLK, disable DACCLK in the CDCE62005 control tab of the DAC348x GUI to shut off DACCLK.

2.3 Experiment Results

2.3.1 DAC34H84 Board

DAC sampling rate is 400 MSPS, so the DATACLK will be 400 MHz, 200 MHz, 100 MHz, 50 MHz, and 25 MHz when the interpolation rate is 1x, 2x, 4x, 8x, and 16x, respectively. The baseband signal generated from TSW1400 is a 5-MHz single tone.

2.3.1.1 When DATACLK Is Gone:

Figure 4 depicts the test snapshot of DAC34H84, 4x, NCO on. The NCO frequency is 5 MHz. The black waveform (#1) is the DATACLK signal, the green waveform (#2) is the ALARM signal, and the blue waveform (#4) is the output signal. Based on the results, after the DATACLK is gone, the ALARM signal becomes HIGH 142 ns afterwards. After the ALARM signal triggers, the DAC outputs mid-code 30 ns afterwards.

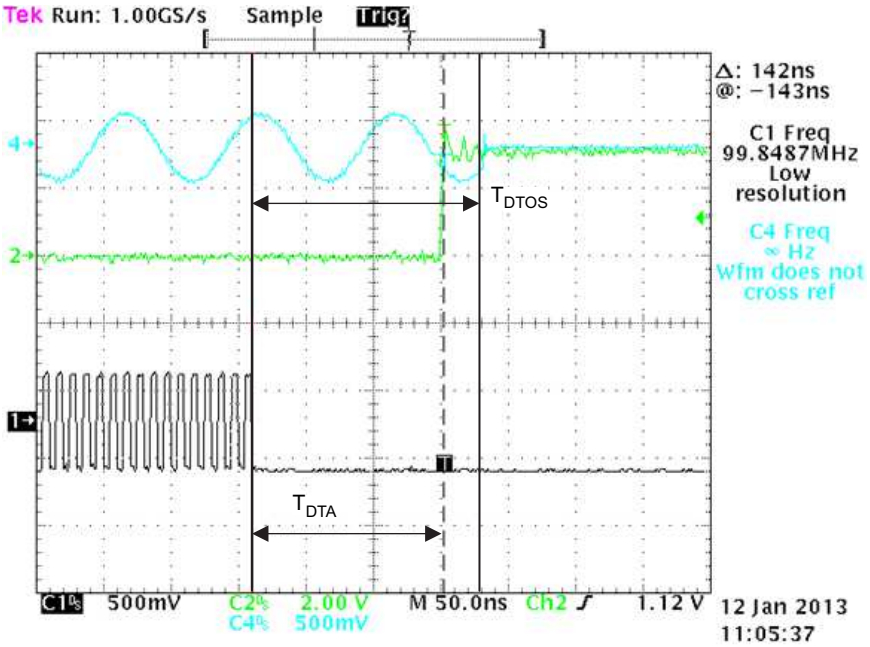

Figure 4. Snapshot of ALARM, DATACLK, and Output Signal of DAC34H84 when DATACLK Is Gone

Table 1 lists DAC34H84 ALARM and output response time versus interpolation rate when DATACLK is gone, NCO off.

Table 1. DAC34H84 ALARM and Output Response Time when DATACLK Is Gone, NCO Off

DAC34H84 NCO Off	DATACLK T = 2.5 ns	DATACLK T = 5 ns	DATACLK T = 10 ns	DATACLK T = 20 ns	DATACLK T = 40 ns
Interpolation rate	1x	2x	4x	8x	16x
T_{DTA}	35 ns 14 dataclk 14 dacclk	55 ns 11 dataclk 22 dacclk	140 ns 14 dataclk 56 dacclk	254 ns 13 dataclk 102 dacclk	494 ns 12 dataclk 198 dacclk
T_{DTOS}	T_{DTA} + 30 ns = 65 ns	T_{DTA} + 30 ns = 85 ns	T_{DTA} – 46 ns = 94 ns	T_{DTA} – 28 ns = 226 ns	T_{DTA} + 32 ns = 526 ns

Table 2 lists DAC34H84 ALARM and output response time versus interpolation rate when DATACLK is gone, NCO on, NCO frequency is 5 MHz.

Table 2. DAC34H84 ALARM and Output Response Time when DATACLK Is Gone, NCO On

DAC34H84 NCO On	DATACLK T = 2.5 ns	DATACLK T = 5 ns	DATACLK T = 10 ns	DATACLK T = 20 ns	DATACLK T = 40 ns
Interpolation rate	1x	2x	4x	8x	16x
T_{DTA}	35 ns 14 dataclk 14 dacclk	66 ns 13 dataclk 26 dacclk	142 ns 14 dataclk 57 dacclk	276 ns 14 dataclk 110 dacclk	454 ns 11 dataclk 182 dacclk
T_{DTOS}	T_{DTA} + 29 ns = 64 ns	T_{DTA} + 44 ns = 110 ns	T_{DTA} + 30 ns = 172 ns	T_{DTA} + 31 ns = 307 ns	T_{DTA} + 32 ns = 486 ns

From the results, T_{DTA} (time delay from DATACLK gone to ALARM HIGH signal) increases as the interpolation increases, but remains approximately 13 periods of DATACLK. T_{DTOS} equals the response time of the ALARM signal plus approximately 30 ns (12 periods of DACCLK) even if DATACLK changes. The 12 periods of DACCLK are needed to update the output. When NCO is on, the response time does not increase significantly. Moreover, due to design implementation, T_{DTOS} could be less than T_{DTA}. This is also beneficial in terms of reducing response time.

2.3.1.2 When DACCLK Is Gone:

Figure 5 depicts the test snapshot of DAC34H84, 4x, NCO on, when DACCLK is gone. The NCO frequency is 5 MHz. The black waveform (#1) is the DACCLK signal, the green waveform (#2) is the output signal, and the red waveform (#3) is the ALARM signal. Based on the results, after DACCLK is gone, the DAC output will stop and hold at the last value immediately. This is because the output decoder runs in the DACCLK domain, and once the DACCLK is stopped, the logic can no longer update the output code.

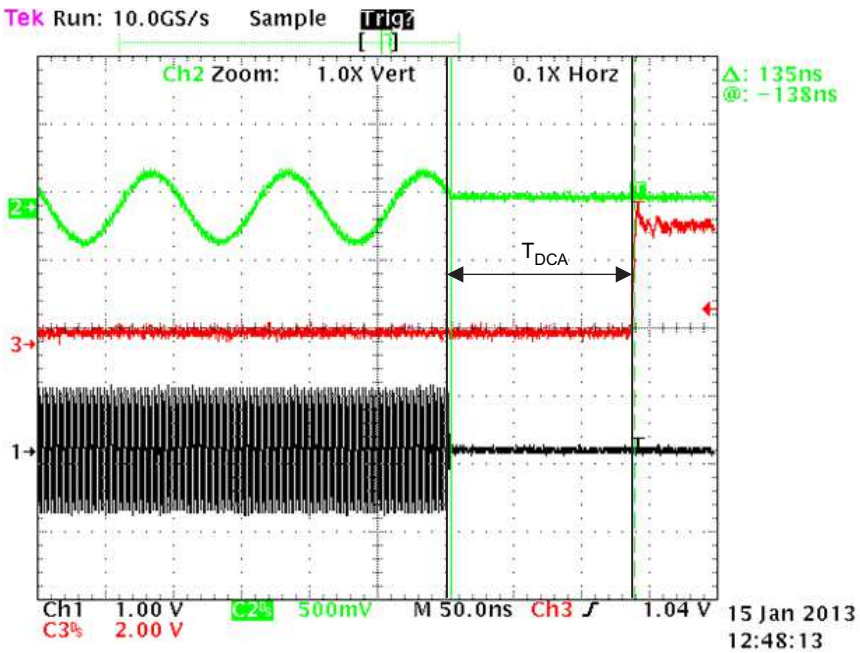

Figure 5. Snapshot of ALARM, DACCLK, and Output Signal of DAC34H84 when DACCLK Is Gone

Table 3 lists DAC34H84 ALARM and output response time versus interpolation rate when DACCLK is gone, NCO off.

Table 3. DAC34H84 ALARM Response Time when DACCLK Is Gone, NCO Off

DAC34H84 NCO OFF	DATACLK T = 2.5 ns	DATACLK T = 5 ns	DATACLK T = 10 ns	DATACLK T = 20 ns	DATACLK T = 40 ns
Interpolation rate	1x	2x	4x	8x	16x
T_{DCA}	37 ns 15 dataclk 15 dacclk	59 ns 12 dataclk 24 dacclk	109 ns 11 dataclk 44 dacclk	261 ns 13 dataclk 104 dacclk	470 ns 12 dataclk 188 dacclk

Table 4 lists DAC34H84 ALARM and output response time versus interpolation rate when DACCLK is gone, NCO on, NCO frequency is 5 MHz.

Table 4. DAC34H84 ALARM Response Time when DACCLK Is Gone, NCO On

DAC34H84 NCO ON	DATACLK T = 2.5 ns	DATACLK T = 5 ns	DATACLK T = 10 ns	DATACLK T = 20 ns	DATACLK T = 40 ns
Interpolation rate	1x	2x	4x	8x	16x
T_{DCA}	43 ns 17 dataclk 17 dacclk	65.5 ns 13 dataclk 26 dacclk	135 ns 14 dataclk 54 dacclk	274 ns 14 dataclk 110 dacclk	422 ns 11 dataclk 169 dacclk

From the test results above, the T_{DCA} (time from DACCLK gone to ALARM HIGH) increases when the interpolation rate increases. It is related with DATACLK. After approximately 14 periods of DATACLK, the ALARM signal will be HIGH. When NCO is on, the response time does not increase significantly.

2.3.2 DAC3484 Board

Since the DAC3484 interleaves 4 channel data into a single 16-bit bus, the data transfer requires two DATACLK cycles to latch all four channels in DDR fashion. Therefore, the maximum data rate is 312.5 MSPS. For the 1x interpolation test case, the DAC sampling rate is set to 200 MSPS to avoid exceeding the limit.

2.3.2.1 When DATACLK Is Gone:

Table 5 and Table 6 list the DAC3484 ALARM and output response time when DATACLK is gone with NCO off and on, respectively. NCO frequency is 5 MHz.

Table 5. DAC3484 ALARM and Output Response Time when DATACLK Is Gone, NCO Off

DAC3484 NCO OFF	DATACLK T = 2.5 ns	DATACLK T = 2.5 ns	DATACLK T = 5 ns	DATACLK T = 10 ns	DATACLK T = 20 ns
Interpolation rate	1x(1)	2x	4x	8x	16x
T_{DTA}	58 ns 23 dataclk 23 dacclk	59 ns 24 dataclk 47 dacclk	108 ns 22 dataclk 87 dacclk	232 ns 23 dataclk 186 dacclk	498 ns 25 dataclk 398 dacclk
T_{DTOS}	T_{DTA} + 59 ns = 117 ns	T_{DTA} + 32 ns = 91 ns	T_{DTA} + 31 ns = 139 ns	T_{DTA} + 30 ns = 262 ns	T_{DTA} + 30 ns = 528 ns

(1) Sampling rate is 200 MSPS

Table 6. DAC3484 ALARM and Output Response Time when DATACLK Is Gone, NCO On

DAC3484 NCO ON	DATACLK T = 2.5 ns	DATACLK T = 2.5 ns	DATACLK T = 5 ns	DATACLK T = 10 ns	DATACLK T = 20 ns
Interpolation rate	1x(1)	2x	4x	8x	16x
T_{DTA}	68 ns 27 dataclk 27 dacclk	70 ns 28 dataclk 56 dacclk	111 ns 22 dataclk 88 dacclk	213 ns 21 dataclk 170 dacclk	458 ns 23 dataclk 366 dacclk
T_{DTOS}	T_{DTA} + 59 ns = 127 ns	T_{DTA} + 31 ns = 101 ns	T_{DTA} + 31 ns = 142 ns	T_{DTA} + 30 ns = 243 ns	T_{DTA} + 30 ns = 488 ns

(1) Sampling rate is 200 MSPS

Based on the test results, the T_{DTA} (time delay from DATACLK gone to ALARM is HIGH) increases as the interpolation increases, but remains around 23 periods of DATACLK. The T_{DTOS} (time delay from DATACLK gone to output shut-off) equals T_{DTA} plus around 30 ns (12 periods of DACCLK) in 2x, 4x, 8x, and 16x cases, even if DATACLK changes. In the 1x case, the T_{DTOS} is the response time of the ALARM signal plus 59 ns, which is 11.8 periods of DACCLK. The 12 periods of DACCLK is needed to update the output. When NCO is on, the response time does not increase significantly.

2.3.2.2 When DACCLK Is Gone:

Table 7 and Table 8 list the DAC3484 ALARM and output response time when DACCLK is gone with NCO off and on, respectively. NCO frequency is 5 MHz.

Table 7. DAC3484 ALARM Response Time when DACCLK Is Gone, NCO Off

DAC3484 NCO OFF	DATACLK T = 2.5 ns	DATACLK T = 2.5 ns	DATACLK T = 5 ns	DATACLK T = 10 ns	DATACLK T = 20 ns
Interpolation	1x(1)	2x	4x	8x	16x
T_{DCA}	62 ns 25 dataclk 25 dacclk	65 ns 26 dataclk 52 dacclk	109 ns 22 dataclk 88 dacclk	243 ns 24 dataclk 194 dacclk	430 ns 22 dataclk 344 dacclk

(1) Sampling rate is 200 MSPS

Table 8. DAC3484 ALARM Response Time when DACCLK Is Gone, NCO On

DAC3484 NCO ON	DATACLK T = 2.5 ns	DATACLK T = 2.5 ns	DATACLK T = 5 ns	DATACLK T = 10 ns	DATACLK T = 20 ns
Interpolation	1x(1)	2x	4x	8x	16x
T_{DCA}	72 ns 29 dataclk 29 dacclk	73 ns 29 dataclk 58 dacclk	144 ns 29 dataclk 115 dacclk	250 ns 25 dataclk 200 dacclk	400 ns 20 dataclk 320 dacclk

(1) Sampling rate is 200 MSPS

Based on the test results, T_{DCA} (time delay from DACCLK gone to ALARM is HIGH) increases when the interpolation rate increases. After approximately 24 periods of DATACLK, the ALARM signal will be triggered. For DAC34H84, it takes 14 periods of DATACLK to trigger ALARM. However, the time delay is almost the same, the DAC3483 data transfer requires two DATACLK cycles when compared to DAC34H84 data transfer. When NCO is on, the response does not increase significantly.

2.3.3 DAC3482 Board

2.3.3.1 When DATACLK Is Gone:

Table 9 and Table 10 list DAC3482 ALARM and output response time when DATACLK is gone with NCO off and on, respectively. NCO frequency is 5 MHz.

Table 9. DAC3482 ALARM and Output Response Time when DATACLK Is Gone, NCO Off

DAC3482 NCO OFF	DATACLK T = 2.5 ns	DATACLK T = 5 ns	DATACLK T = 10 ns	DATACLK T = 20 ns	DATACLK T = 40 ns
Interpolation	1x	2x	4x	8x	16x
T_{DTA}	64 ns 26 dataclk 26 dacclk	130 ns 26 dataclk 52 dacclk	224 ns 22 dataclk 90 dacclk	456 ns 23 dataclk 182 dacclk	772 ns 19 dataclk 309 dacclk
T_{DTOS}	T_{DTA} + 31.5 ns = 95.5 ns	T_{DTA} + 31 ns = 161 ns	T_{DTA} + 30 ns = 254 ns	T_{DTA} + 30 ns = 486 ns	T_{DTA} + 30 ns = 802 ns

Table 10. DAC3482 ALARM and Output Response Time when DATACLK Is Gone, NCO On

DAC3482 NCO ON	DATACLK T = 2.5 ns	DATACLK T = 5 ns	DATACLK T = 10 ns	DATACLK T = 20 ns	DATACLK T = 40 ns
Interpolation	1x	2x	4x	8x	16x
T_{DTA}	64 ns 26 dataclk 26 dataclk	130 ns 26 dataclk 52 dacclk	266 ns 27 dataclk 106 dacclk	454 ns 23 dataclk 182 dacclk	930 ns 24 dataclk 372 dacclk
T_{DTOS}	T_{DTA} + 31.5 ns = 95.5 ns	T_{DTA} + 31 ns = 161 ns	T_{DTA} + 32 ns = 298 ns	T_{DTA} + 30 ns = 484 ns	T_{DTA} + 30 ns = 960 ns

Based on the results, the T_{DTA} (time delay from DATACLK gone to ALARM is HIGH) increases as the interpolation increases, but remains approximately 23 periods of DATACLK. The T_{DTOS} (time delay from DATACLK gone to output shut-off) equals T_{DTA} plus approximately 30 ns (12 periods of DACCLK) even if DATACLK changes. The 12 periods of DACCLK is needed to update the output. When NCO is on, the response time does not increase significantly.

2.3.3.2 When DACCLK Is Gone:

Table 11 and Table 12 list the DAC3482 ALARM and output response time when DACCLK is gone with NCO off and on, respectively. NCO frequency is 5 MHz.

Table 11. DAC3482 ALARM and Output Response Time when DACCLK Is Gone, NCO Off

DAC3482 NCO OFF	DATACLK T = 2.5 ns	DATACLK T = 5 ns	DATACLK T = 10 ns	DATACLK T = 20 ns	DATACLK T = 40 ns
Interpolation	1x	2x	4x	8x	16x
T_{DCA}	77 ns 31 dataclk 31 dacclk	106 ns 21 dataclk 42 dacclk	236 ns 24 dataclk 94 dacclk	434 ns 22 dataclk 174 dacclk	935 ns 23 dataclk 374 dacclk

Table 12. DAC3482 ALARM and Output Response Time when DACCLK Is Gone, NCO On

DAC3482 NCO ON	DATACLK T = 2.5 ns	DATACLK T = 5 ns	DATACLK T = 10 ns	DATACLK T = 20 ns	DATACLK T = 40 ns
Interpolation	1x	2x	4x	8x	16x
T_{DCA}	65.5 ns 26 dataclk 26 dacclk	134 ns 27 dataclk 54 dacclk	210 ns 21 dataclk 84 dacclk	518 ns 26 dataclk 207 dacclk	1.025 µs 26 dataclk 410 dacclk

Based on the results, T_{DCA} (time delay from DACCLK gone to ALARM is HIGH) increases when interpolation rate increases. After approximately 24 periods of DATACLK, the ALARM signal will be high. When NCO is on, the response time does not increase significantly.

3 Conclusion

Based on the test results, the DAC348x family has a prompt response time when a catastrophic event occurs. As for the DAC34H84, in the DATACLK-gone case, it takes approximately 13 periods of DATACLK to trigger the ALARM pin, and after the ALARM pin is set to HIGH, it takes approximately another 12 periods of DACCLK to switch off the output to mid-code. In DACCLK-gone case, it takes 13 periods of DATACLK to trigger the ALARM signal. In a real application, the DACCLK of the DAC348X family can reach up to 1.25 GSPS, therefore, 12 periods of DACCLK only takes a few nanoseconds to shut off the DAC output, 13 periods of DATACLK only takes a hundred nanoseconds, consider the cases for the maximum interpolation rates. For DAC3484 and DAC3482, situations are similar.

When the output becomes distorted, the PA may become damaged if the output is not shut off in time. Based on the test results, the T_{DTA} and T_{DTOS} response time is far less than a microsecond. Therefore, the DAC348x family provides prompt and reliable solutions to protect the PA signal chain in the transmitter system.

4 Reference

1. *DAC34H84 datasheet* (SLAS751).
2. *DAC3484 datasheet* (SLAS749).
3. *DAC3482 datasheet* (SLAS748).
4. *TSW1400 Pattern Generators* (SLWU082).
5. Synchronization and Device Configuration of the DAC348x (SLAA584).

Appendix A

Alarm types in register config5:

Zero check alarm	
alarm_from_zerochk	This occurs when the FIFO write pointer has an all zeros pattern. Since the write pointer is a shift register, all zeros will cause the input point to be stuck until the next sync event. When this happens, a sync to the FIFO block is required.
FIFO alarms	
alarm_from_fifo	Occurs when there is a collision in the FIFO pointers or a collision event is close
alarm_fifo_2away	Pointers are within two addresses of each other
alarm_fifo_1away	Pointers are within one address of each other
alarm_fifo_collision	Pointers are equal to each other
Clock alarms	
clock_gone	Occurs when either the DACCLK or DATACLOCK have been stopped
alarm_dacclk_gone	Occurs when the DACCLK has been stopped
alarm_dataclk_gone	Occurs when the DATACLK has been stopped
Pattern checker alarm	
alarm_from_iotest	Occurs when the input data pattern does not match the pattern key
PLL alarm	
alarm_from_pll	Occurs when the PLL is out of lock
Parity alarms	
alarm_Aparity	In dual parity mode, alarm indicating a parity error on the A word. In single parity mode, alarm on the 32-bit data captured on the rising edge of DATACLKP/N.
alarm_Bparity	In dual parity mode, alarm indicating a parity error on the B word. In single parity mode, alarm on the 32-bit data captured on the falling edge of DATACLKP/N.
alarm_Cparity	In dual parity mode, alarm indicating a parity error on the C word
alarm_Dparity	In dual parity mode, alarm indicating a parity error on the D word

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