Application Note

TAX5X1X Synchronous Sample Rate Conversion

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ABSTRACT

Sample Rate Converters (SRC) are used whenever there is a need to convert an input sampling frequency to a different sampling rate. This application note introduces the TAX5X1X Synchronous SRC (SSRC), the supported sampling ratios, the different modes and follow by some use case examples.

SSRC is supported in TAC5212, TAC5211,TAC5112, TAC5111, TAD5212, TAD5112, and TAA5212 devices.

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Trademarks

1 Introduction

In a system where different sample rates are running, there are times a Sampling Rate Converter is needed to convert one sampling rate to another. The idea of SRC is using the sequence of discrete time sampled at a certain input sampling frequency, and with some conversion technique, create a new sequence of discrete sampled at a different rate from the input. There are Synchronous and Asynchronous converters. Synchronous converters are those with a known input sampling frequency and conversion factor, where as Asynchronous converters are systems where the exact sampling frequencies are not known. The conversion process interpolates or decimates the input signal sampled at the input signal sampling rate to the desired signal at output sample rate. Figure 1-1 shows a Sampling Rate Converter model.

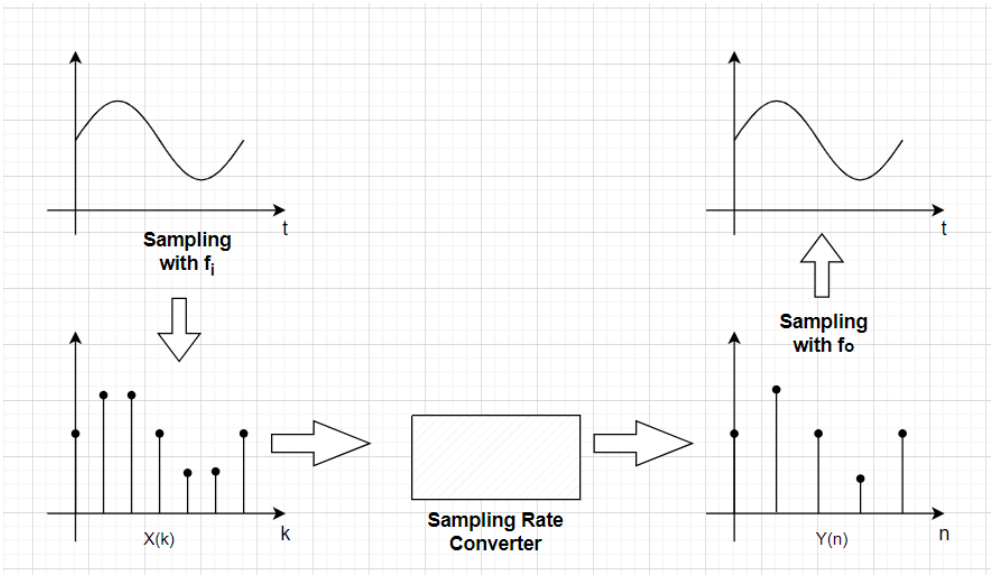

Figure 1-1. Sampling Rate Converter Model

2 TAX5X1X Audio Serial Interface

TAX5X1X Converter supports 2 independent Audio Serial Interface (ASI); Primary ASI (PASI) and Secondary ASI (SASI). Primary ASI bus has direct mapping to the external pins and Secondary ASI bus is mapped or muxed through General Purpose Input Output pins. This is shown in the diagram below for TAX5212, TAX5112, TAX5211, TAX5111 device family and TAX5412, TAX5312, TAX5411, TAX5311 family.

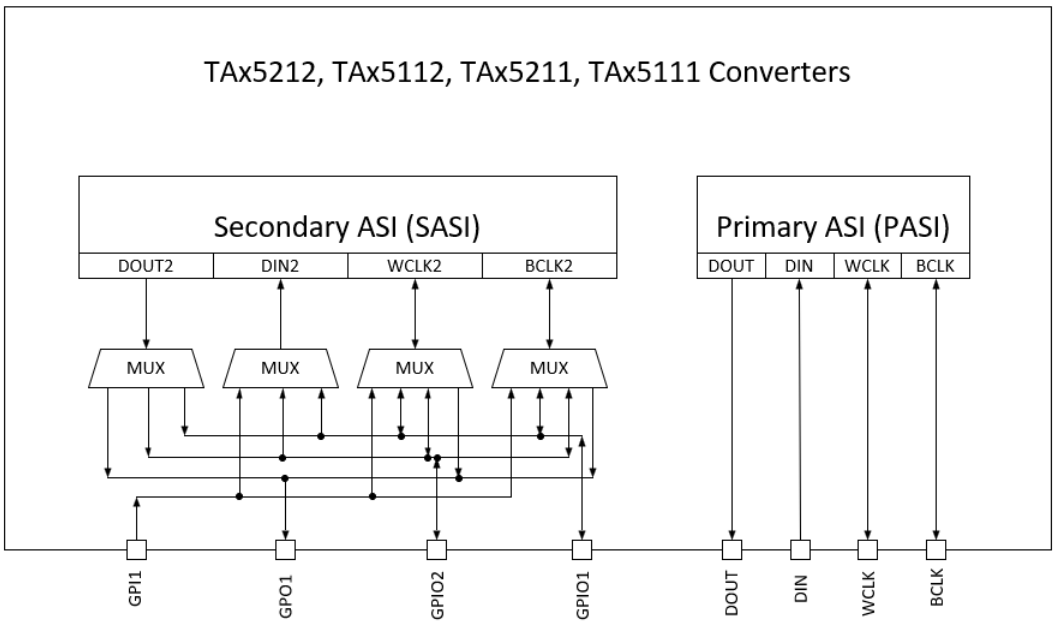

Figure 2-1. TAX511X and TAX521X ASI Mapping

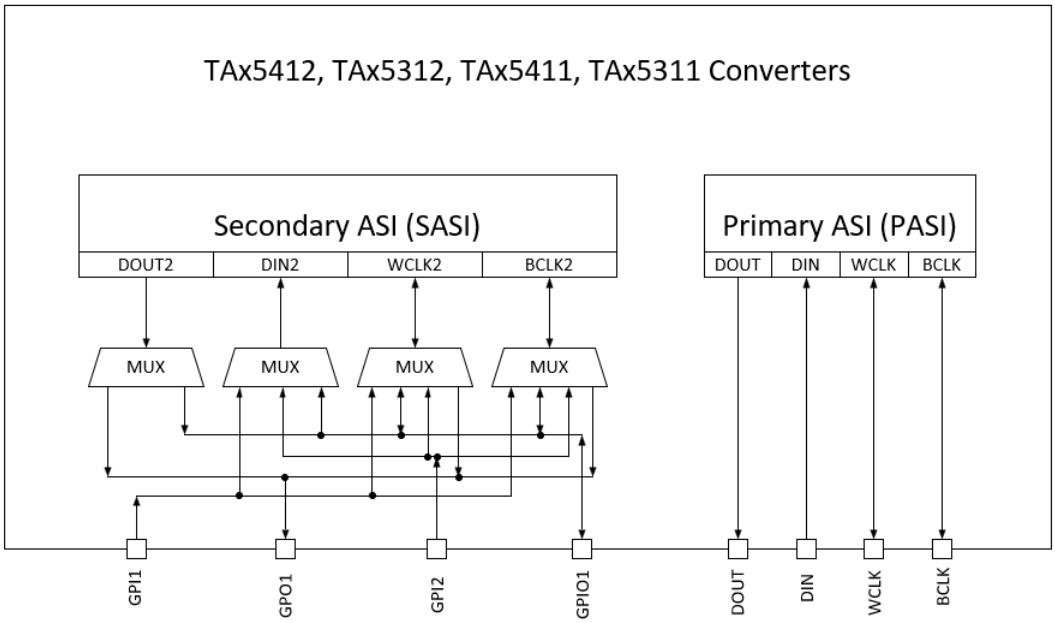

Figure 2-2. TAX531X and TAX541X ASI Mapping

3 TAX5X1X Synchronous Sampling Rate Converter

TAC5X1X supports synchronous sampling rate converter in ADC and DAC with ratios between the primary and secondary interface shown in Table 3-1. Ratio which is not listed in the table are not supported. Different sampling rates from the table are supported, but the ratio between the PASI and SASI rates must adhere to the ratio listed in the table as interpolators and decimators are designed according to the ratio.

Table 3-1. SRC Supported Ratio

Secondary ASI Rate (KHz)	Primary ASI Rate (KHz)						
	8	12	16	24	32	48	96
8	1 : 1	3 : 2	2 : 1	3 : 1	Not Supported	6 : 1	Not Supported
12	2 : 3	1 : 1	4 : 3	2 : 1	Not Supported	4 : 1	Not Supported
16	1 : 2	3 : 4	1 : 1	3 : 2	2 : 1	3 : 1	6 : 1
24	1 : 3	1 : 2	2 : 3	1 : 1	4 : 3	2 : 1	4 : 1
32	Not Supported	Not Supported	1 : 2	3 : 4	1 : 1	3 : 2	3 : 1
48	1 : 6	1 : 4	1 : 3	1 : 2	2 : 3	1 : 1	2 : 1
96	Not Supported	Not Supported	1 : 6	1 : 4	1 : 3	1 : 2	1 : 1

In a system with TAC5x1x device, when different sampling rates are detected in PASI and SASI with rates listed in the table above, SRC is automatically enabled without the need of setting SRC_EN bit in B0_P1_R23_D[7] to "1". Sampling rates which are not in the specified list but having the supported ratio are required to set SRC_EN bit to "1" to enable SRC and to set the ratio accordingly in B0_P1_R24_D[5:0]. SRC can be disabled through register B0_P1_R23_D[7] if needed.

SRC in the TAC5X1X has 2 possible modes:

- Auto-detect Mode: TAC5x1x detects the highest sampling rate (Fs) of the 2 ASI regardless that it is from the Primary ASI or Secondary ASI and consider the higher rate as the main Fs and the lower rate as auxiliary Fs. This is the default mode and TAC5X1X uses higher resources (MIPS) as decimator or interpolator runs at higher rate. The auto-detect mode can be disabled through register B0_P1_R23_D[6].
- Custom Mode: User decides which ASI; Primary or Secondary sampling frequency to be the main Fs for SRC. This is where lower rate is set as main Fs. This is used where higher use of resources are a concern, but it has disadvantage of losing information on Rx path.

3.1 ADC Sampling Rate Conversion

An overview of ADC SRC flow in default mode is shown in the block diagram below where an ADC input running at higher sampling rate (main Fs) is converted to a lower sampling rate (auxiliary Fs) and be available on the other ASI. User has the choice to choose Primary ASI or Secondary ASI with the higher or lower rate interface. The flow applies also when main Fs is chosen from the lower rate thus SRC is converting from lower to higher rate.

The SRC process has option to mix with a DAC loopback data for example adding audio data from host to the recorded voice data.

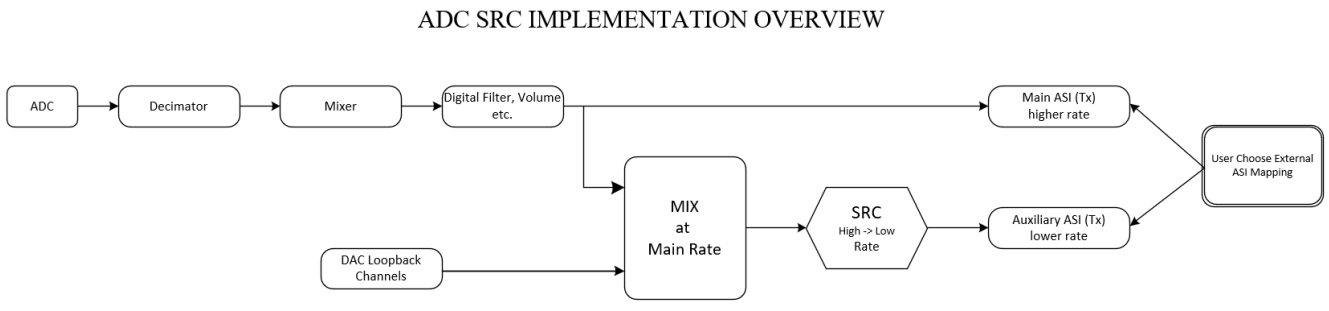

Figure 3-1. TAx5x1x ADC SRC Overview - Default Mode

Users can watch the levels when mixing, set the coefficients so the output does not exceed the maximum allowed as higher level causes clipping or distortion. The mixer output levels are defined by the following equations.

$$\begin{aligned} Out1 &= ADC\ \ Ch1\ \ Level*(1-Coeff) + DAC\ \ Loopback\ \ 1\ \ Level*Coeff \\ Out2 &= ADC\ \ Ch2\ \ Level*(1-Coeff) + DAC\ \ Loopback\ \ 2\ \ Level*Coeff \end{aligned} \quad (1)$$

For ADC mixer, the equation to set the mixing coefficients is given below where *w* represents the weight or scale of magnitude. For example w=0.5 represents half of the magnitude which translates into 'h40000000 in the 32-bit DAC mixer coefficients. The default on some of the path coefficients are 'h7FFFFFFF for the full scale magnitude of 1. The ADC mixer coefficients are configured through register page address 0x0A and register address from 0x08 to 0x47.

$$Coeff_{(hex)} = hex\left(2^{31} \times w\right) \quad (2)$$

For Digital Loopback (ADC to DAC) mixer, the equation to set the mixing coefficients is the same as the ADC mixer equation given above and is set through register page address 0x0A with register address from 0x48 to 0x67.

For ADC Auxiliary mixer, the equation to set the mixing coefficients is given below where *w* represents the weight or scale of magnitude. This Auxiliary ADC mixer coefficients are configured through register page address 0x0B and register address from 0x30 to 0x37.

$$Coeff_{(hex)} = hex\left(2^{30} \times w\right) \quad (3)$$

Examples for this ADC SRC are demonstrated in the subsequent section.

3.2 DAC Sampling Rate Conversion

In DAC SRC flow, the received ASI bus can pass through the Sampling Rate Converter first as mixing or muxing can run at the main Fs rate. The default DAC flow is shown in Figure 3-2 where 2 ASI digital inputs running at different sampling rates are mixed/muxed before any digital filtering, volume control, interpolation and DAC drivers. Similar to the ADC SRC, user can choose Primary ASI or Secondary ASI for the two rates. Figure 3-2 shows main Fs as the higher rate (default mode).

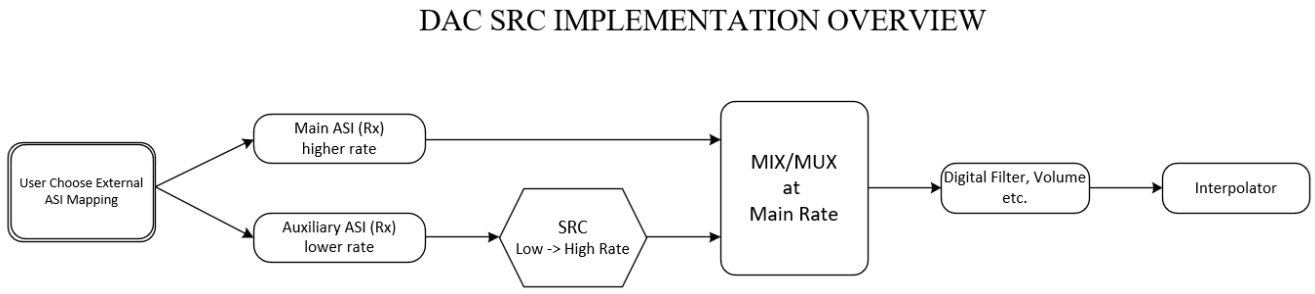

Figure 3-2. TAx5x1x DAC SRC Overview - Default Mode

Similar to ADC, the user needs to watch the levels when mixing 2 signals and the equation to set the mixing coefficients for DAC is given below where *w* represents the weight or scale of magnitude. For example w=0.5 represents half of the magnitude which translates into 'h2000 in the 16-bit DAC mixer coefficients. The default on some of the path coefficients are 'h4000 for the full scale magnitude of 1.

$$Coeff_{(hex)} = hex\left(2^{14} \times w\right) \quad (4)$$

The DAC mixer coefficients are configured through register page address 0x11 register address 0x08 to 0x47 for main ASI (higher rate interface) and for auxiliary ASI (lower rate), it's configured through register page address 0x11 register address 0x48 to 0x57.

For Side Chain DAC mixer, the coefficients are configured through register page address 0x11 and register address from 0x58 to 0x77 using the same coefficient Equation 4.

3.3 SRC Use Case Examples

The following are several use cases to demonstrate this SRC feature. On each of the use case, 2 Audio Precision APx555 are used and configured either as PASI or SASI and the rates are either 48 KHz or 16 KHz.

3.3.1 Default Mode (Main Fs - Higher rate)

Figure 3-3 is a block diagram for this use case with PASI and SASI mapping. PASI is running at 48 KHz and SASI is at 16 KHz. In this use case the analog (MIC) input sampled at main Fs and down-sampled with SRC to a lower rate for SASI TX. The PASI TX is available as well at 48 KHz. On the DAC side, SASI RX data can mix with PASI RX data prior to DAC output (Speaker).

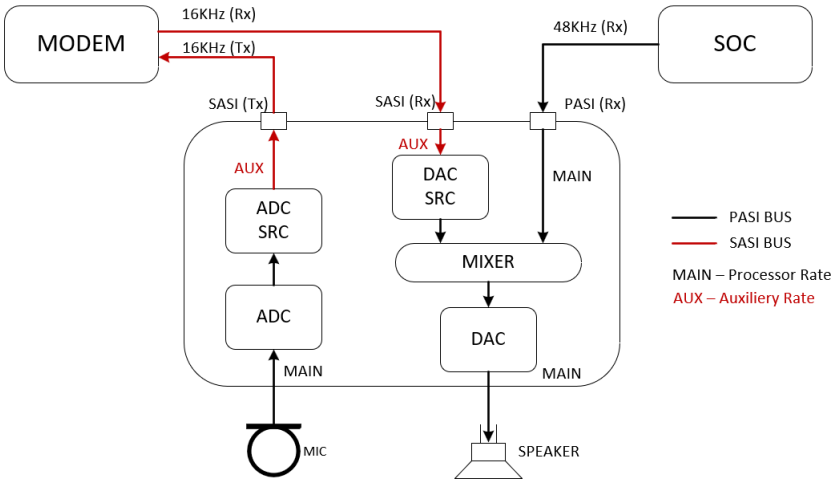

Figure 3-3. Default Mode Diagram

The Audio Precision APx555 configurations for PASI and SASI are shown below. In this test case mixer coefficients are kept to its default (full-sacle) and the input levels are adjusted as not to exceed the maximum allowed level for example -6dBrG instead of 0dBrG.

PASI APx555:

Generator:

Analog Output (MIC): 1KHz Sine, -6 dBrG (0dBrG = 2Vrms)

Analyzer:

Input 1: Digital audio for PASI Tx with Fs = 48 KHz, TDM, 32 bit depth

Input 2: Analog input from DAC output (Speaker)

SASI APx555:

Generator:

Digital Output: 750Hz Sine, -6 dBFS

Analyzer:

Input 1: Digital audio for SASI Tx with Fs = 16 KHz, TDM, 32 bit depth

```
##### PASI higher rate, default SRC Mode Testing ######
# Target Mode, TDM, 32-bit
# Primary and Secondary ASI, multiple of 48KHz Sampling
# GPIO2=Secondary FSYNC, GPIO1=Secondary BCLK, GPI1=Secondary DIN, GPO1=Secondary DOUT for 4x4
#
w a0 00 00        # Set page 0
w a0 01 01        # Software Reset
w a0 02 09        # Wake up with AVDD > 2v and all VDDIO level
w a0 0a 10        # GPIO1 as input
w a0 0b 10        # GPIO2 as input
w a0 0d 02        # GPI1 as input
```

```
w a0 0c 71        # GPO1 as Secondary DOUT
w a0 11 a2        # Enable PASI DIN and Set GPI2A as Secondary FSYNC and GPIO1 as Secondary BCLK
w a0 12 60        # Set GPI1A as Secondary DIN
w a0 18 00        # Enable both Primary and Secondary ASI as independent
w a0 34 40        # PASI BCLK is the input clock source
w a0 19 00        # 1 data input and 1 data output for PASI and SASI
w a0 1a 30        # PASI TDM, 32 bit format
w a0 1e 20        # PASI DOUT Ch1 on TDM slot 0
w a0 1f 21        # PASI DOUT Ch2 on TDM slot 1
w a0 28 20        # PASI DIN Ch1 on TDM slot 0
w a0 29 21        # PASI DIN Ch2 on TDM slot 1
w a0 00 03        # Set page 3
w a0 1a 30        # SASI TDM, 32 bit format
w a0 1e 20        # SASI DOUT Ch1 on TDM slot 0
w a0 1f 21        # SASI DOUT Ch2 on TDM slot 1
w a0 28 20        # SASI DIN Ch1 on TDM slot 0
w a0 29 21        # SASI DIN Ch2 on TDM slot 1
w a0 00 01        # Set page 1
w a0 17 00        # Default SR-Converter with auto-detect
w a0 18 00        # auto m:n ratio
w a0 2c 80        # Enable DAC ASI Mixer
w a0 00 00        # Set page 0
w a0 50 00        # ADC Ch1 diff input, 5KOhm, 2Vrms ac-coupled, audio band
w a0 55 00        # ADC Ch2 diff input, 5KOhm, 2Vrms ac-coupled, audio band
w a0 64 20        # Configure OUT1P/M as differential from DAC1
w a0 65 20        # Configure OUT1P LINEOUT 0dB audio band
w a0 66 20        # Configure OUT1M LINEOUT 0dB 2Vrms Differential
w a0 6b 20        # Configure OUT2P/M as differential from DAC2
w a0 6c 20        # Configure OUT2P LINEOUT 0dB audio band
w a0 6d 20        # Configure OUT2M LINEOUT 0dB 2Vrms Differential
w a0 76 cc        # Enable Input and Output Ch1 and Ch2
w a0 78 e0        # Power up ADC, DAC and MICBIAS
```

Test Results

The following plots show the results of the ADC output at SASI TX after SRC. The frequency response (FFT) ends at 8 KHz (Fs/2 of SASI rate of 16 KHz) as expected.

On Speaker output, the tone captured is the SASI RX tone of 750 Hz after SRC. PASI RX tone is muted in this case.

Figure 3-4 shows SASI TX 1 KHz tone from MIC input after SRC.

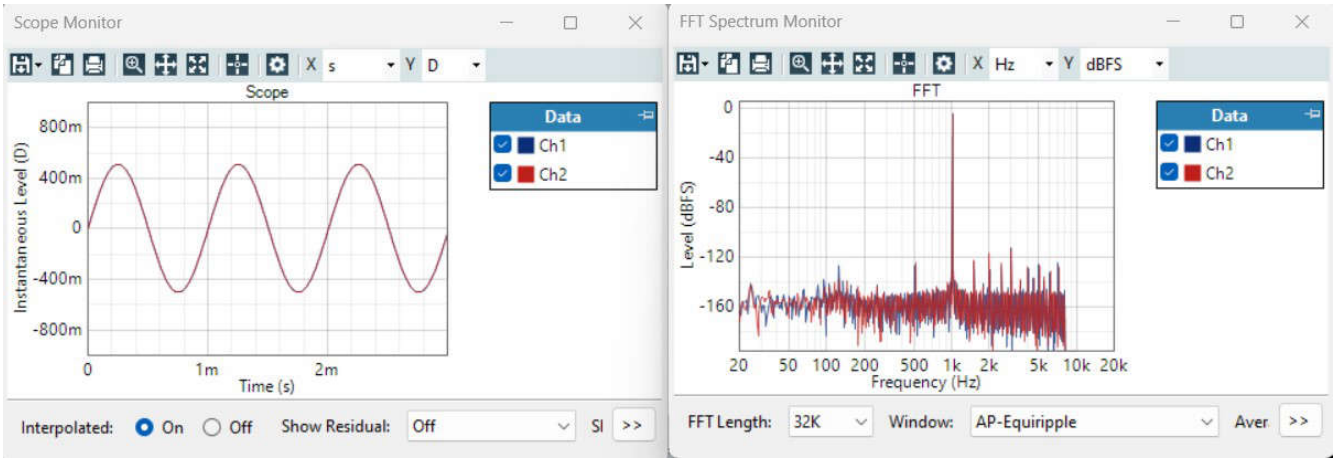

Figure 3-4. SASI ADC Output

Figure 3-5 shows 750 Hz tone from SASI RX after SRC, PASI RX tone is muted.

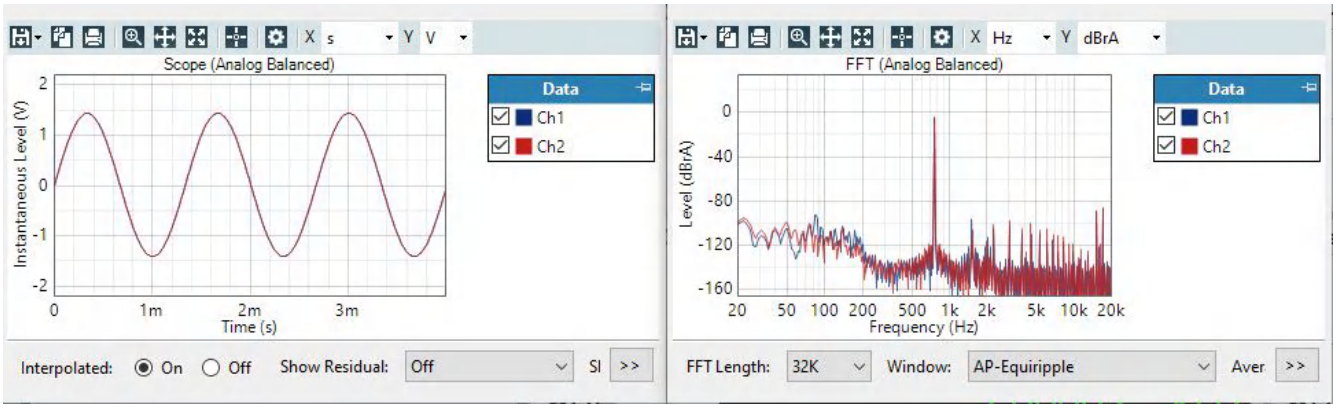

Figure 3-5. Speaker Output

3.3.2 Default Mode (Main Fs - Higher rate) with Recording

Figure 3-6 shows a block diagram for this use case. PASI is running at 48 KHz and SASI is at 16 KHz. In this use case analog input (MIC) sampled at main Fs and down-sampled with SRC to lower rate for SASI. The PASI TX is mixed of sampled MIC input with SASI RX or PASI RX. On the DAC side, SASI RX data can mix with PASI RX data prior to DAC output (Speaker).

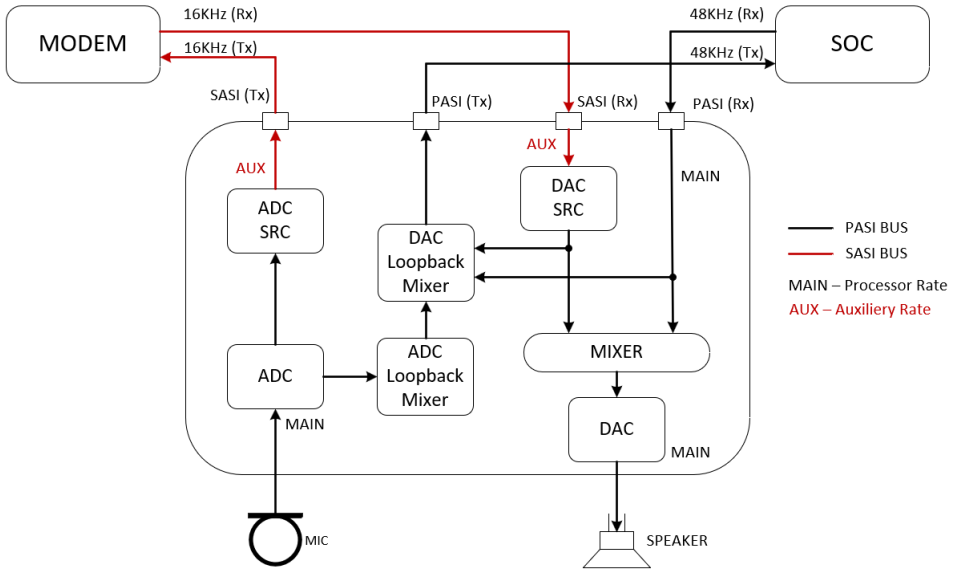

Figure 3-6. Default Mode diagram with Recording

The Audio Precision APx555 configurations for PASI and SASI are shown below. In this test case, mixer coefficients are kept to its default (full-sacle) and the input levels are adjusted as not to exceed the maximum allowed level for example -9dBrG instead of 0dBrG.

PASI APx555:

Generator:

Analog Output (MIC): 1KHz Sine, -9 dBrG (0dBrG = 2Vrms)

Analyzer:

Input 1: Digital audio for PASI Tx with Fs = 48 KHz, TDM, 32 bit depth

Input 2: Analog input from DAC output (Speaker)

SASI APx555:

Generator:

Digital Output: 750Hz Sine, -9 dBFS

Analyzer:

Input 1: Digital audio for SASI Tx with Fs = 16 KHz, TDM, 32 bit depth

```
##### PASI higher rate than SASI ADC and DAC SRC Testing with Recording ######
# Target Mode, TDM, 32-bit
# Primary and Secondary ASI, multiple of 48KHz Sampling
# GPIO2=Secondary FSYNC, GPIO1=Secondary BCLK, GPI1=Secondary DIN, GPO1=Secondary DOUT for 4x4
#
w a0 00 00            # Set page 0
w a0 01 01            # Software Reset
w a0 02 09            # Wake up with AVDD > 2v and all VDDIO level
w a0 0a 10            # GPIO1 as input
w a0 0b 10            # GPIO2 as input
w a0 0d 02            # GPI1 as input
w a0 0c 71            # GPO1 as Secondary DOUT
w a0 11 a2            # Enable PASI DIN and Set GPI2A as Secondary FSYNC and GPIO1 as Secondary BCLK
w a0 12 60            # Set GPI1A as Secondary DIN
w a0 18 00            # Enable both Primary and Secondary ASI as independent
w a0 34 40            # PASI BCLK is the input clock source
w a0 19 00            # 1 data input and 1 data output for PASI and SASI
w a0 1a 30            # PASI TDM, 32 bit format
w a0 1e 00            # Tri-state PASI Ch1 to avoid conflict with mix on TDM slot 0
w a0 1f 01            # Tri-state PASI Ch2 to avoid conflict with mix on TDM slot 1
w a0 22 20            # PASI DOUT Ch5 - ASI Loopback data on TDM slot 0
w a0 23 21            # PASI DOUT Ch6 - ASI Loopback data on TDM slot 1
w a0 28 20            # PASI DIN Ch1 on TDM slot 0
w a0 29 21            # PASI DIN Ch2 on TDM slot 1
w a0 00 03            # Set page 3
w a0 1a 30            # SASI TDM, 32 bit format
w a0 1e 20            # SASI DOUT Ch1 on TDM slot 0
w a0 1f 21            # SASI DOUT Ch2 on TDM slot 1
w a0 28 20            # SASI DIN Ch1 on TDM slot 0
w a0 29 21            # SASI DIN Ch2 on TDM slot 1
w a0 00 01            # Set page 1
w a0 17 00            # Default SR-Converter with auto-detect enable
w a0 18 00            # Default auto m:n ratio
w a0 2c d0            # Enable DAC, Side Chain and Loopback Mixer
w a0 00 11            # Set page 0x11
w a0 0c 00 00 40 00   # Route Main DIN Ch1 to LDAC2 Mixer, full scale
w a0 14 40 00 00 00   # Route Main DIN Ch2 to RDAC2 Mixer, full scale
w a0 4c 00 00 40 00   # Route Aux DIN Ch1 to LDAC2 Mixer, full scale
w a0 54 40 00 00 00   # Route Aux DIN Ch2 to RDAC2 Mixer, full scale
w a0 5e 40 00         # ADC Loopback Ch1 to SC_LDAC2 Mixer to mix with LDAC2, full scale
w a0 64 40 00         # ADC Loopback Ch2 to SC_RDAC2 Mixer to mix with RDAC2, full scale
w a0 00 00            # Set page 0
w a0 50 00            # ADC Ch1 diff input, 5KOhm, 2Vrms ac-coupled, audio band
w a0 55 00            # ADC Ch2 diff input, 5KOhm, 2Vrms ac-coupled, audio band
w a0 64 20            # Configure OUT1P/M as differential from DAC1
w a0 65 20            # Configure OUT1P LINEOUT 0dB audio band
w a0 66 20            # Configure OUT1M LINEOUT 0dB 2Vrms Differential
w a0 6b 20            # Configure OUT2P/M as differential from DAC2
w a0 6c 20            # Configure OUT2P LINEOUT 0dB audio band
w a0 6d 20            # Configure OUT2M LINEOUT 0dB 2Vrms Differential
w a0 76 cc            # Enable Input and Output Ch1 and Ch2
w a0 78 e0            # Power up ADC, DAC and MICBIAS
```

Test Results

The following plots show the results of the ADC output at SASI TX after SRC. As expected the frequency response (FFT) ends at 8 KHz (Fs/2 of SASI rate of 1 6KHz).

Figure 3-7 SASI TX 1 KHz tone from MIC input after SRC:

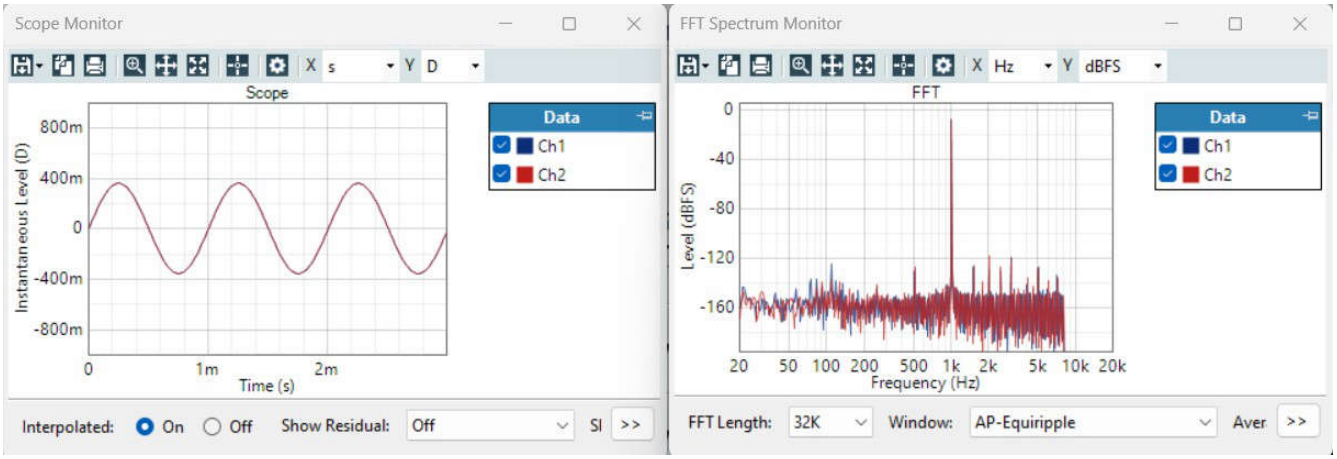

Figure 3-7. SASI ADC Output

On Speaker output, the tone captured is the SASI RX tone of 750 Hz after SRC. PASI RX tone is muted. PASI TX is a mixed of MIC input with SASI RX tone of 750Hz.

Figure 3-8 shows PASI TX is a mixed of MIC input and SASI RX after SRC.

Figure 3-9 shows 750 Hz tone from SASI RX after SRC, PASI tone is muted:

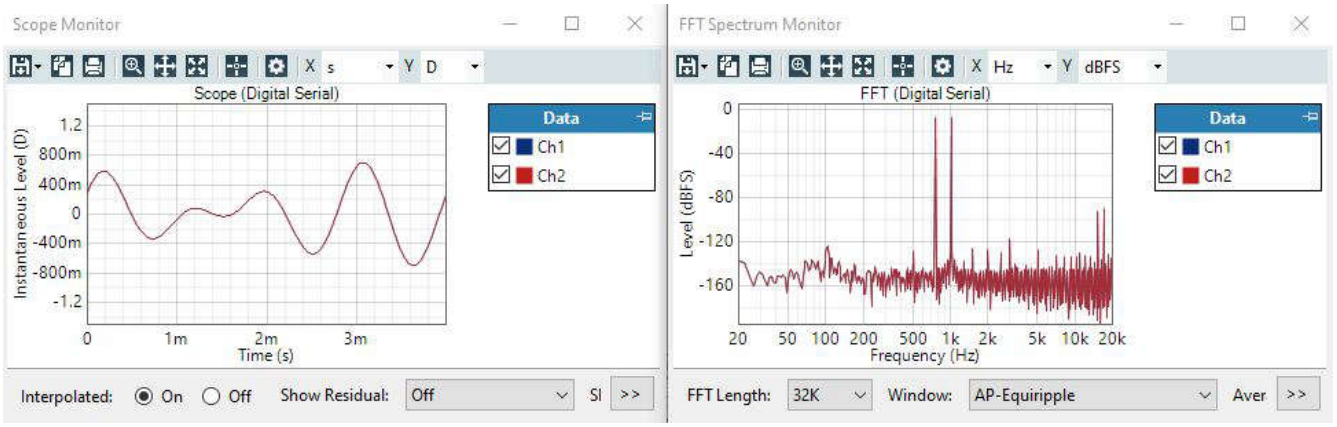

Figure 3-8. PASI ADC Output

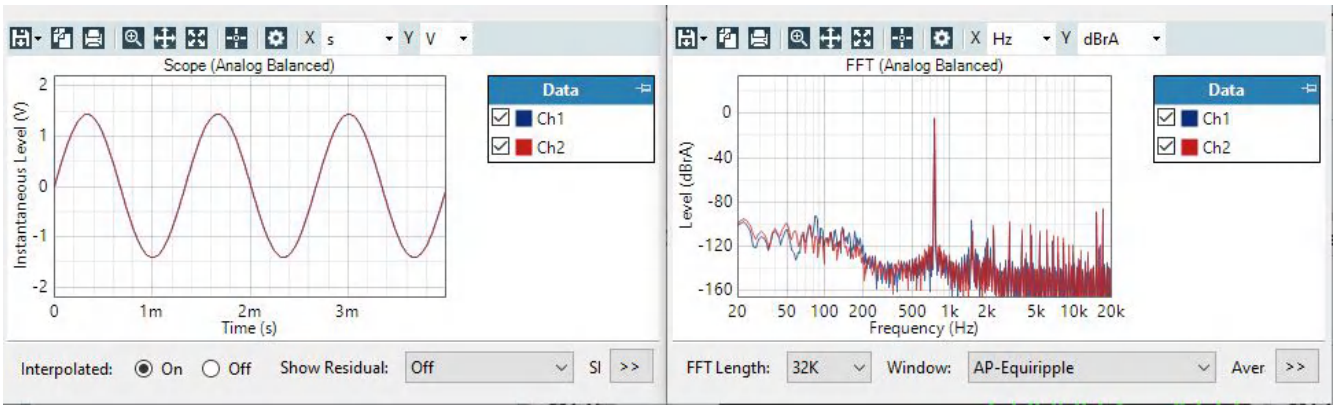

Figure 3-9. Speaker Output

3.3.3 Custom Mode (Main Fs - Lower rate)

Figure 3-10 shows a block diagram for this use case with PASI and SASI mapping. PASI is running at 16 KHz and SASI is at 48 KHz. In this use case the analog (MIC) input is sampled at main Fs (lower rate). On the DAC side, SASI RX data can mix with PASI RX data prior to DAC output (Speaker).

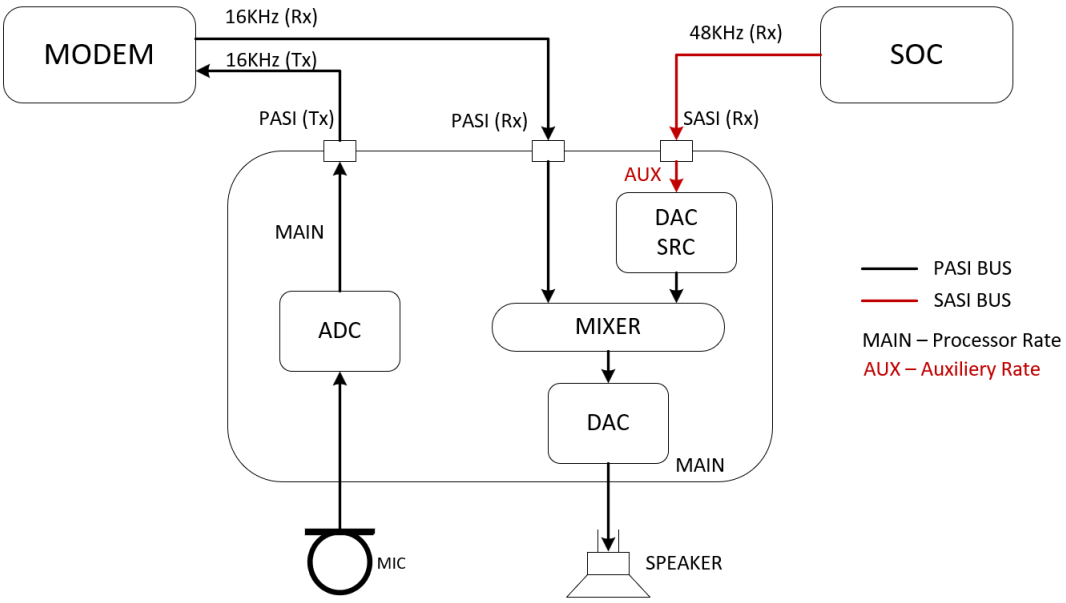

Figure 3-10. Custom Mode diagram

The Audio Precision APx555 configurations for PASI and SASI are shown below. In this test case mixer coefficients are kept to its default (full-sacle) and the input levels are adjusted as not to exceed the maximum allowed level for example -6dBrG instead of 0dBrG.

PASI APx555:

Generator:

Analog Output (MIC): 750Hz Sine, -1 dBrG (0dBrG = 2Vrms)

Analyzer:

Input 1: Digital audio for PASI Tx with Fs = 16KHz, TDM, 32 bit depth

Input 2: Analog input from DAC output (Speaker)

SASI APx555:

Generator:

Digital Output: 1KHz Sine, -6 dBFS

Analyzer:

Input 1: Digital audio for SASI Tx with Fs = 48KHz, TDM, 32 bit depth

```
##### PASI lower rate than SASI ADC and DAC SRC Testing ######
# Target Mode, TDM, 32-bit
# Primary and Secondary ASI, multiple of 48KHz Sampling
# GPIO2=Secondary FSYNC, GPIO1=Secondary BCLK, GPI1=Secondary DIN, GPO1=Secondary DOUT for 4x4
#
w a0 00 00        # Set page 0
w a0 01 01        # Software Reset
w a0 02 09        # Wake up with AVDD > 2v and all VDDIO level
w a0 0a 10        # GPIO1 as input
w a0 0b 10        # GPIO2 as input
w a0 0d 02        # GPI1 as input
w a0 0c 71        # GPO1 as Secondary DOUT
w a0 11 a2        # Enable PASI DIN and Set GPI2A as Secondary FSYNC and GPIO1 as Secondary BCLK
w a0 12 60        # Set GPI1A as Secondary DIN
w a0 18 00        # Enable both Primary and Secondary ASI as independent
w a0 34 40        # PASI BCLK is the input clock source
w a0 19 00        # 1 data input and 1 data output for PASI and SASI
```

```
w a0 1a 30        # PASI TDM, 32 bit format
w a0 1e 20        # PASI DOUT Ch1 on TDM slot 0
w a0 1f 21        # PASI DOUT Ch2 on TDM slot 1
w a0 28 20        # PASI DIN Ch1 on TDM slot 0
w a0 29 21        # PASI DIN Ch2 on TDM slot 1
w a0 00 03        # Set page 3
w a0 1a 30        # SASI TDM, 32 bit format
w a0 1e 20        # SASI DOUT Ch1 on TDM slot 0
w a0 1f 21        # SASI DOUT Ch2 on TDM slot 1
w a0 28 20        # SASI DIN Ch1 on TDM slot 0
w a0 29 21        # SASI DIN Ch2 on TDM slot 1
w a0 00 01        # Set page 1
w a0 17 40        # SR-Converter without auto-detect
w a0 18 80        # Use PASI Fs as Main Fs
w a0 2c 80        # Enable DAC ASI Mixer
w a0 00 00        # Set page 0
w a0 50 00        # ADC Ch1 diff input, 5KOhm, 2Vrms ac-coupled, audio band
w a0 55 00        # ADC Ch2 diff input, 5KOhm, 2Vrms ac-coupled, audio band
w a0 64 20        # Configure OUT1P/M as differential from DAC1
w a0 65 20        # Configure OUT1P LINEOUT 0dB audio band
w a0 66 20        # Configure OUT1M LINEOUT 0dB 2Vrms Differential
w a0 6b 20        # Configure OUT2P/M as differential from DAC2
w a0 6c 20        # Configure OUT2P LINEOUT 0dB audio band
w a0 6d 20        # Configure OUT2M LINEOUT 0dB 2Vrms Differential
w a0 76 cc        # Enable Input and Output Ch1 and Ch2
w a0 78 e0        # Power up ADC, DAC and MICBIAS
```

Test Results

The following plots show the results of the ADC output at PASI TX sampled at 16 KHz.

On Speaker output, the tone captured is the SASI RX tone of 750 Hz after SRC. PASI RX tone is muted.

Figure 3-11 shows PASI TX 750 Hz tone from MIC input sampled at 16 KHz:

Figure 3-12 shows 1 KHz tone from SASI RX after SRC, PASI tone is muted:

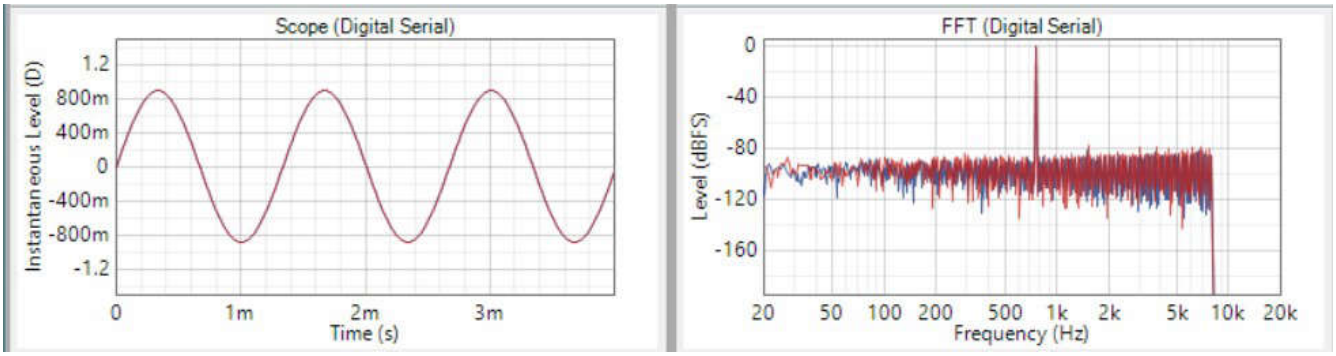

Figure 3-11. PASI ADC Output

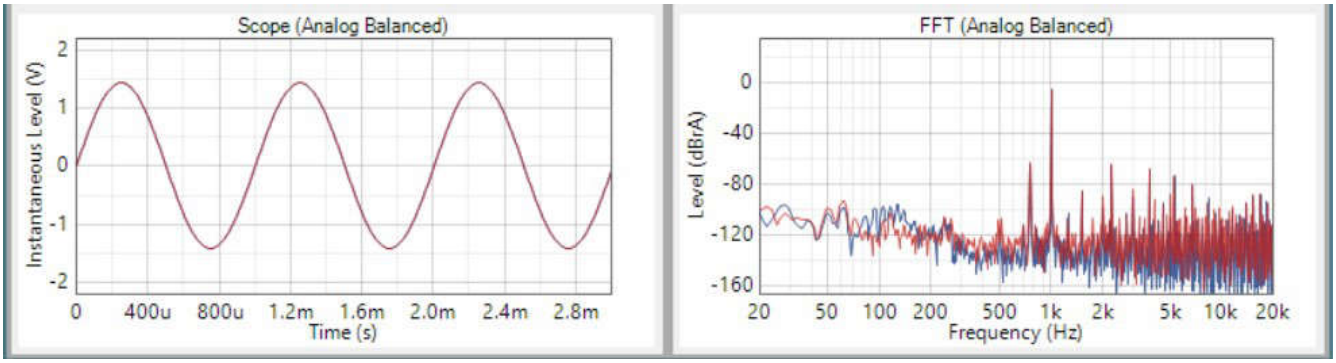

Figure 3-12. Speaker Output

3.3.4 Custom Mode (Main Fs - Lower rate) with Recording

Figure 3-13 shows a block diagram for this use case. PASI is running at 16KHz and SASI is at 48KHz. In this use case analog input (MIC) is sampled at main Fs (lower rate) and send out to PASI TX. The same MIC input can mix with DAC inputs from PASI RX, SASI RX or both and up-sampled with SRC for SASI TX. On the DAC side, SASI RX data can mix with PASI RX data prior to DAC output (Speaker).

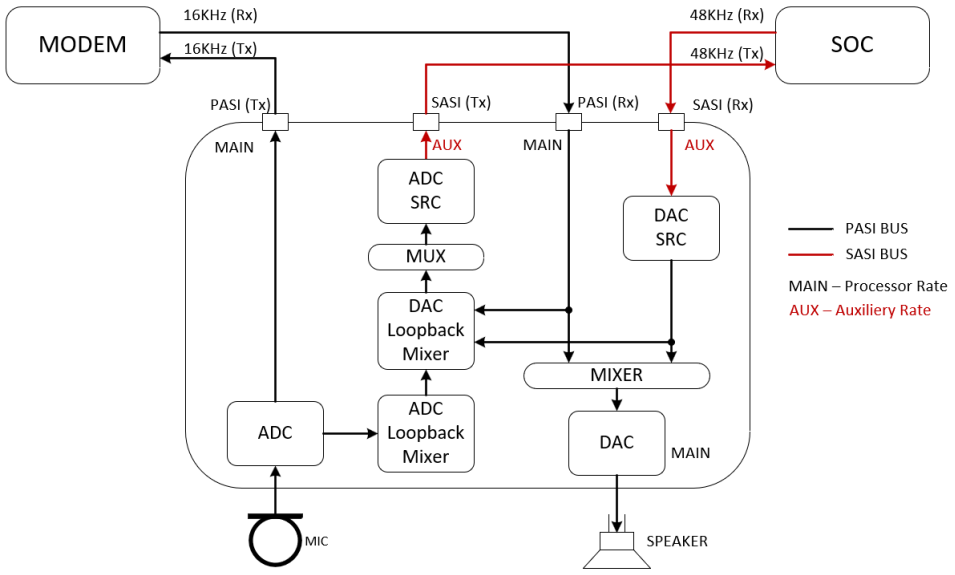

Figure 3-13. Custom Mode Diagram with Recording

The Audio Precision APx555 configurations for PASI and SASI is shown below. In this test case mixer coefficients are kept to its default (full-sacle) and the input levels are adjusted as not to exceed the maximum allowed level for example -9dBrG instead of 0dBrG.

PASI APx555:

Generator:

Analog Output (MIC): 1KHz Sine, -9 dBrG (0dBrG = 2Vrms)

Analyzer:

Input 1: Digital audio for PASI Tx with Fs = 16 KHz, TDM, 32 bit depth

Input 2: Analog input from DAC output (Speaker)

SASI APx555:

Generator:

Digital Output: 750Hz Sine, -9 dBFS

Analyzer:

Input 1: Digital audio for SASI Tx with Fs = 48 KHz, TDM, 32 bit depth

```
##### PASI lower rate than SASI ADC and DAC SRC Testing with Recording ######
# Target Mode, TDM, 32-bit
# Primary and Secondary ASI, multiple of 48KHz Sampling
# GPIO2=Secondary FSYNC, GPIO1=Secondary BCLK, GPI1=Secondary DIN, GPO1=Secondary DOUT for 4x4
#
w a0 00 00            # Set page 0
w a0 01 01            # Software Reset
w a0 02 09            # Wake up with AVDD > 2v and all VDDIO level
w a0 0a 10            # GPIO1 as input
w a0 0b 10            # GPIO2 as input
w a0 0d 02            # GPI1 as input
w a0 0c 71            # GPO1 as Secondary DOUT
w a0 11 a2            # Enable PASI DIN and Set GPI2A as Secondary FSYNC and GPIO1 as Secondary BCLK
w a0 12 60            # Set GPI1A as Secondary DIN
w a0 18 00            # Enable both Primary and Secondary ASI as independent
w a0 34 40            # PASI BCLK is the input clock source
w a0 19 00            # 1 data input and 1 data output for PASI and SASI
```

```
w a0 1a 30            # PASI TDM, 32 bit format
w a0 1e 20            # PASI DOUT Ch1 on TDM slot 0
w a0 1f 21            # PASI DOUT Ch2 on TDM slot 1
w a0 28 20            # PASI DIN Ch1 on TDM slot 0
w a0 29 21            # PASI DIN Ch2 on TDM slot 1
w a0 00 03            # Set page 3
w a0 1a 30            # SASI TDM, 32 bit format
w a0 1e 00            # Tri-state SASI DOUT Ch1 on TDM slot 0
w a0 1f 01            # Tri-state SASI DOUT Ch2 on TDM slot 1
w a0 22 20            # SASI DOUT Ch5 on TDM slot 0
w a0 23 21            # SASI DOUT Ch5 on TDM slot 1
w a0 28 20            # SASI DIN Ch1 on TDM slot 0
w a0 29 21            # SASI DIN Ch2 on TDM slot 1
w a0 00 01            # Set page 1
w a0 17 40            # SR-Converter without auto detect
w a0 18 40            # Use PASI Fs as Main Fs
w a0 2c d0            # Enable DAC, Side Chain and Loopback Mixer
w a0 00 11            # Set page 0x11
w a0 0c 00 00 40 00   # Route Main Ch1 to LDAC2 Mixer, full scale
w a0 14 40 00 00 00   # Route Main Ch2 to RDAC2 Mixer, full scale
w a0 4c 00 00 40 00   # Route AUX Ch1 to LDAC2 Mixer, full scale
w a0 54 40 00 00 00   # Route AUX Ch2 to RDAC2 Mixer, full scale
w a0 5e 40 00         # ADC Loopback Ch1 to SC_LDAC2 Mixer to mix with LDAC2, full scale
w a0 64 40 00         # ADC Loopback Ch2 to SC_RDAC2 Mixer to mix with RDAC2, full scale
w a0 00 00            # Set page 0
w a0 50 00            # ADC Ch1 diff input, 5KOhm, 2Vrms ac-coupled, audio band
w a0 55 00            # ADC Ch2 diff input, 5KOhm, 2Vrms ac-coupled, audio band
w a0 64 20            # Configure OUT1P/M as differential from DAC1
w a0 65 20            # Configure OUT1P LINEOUT 0dB audio band
w a0 66 20            # Configure OUT1M LINEOUT 0dB 2Vrms Differential
w a0 6b 20            # Configure OUT2P/M as differential from DAC2
w a0 6c 20            # Configure OUT2P LINEOUT 0dB audio band
w a0 6d 20            # Configure OUT2M LINEOUT 0dB 2Vrms Differential
w a0 76 cc            # Enable Input and Output Ch1 and Ch2
w a0 78 e0            # Power up ADC, DAC and MICBIAS
```

Test Results

The following plots show the results of the ADC output at SASI after SRC. As seen here the frequency response (FFT) sweeps through 20 KHz (up-sampled to 48 KHz).

Figure 3-14 shows SASI TX output a mixed of MIC input and SASI RX after SRC.

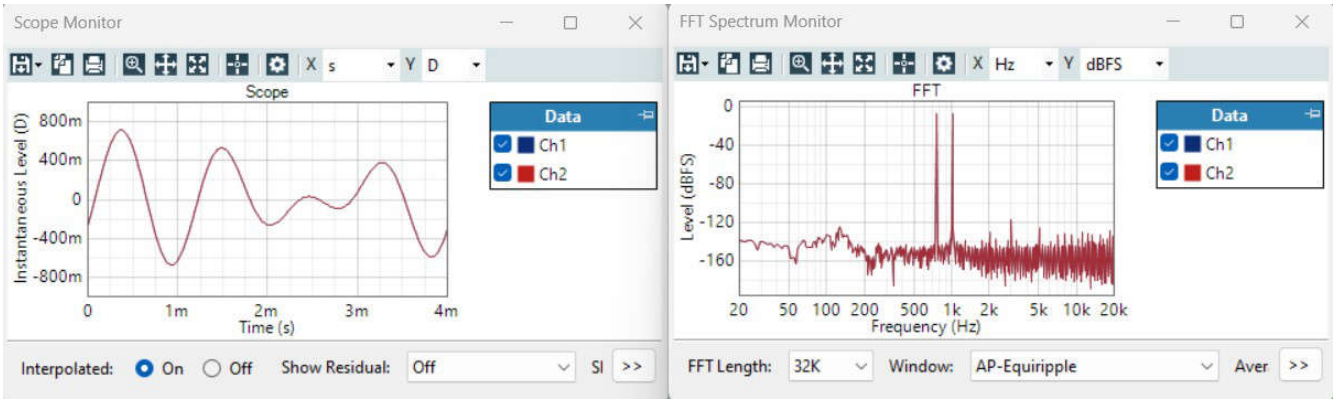

Figure 3-14. SASI ADC output

On Speaker output, the tone captured is the SASI RX tone of 750 Hz after SRC. PASI RX tone is muted and PASI TX is MIC input of 1 KHz.

Figure 3-15 shows PASI TX 1KHz tone from MIC input sampled at 16 KHz.

Figure 3-16 shows that this 750 Hz tone is of SASI RX after SRC, PASI tone is off or muted.

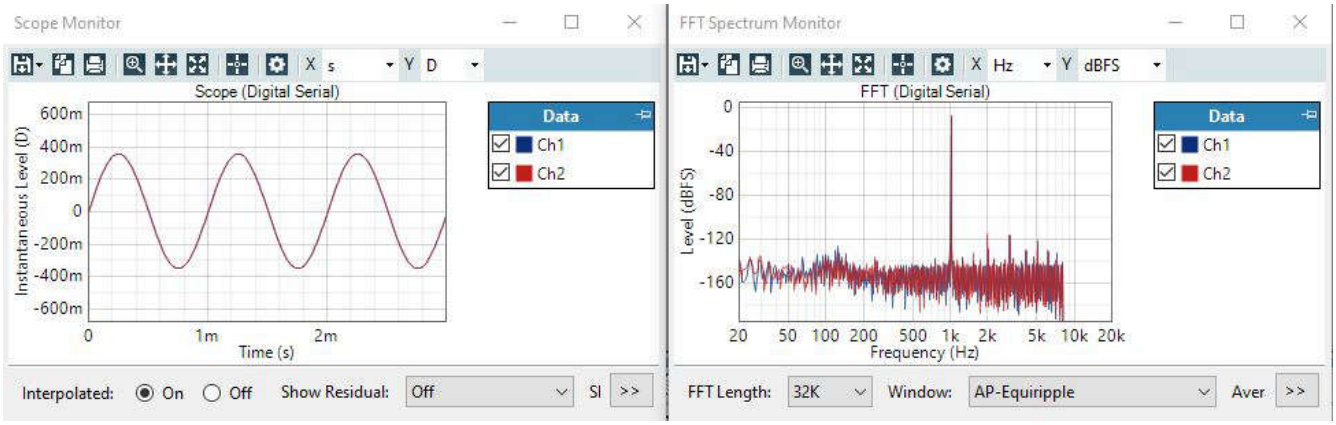

Figure 3-15. PASI ADC Output

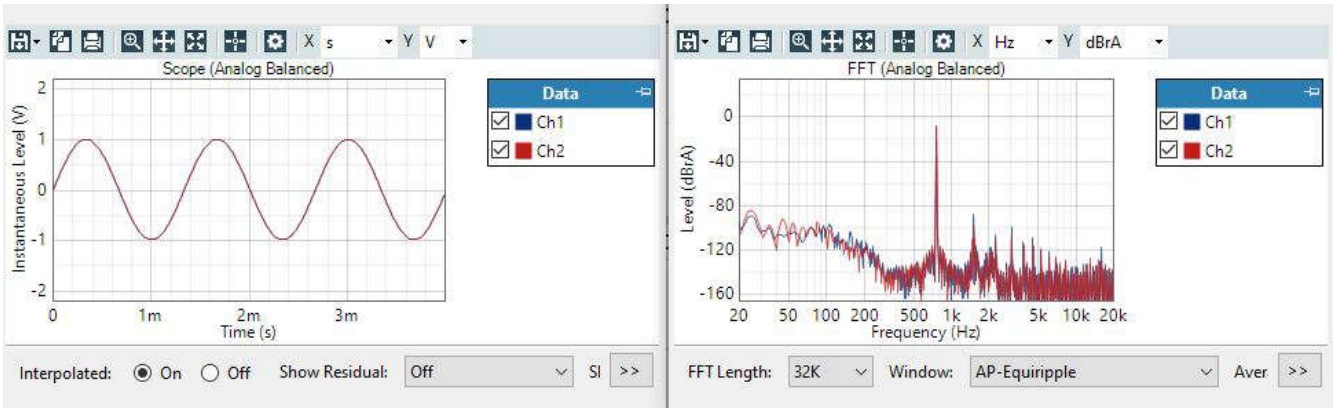

Figure 3-16. Speaker Output

4 Summary

Synchronous Sampling Rate Conversion were demonstrated with TAC5212 device through several use case examples. The same scheme applies to other device variants listed in the references.

5 References

- Texas Instruments, *TAC5212 High-Performance Stereo Audio Codec With 115dB Dynamic Range ADC and 120dB Dynamic Range DAC*, data sheet.
- Texas Instruments, *TAC5211 High-Performance Mono Audio Codec With 115dB Dynamic Range ADC and 115dB Dynamic Range DAC*, data sheet.
- Texas Instruments, *TAC5112 Low-Power Stereo Audio Codec With 102dB Dynamic Range ADC and 106dB Dynamic Range DAC*, data sheet.
- Texas Instruments, *TAC5111 Low-Power Mono Audio Codec With 108dB Dynamic Range ADC and 108dB Dynamic Range DAC*, data sheet.
- Texas Instruments, *TAA5212 Low-Power High-Performance Stereo Audio ADC With 115dB Dynamic Range*, data sheet.
- Texas Instruments, *TAD5212 High-Performance Stereo Audio DAC With 115dB Dynamic Range DAC*, data sheet.
- Texas Instruments, *TAD5112 Automotive Stereo Audio DAC With 106dB Dynamic Range DAC*, data sheet.

6 Revision History

Changes from Revision * (December 2023) to Revision A (June 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated *SRC Supported Ratio* table	4

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