TVP5150A VBI Quick Start

HPA Digital Audio Video

Introduction

The TVP5150A Video Decoder has an internal Vertical Data Processor (VDP) that can be used to slice various VBI data services such as V-CHIP, Teletext (WST, NABTS), Closed Caption (CC), Wide Screen Signaling (WSS), Program Delivery Control (PDC), Vertical Interval Time Code (VITC), and Video Program System (VPS). These data services are typically transmitted during the vertical blanking interval of the video frame.

Table 1. Supported Data Services

VBI System	Standard	Line Number	Number of Bytes	Specification
Teletext WST A	SECAM	6-23 (Field 1, Field 2)	38	ITU-R BT 653-2
Teletext WST B	PAL	6-22 (Field 1, Field 2)	43	ITU-R BT 653-2
Teletext NABTS C	NTSC	10-21 (Field 1, Field 2)	34	ITU-R BT 653-2
Teletext NABTS D	NTSC-J	10-21 (Field 1, Field 2)	35	ITU-R BT 653-2
Closed Caption	PAL	22 (Field 1, Field 2)	2	EIA-608
Closed Caption	NTSC	21 (Field 1, Field 2)	2	EIA-608
WSS	PAL	23 (Field 1, Field 2)	14 bits	ITU-R BT 1119-1
WSS-CGMS	NTSC	20 (Field 1, Field 2)	20 bits	IEC 61880
VITC	PAL	6-22	9	SMPTE 12M
VITC	NTSC	10-20	9	SMPTE 12M
VPS (PDC)	PAL	16	13	ETS 300 231
V-CHIP	NTSC	21 (Field 2)	2	EIA-744
Gemstar 1x	NTSC		2	
Gemstar 2x	NTSC		5 with frame byte	
User	Any	Programmable	Programmable	

A host or backend receiver can retrieve the sliced data using one of 3 methods:

1. I2C access of dedicated Closed Caption, WSS, VITC, VPS, and Gemstar data registers.
2. I2C access of an internal 512-byte FIFO used primarily for high-bandwidth data services such as full field teletext.
3. As ITU-R BT.656 ancillary data, inserted by the TVP5150A in the data stream during the horizontal blanking interval.

Note: This document will focus primarily on the more commonly used dedicated I2C data registers.

Prior to accessing sliced VBI data, the TVP5150A must be configured for the desired VBI data service. This includes loading of the VDP Configuration Ram (C-RAM) and the Line Mode registers that are used to enable various data services.

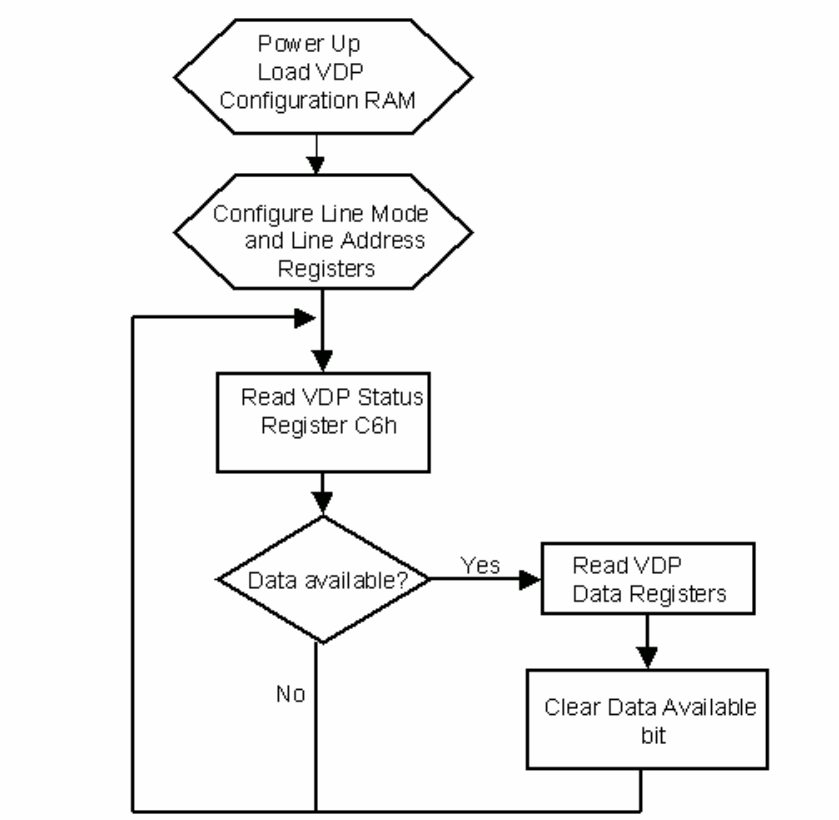

Figure 1. The VDP Configuration Ram Is Loaded Prior to Line Mode Register Setup

VDP Configuration RAM

The first step in configuring the TVP5150A for VBI data slicing is to load the VDP Configuration RAM (C-RAM). The C- RAM defines the data slicing modes for the various data services, with each mode having its own unique RAM address and 16 byte block of memory. Table 2 shows the recommended setup values for the various data services that are supported. Prior to loading the C-RAM, the Line Mode registers must all be programmed with a value of FFh to avoid conflict between the VDP and microprocessor during the load process. Full field mode must also be disabled in I2C register CFh.

Table 2. TVP5150A Configuration RAM Recommended Settings

Index	Addres	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Reserved	000	Reserved															
WST SECAM	010	AA	AA	FF	FF	E7	2E	20	26	E6	B4	OE	0	0	0	10	0
Reserved	020	Reserved															
WST PAL B	030	AA	AA	FF	FF	27	2E	20	2B	A6	72	10	0	0	0	10	0
Reserved	040	Reserved															
WST PAL C	050	AA	AA	FF	FF	E7	2E	20	22	A6	98	0D	0	0	0	10	0
Reserved	060	Reserved															
WST NTSC	070	AA	AA	FF	FF	27	2E	20	23	69	93	0D	0	0	0	10	0
Reserved	080	Reserved															
NABTS, NTSC	090	AA	AA	FF	FF	E7	2E	20	22	69	93	0D	0	0	0	15	0
Reserved	0A0	Reserved															
NABTS, NTSC–J	0B0	AA	AA	FF	FF	A7	2E	20	23	69	93	0D	0	0	0	10	0
Reserved	0C0	Reserved															
CC, PAL/SECAM	0D0	AA	2A	FF	3F	04	51	6E	02	A6	7B	09	0	0	0	27	0
Reserved	0E0	Reserved															
CC, NTSC	0F0	AA	2A	FF	3F	04	51	6E	02	69	8C	09	0	0	0	27	0
Reserved	100	Reserved															
WSS, PAL/SECAM	110	5B	55	C5	FF	0	71	6E	42	A6	CD	0F	0	0	0	3A	0
Reserved	120	Reserved															
WSS, NTSC C	130	38	00	3F	00	0	71	6E	43	69	7C	08	0	0	0	39	0
Reserved	140	Reserved															
VITC, PAL/SECAM	150	0	0	0	0	0	8F	6D	49	A6	85	08	0	0	0	4C	0
Reserved	160	Reserved															
VITC, NTSC	170	0	0	0	0	0	8F	6D	49	69	94	08	0	0	0	4C	0
Reserved	180	Reserved															
VPS, PAL	190	AA	AA	FF	FF	BA	CE	2B	0D	A6	DA	0B	0	0	0	60	0
Reserved	1A0	Programmable															
Gemstar Custom 1	1B0	CC	CC	FF	FF	05	51	6E	05	69	19	13	0	0	0	60	0

The C-RAM is accessed through the use of three I2C registers (C3h-C5h). Registers C4h and C5h must be programmed with the 9-bit starting address of the block of C-RAM to be programmed. I2C read and write operations are then performed indirectly using register C3h. The C-RAM address is automatically incremented following each I2C transaction. Only the portion of the C-RAM that includes the data service to be used needs to be programmed. If WSS for NTSC is the only desired data service, for example, only the 16 bytes starting at C-RAM address 130h need to be programmed. Figure 3 shows example C code for loading the WSS C-RAM.

Address	C3h-C5h

Address	7	6	5	4	3	2	1	0
C3h	Configuration data							
C4h	RAM address (7:0)							
C5h	Reserved							RAM address 8

Figure 2. TVP5150A Configuration RAM I2C Access Registers

Example (Write 2 data bytes starting at C-RAM address 130h)

1. Set C-RAM starting address.
    a. Write 0x30 to register 0xC4 (C-RAM address (7:0)).
    b. Write 0x01 to register 0xC5 (C-RAM address (8)).
2. Write the two bytes (0x38 and 0x00)
    a. Write 0x38 to register 0xC3. Write first byte to C-RAM address 130h.
    b. Write 0x00 to register 0xC3. Write next byte to C-RAM address 131h.

```
                    // TVP5150A NTSC WSS C-RAM Load Example
#define TVP5150A 0xB8;                      // TVP5150A main I2C address

byte I2C_RegAddress;
byte I2C_Data;
int CRAM_Address, count;
// recommended WSS settings
byte WSS_ARRAY[]={0x38,0,0x3F,0,0,0x71,0x6E,0x43,0x69,0x7C,0x08,0,0,0,0x39,0};

I2C_RegAddress = 0xD0;                      // starting address of Line Mode Registers
I2C_Data = 0xFF;
For (count = 0; count < 44; count ++)
{
   I2CWriteByte(TVP5150A, I2C_RegAddress, I2C_Data);  //write FFh to LineMode registers
   I2C_RegAddress ++;
}
I2CWriteByte(TVP5150A, 0xCF, 0);                 // disable full field mode
CRAM_Address = 0x130;                            // address of NTSC WSS C-RAM block

I2CWriteByte(TVP5150A, 0xC4, 0x30);              // load C4h with C-RAM address[7:0]

I2CWriteByte(TVP5150A, 0xC5, 0x01);              // load C5h with C-RAM address[8]

For (count = 0; count < 16; count++)
{
 I2CWriteByte(TVP5150A, 0xC3, WSS_ARRAY[count]);   // write 16 bytes of WSS C-RAM data
}                                                   // to register C3h.
```

Figure 3. Example Load of WSS Configuration RAM

Line Mode Registers

After the VDP Configuration RAM is loaded, the Line Mode Registers (D0h-FBh) must be properly configured for the desired VBI data service. Each register in this register bank is linked to a specific video line number and video field. Video lines 6 through 27 of both Field1 and Field2 are supported. For each desired data service, the proper mode configuration bits need to be loaded into the Line Mode register that is linked to the correct video line number. Additional data slicing options such as filtering, error correction, and FIFO routing are also available in the Line Mode registers. Unused Line Mode and Line Address registers must be programmed with FFh. A detailed description of these registers is shown in Appendix A.

The TVP5150A VDP is based on an NTSC line numbering convention, resulting in a 3-line VDP offset relative to actual PAL line numbers. For PAL systems, the Line Mode register for line “N+3” must be used to configure a data service transmitted on line N of the input source. Figure 4 shows example C code for configuring WSS data services for NTSC and PAL. Included in this example is an I2C write to the Pixel Alignment Registers (CBh-CCh), which define the horizontal position where data slicing begins. The value used (0x4E) is recommended for all data services.

Table 3. Line Mode Configuration Bits for Supported Modes

LINE MODE REGISTER (D0h-FCh) BITS [3:0]	NAME	VIDEO LINE NUMBER	DESCRIPTION
0000b	*WST SECAM*	*6-23 (Field 1, 2)*	Teletext, SECAM
0001b	WST PAL B	6-22 (Field 1, 2)	Teletext, PAL, System B,
0010b	WST PAL C	6-22 (Field 1, 2)	Teletext, PAL, System C
0011b	WST, NTSC B	10-21 (Field 1, 2)	Teletext, NTSC, System B,
0100b	NABTS, NTSC C	10-21 (Field 1, 2)	Teletext, NTSC, System C
0101b	NABTS, NTSC D	10-21 (Field 1, 2)	Teletext, NTSC, System D (Japan)
0110b	CC, PAL/SECAM	22 (Field 1, 2)	Closed caption PAL/SECAM
0111b	CC, NTSC	21 (Field 1, 2)	Closed caption NTSC
1000b	WSS, PAL/SECAM	23 (Field 1, 2)	Wide–screen signal, PAL/SECAM
1001b	WSS, NTSC	20 (Field 1, 2)	Wide–screen signal, NTSC
1010b	VITC, PAL/SECAM	6-22	Vertical interval timecode, PAL/SECAM
1011b	VITC, NTSC	10-20	Vertical interval timecode, NTSC
1100b	VPS, PAL	16	Video program system, PAL
1101b	EPG/Gemstar		Electronic program guide – Custom mode
1110b	x	x	Reserved
1111b	Active Video	Active Video	Active video/full field

```
// Example C Code for setting up WSS Line Mode Registers
//
// …Load CRAM
//
//  NTSC WSS Line Mode setup for line 20 of both fields

I2CWriteByte(TVP5150A, 0xEC, 0x09);    // line 20 field 1 (0xEC), mode bits = 0x09
I2CWriteByte(TVP5150A, 0xED, 0x09);    // line 20 field 2 (0xED), mode bits = 0x09

I2CWriteByte(TVP5150A, 0xCB, 0x4E);    // Set Pixel Alignment [7:0]to 0x4E
I2CWriteByte(TVP5150A, 0xCC, 0x00);    // Set Pixel Alignment [9:8]to 0x00



//  PAL WSS Line Mode setup for line 23 (source input) of both fields.  PAL line
// numbering has 3 line offset so the Line 26 line mode registers are used.

I2CWriteByte(TVP5150A, 0xF8, 0x08);    // line 26 field 1 (0xF8), mode bits = 0x08
I2CWriteByte(TVP5150A, 0xF9, 0x08);    // line 26 field 2 (0xF9), mode bits = 0x08

I2CWriteByte(TVP5150A, 0xCB, 0x4E);    // Set Pixel Alignment [7:0]to 0x4E
I2CWriteByte(TVP5150A, 0xCC, 0x00);    // Set Pixel Alignment [9:8]to 0x00
```

Figure 4. Line Mode Setup for WSS (Wide Screen Signaling)

Sliced Data Retrieval

The TVP5150A provides dedicated I2C registers (see Table 4) for the retrieval of sliced data. Due to higher bandwidth requirements, teletext data is stored in a 512-byte FIFO. With all other data services, sliced data can be automatically sent to the dedicated registers or to the FIFO depending on the Line Mode setup. The WSS example in Figure 4 results in WSS data being routed to the dedicated WSS data registers.

Table 4. TVP5150A Dedicated VDP Data Registers

Register Name	VBUS Address
VDP Closed Caption (Field 1)	90h – 91h
VDP Closed Caption (Field 2)	92h – 93h
VDP WSS Data (Field 1) (NTSC)	94h – 96h
VDP WSS Data (Field 2) (NTSC)	97h– 99h
VDP WSS Data (Field 1) (PAL)	94h – 95h
VDP WSS Data (Field 2) (PAL)	97h– 98h
VDP VPS (PAL) or Gemstar (NTSC)	9Ah – A6h
VDP VITC Data	A7h – AFh

The internal 512-byte FIFO is used primarily for high-bandwidth teletext acquisition but can also be used for capture of the other data services if enable in the Line Mode register. A header containing information about the sliced data precedes all sliced data that is routed to the FIFO. The FIFO can be directly accessed by the host at I2C address B0h. Bit 0 of the FIFO Output Control register (CDh) must be set to a logic1 to enable host access to the FIFO.

Managing Data Retrieval

The VDP Status Registers (C6h) can be used to determine if sliced data is available. Unmasked data available bits for the supported data services are available in this register.

VDP Status Register

Address	C6h

7	6	5	4	3	2	1	0
FIFO full error	FIFO empty	TTX available	CC field 1 available	CC field 2 available	WSS available	VPS available	VITC available

A logic 1 indicates that sliced data is available. Once set, these bits need to be cleared after data retrieval. Writing a 1 to the appropriate bit(s) in this register clears the status bit. Figure 5 shows an example WSS data retrieval.

```
// Example C Code for WSS-NTSC Sliced Data Read

// Load C-RAM

// Configure Line Mode Registers

byte Status;
byte WSSData[3];

I2CReadBuffer(TVP5150A,0xC6,&Status,1);   //read 1 byte(status)from register C6h

If ((Status & 0x20) ==1)
{
   I2CReadBuffer(TVP5150A,0x94,&WSSData[0],3);   //if WSS bit set, read the 3 WSS bytes
//                                               // at WSS Data registers 94h–96h.
   I2CWriteByte(TVP5150A,0xC6,0x20);             // clear WSS available status bit
}
```

Figure 5. Example WSS Data Retrieval

FIFO Access

The internal 512-byte FIFO is used primarily for high-bandwidth teletext acquisition but can also be used for capture of the other data services. The FIFO can be directly accessed by the host at I2C address B0h. Bit 0 of FIFO Output Control register (CDh) must be set to Logic 1 to enable FIFO access. A header containing information about the sliced data precedes all sliced data that is routed to the FIFO. A VDP FIFO Interrupt Threshold register (C8h), FIFO Word Count Register (C7h), and FIFO full/empty status bits (C6h) are available for managing FIFO data flow.

Ancillary Data

An option is available to enable transmission of sliced VBI data as ancillary data in the ITU-R BT.656 video data stream. In this mode, the sliced data is inserted on the Y[7:0] output terminals during the horizontal blanking interval. An 8-byte header containing information about the sliced data is also inserted in the data stream prior to the sliced data. The header includes a 00h, FFh, FFh preamble that identifies the data as VBI ancillary data, so the host or backend must be able to distinguish between this preamble and the ITU-R BT.656 embedded sync codes (FFh, 00h,00h,E/SAV). The first header byte is inserted immediately following the EAV code during the horizontal blanking interval of the digital line where it occurred. The ancillary data header is summarized in Table 5.

Ancillary data mode is enabled by setting bit[6] in the appropriate Line Mode register to a Logic 1 and the Host Access enable bit(0) in register CDh to a Logic 0. When the ancillary data mode is enabled in register CDh, sliced data is not routed to the internal 512-byte FIFO.

Table 5. Ancillary Data Header

Byte No.	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	Description	
0	0	0	0	0	0	0	0	0	Ancillary data preamble	
1	1	1	1	1	1	1	1	1		
2	1	1	1	1	1	1	1	1		
3	NEP	EP	0	1	0	DID2	DID1	DID0	Data ID (DID)	
4	NEP	EP	F5	F4	F3	F2	F1	F0	Secondary data ID (SDID)	
5	NEP	EP	N5	N4	N3	N2	N1	N0	Number of 32 bit data (NN)	
6	Video line # [7:0]								Internal Data ID0 (IDID0)	
7	0	0	0	Data error	Match #1	Match #2	Video line # [9:8]		Internal Data ID1 (IDID1)	
8	1. Data								Data byte	1st word
9	2. Data								Data byte	
10	3. Data								Data byte	
11	4. Data								Data byte	
:	:								:	
	.								Data byte	Nth word
	m. Data								Data byte	
	CS[7:0]								Checksum	
4N+7	0	0	0	0	0	0	0	0	Fill byte	

EP: Even Parity for D0-D5 NEP: Negate Even Parity

DID: 91h: Sliced data from the vertical blanking interval of first field
53h: Sliced data from outside of the vertical blanking interval of first field

55h: Sliced data from the vertical blanking interval of second field
97h: Sliced data from outside of the vertical blanking interval of second field

SDID: This field holds the data format taken from the Line Mode register of the corresponding line.

NN: Number of Dwords beginning with byte 8 through 4N+7. Note this value is the number of Dwords where each Dword is 4 bytes.

IDID0: Transaction video line number [7:0]

IDID1: Bit 0/1 – Transaction video line number [9:8].
Bit 2 – Match 2 flag.
Bit 3 – Match 1 flag.
Bit 4 – 1 if a single error was detected in the EDC block. 0 if no error was detected.

CS: Sum of D0-D7 of 1.Data through last data byte.

Fill byte: Fill byte makes a multiple of 4 bytes from byte zero to last fill byte.

Note: The number of bytes (m) will vary depending on the VBI data service.

Appendix A. Subset of the TVP5150A VDP I2C Registers

Closed Caption Data Registers

Address	90h-93h

Address	7	6	5	4	3	2	1	0
90h	Closed caption field 1 byte 1							
91h	Closed caption field 1 byte 2							
92h	Closed caption field 2 byte 1							
93h	Closed caption field 2 byte 2							

These registers contain the closed caption data arranged in bytes per field.

WSS Data Registers

Address	94h-99h

NTSC

ADDRESS	7	6	5	4	3	2	1	0	BYTE
94h			b5	b4	b3	b2	b1	b0	WSS field 1 byte 1
95h	b13	b12	b11	b10	b9	b8	b7	b6	WSS field 1 byte 2
96h			b19	b18	b17	b16	b15	b14	WSS field 1 byte 3
97h			b5	b4	b3	b2	b1	b0	WSS field 2 byte 1
98h	b13	b12	b11	b10	b9	b8	b7	b6	WSS field 2 byte 2
99h			b19	b18	b17	b16	b15	b14	WSS field 2 byte 3

These registers contain the wide screen signaling (WSS) data for NTSC.

Bits 0-1 represent word 0, aspect ratio
Bits 2-5 represent word 1, header code for word 2
Bits 6-13 represent word 2, copy control
Bits 14-19 represent word 3, CRC

PAL/SECAM

ADDRESS	7	6	5	4	3	2	1	0	BYTE
94h	b7	b6	b5	b4	b3	b2	b1	b0	WSS field 1 byte 1
95h			b13	b12	b11	b10	b9	b8	WSS field 1 byte 2
96h	Reserved								
97h	b7	b6	b5	b4	b3	b2	b1	b0	WSS field 2 byte 1
98h			b13	b12	b11	b10	b9	b8	WSS field 2 byte 2
99h	Reserved								

PAL/SECAM:

Bits 0-3 represent group 1, aspect ratio
Bits 4-7 represent group 2, enhanced services
Bits 8-10 represent group 3, subtitles
Bits 11-13 represent group 4, others

VPS Data Registers

Address	9Ah–A6h

ADDRESS	7	6	5	4	3	2	1	0
9Ah	VPS byte 1							
9Bh	VPS byte 2							
9Ch	VPS byte 3							
9Dh	VPS byte 4							
9Eh	VPS byte 5							
9Fh	VPS byte 6							
A0h	VPS byte 7							
A1h	VPS byte 8							
A2h	VPS byte 9							
A3h	VPS byte 10							
A4h	VPS byte 11							
A5h	VPS byte 12							
A6h	VPS byte 13							

These registers contain the entire VPS data line except the clock run–in code or the start code.

VITC Data Registers

Address	A7h–AFh

ADDRESS	7	6	5	4	3	2	1	0
A7h	VITC byte 1, frame byte 1							
A8h	VITC byte 2, frame byte 2							
A9h	VITC byte 3, seconds byte 1							
AAh	VITC byte 4, seconds byte 2							
ABh	VITC byte 5, minutes byte 1							
ACh	VITC byte 6, minutes byte 2							
ADh	VITC byte 7, hour byte 1							
AEh	VITC byte 8, hour byte 2							
AFh	VITC byte 9, CRC							

These registers contain the VITC data.

VBI FIFO Read Data Register

Address	B0h

7	6	5	4	3	2	1	0
FIFO read data							

This address is provided to access VBI data in the FIFO through the host port. All forms of teletext data come directly from the FIFO, while all other forms of VBI data can be programmed to come from the registers or from the FIFO. Current status of the FIFO can be found at address C6h and the number of bytes in the FIFO is located at address C7h. If the host port is to be used to read data from the FIFO, then the output formatter must be disabled at address CDh bit 0.

VDP Configuration RAM Register

Address	C3h-C5h

Address	7	6	5	4	3	2	1	0
C3h	Configuration data							
C4h	RAM address (7:0)							
C5h	Reserved							RAM address 8

The configuration RAM data is provided to initialize the VDP with initial constants. The configuration RAM is 512 bytes organized as 32 different configurations of 16 bytes each. The first 12 configurations are defined for the current VBI standards. An additional 2 configurations can be used as a custom programmed mode for unique standards like Gemstar.

Address C3h is used to read or write to the RAM. The RAM internal address counter is automatically incremented with each transaction. Addresses C5h and C4h make up a 9–bit address to load the internal address counter with a specific start address. This can be used to write a subset of the RAM for only those standards of interest. Registers D0h-FBh must all be programmed with FFh, before writing or reading the configuration RAM. Full field mode (CFh) must be disabled as well.

VDP Status Register

Address	C6h

7	6	5	4	3	2	1	0
FIFO full error	FIFO empty	TTX available	CC field 1 available	CC field 2 available	WSS available	VPS available	VITC available

The VDP status register indicates whether data is available in either the FIFO or data registers, and status information about the FIFO. Reading data from the corresponding register does not clear the status flags automatically. These flags are only reset by writing a 1 to the respective bit. However, bit 6 is updated automatically.

FIFO full error:

0 = No FIFO full error
1 = FIFO was full during a write to FIFO.

The FIFO full error flag is set when the current line of VBI data can not enter the FIFO. For example, if the FIFO has only 10 bytes left and teletext is the current VBI line, the FIFO full error flag is set, but no data is written because the entire teletext line will not fit. However, if the next VBI line is closed caption requiring only 2 bytes of data plus the header, this goes into the FIFO. Even if the full error flag is set.

FIFO empty:

0 = FIFO is not empty.
1 = FIFO is empty.

TTX available:

0 = Teletext data is not available.
1 = Teletext data is available.

CC field 1 available:

0 = Closed caption data from field 1 is not available.
1 = Closed caption data from field 1 is available.

CC field 2 available:

0 = Closed caption data from field 2 is not available.
1 = Closed caption data from field 2 is available.

WSS available:

0 = WSS data is not available.
1 = WSS data is available.

VPS available:

0 = VPS data is not available.
1 = VPS data is available.

VITC available:

0 = VITC data is not available.
1 = VITC data is available.

FIFO Word Count Register

Address	C7h

7	6	5	4	3	2	1	0
Number of words							

This register provides the number of words in the FIFO. 1 word equals 2 bytes.

FIFO Interrupt Threshold Register

Address	C8h

7	6	5	4	3	2	1	0
Number of words							

This register is programmed to trigger an interrupt when the number of words in the FIFO exceeds this value (default 80h). This interrupt must be enabled at address C1h. 1 word equals 2 bytes.

FIFO Reset Register

Address	C9h

7	6	5	4	3	2	1	0
Any data							

Writing any data to this register resets the FIFO and clears any data present.

Line Number Interrupt Register

Address	CAh

7	6	5	4	3	2	1	0
Field 1 enable	Field 2 enable	Line number					

This register is programmed to trigger an interrupt when the video line number matches this value in bits 5:0. This interrupt must be enabled at address C1h. The value of 0 or 1 does not generate an interrupt.

Field 1 enable:

0 = Disabled (default)
1 = Enabled

Field 2 enable:

0 = Disabled (default)
1 = Enabled

Line number: (default 00h)

Pixel Alignment Registers

Address	CBh-CCh

Address	7	6	5	4	3	2	1	0
CBh	Switch pixel [7:0]							
CCh	Reserved						Switch pixel [9:8]	

These registers form a 10–bit horizontal pixel position from the falling edge of sync, where the VDP controller initiates the program from one line standard to the next line standard. For example, the previous line of teletext to the next line of closed caption. This value must be set so that the switch occurs after the previous transaction has cleared the delay in the VDP, but early enough to allow the new values to be programmed before the current settings are required.

FIFO Output Control Register

Address	CDh

7	6	5	4	3	2	1	0
Reserved							Host access enable

This register is programmed to allow I^2C access to the FIFO or allowing all VDP data to go out the video port.

Host access enable:

0 = Output FIFO data to the video output Y[7:0]
1 = Allow I^2C access to the FIFO data (default)

Full Field Enable Register

Address	CFh

7	6	5	4	3	2	1	0
Reserved							Full field enable

This register enables the full field mode. In this mode, all lines outside the vertical blank area and all lines in the line mode registers programmed with FFh are sliced with the definition of register FCh. Values other than FFh in the line mode registers allow a different slice mode for that particular line.

Full field enable:

0 = Disable full field mode (default)
1 = Enable full field mode

Line Mode Registers

Address	D0h-FBh

ADDRESS	7	6	5	4	3	2	1	0
D0h	Line 6 Field 1							
D1h	Line 6 Field 2							
D2h	Line 7 Field 1							
D3h	Line 7 Field 2							
D4h	Line 8 Field 1							
D5h	Line 8 Field 2							
D6h	Line 9 Field 1							
D7h	Line 9 Field 2							
D8h	Line 10 Field 1							
D9h	Line 10 Field 2							
DAh	Line 11 Field 1							
DBh	Line 11 Field 2							
DCh	Line 12 Field 1							
DDh	Line 12 Field 2							
DEh	Line 13 Field 1							
DFh	Line 13 Field 2							
E0h	Line 14 Field 1							
E1h	Line 14 Field 2							
E2h	Line 15 Field 1							
E3h	Line 15 Field 2							
E4h	Line 16 Field 1							
E5h	Line 16 Field 2							
E6h	Line 17 Field 1							
E7h	Line 17 Field 2							
E8h	Line 18 Field 1							
E9h	Line 18 Field 2							
EAh	Line 19 Field 1							
EBh	Line 19 Field 2							
ECh	Line 20 Field 1							
EDh	Line 20 Field 2							
EEh	Line 21 Field 1							
EFh	Line 21 Field 2							
F0h	Line 22 Field 1							
F1h	Line 22 Field 2							
F2h	Line 23 Field 1							
F3h	Line 23 Field 2							
F4h	Line 24 Field 1							
F5h	Line 24 Field 2							
F6h	Line 25 Field 1							

F7h	Line 25 Field 2
F8h	Line 26 Field 1
F9h	Line 26 Field 2
FAh	Line 27 Field 1
FBh	Line 27 Field 2

These registers program the specific VBI standard at a specific line in the video field.

Bit 7:

0 = Disable filtering of null bytes in closed caption modes
1 = Enable filtering of null bytes in closed caption modes (default)

In teletext modes, bit 7 enables the data filter function for that particular line. If it is set to 0, then the data filter passes all data on that line.

Bit 6:

0 = Send VBI data to registers only.
1 = Send VBI data to FIFO and the registers. Teletext data only goes to FIFO. (default)

Bit 5:

0 = Allow VBI data with errors in the FIFO
1 = Do not allow VBI data with errors in the FIFO (default)

Bit 4:

0 = Do not enable error detection and correction
1 = Enable error detection and correction (when bits [3:0] = 1 2, 3, and 4 only) (default)

Bits [3:0]:

0000 = WST SECAM
0001 = WST PAL B
0010 = WST PAL C
0011 = WST NTSC
0100 = NABTS NTSC
0101 = TTX NTSC
0110 = CC PAL
0111 = CC NTSC
1000 = WSS PAL
1001 = WSS NTSC
1010 = VITC PAL
1011 = VITC NTSC
1100 = VPS PAL
1101 = Custom 1
1110 = Custom 2
1111 = Active video (VDP off) (default)

A value of FFh in the line mode registers is required for any line to be sliced as part of the full field mode.

Full Field Mode Register

Address	FCh

7	6	5	4	3	2	1	0
Full field mode							

This register programs the specific VBI standard for full field mode. It can be any VBI standard. Individual line settings take priority over the full field register. This allows each VBI line to be programmed independently but have the remaining lines in full field mode. The full field mode register has the same definitions as the line mode registers (default 7Fh).

Appendix B. Sample TVP5150A WinVCC4 CMD File for VBI Setup

```
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
//  These commands can be used with the WinVCC4 EVM software to configure the Line Mode
//   registers for a typical NTSC VBI setup.
//   The WR_REG commands are direct writes to the I2C registers.
//   Each command shown writes 1 byte to the VBUS address
//  specified in the command line.
BEGIN_DATASET

DATASET_NAME,"TVP5150A NTSC VDP/VBI SETUP"
INCLUDE, VDPRegsIdle.inc                // Set VDP registers to their default state
INCLUDE, SlicerRAM_601.inc              // Load VDP configuration RAM

WR_REG,VID_DEC,0x01,0xD8,0x44           // Line10  (Field 1)-TTX NTSC
WR_REG,VID_DEC,0x01,0xD9,0x44           // Line10 (Field 2)-TTX NTSC
WR_REG,VID_DEC,0x01,0xE0,0x0B           // Line14 (Field 1)-VITC NTSC
WR_REG,VID_DEC,0x01,0xE1,0x0B           // Line14 (Field 2)-VITC NTSC
WR_REG,VID_DEC,0x01,0xEC,0x09           // Line20  (Field 1)-WSS NTSC
WR_REG,VID_DEC,0x01,0xED,0x09           // Line20 (Field 2)-WSS NTSC
WR_REG,VID_DEC,0x01,0xEE,0x07           // Line21 (Field 1)- CC NTSC
WR_REG,VID_DEC,0x01,0xEF,0x07           // Line21 (Field 2)- CC NTSC

WR_REG,VID_DEC,0x01,0xCD,0x01           // Enable FIFO access, disable ANC data
WR_REG,VID_DEC,0x01,0xCB,0x4E           // Set Pixel Alignment [7:0] to 4Eh
WR_REG,VID_DEC,0x01,0xCC,0x00           // Set pixel Alignment [9:8] to 0

END_DATASET
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
```

```
//  These commands can be used with the WinVCC4 EVM software to configure the Line Mode
//  registers for a typical PAL VBI setup.  For PAL systems, the Line Mode register has a +3 line
//  offset relative to the actual line number.  Each command shown writes 1 byte to the I2C
//  address  specified in the command line.
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
BEGIN_DATASET
DATASET_NAME,"TVP5150A PAL VDP/VBI SETUP"
INCLUDE, VDPRegsIdle.inc                // Set VDP registers to their default FFh state
INCLUDE, SlicerRAM_601.inc              // Load VDP configuration RAM

WR_REG,VID_DEC,0x01,0xD8,0x41           // Line10  (Field 1)-TTX-B PAL(Line7)
WR_REG,VID_DEC,0x01,0xD9,0x41           // Line10 (Field 2)-TTX-B PAL (Line7
WR_REG,VID_DEC,0x01,0xEA,0x0C           // Line19  (Field 1)-VPS PAL (Line 16)
WR_REG,VID_DEC,0x01,0xEB,0x0C           // Line19 (Field 2)-VPS PAL (Line 16)
WR_REG,VID_DEC,0x01,0xF0,0x0A           // Line22 (Field 1)-VITC PAL(Line 19)
WR_REG,VID_DEC,0x01,0xF1,0x0A           // Line22 (Field 2)-VITC PAL(Line 19)
WR_REG,VID_DEC,0x01,0xF6,0x06           // Line25  (Field 1)-CC PAL(Line 22)
WR_REG,VID_DEC,0x01,0xF7,0x06           // Line25 (Field 2)- CC PAL(Line 22)
WR_REG,VID_DEC,0x01,0xF8,0x08           // Line26  (Field 1)-WSS PAL(Line 23)
WR_REG,VID_DEC,0x01,0xF9,0x08           // Line26  (Field 2)-WSS PAL(Line 23)

WR_REG,VID_DEC,0x01,0xCD,0x01           // Enable FIFO access, disable ANC data
WR_REG,VID_DEC,0x01,0xCB,0x4E           // Set Pixel Alignment [7:0] to 4Eh
WR_REG,VID_DEC,0x01,0xCC,0x00           // Set pixel Alignment [9:8] to 0
END_DATASET
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
```

Appendix C. Example TVP5150A C Code

```
// TVP5150A WSS Example

#define TVP5150A 0xB8;                        // TVP5150A main I2C address
byte I2C_RegAddress,Status;
byte I2C_Data;
int CRAM_Address, count;
// recommended WSS settings
byte WSS_ARRAY[]={0x38,0,0x3F,0,0,0x71,0x6E,0x43,0x69,0x7C,0x08,0,0,0,0x39,0};
byte WSSData[3];      // data array for WSS

////////////////////////////////////////////////////////////////////////////
// initialize
////////////////////////////////////////////////////////////////////////////
// load WSS C-RAM
I2C_RegAddress = 0xD0;                        // starting address of Line Mode Registers
I2C_Data = 0xFF;
For (count = 0; count < 44; count ++)
{
   I2CWriteByte(TVP5150A, I2C_RegAddress, I2C_Data);  //write FFh to LineMode registers
   I2C_RegAddress ++;
}
I2CWriteByte(TVP5150A, 0xCF, 0);                 // disable full field mode
CRAM_Address = 0x130;                            // address of NTSC WSS C-RAM block

I2CWriteByte(TVP5150A, 0xC4, 0x30);              // load C4h with C-RAM address[7:0]
I2CWriteByte(TVP5150A, 0xC5, 0x01);              // load C5h with C-RAM address[8]

For (count = 0; count < 16; count++)
{
 I2CWriteByte(TVP5150A, 0xC3, WSS_ARRAY[count]);   // write 16 bytes of WSS C-RAM data
}                                                   // to register C3h.
I2CWriteByte(TVP5150A, 0xCB, 0x4E);    // Set Pixel Alignment [7:0]to 0x4E
I2CWriteByte(TVP5150A, 0xCC, 0x00);    // Set Pixel Alignment [9:8]to 0x00

//  NTSC WSS Line Mode setup for line 20 of both fields
I2CWriteByte(TVP5150A, 0xEC, 0x09);    // line 20 field 1 (0xEC), mode bits = 0x09
I2CWriteByte(TVP5150A, 0xED, 0x09);    // line 20 field 2 (0xED), mode bits = 0x09

//  PAL WSS Line Mode setup for line 23 (source input) of both fields.  PAL line
// numbering has 3 line offset so the Line 26 line mode registers are used.

I2CWriteByte(TVP5150A, 0xF8, 0x08);    // line 26 field 1 (0xF8), mode bits = 0x08
I2CWriteByte(TVP5150A, 0xF9, 0x08);    // line 26 field 2 (0xF9), mode bits = 0x08
I2CWriteByte(TVP5150A, 0xCD, 0x01);    // disable ANC data, enable FIFO access.

////////////////////////////////////////////////////////////////////////////////
// check status and get sliced data
////////////////////////////////////////////////////////////////////////////////

I2CReadBuffer(TVP5150A,0xC6,&Status,1);   //read 1 byte(status)from register C6h

If ((Status & 0x20) ==1)
{
   I2CReadBuffer(TVP5150A,0x94,&WSSData[0],3);   //if WSS bit set, read the 3 WSS bytes
//                                                 // at WSS Data registers 94h–96h.
   I2CWriteByte(TVP5150A,0xC6,0x20);              // clear WSS available status bit
}
```

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