Application Report
SLLA338–June 2013

The Benefits of Using Linear Equalization in Backplane and Cable Applications

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ABSTRACT

Signal integrity has been an important topic for many years and will continue to be an important topic as data rates keep increasing. Signals have to travel through various interconnects inside a system to reach their destination so any electrical degradation induced at the transmitter, connectors, traces, cabling, and the receiver will have an effect on the timing and quality of the signal. These waveform distortions are caused by impedance mismatches like stubs and vias, frequency dependent attenuation, and electromagnetic coupling between signal traces (crosstalk). As system designs get more complicated with additional channels being added side by side signal integrity issues become even more critical and demand appropriate countermeasures. The scope of this application report is to examine Linear Equalization and the benefits that it brings to backplane and active cable designs especially if any type of link training is involved or assumptions about the channel are made.

Contents

List of Figures

List of Tables

1 Introduction

A high speed signal moving through a channel is subjected to high frequency impairments such as reflections, dielectric loss, and loss due to the skin effect. These impairments degrade the quality of the signal making it problematic for a receiver to interpret it correctly. Copper channels are described as a linear time invariant (LTI) system that is represented in the frequency domain using s-parameters or in the time domain using a symbol or step response. Figure 1 and Figure 2 respectively show the frequency response and symbol response of a 24 inch by 4 mil differential stripline implemented on FR4.

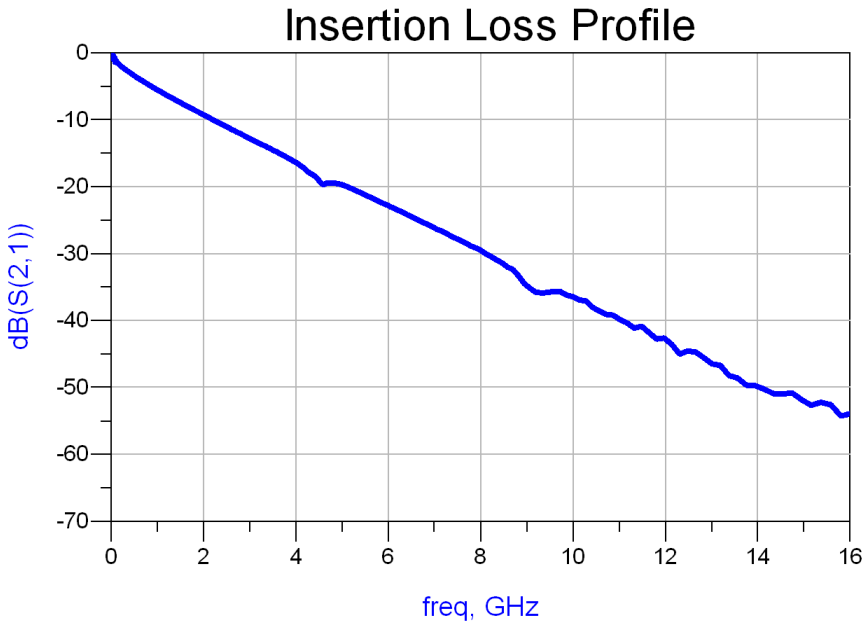

Figure 1. Insertion Loss (SDD21) – 24in x 4mil Trace

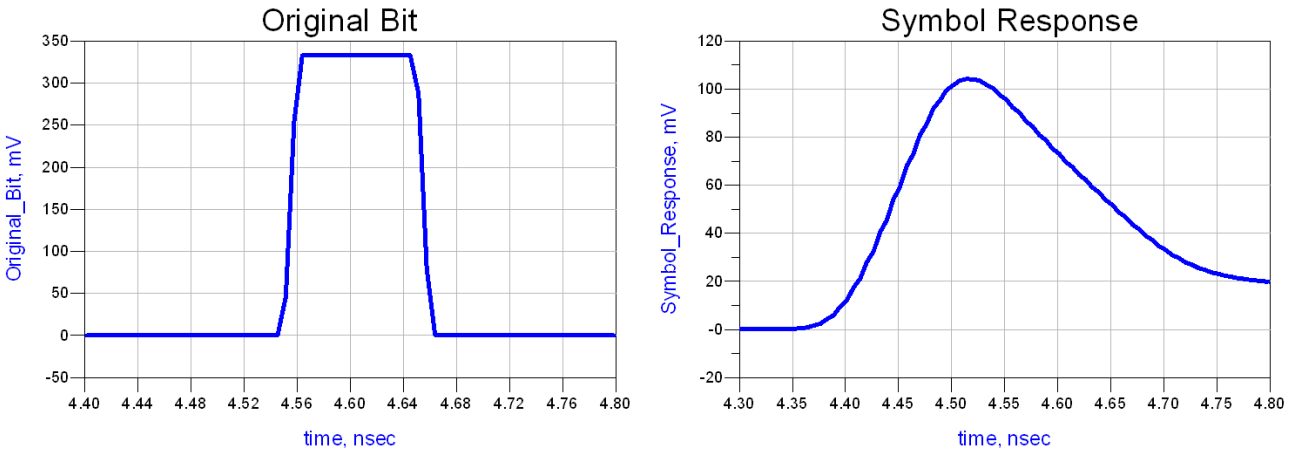

Figure 2. Symbol Response – 24in x 4mil Trace

Legacy copper backplanes do not provide adequate bandwidth to support the higher signaling rates of 5-10Gbps or more. So, to improve upon the quality of a link engineers can design in signal conditioning devices such as equalizers. Equalizers are devices that compensate high frequency impairments induced by a channel between a transmitter and receiver. Analog equalization can be achieved through Continuous Time Linear Equalizers (CTLE) while discrete time equalization can be achieved through Feed

Forward Equalization (FFE) and/or Decision Feedback Equalization (DFE). At data rates of 8 Gbps and greater one or more of these equalization schemes is typically implemented in end to end communication systems. If the impairments associated with these signaling rates through traditional copper mediums exceed the allowable link budget that is defined in the various supporting standards additional equalization can be applied.

2 Equalization

Equalization is a signal conditioning technique in which a waveform is manipulated either at the transmitter, at the receiver, or by a signal conditioner somewhere throughout a link in order to compensate the distortions due to a channel. In copper channels the goal is to provide a flat frequency response up to the fundamental frequency by compensating the frequency dependent loss of the LTI channel. Equalization can also be used to effectively shorten the electrical length of the channel by providing partial *linear equalization* thus aiding designers in meeting or exceeding the link budget that they planned for in their design.

Transmit equalization is implemented in FPGAs, repeaters, redrivers, and in Texas Instruments SerDes devices like the TLK10034 and the TLK10232. Transmit equalization pre-distorts a transmitted signal by amplifying the high frequency content of the signal to compensate for the expected amount of loss through the channel. The emphasized portion of the signal is attenuated by the channel resulting in an open eye that can be easily interpreted by the receiver. Figure 3 shows an example of transmit equalization.

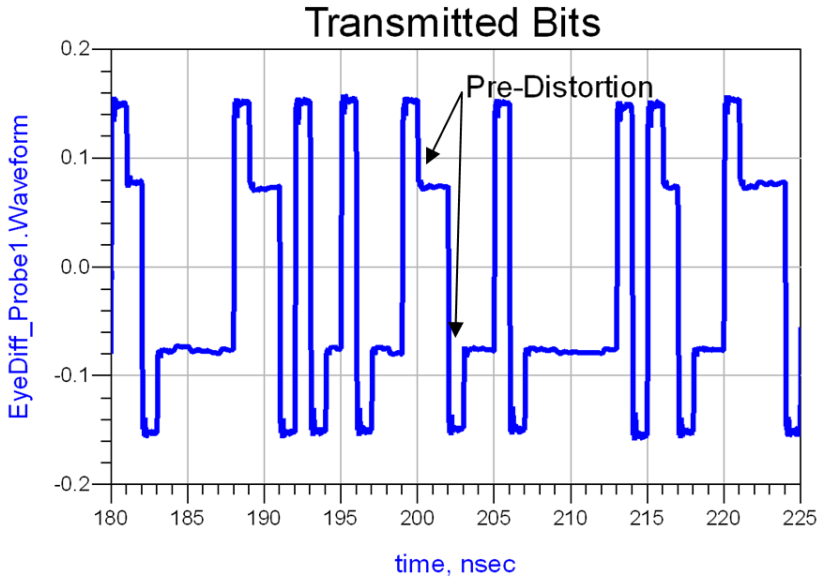

Figure 3. Transmit Equalization

Equalization can be implemented in the receiver side as well compensating loss after a signal travels through a channel by restoring high frequency content that was lost due to the channel attenuation. Figure 4 below shows an example of the effect equalization has when implemented in a 10Gbps link transmitting 8B/10B encoded data distorted by the channel.

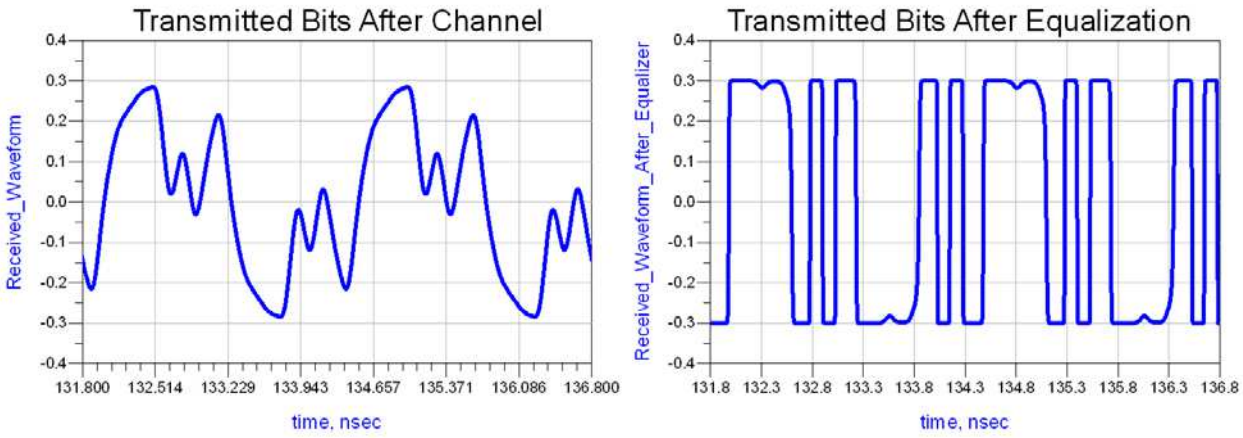

Figure 4. Receive Equalization

Transmit and receive equalization are techniques that can be part of a redriver or repeater, designers can insert in the channel of their designs to provide the advantage of extended reach or more link margin while also overcoming the bandwidth limitations of copper channels at higher data rates. If devices are injected in the channel they have to work seamlessly in the system providing as small as possible latency, low power, and low cost. Multi stage CTLEs are the most inexpensive, low power option for these kinds of devices. The multiple stages can be adapted very well to the channel loss. Another advantage is that these devices are pretty much transparent to data rates and don't need reference clocks. If the device is kept fully linear people speak of "*Linear Equalizers*" if a limiting amplifier is added after the CTLE the device is called a "Limiting Equalizer" although the equalization process is linear in both devices.

2.1 Limiting Equalizers

Limiting equalizers such as the TLK1101E have the advantage of restoring a signals amplitude after the equalization so that a device that follows it would not need any equalization. Active copper cables with SFP+ connectors are an application candidate for these types of devices.

2.2 Linear Equalization and the SN65LVCP141x

Linear Equalizers do not have a limiter after the CTLE. This has a couple advantages in channels especially if there is already end to end equalization available. They can be thought of as electrically shortening the channel leaving the nature of the channel and the transmitted signal intact so the end to end equalization can still be reused. This allows a very low power link or margin increase. Compared to retimed solution the latency of *Linear Equalizers* is negligible and they are transparent for the link training. Boosting the attenuated signal in front of a crosstalk sensitive part of the channel can help to improve bit error rate.

Texas Instruments recently introduced two *Linear Equalizers* in the SN65LVCP1412 and SN65LVCP1414. These two devices deliver an asynchronous, protocol-agnostic, low latency, two and four channel architecture for use up to 14.2Gbps in backplane and active cable applications. The architectures of the SN65LVCP1412 and SN65LVCP1414 are designed to work with an ASIC or an FPGA which employ decision feedback equalization (DFE). Figure 5 shows the typical EQ gain curves for both the SN65LVCP1412 and SN65LVCP1414. As a signal travels through an LTI channel the lower frequencies are attenuated less than the higher frequencies. The SN65LVCP141x family of devices compensates for this behavior by providing a channel matched high pass frequency response, with either no attenuation or an attenuation of -6dB, across the lower frequencies while adding a selectable amount of gain at the upper frequencies. With up to 17dB of gain at 7.1GHz the SN65LVCP141x devices allow designers the flexibility to plan for an extended link budget in copper systems that traditionally would not support it.

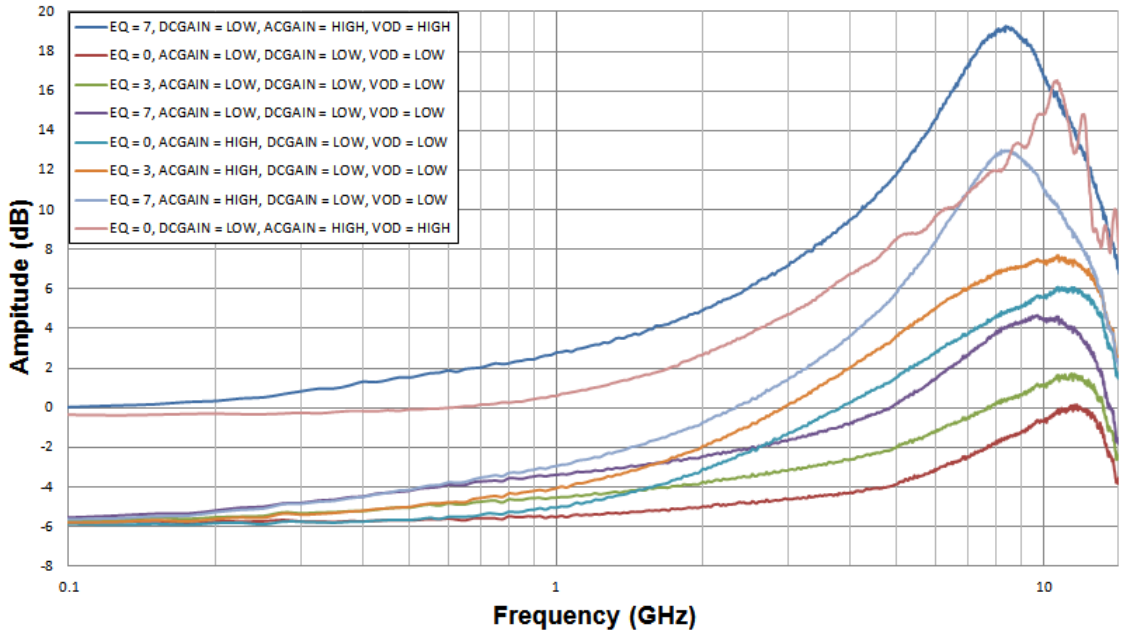

Figure 5. SN65LVCP141x Gain Profile Curves

Figure 6 and Figure 7 demonstrates the capability of the SN65LVCP141x devices to shorten the electrical channel length between devices. The symbol response illustrates how the SN65LVCP1414 removes the effects of ISI from the 6-meter cable reducing the number of taps that will be required by a DFE receiver. The frequency response plot shows the insertion loss profile (S_{21}) of a 3-meter cable, 6-meter cable, and 6-meter active cable with a SN65LVCP1414 device implemented. The insertion loss of the 6-meter cable is effectively cut in half making the 6-meter cable appear in the system as a 3-meter cable.

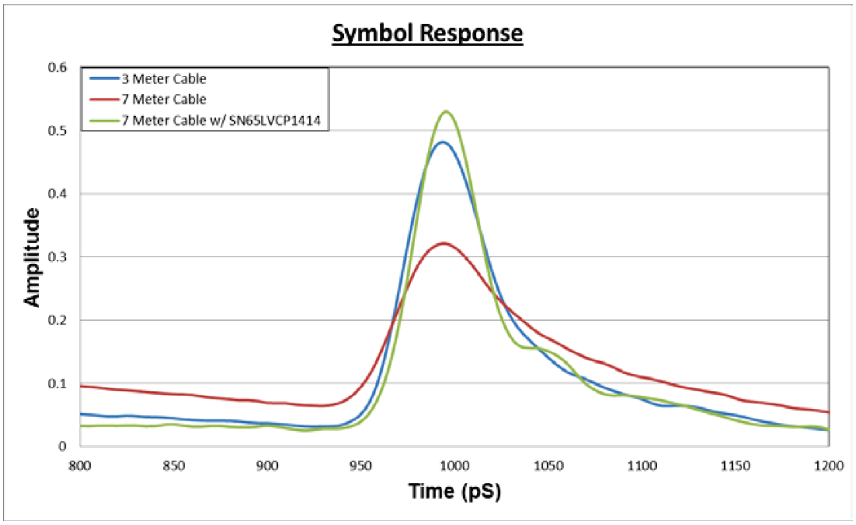

Figure 6. Symbol Response

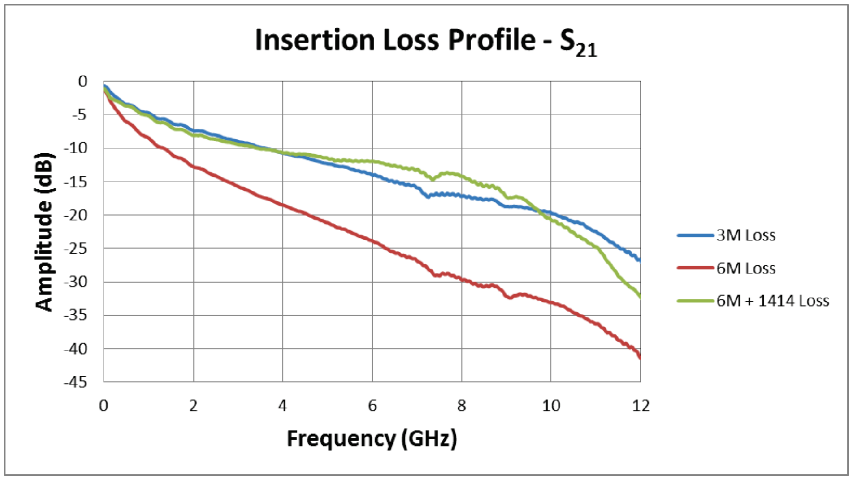

Figure 7. Insertion Loss Profile - S21

3 Simulations

Appropriate simulation is vital to predict performance in a design. This section of the application report uses Agilent's Advanced Design System tool (ADS) to showcase the performance and feature set of the SN65LVCP1412 and SN65LVCP1414 *Linear Equalizers*. The modeling is done using an s-parameter model for the devices which is available for download at http://www.ti.com/product/sn65lvcp1412 and http://www.ti.com/product/sn65lvcp1414. Texas Instruments also offers AMI models for these devices and it is available upon request at http://e2e.ti.com/support/interface/high_speed_interface/default.aspx.

A simple test bench was created in ADS to plot the eye diagrams across various lengths of trace. The results show that a good correlation can be made between the simulated data and measured data presented later in this application report. Figure 8 below shows the ADS test bench design that was used to simulate the eye diagram plots for a 4in x 4mil, 8in x 4mil and 16in x 4mil trace with and without the SN65LVCP1414 device implemented.

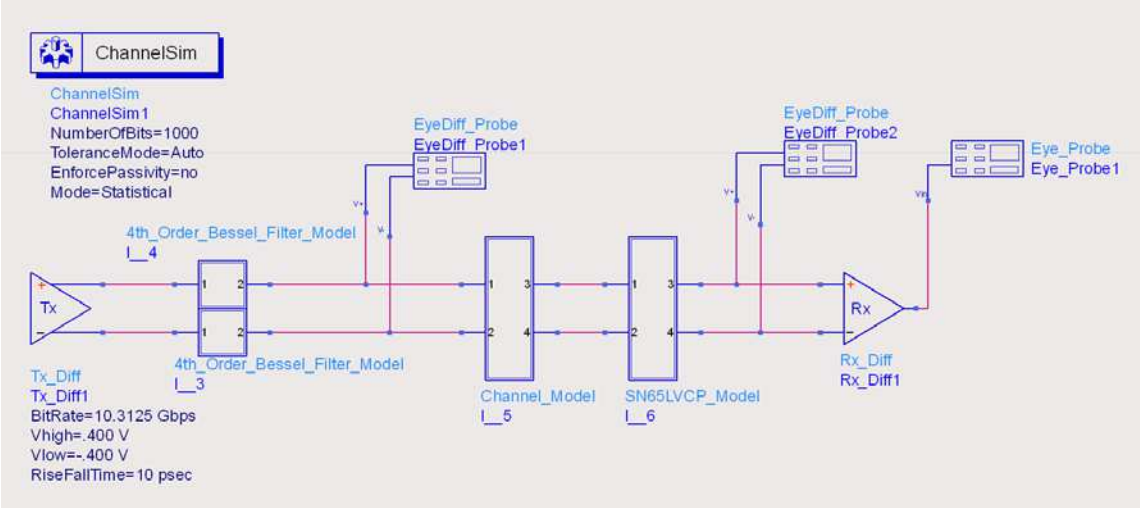

Figure 8. ADS Test Bench

Figure 9 shows that in simulation the SN65LVCP1414 passes a pre-distorted waveform unimpeded and recovers the transmitted pre-emphasis levels. Figure 10 through Figure 12 depict the eye plots that were collected across various loss profiles during simulations.

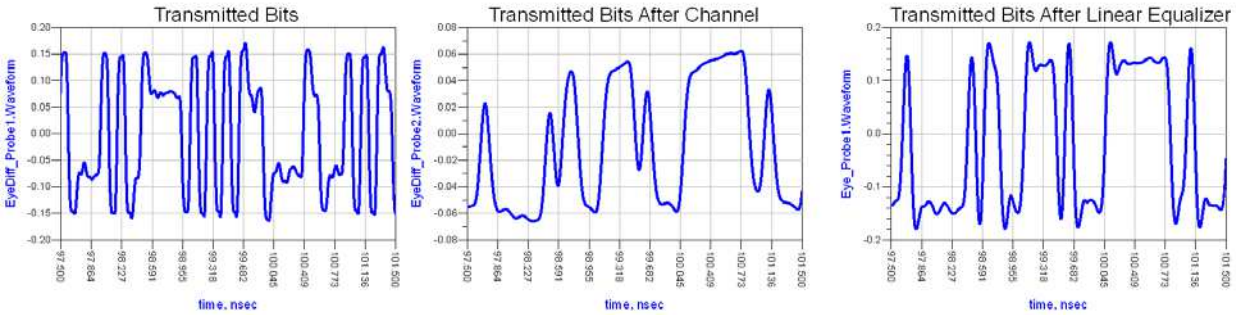

Figure 9. Pre Cursor and Post Cursor Taps Applied to Channel with Linear Equalizer Present

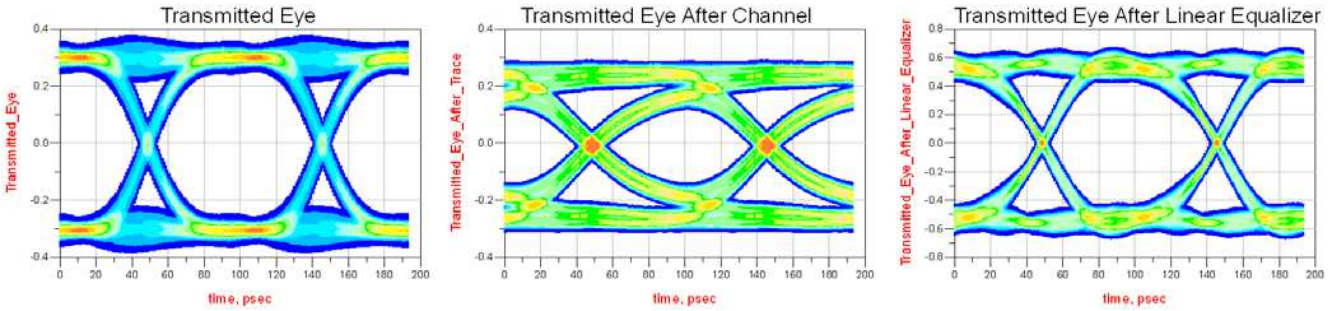

Figure 10. Eye Diagram - 4in x 4mil Trace

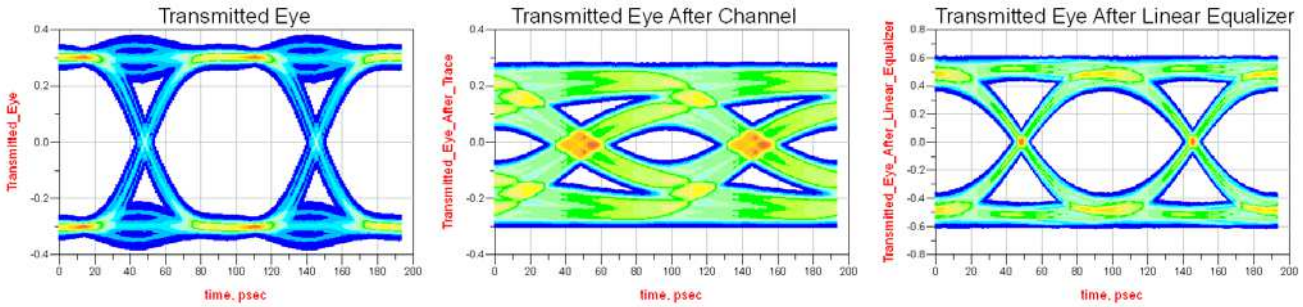

Figure 11. Eye Diagram - 8in x 4mil Trace

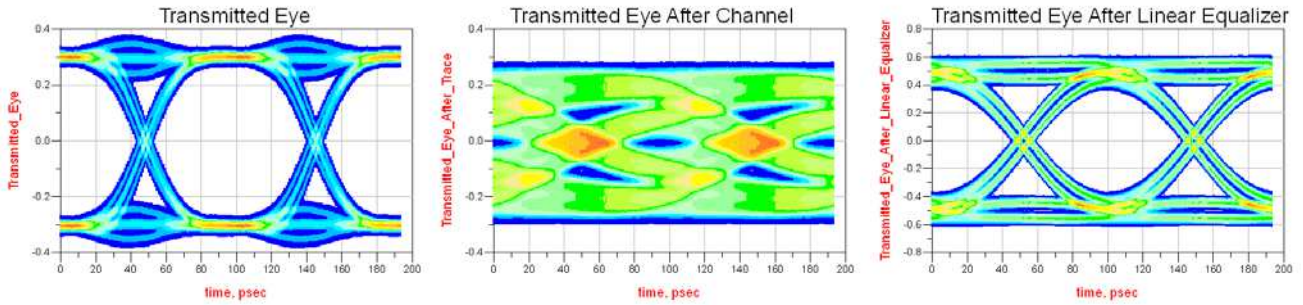

Figure 12. Eye Diagram - 16in x 4mil Trace

More detailed channel modeling simulations are possible using both the s-parameter model and the IBIS-AMI model. These examples just show the ease of implementation and reliability that simulation can bring to your design process.

4 Lab Data

This section of the application report validates the effectiveness of *Linear Equalization* by showing that a waveform containing pre cursor and post cursor taps from the TLK10034 SerDes is passed by the SN65LVCP1414 device unimpeded. Also, eye diagrams for a 4in x 4mil, 8in x 4mil and 16in x 4mil trace with and without the SN65LVCP1414 device are plotted for comparison to those that were generated using the s-parameter model in the simulation section of this application report.

4.1 Expriment Setup

The lab testing was performed using Texas Instruments TLK10034 EVM and GUI because it is a KR compliant SerDes device with pre cursor and post cursor taps that can be configured on the fly. Figure 13 shows that Channel D of the TLK10034 is set up to pass 10G data through an FR4 backplane, the SN65LVCP1414 device and into a Lecroy SDA 825Zi oscilloscope. The results of this test demonstrate that the *Linear Equalizer* can be injected into a link allowing the channel to keep its natural flow through characteristics, while providing the ability to electrically shorten the channel.

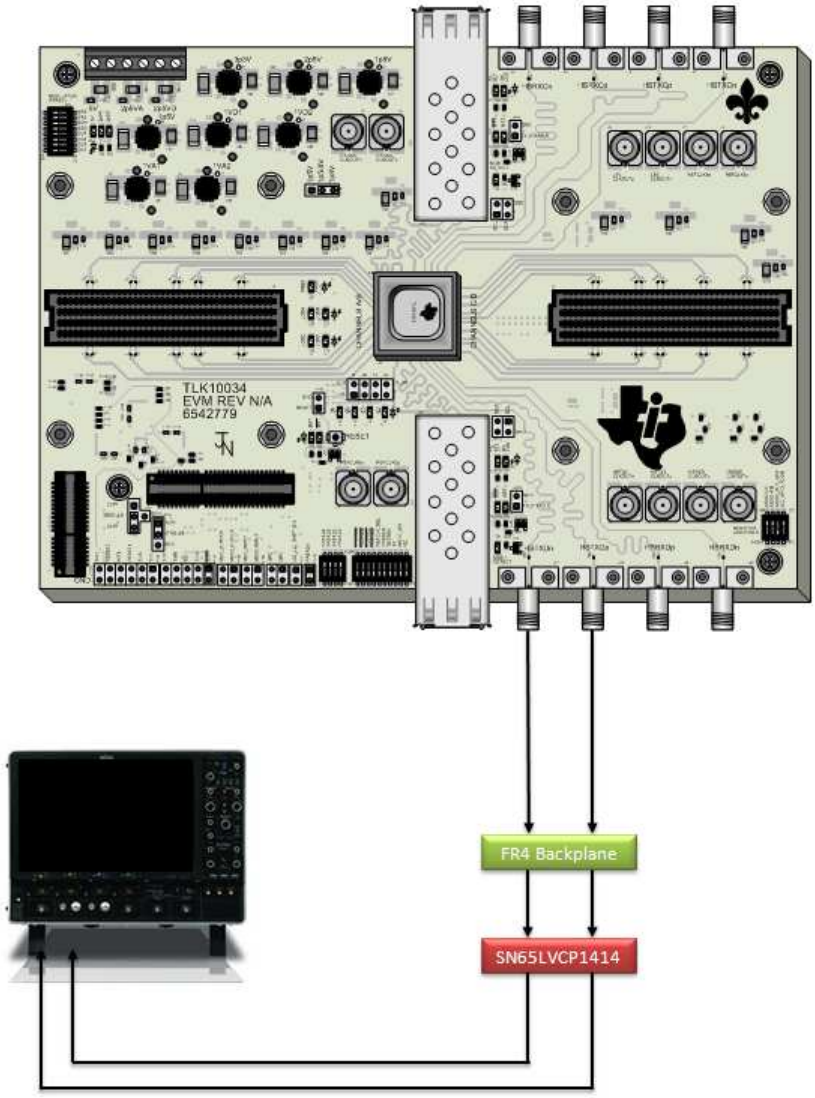

Figure 13. *Linear Equalization* **Test Setup**

4.2 Experiment Result

Figure 14, Figure 15, and Figure 16 shows screen captures from the oscilloscope of a pre-distorted waveform before and after the equalizer is implemented. It can be observed from the scope capture in Figure 14 that pre and post cursor taps have been implemented on the transmitted waveform prior to entering the SN65LVCP1414. Figure 15 and Figure 16 show that the *Linear Equalizer* pass the original waveform unimpeded by the output buffer stage. Figure 15 shows the output waveform with no EQ applied to the signal after a channel with ~3.5db of loss. Figure 16 shows the output waveform with a gain of ~5.98dB from the SN65LVCP1414 and a channel loss of ~6.6dB.

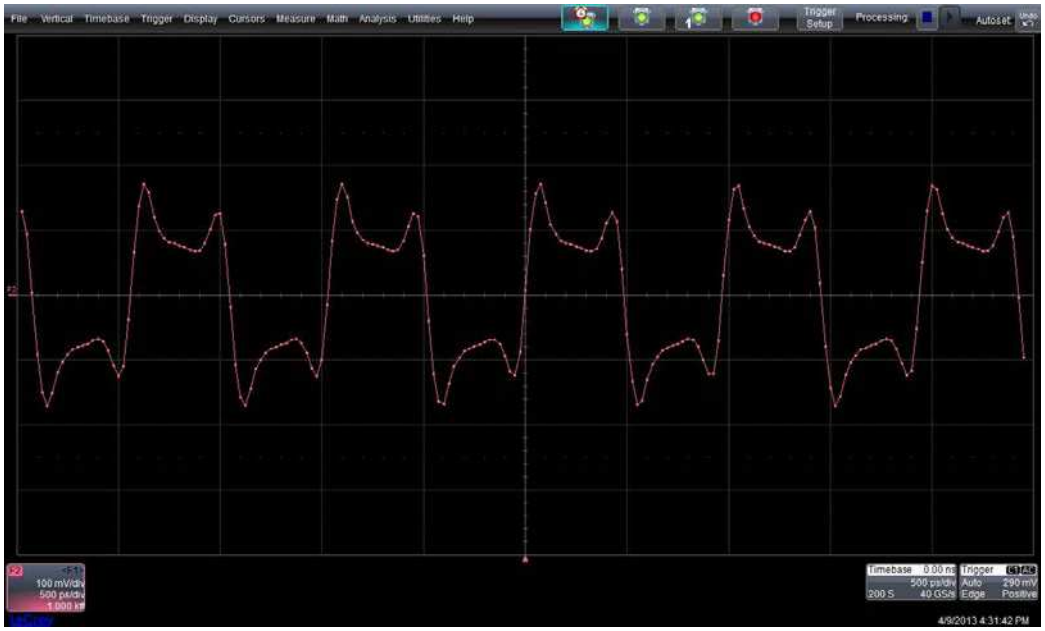

Figure 14. Pre Cursor and Post Cursor Taps Applied to Channel with 3.5dB of Loss

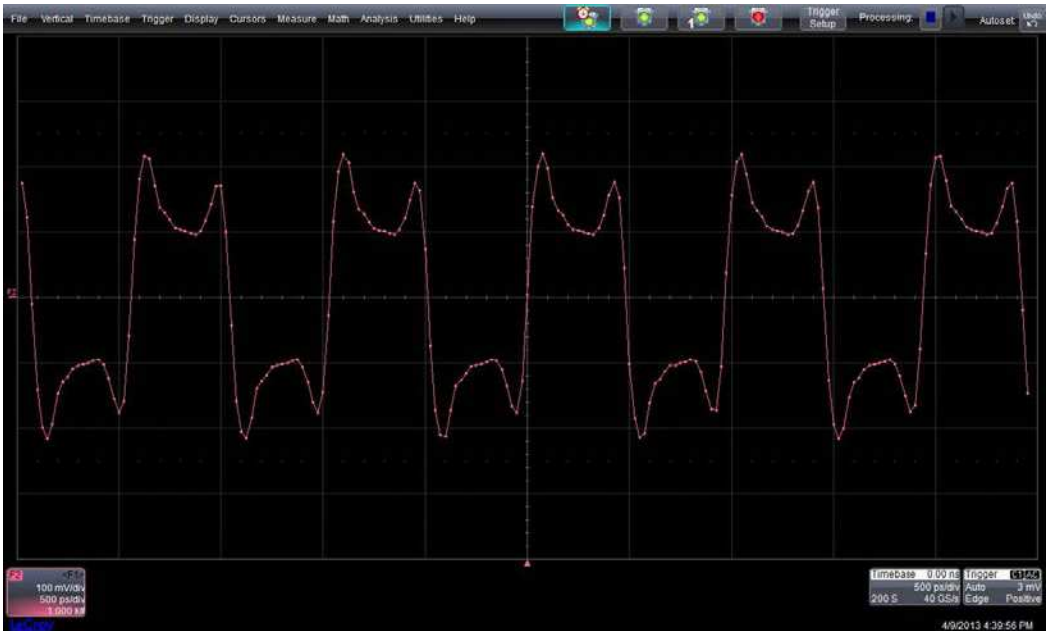

Figure 15. Pre Cursor & Post Cursor Taps Applied to Channel & *Linear Equalizer* with 3.5dB of Loss

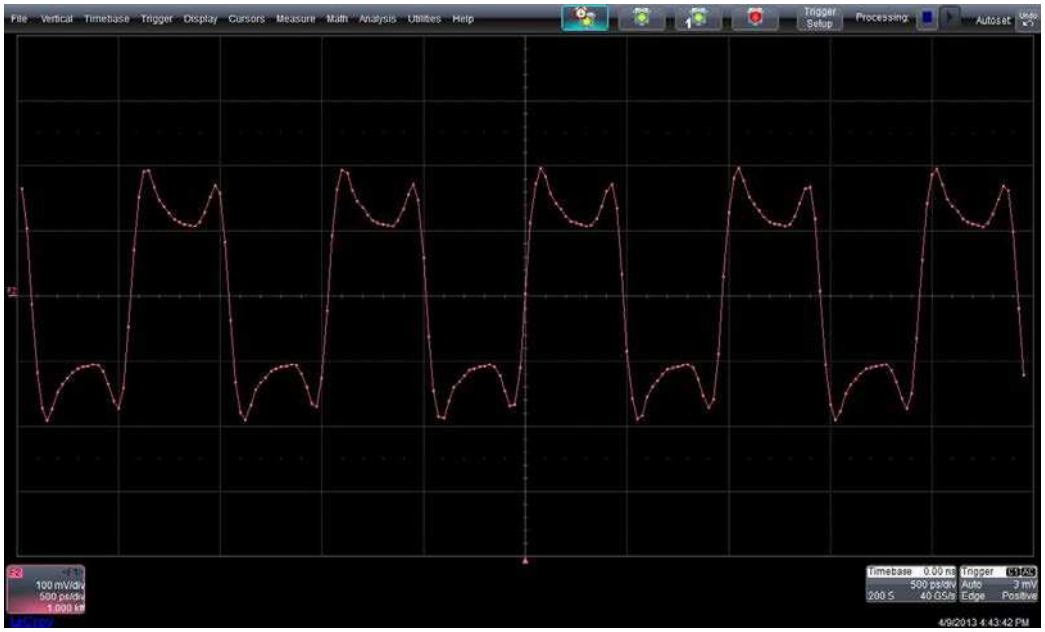

Figure 16. Pre Cursor & Post Cursor Taps Applied to Channel & *Linear Equalizer*with 6.6dB of Loss

Next, several eye diagrams were collected across various trace lengths to demonstrate the channel shortening ability of the SN65LVCP1414. No pre-emphasis or de-emphasis was implemented during these tests so that the loss induced due to the channel takes its full effect on the transmitted waveform. Figure 15 through Figure 20 show that *Linear Equalization* removes the effects of ISI induced by a channel lowering the total jitter (T_J) present in the system.

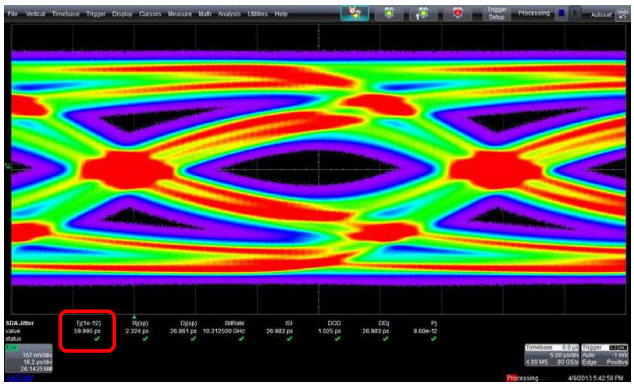

Figure 17. 4" x 4mil Channel No Equalizer Present (~3.5dB Loss)

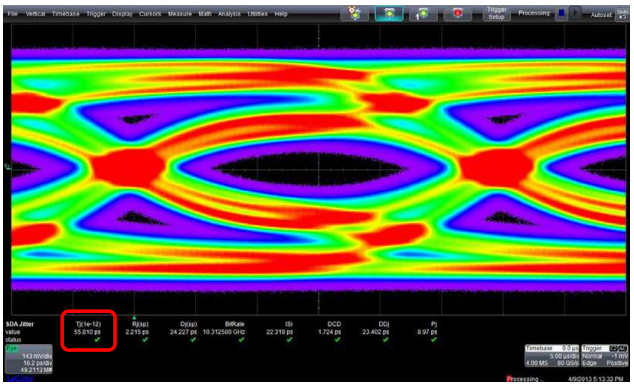

Figure 18. 4" x 4mil Channel – Equalizer Present (Eq=0/-3.5dB Loss)

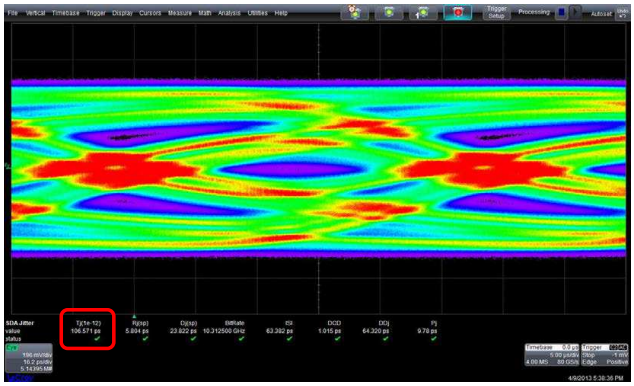

Figure 19. 8" x 4mil Channel – No Equalizer Present (>1UI of Total Jitter/~6dB of Loss)

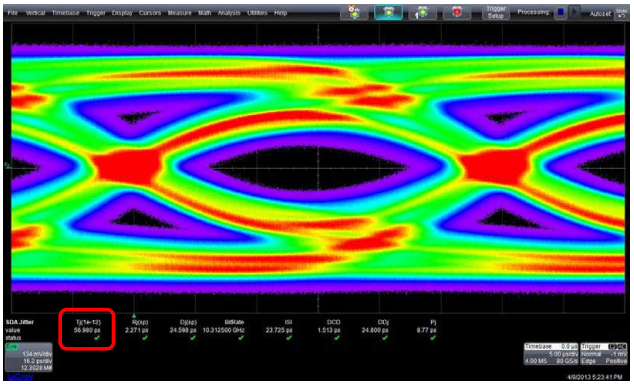

Figure 20. 8" x 4mil Channel – Equalizer Present (0 EQ Implemented/AC Gain Set to Medium/~6dB of Loss)

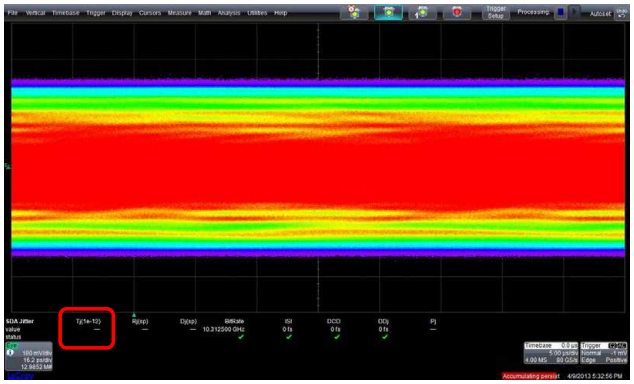

Figure 21. 16" x 4mil Channel – No Equalizer Present (>2UI of Total Jitter/~13dB of Loss)

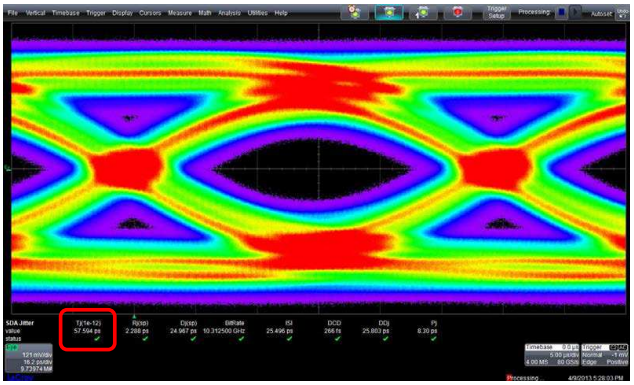

Figure 22. 16" x 4mil Channel – Equalizer Present (AC Gain Medium/Eq=2/Driver Peaking Enabled/~13dB of Loss)

Table 1. SN65LVCP141x Configuration

Trace Dimensions	Loss at 5 GHz (dB)[(1)]	$V_{OD(mV)}$	DC Gain	AC Gain	Driver Peaking	EQ	Total Jitter(pS)
4" x 4 mils	~3.5	–	–	–	–	–	59.995
4" x 4 mils	~3.5	1200	0.5	Low	Disabled	0	55.810
8" x 4 mils	~6	–	–	–	–	–	106.571 (>1 UI)
8" x 4 mils	~6	1200	0.5	Medium	Disabled	0	56.980
16" x 4 mils	~13	–	–	–	–	–	>2 UI
16" x 4 mils	~13	1200	0.5	Medium	Enabled	2	57.984

(1) All loss values were collected using an Agilent N5230A PNA-L Network Analyzer (VNA).

5 Conclusion

Linear Equalizers are cost and power effective devices that can be used to shorten a channel's electrical length by providing an extra boost to a signal aiding designers in meeting or exceeding their link budget. Limiting and *Linear Equalizers* both possess the ability to perform this function but *Linear Equalizers* are differentiated by their ability to be transparent and linear in nature when injected into a link. *Linear Equalizers* are ideal for application that implement out of band signaling (OOB), Auto Negotiation, or 10G-KR links as their linear input and output allow them to be protocol agnostic. With up to 17dB of gain at 7.1GHz the SN65LVCP141x devices give designers the flexibility of repurposing legacy copper designs or designing new extended reach copper channels at higher data rates for next generation designs.

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