Time-Base Oscillator for RTC ICs

Introduction

The operation of the time-base oscillator is critical to the time-keeping functions of the bq3285, bq4285, and bq4845 series of Real-Time-Clocks. For simplicity, the term "RTC" refers to this product family.

This application note describes some basic characteristics of the piezoelectric crystal and the on-chip crystal oscillator circuitry designed into the RTC. This application note also includes suggestions for achieving time-keeping accuracy and circumventing oscillator start-up problems.

Time-Base Crystal

The RTC time-base oscillator is designed to work with an external piezoelectric 32.768kHz crystal. A crystal can be represented by its electrical equivalent circuit and associated parameters as shown in Figure 1 and Table 1, respectively.

L_1, C_1, and R_1 are known as the motional arm of the circuit. L_1 is the motional inductance, C1 represents the motional capacitance of the quartz, and R_1 represents the equivalent motional arm resistance or series resistance. C_0 is the static or shunt capacitance and is the sum of the capacitance between electrodes and the capacitances added by the leads and mounting structure.

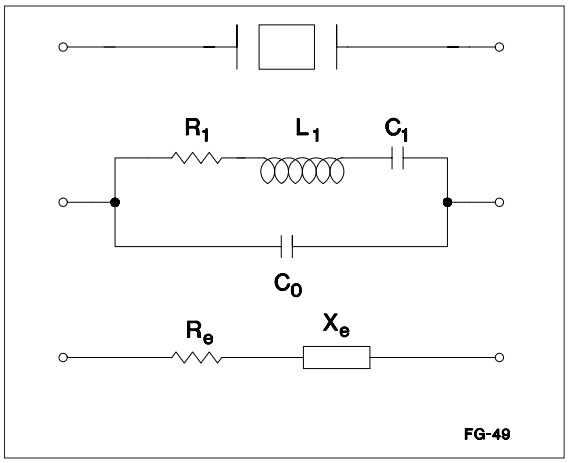

Figure 1. Equivalent Circuit of a Quartz Crystal

Table 1. Crystal Parameters

Parameter	Symbol	Unit
Nominal frequency	F	kHz
Load capacitance	C_L	pF
Motional inductance	L_1	H
Motional capacitance	C_1	pF
Motional resistance	R_1	KΩ
Shunt capacitance	C_0	pF

The basic circuit can be resolved into equivalent resistive (R_e) and reactive (X_e) components.

Crystal Operating Mode

The equivalent crystal impedance varies with the frequency of oscillation. Figures 2 and 3 show the variation of the equivalent reactance, X_e, with respect to frequency for KDS's DT-26 crystal. Figure 2 shows two points at which the crystal appears purely resistive

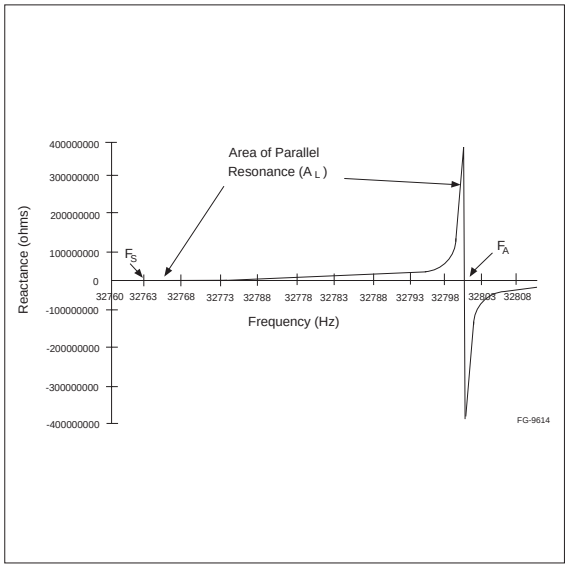

Figure 2. Variation of Reactance Around Resonance Points

(points at which $X_e = 0$). These points are defined as the series resonant (Fs) and anti-resonant (Fa) frequencies. Series resonant oscillator circuits are designed to oscillate at or near Fs. Parallel resonant circuits oscillate between Fs and Fa, depending upon the value of a parallel loading capacitor, C_L. The Benchmarq RTC uses a parallel resonant oscillator circuit.

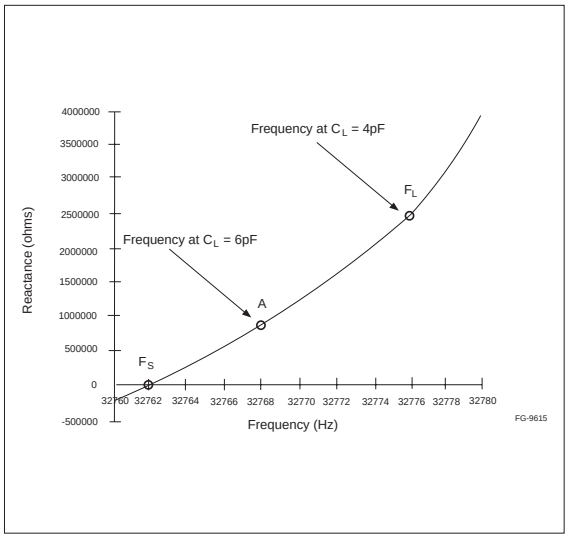

Figure 3. Detailed Area of Parallel Resonance

When a crystal is operating at parallel resonance, it looks inductive in a circuit (see Figure 4). Frequency will increase as load capacitance decreases. The load capacitance is the dynamic capacitance of the total circuit as measured or computed across the crystal terminals. In parallel circuit designs, the load capacitance should be selected to operate the crystal at a stable point on the Fs-Fa reactance curve as close to Fs as possible.

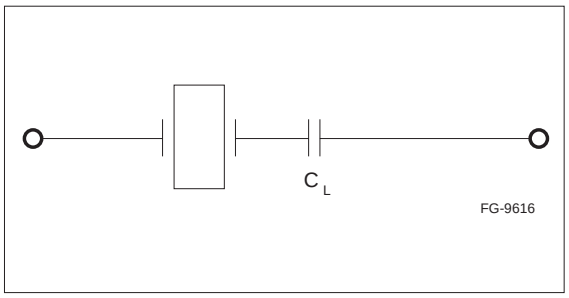

Figure 4. Parallel Resonance

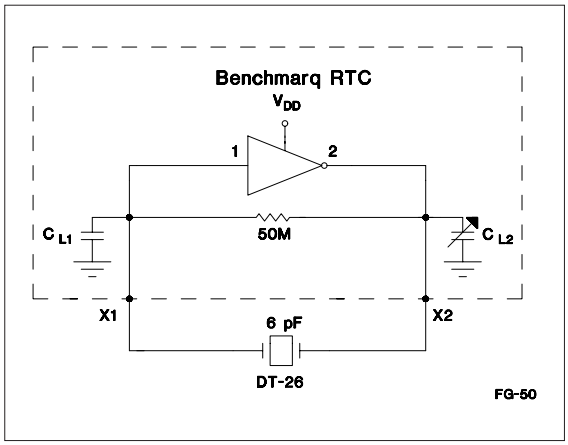

Figure 5. RTC Oscillator Circuit Block Diagram

Benchmarq RTC Oscillator

The parallel resonant RTC oscillator circuit comprises an inverting micro-power amplifier with a PI-type feedback network. Figure 5 illustrates a block diagram of the oscillator circuit with the crystal as part of the PI-feedback network. The oscillator circuit ensures that the crystal is operating in the area of parallel resonance (A_L) as shown in Figure 2.

Again, the actual frequency at which the circuit will oscillate depends on the load capacitance, C_L. A parallel resonant crystal, such as the DT-26 with a specified C_L = 6pF, is calibrated using a parallel resonant circuit. The approximate expression of the load capacitance, C_L, is computed from C_{L1} and C_{L2} as given below:

$$C_L \approx \frac{(C_{L1} * C_{L2})}{(C_{L1} + C_{L2})}$$

The RTC C_{L1} and C_{L2} values are trimmed to provide approximately a load capacitance of 6pF across the crystal terminals, thus matching the specified load capacitance at which the crystal is calibrated to resonate at the nominal frequency of 32.768kHz. Referring to the impedance curve of Figure 3, "A" indicates the point of resonance when C_L equals the specified load capacitance of the crystal.

Time-Keeping Accuracy

The RTC time-keeping accuracy mostly depends on the accuracy of the crystal, even though other considerations may affect it. The accuracy of the frequency of oscillation depends on the following:

- Crystal frequency tolerance

- Crystal frequency stability
- Crystal aging
- Effective load capacitance in oscillator circuit
- Board layout
- Drive level

Crystal Frequency Tolerance

The frequency tolerance parameter is the maximum frequency deviation from the nominal frequency (in this case, 32.768kHz) at a specified temperature, expressed in ppm of nominal frequency. The frequency tolerance, Δf/f, should typically be around ±20ppm at 25°C, which is the case for the Grade A, DT-26 crystal.

Crystal Frequency Stability

The maximum allowable deviation from nominal frequency over a specified range is the stability tolerance or temperature coefficient. This factor depends upon the angle of cut, the width/length ratio, the mode of vibration, and harmonics. This factor is normally expressed in terms of ppm or % of nominal frequency. Figure 6 shows a typical curve of frequency variation with temperature for the KDS DT-26 crystal.

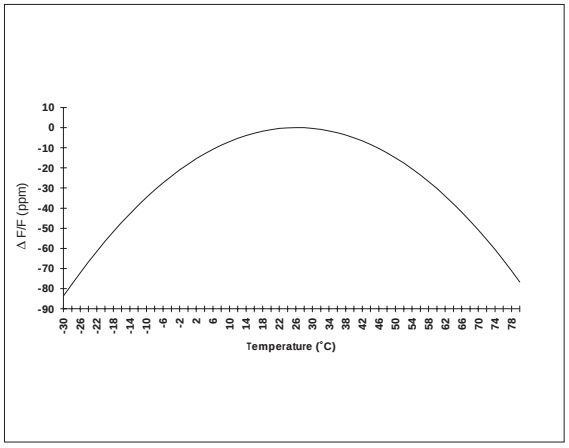

Figure 6. Typical Temperature Characteristics

Crystal Aging

Quartz crystal aging refers to the permanent change in operating frequency which occurs over time. The rate of change in frequency is fastest during the first 45 days of operation. Many factors affect aging, and the most common include the following: drive level, internal contamination, crystal surface change, ambient temperature, wire fatigue, and frictional wear. Drift with age is typically 4 ppm for the first year and 2 ppm per year for the life of the DT-26 crystal.

Load Capacitance

For a parallel resonant calibrated crystal, the crystal manufacturer specifies the load capacitance at which the crystal will "parallel" resonate at the nominal frequency. As the graph in Figure 3 displays, increasing the effective load capacitance by hanging additional capacitors on either of the RTC's X_1 or X_2 pins will effectively lower the resonant frequency, point "A," toward Fs. The resonant frequency with load capacitance, F_L, is given by the following:

$$F_L = F_S\left(1 + \frac{C_1}{2(C_0 + C_L)}\right)$$

where C_L is the effective load capacitance across the crystal inputs, which includes any stray capacitances.

Allowing for capacitance due to board layout traces leading to the X_1 and X_2 pins, the RTC oscillator circuit is trimmed internally to provide an effective load capacitance of less than 6pF. Therefore, if the X_1 and X_2 pins were bent up from the PCB traces and a crystal specified with a C_L of 6pF was soldered directly to these pins, the clock should oscillate approximately 40-50 ppm faster than the nominal frequency of 32.768kHz.

Load Capacitance Trimming

If the RTC clock is running faster than the nominal frequency, a small trim capacitor (preferably <8pF) should be placed from the X_2 pin to ground to move the resonant point closer to the nominal frequency. The graph of Figure 7 shows the variation of frequency with additional load capacitance on the RTC X_2 pin.

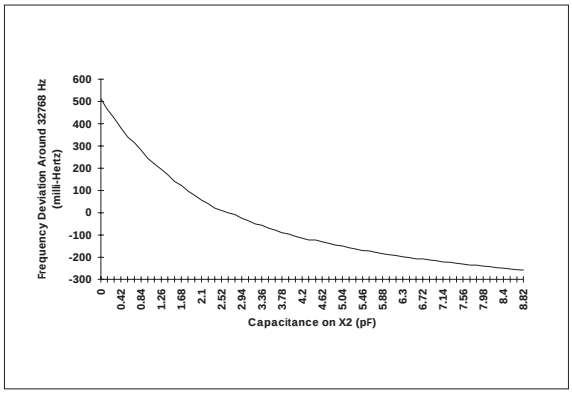

Figure 7. Frequency Variation Versus Load Capacitance

The trimming capacitors normally should be ceramic. Ideally, use a COG- or NPO-type of ceramic or a polyester film capacitor, as these are better suited for timing applications.

Here is a practical rule of thumb deriving from the data in Figure 7: for every additional 1.54pF capacitance on the X_2 pin, the frequency will decrease by 0.8Hz or a $\Delta f/f$ of -24.4 ppm around 32.768kHz.

Using Crystals With C_L Other Than 6pF

Sometimes, a crystal with a C_L specification other than 6pF is used, either because of availability or a stocking issue. Again, because Benchmarq's RTCs are trimmed for use with C_L = 6pF crystals, timing accuracy will most likely be outside ±20 ppm.

A popular alternative is a crystal with a C_L = 12.5pF. By using a crystal with this load capacitance specification, the RTC will resonate much closer to the anti-resonant frequency, Fa. Thus, a larger trim capacitor is necessary. Benchmarq suggests using a 10pF from the X_2 pin to ground in order to achieve ±30 ppm accuracy. Please take into consideration board trace capacitances.

Parallel trim capacitors can also be used, which would place the trim capacitor directly across the X_1, X_2 pins. Parallel trim capacitors, however, require an increased voltage on the BC pin to maintain oscillations in battery backup mode. Hence, Benchmarq still suggests using a trim capacitor from the X_2 pin to ground.

Table 2 represents typical data taken with a bq3285 using a KDS crystal with a C_L = 12.5pF and parallel trim capacitors. The leads were bent up, directly connecting the crystal to them, so a 2-3pF capacitor from both the X_1, X_2 pins to ground were added to simulate trace capacitances. The part was monitored by using an HP5370B Universal Time Interval Counter tied to the SQW output pin.

This data shows that a 6.8pF parallel trim capacitor has better ppm performance, but the oscillator was not sustained in battery back-up mode at the minimum battery voltage of 2.5V. Benchmarq suggests using a 4.7pF parallel trim capacitor if using a crystal with a C_L = 12.5pF.

Board Layout

Given the high-input impedance of the crystal input pins X_1 and X_2, take care to route high-speed switching signal traces away from them. Preferably use a ground-plane layer around the crystal area to isolate capacitive-coupling of high-frequency signals. The traces from the crystal leads to the X_1, X_2 pins must be kept short with minimal bends. A good rule of thumb is to keep the crystal traces within 5mm of the X_1, X_2 pins.

Table 2. Parallel Trim Capacitance Data

Cp	BC Voltage	ppm	Oscillator sustained	Start-up
6.8pF	2.1V	+7-10	No	Yes
	2.15V		No	Yes
	2.5V		No	Yes
	3.0V		Yes	Yes
4.7pF	<2.15V	+15-20	No	No
	2.15V		Yes	Yes
	2.5V		Yes	Yes
	3.0V		Yes	Yes

Notes:
1. Cp = Parallel trim capacitor
2. BC voltage = Voltage present on BC pin
3. ppm = ppm data
4. Osc. sustained = Oscillator running in battery backup mode?
5. Start-up = Did oscillator start up on power-up?

Finally, place a 0.1µF ceramic by-pass capacitor close to the RTC V_{CC} pin to provide an improved supply into the clock.

Drive Level

The drive level is the power dissipated through a crystal in an operating circuit. A drive level (measured in microwatts) which is too high or too low can cause undesirable effects. If the level is too high, it can cause the oscillator frequency to change, cause a fracture of the quartz element, or lead to a permanent shift in frequency output. If the drive level is too low, it can prevent oscillator function completely. Generally, keep the drive level at the minimum level required for high stability and adequate oscillator output. Benchmarq designs RTCs for minimum drive level for reduced power dissipation to achieve maximum battery life when oscillating in battery backup mode.

Measuring for Accuracy

When checking for clock accuracy, use either a scope or a universal time counter connected to the SQW output pin.

Do not place probes on the X_1 or X_2 pins to check for oscillations, as this action may load the crystal and reduce the output amplitude or prevent the oscillator from functioning.

Oscillator Start-up

Barring accuracy issues, the RTC will oscillate with any 32.768kHz crystal. When hooked to the X_1, X_2 pins in certain configurations, however, passive components can lead to oscillator start-up problems through the following:

- Excessive loading on the crystal input pins X_1, X_2.

  Table 2 shows a 6.8pF parallel trim cap trimming in a 12.5pF C_L crystal. The 6.8pF trim cap provides for better ppm accuracy, but the oscillator will not oscillate in battery backup mode with the minimum battery voltage of 2.5V, even though the oscillator will start-up upon power-up.

- Use of a resistive feedback element across the crystal.

  Benchmarq builds the feedback element into the RTC for start-up, so no resistive feedback external to the part is required.

Also, for start-up, a voltage within the V_{BC} voltage range must be present on the BC pin upon power-up for the oscillator to start-up. This voltage provides biasing to the oscillator circuit for operation.

Figure 8 shows "good"and "bad" circuit configurations for the RTC oscillator.

References

1. KDS America, *Quartz Crystals and Oscillators User's Guide*

2. Eaton, S. S., *Timekeeping Advances Through COS/MOS Technology*, RCA Application Note ICAN 6086.

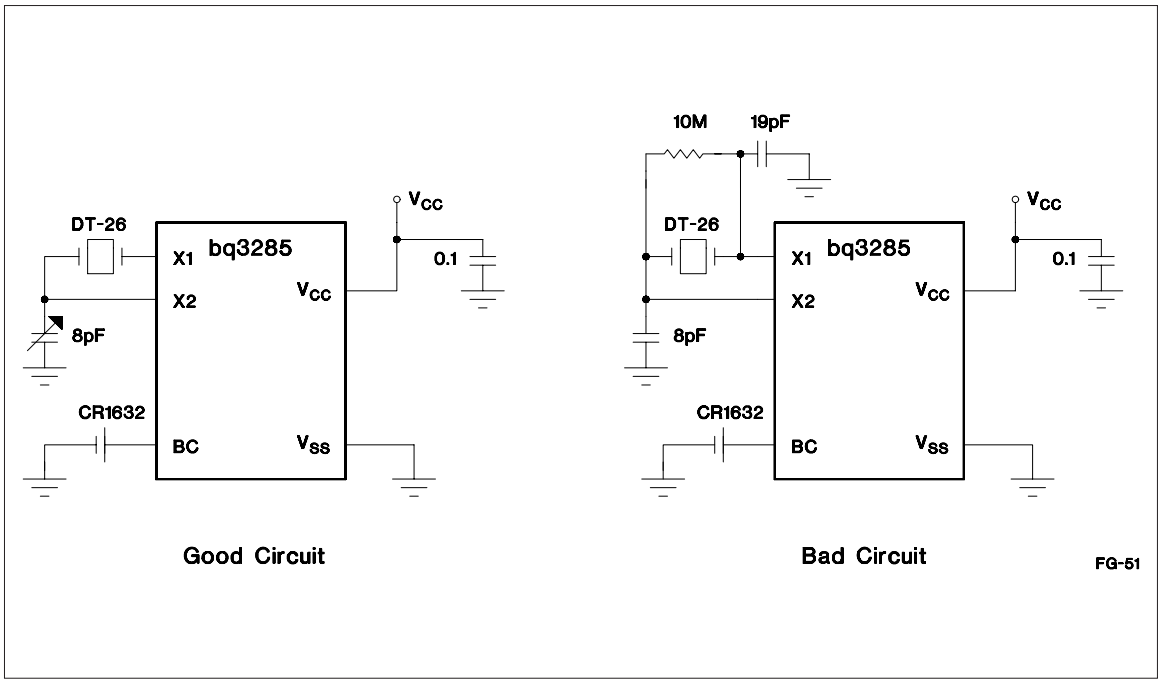

Figure 8. Typical Crystal Hookup Circuits

Suggested Crystals and Manufacturers

Here are a few suggestions for 32.768kHz crystals for use with Benchmarq RTCs:

Item		Symbol	KDS DT-26	Epson C-002RX	Epson MC-306	Epson MC-405/406
Frequency range		f	32.768kHz			
Temperature range	Storage	T_{STG}	-30°C to +70°C	-10°C to +60°C	-55°C to +125°C	-55°C to +125°C
	Operating	T_{OPR}	-10°C to +60°C	-10°C to +60°C	-40°C to +85°C	-40°C to +85°C
Maximum drive level		GL	1.0µW			
Soldering condition		T_{SOL}	240°C-250°C 10s maximum	under 280°C within 5s	under 230°C within 3 min.	under 230°C within 3 min.
Frequency tolerance		Δf/f	Grade A: ±20 ppm Grade B: ±30 ppm	±20 ppm	±20 ppm or ±50 ppm	±20 ppm or ±50 ppm
Peak temperature (frequency)		ΘT	25°C ± 5°C			
Temperature coefficient (freq.)		a	-0.04 ppm / $°C^2$ max.			
Load capacitance		C_L	6pF (please specify)			
Series resistance		R_1	45kΩ max.	50kΩ max.	50kΩ max.	50kΩ max.
Motional capacitance		C_1	2.6fF typ.	2.0fF typ.	1.8fF typ.	2.0fF typ.
Shunt capacitance		C_0	1.1pF typ.	0.8pF typ.	0.9pF typ.	0.85pF typ.
Insulation resistance		IR	500MΩ min.			
Aging		fa	-	±5 ppm/year max.	±3 ppm/year max.	±3 ppm/year max.
Shock resistance		S.R.	±3 ppm max.	±5 ppm max.	±5 ppm max.	±5 ppm max.

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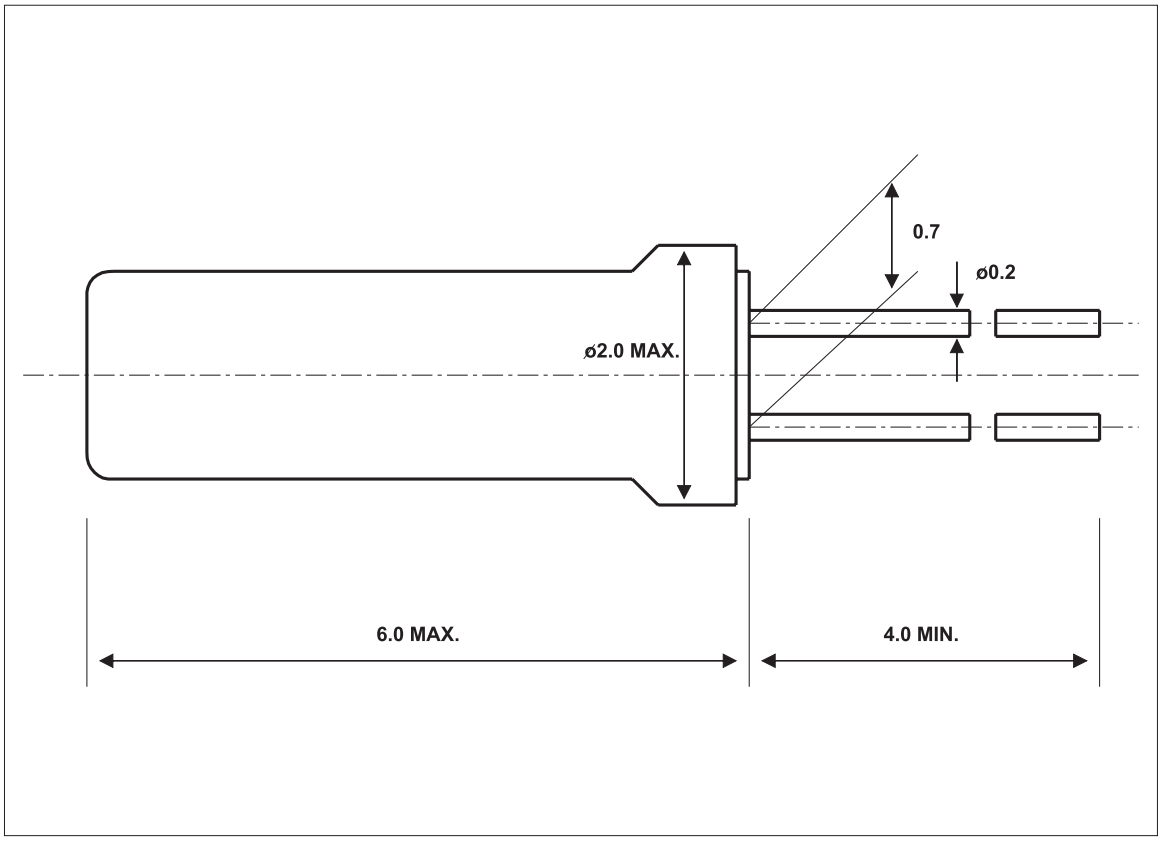
External Dimensions

- DT-26, C-002RX

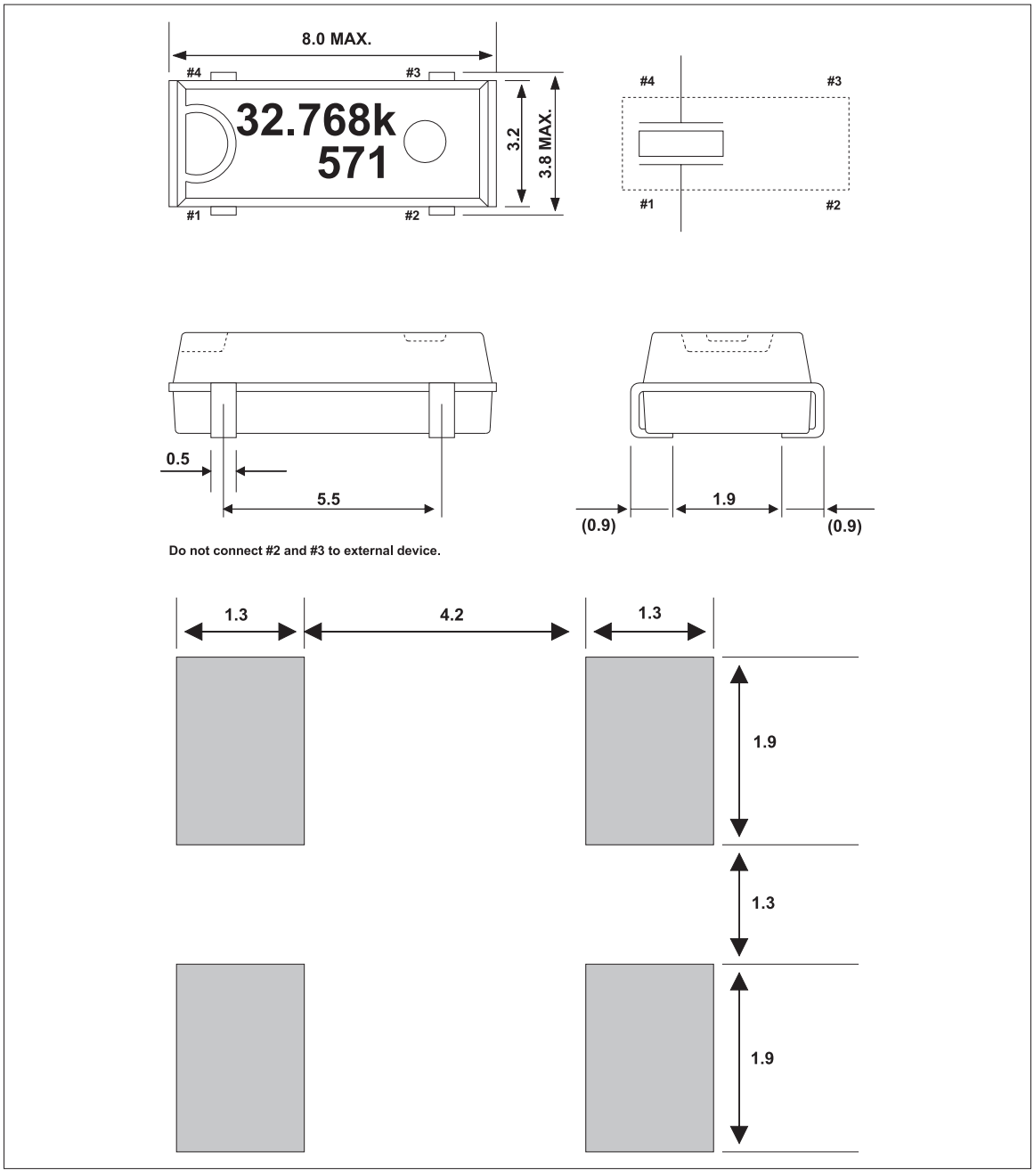
(Unit : mm)



External Dimensions and Soldering Patterns

- MC-306

(Unit : mm)



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External Dimensions and Soldering Patterns

- MC-405/406

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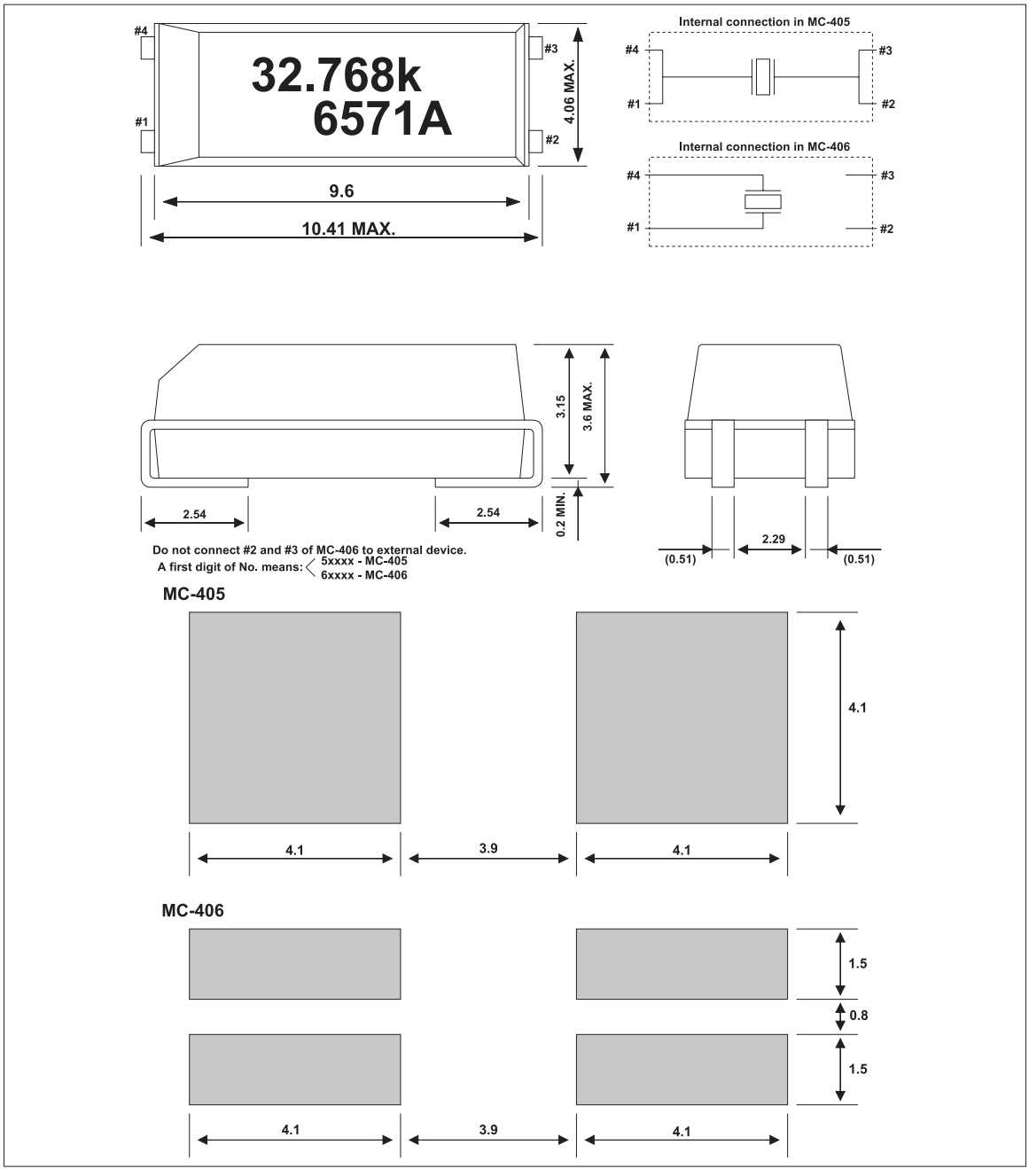

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Notes

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