APPLICATION NOTE U-169

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A Complete Control Solution for a Four-Quadrant Flyback Converter Using the New UCC3750 Source Ringer Controller

UNITRODE

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By Dhaval Dalal

Abstract

With the emergence of newer telecom distribution networks, there is a need for innovative power conversion solutions. Ring signal generation is a perennial requirement which can be addressed from a power conversion viewpoint with a switching amplifier or a dc-ac inverter. A unique flyback derived four-quadrant power inverter is discussed with a complete design procedure and control solution. While the emphasis is placed on the ring generator solution, it is clear that this approach is suitable for many other low power inverter applications such as UPS systems, audio amplifiers etc.

Introduction

The emergence of high bandwidth telecom architectures involving Fiber in the Loop (FITL) have created new challenges for powering the communication networks. One of the most demanding functions from the power management perspective is the generation of an appropriate ring signal for ringing telephones. While many of us have switched over to electronic phones, backward compatibility with the older mechanical bells is still necessary. A typical North American mechanical bell requires a ring signal of at least 45V (RMS) at a frequency of 20Hz (±1Hz) to provide an acceptable ringing tone. The ring frequencies in other international phone systems may be different (25Hz and 50Hz are other common frequencies), but the voltage level is quite similar. It is also important for the ring signal to have very low harmonic content in order to minimize interference in adjacent phone lines.

Historically, ring signal generation was done at the central office (CO) with long transmission paths requiring a high ring voltage (>80V) at the source. With the emergence of fiber networks to reduce distribution costs and increase bandwidth, ring generation and other powering functions have to be near the subscriber end. Typically, this is done at the remote switching modules (RSMs) located at the curb. Reduced transmission length implies that the ring signal amplitude can be lower (60V-70V) at the RSM, but the ring generator unit (RGU) now needs to support a higher Ringer Equivalent Number (REN) per line than the CO ring generator.

The traditional distributed power supply for telecom applications such as RSM has been a –48V battery backed voltage. For ring generation, this input voltage has to be converted into a ring signal of desired amplitude and frequency with a typical DC offset of –48V. In addition, the RGU has to provide the flexibility to control any of these parameters in addition to galvanic isolation. Many existing RGU designs use multiple conversion stages. As shown in Figure 1, the first stage is a DC-DC isolated conversion stage which creates two high voltage rails (positive and negative). These rails serve as the upper and lower bounds of the output signal. The second stage is either a linear amplifier as shown in Figure 1a (for lower power RGUs) or a full-bridge switching amplifier as shown in Figure 1b (for higher power).

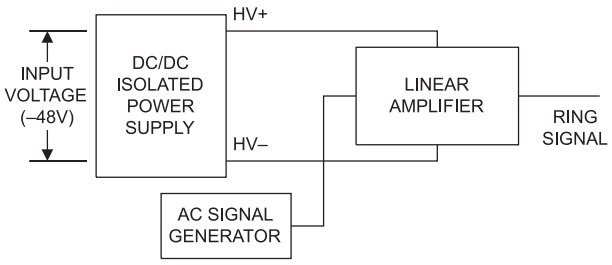

Figure 1a. Conventional Ring Generation Using Linear Amplifier

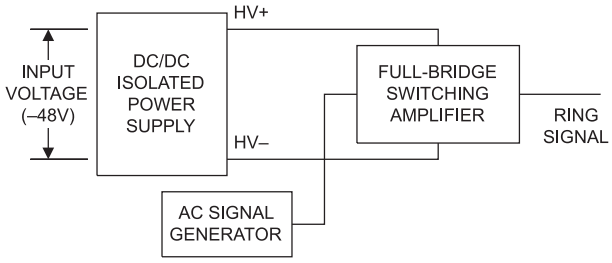

Figure 1b. Conventional Ring Generation Using Full-Bridge Amplifier

The second stage is modulated by an AC signal that has to be generated externally to provide a high voltage AC output. In some cases the modulating signal is a trapezoid (instead of the ideal sinusoid) for lower cost and complexity. The efficiency of these approaches suffers from dual stage power conversion as well as the inability to fully support the reactive phone loads encountered in some applications. A limitation of the linear approach is the lack of flexibility. The DC rail voltages set the bounds for the output ring signal and any change in DC offset or the AC amplitude requires redesign of both conversion stages. The linear amplifier also suffers from higher losses when the AC amplitude needs to be attenuated under AC current limit. While the full-bridge switching amplifier circumvents these problems, it adds significant cost and complexity.

Table I. Operating Mode Determination for Sinusoidal Signal

Mode	Output Current	Reference Polarity	Power Flow	E.A. Output	Source (PWM) Switch	Rectifier Switch
1	+	+	+	–	Q1	Q2
2	–	+	–	+	Q3	(D1)
3	–	–	+	+	Q1	Q3
4	+	–	–	–	Q2	(D1)

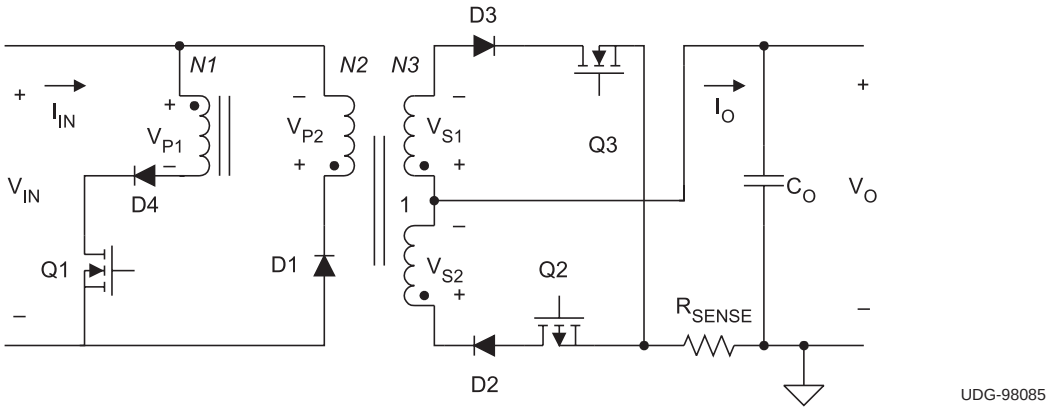

Figure 2. Four-quadrant Flyback Converter Topology

The Four-Quadrant Flyback Topology

The four-quadrant flyback topology is a unique power stage approach which simplifies the RGU implementation considerably, while providing a high degree of design versatility. This approach (Figure 2) provides a single stage solution for ring generation with isolation and the ability to return the reactive power to the source as needed.

The operating modes of the converter are summarized in Table 1 and relevant waveforms are provided in Figures 3 and 4. Figure 3 is drawn for a purely capacitive load in order to provide a clear depiction of all four operating modes (quadrants). In most applications, the load will have a resistive component to it and the circuit will operate primarily in quadrants 1 and 3. The waveforms in Figure 3 (output voltage and current) are the low frequency sinusoidal signals. Within each mode, there are number of switching cycles which follow the waveforms shown in Figure 4. The switching cycle consists of PWM and rectification intervals. During the PWM interval, one of the switches (Q1-Q3) is turned on. The selection of which switch to PWM is made based on Table 1. In modes 1 and 3, the rectification interval (rising edge of the clock signal) is accompanied by turning on of appropriate switch (Q2 or Q3). The operation of the power supply is as a flyback converter in discontinuous conduction mode (DCM) in all four quadrants. The output impedance of the converter including its output capacitor and the load determines the operating modes.

In modes 1 and 3, input to output power transfer takes place. The operation is very similar to conventional flyback operation where the primary switch (Q1) is pulsewidth modulated to build energy in the flyback winding. For the rest of the switching cycle, the stored energy is fed to the output through the rectifying diode and switch combi-

nation. In mode 1, the output (voltage and current) polarity is positive and Q2/D2 provide the rectifying path. In mode 3, the output polarity is negative and the rectifying path is through Q3/D3. Also, the negative polarity in mode 3 requires a phase reversal in the feedback path.

In modes 2 and 4, the secondary switches (Q3 and Q2 respectively) are modulated to enable energy transfer in reverse direction. As a result, the reactive power finds its way back to the input. In both modes, D1 provides the rectifying path to the input. The operation of the converter is still in flyback mode, but the secondary side functions as the input. However, the controlled variable is still the output voltage. As a result, the duty cycle to output relationship in these modes is given by:

$$\frac{|V_O|}{|I_O|} = \frac{2 \bullet L_{sec}}{D^2 \bullet T_S} \quad (1)$$

where $|Vo|$ and $|Io|$ are the magnitudes of slowly varying sinusoidal output voltage and current respectively and can be assumed to be constant for a switching cycle.

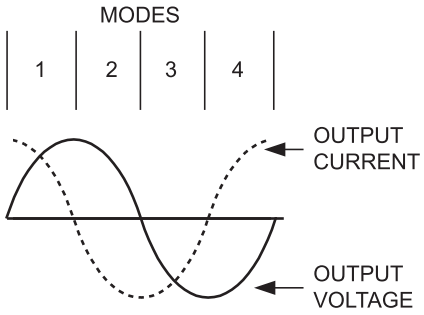

Figure 3. Operating Modes (Ring Frequency)

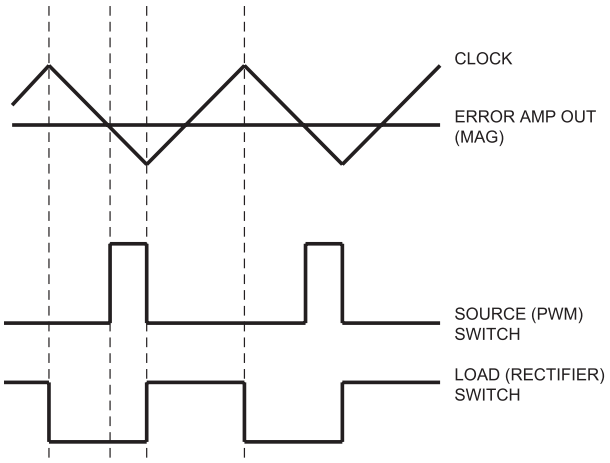

Figure 4. Circuit Waveforms (Switching Frequency)

Power Stage Design Procedure

Following specifications are required for design of the four-quadrant flyback converter. The target specifications for the reference design are also provided.

1. Input voltage range: [$V_{in(min)}$ – $V_{in(max)}$] [40V-60V].
2. Full load output voltage (RMS): V_{rms} [85V]
3. Output offset voltage: V_{os} [0V]
4. Maximum output current / Min. load impedance. [125 mA/10REN]
5. Short circuit current – Isc [200 mA]
6. Output frequency: f_{ring} [20 Hz]
7. Switching frequency: f_{sw} [130 kHz]

The voltages across the switching elements for different modes can be derived (with reference to Figure 2) using the following relationships. Voltage polarities are drain-to-source for FETs and cathode to anode for diodes. In case of diode-FET combinations, the FET polarity is used across the combination. Also, it should be noted that Q2 is assumed to be a p-channel FET. As shown in Figure 2, the turns ratios N1, N2 and N3 are all derived with respect to the secondary winding in series with Q2/D2. The polarities and the variable designations are as depicted in Figure 2.

$$\frac{V_{p1}}{N_1} = \frac{V_{p2}}{N_2} = \frac{V_{s1}}{N_3} = V_{s2} \quad (2)$$

$$V(Q1/D4) = V_{in} - V_{p1} \quad (3)$$

$$V(D1) = V_{in} + V_{p2} \quad (4)$$

$$V(Q2/D2) = V_o - V_{s2} \quad (5)$$

$$V(Q3/D3) = V_o - V_{s1} \quad (6)$$

Values of these voltages are summarized in Table 2 for all modes of operation. Sub-modes A and B within each mode represent the PWM and rectification intervals of a switching cycle respectively. It must also be recognized that within each switching cycle, there is an idle mode when neither PWM nor rectification is taking place. The values in Table 2 are used to select switching elements and the turns ratios of the converter. The table also underlines the need for a diode-FET combination as used in the secondary (to prevent the anti-parallel diode of the FET from conducting

when the voltage across it is negative). As shown later, if correct turns ratios are selected, the primary diode (D4) in series with Q1 can be eliminated.

Table II. Voltage Stresses Across Switching Elements

Mode	Polarities			Active Switch	Transformer Voltages			Component Voltage Stresses			
	I_{in}	V_o	I_o		V_{p1}	V_{p2}	V_{s2}	$Q1$	$D1$	$Q2/D2$	$Q3/D3$
1A	+	+	0	$Q1$	V_{in}	$\frac{V_{in} \bullet N_2}{N_1}$	$\frac{V_{in}}{N_1}$	0	$\left(1+\frac{N_2}{N_1}\right)V_{in}$	$V_o+\left(\frac{V_{in}}{N_1}\right)$	$V_o-\left(\frac{N_3 V_{in}}{N_1}\right)$
1B	0	+	+	$Q2/D2$	$-N_1V_o$	$-N_2V_o$	$-Vo$	$V_{in}+N_1V_o$	$V_{in}-N_2V_o$	0	$(1+N_3)\bullet V_o$
2A	0	+	–	$Q3/D3$	$\frac{N_1V_0}{N_3}$	$\frac{N_2V_0}{N_3}$	$\frac{V_0}{N_3}$	$V_{in}-\left(\frac{N_1V_0}{N_3}\right)$	$V_{in}+\left(\frac{N_2V_0}{N_3}\right)$	$V_o+\left(\frac{V_o}{N_3}\right)$	0
2B	–	+	0	$D1$	$\frac{-N_1V_{in}}{N_2}$	$-V_{in}$	$-\frac{V_{in}}{N_2}$	$\left(1+\frac{N_1}{N_2}\right)V_{in}$	0	$V_o+\left(\frac{V_{in}}{N_2}\right)$	$V_o+\left(\frac{N_3V_{in}}{N_2}\right)$
3A	+	–	0	$Q1$	V_{in}	$\frac{V_{in} \bullet N_2}{N_1}$	$\frac{V_{in}}{N_1}$	0	$\left(1+\frac{N_2}{N_1}\right)V_{in}$	$V_o+\left(\frac{V_{in}}{N_1}\right)$	$V_o-\left(\frac{N_3V_{in}}{N_1}\right)$
3B	0	–	–	$Q3/D3$	$\frac{N_1V_0}{N_3}$	$\frac{N_2V_0}{N_3}$	$\frac{V_0}{N_3}$	$V_{in}-\left(\frac{N_1V_0}{N_3}\right)$	$V_{in}+\left(\frac{N_2V_0}{N_3}\right)$	$V_o+\left(\frac{V_o}{N_3}\right)$	0
4A	0	–	+	$Q2/D2$	$-N_1V_o$	$-N_2V_o$	$-V_0$	$V_{in}+N_1V_o$	$V_{in}-N_2V_o$	0	$(1+N_3)\bullet V_o$
4B	–	–	0	D1	$\frac{-N_1V_{in}}{N_2}$	$-V_{in}$	$-\frac{V_{in}}{N_2}$	$\left(1+\frac{N_1}{N_2}\right)V_{in}$	0	$V_o-\left(\frac{V_{in}}{N_2}\right)$	$V_o+\left(\frac{N_3V_{in}}{N_2}\right)$

Step 1. Peak Output Voltage

Determine the peak positive and negative output voltages, Vo(pk+) and Vo(pk–)

$$V_o(pk+) = 1.414 \bullet V_{rms} + V_{os} \qquad (7a)$$

and

$$V_o(pk-) = 1.414 \bullet V_{rms} - V_{os} \qquad (7b)$$

For the reference design, since

$$V_{os} = 0V, V_o(pk+) = V_o(pk-) = 120V.$$

For many designs requiring a –48V offset, the V_o(pk+) value will be lower than the V_o(pk–) value.

Step 2. Turns ratios (N_1, N_2 and N_3)

The additional clamp winding for reverse power transfer can potentially block the normal power transfer to the output if the correct turns ratio is not used. From Table 2, it can be seen that in order to prevent D1 from conducting in modes 1B and 3B, following conditions must be satisfied:

$$V_{in} - N_2V_o > 0 \text{ (when } V_o \text{ is positive)} \qquad (8a)$$

and

$$V_{in} + \frac{N_2V_o}{N_3} > 0 \text{ (when } V_o \text{ is negative)} \qquad (8b)$$

Thus,

$$N_2 < \frac{V_{in}(\min)}{V_o(pk+)} \qquad (8c)$$

and

$$\frac{N_2}{N_3} < \frac{V_{in}(\min)}{V_o(pk-)} \qquad (8d)$$

N_2 should be selected to be the highest possible value to meet the above constraints. To optimize the turns ratios, N_3 may be selected such that:

$$N_3 = \frac{V_o(pk-)}{V_o(pk+)}. \qquad (9)$$

Lower values of N_2 will increase the stress on the secondary switches (Q2,Q3). On the other hand, a high value of N_2 contributes to higher stress on D1.

The value of N_1 determines if the voltage across Q1/D4 ever goes negative in modes 2A and 4A. If D4 is used, there is no theoretical upper bound on N_1 as the automatic conduction of Q1's body diode is prevented. If, however, we limit N_1 according to the following relationship we can prevent the voltage from going negative and eliminate D4:

$$N_1 < \frac{V_{in}(\min)}{V_o(pk-)} \qquad (9a)$$

and

$$N_1 < N_3 \frac{V_{in}(\min)}{V_o(pk+)} \quad (9b)$$

If the value of N_3 is selected using the guideline above, the condition for N_1 becomes:

$$N_1 < \frac{V_{in}(\min)}{V_o(pk-)} \quad (10)$$

for N_3>1(i.e. negative bias voltages).

A high value of N_1 increases the voltage stress on Q1 while a low value of N_1 increases the voltage stress on D1-D3.

For the reference design, since $V_o(pk-) = V_o(pk+)$, $N_1 = N_2 < 0.33$ (chosen to be 0.2 for some margin) and $N_3 = 1$

Step 3. Load Considerations

The load for the ring generator is normally reactive. Each mechanical ringer can be represented by a 6930Ω resistor in series with a 8μF capacitor (this specification is typical for the North American phone systems, other phone systems have different definitions of Ringer Equivalence). This load is considered as 1 REN (Ringer Equivalent Number). A load of n REN is equivalent to a 6930/nΩ resistor in series with an 8·nμF capacitor. Also, in contrast to the conventional DC-DC power supply, the output filter capacitor is considered as part of the load for the low frequency analysis. The resulting effective load for the ring generator is as shown in Figure 5. The admittance of this load can be represented as Y (= $|Y|\angle\theta$), as defined in equations 11-15:

$$\theta = \tan^{-1}\left(\frac{C_o \bullet k^2 + C_o + C_l}{k \bullet C_l}\right) \quad (13)$$

$$k = \omega \bullet R_l \bullet C_l \quad (14)$$

$$\omega = 2\pi \bullet f_{ring} \quad (15)$$

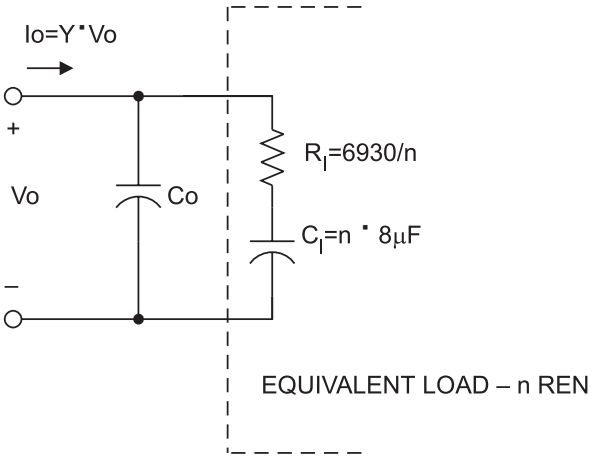

Figure 5. Equivalent Load of n Phones as Seen by the 4-Quadrant Ring Generator

The output voltage, current and power are represented by equations 16, 17 and 18.

$$V_o(t) = V_{os} + \sqrt{2} \bullet V_{rms} \bullet \cos(\omega t) \quad (16)$$

$$I_o(t) = \sqrt{2} \bullet V_{rms} \bullet |Y| \bullet \cos(\omega t + \theta) \quad (17)$$

From the power equation, it can be seen that the average power delivered to the load is given by:

$$P_o(avg) = V_{rms}{}^2 \bullet |Y| \bullet \cos\theta \quad (19)$$

However, the flyback converter components should be chosen to handle the peak power delivered. The flyback transformer energy storage is at the switching frequency and it should be designed to process the peak (not the average) power demanded by the slowly changing output. It can be shown that (for negative values of Vos) the positive peak value of $P_o(t)$ occurs when $2\omega t + \theta = 2\pi$. The resultant peak power is given by: (20)

Table 3 shows the values of RI, CI, $|Y|$, θ and Po(pk) for different load conditions and values of Vos and Co. These values are calculated for a ring frequency of 20 Hz and an output RMS voltage of 90V. As can be seen from the table, at higher REN

$$Y = \frac{\omega}{1+k^2} \bullet \left[k \bullet C_l + j\left(C_O \bullet k^2 + C_O + C_l\right)\right] \quad (11)$$

$$|Y| = \frac{\omega}{1+k^2} \bullet \sqrt{\left(k \bullet C_l\right)^2 + \left(C_O \bullet k^2 + C_O + C_l\right)^2} \quad (12)$$

$$P_O(t) = V_O(t) \bullet I_O(t) = V_{rms}{}^2 \bullet |Y| \bullet \left[\cos\theta + \cos(2\omega t + \theta)\right] + \sqrt{2} \bullet V_{rms} \bullet V_{OS} \bullet |Y| \bullet \cos(\omega t + \theta) \quad (18)$$

Table III. Output Average and Peak Power Levels for Different Load Conditions

REN	Vos (V)	Co (μF)	Rl (Ω)	Cl (μF)	|Y| (S)	θ (deg)	Po(avg) (W)	+Po(pk) (W)	–Po(pk) (W)
0	0	1	-	0	1.257e-4	90	0	1.016	–1.016
0	–48	1	-	0	1.257e-4	90	0	1.59	–1.59
0	–48	2.2	-	0	2.765e-4	90	0	3.50	–3.50
1	0	1	6930	8	2.032e-4	45.91	1.145	2.789	–0.499
1	–48	1	6930	8	2.032e-4	45.91	1.145	3.947	–1.077
1	–48	2.2	6930	8	3.287e-4	64.52	1.145	5.550	–2.710
5	0	1	1386	40	7.425e-4	17.81	5.726	11.73	–0.278
5	–48	1	1386	40	7.425e-4	17.81	5.726	16.23	–1.387
5	–48	2.2	1386	40	8.016e-4	28.13	5.726	16.98	–2.372
10	0	1	693	80	1.452e-3	13.08	11.45	23.21	–0.300
10	–48	1	693	80	1.452e-3	13.08	11.45	32.03	–2.122
10	–48	2.2	693	80	1.493e-3	18.73	11.45	32.56	-2.930

levels, the load appears highly resistive and the operation in the reverse power transfer modes is minimized. This is also illustrated by plots in Figure 6, which depict instantaneous output power for various operating conditions.

In addition to computing the peak power as described above, the ring generator circuit must also be designed to handle the “off-hook” condition of the phone. Under an off-hook condition the ring generator must support a much higher load current since the off-hook resistance of a single phone is 200Ω. For each design, an estimate must be made of the number of phones going off-hook simultaneously. Once the off-hook condition is detected, an external relay circuit will disconnect the ringer from the corresponding phone lines. However, the ringer circuit is required to maintain the bias voltage(VB) under off-hook conditions for at least 200ms to allow for relay switching to the talk battery voltage.

Step 4. Switching Device Selection

From Table 2, the worst case voltage stresses on individual devices [and the calculated values for the example circuit] are:

$$\text{Q1:}\left(1+\frac{N_1}{N_2}\right)\bullet V_{in}(\max)\ \text{[120 V]} \tag{21}$$

$$\text{D1:}\ \left(1+\frac{N_2}{N_1}\right)\bullet V_{in}(\max)\ \text{[120 V]} \tag{22}$$

$$\text{Q2}: -V_o(pk-)-\frac{V_{in}(\max)}{N_2}\ \text{[–420V]} \tag{23}$$

$$\text{D2:}\ V_o(pk+)+\frac{V_{in}(\max)}{N_1}\ \text{[420V]} \tag{24}$$

$$\text{Q3:}\,V_o(pk+)+N_3\bullet\left(\frac{V_{in}(\max)}{N_2}\right)\ \text{[420V]} \tag{25}$$

$$\text{D3}:\left|V_o\right|(pk-)+N_3\bullet\left(\frac{V_{in}(\max)}{N_1}\right)\ \text{[420V]} \tag{26}$$

Select the switching devices and rectifiers to handle the above stresses in addition to the leakage spikes associated with the flyback transformers.

The current ratings of these devices are selected by first calculating the peak current levels and then translating them into the RMS currents. The forward power transfer typically has a higher current requirement when compared to the reverse power transfer. The peak current value is given by:

$$Ipk(t)=\frac{V_{in}\bullet d(t)\bullet T_s}{L_p} \tag{27}$$

where Ipk(t) is the peak current level for duty cycle d(t). T_S is the switching period. The duty cycle d(t) varies proportionally to output voltage $V_o(t)$ and is given by:

$$P_o(pk)=V_{rms}{}^2\bullet|Y|\bullet(1+\cos\theta)-\sqrt{2}\bullet V_{rms}\bullet V_{OS}\bullet|Y|\bullet\cos\left(\frac{\theta}{2}\right) \tag{20}$$

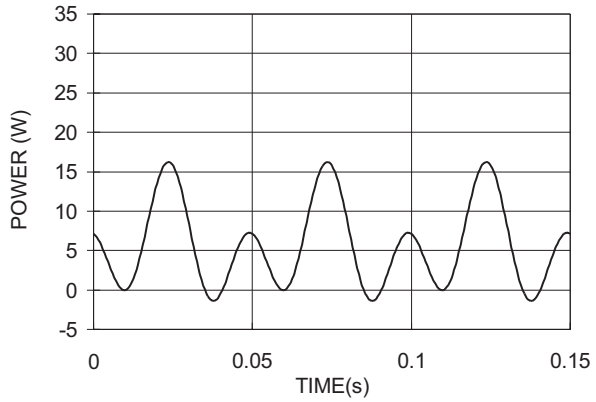

Figure 6a. Instantaneous output power for ring generator (5 REN, Vos = –48V)

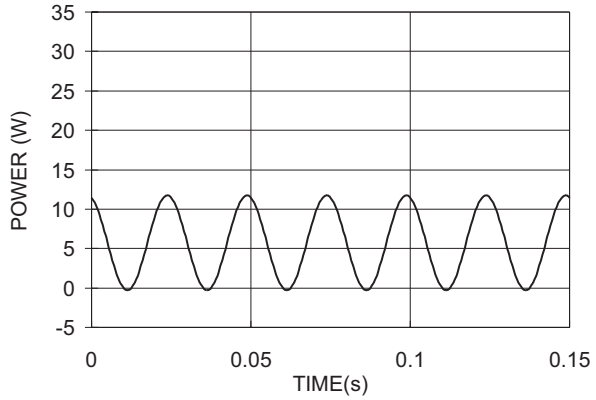

Figure 6b. Instantaneous Output Power for Ring Generator (5 REN, Vos = 0V)

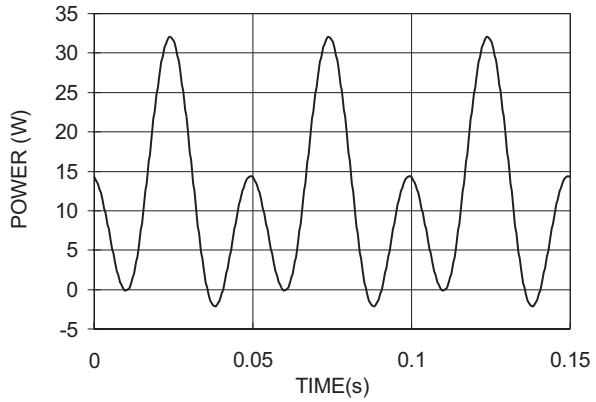

Figure 6c. Instantaneous Output Power for Ring Generator (10 REN, Vos = –48V)

$$d(t) = \frac{|V_o(t)|}{V_{in} \bullet k1} \tag{28}$$

where k1 is defined as:

$$k1 = \sqrt{\frac{T_s}{2 \bullet L_p \bullet |Y|}} \tag{29}$$

The RMS primary switch current can be determined by first taking the RMS value of the Ipk(t) current over a switching cycle and then computing the RMS value of the resultant quantity over the ring frequency cycle. A Mathcad program can be used for this exercise and results in a primary RMS current of 1.15A and a secondary RMS current of 0.38 A for the reference design. For the off-hook condition these currents are calculated to be 1A and 0.6A respectively. The peak currents for the primary and secondary switches are calculated in the same manner and result in values of 5.5A and 1.8A respectively.

Step 5. Transformer Design

While the transformer design is very similar to the DCM flyback design, it is important to take into consideration the peak instantaneous output power and not the average power drawn by the output. After selecting the turns ratios, calculate the maximum magnetizing inductance of the main primary winding using:

$$L_p \le \left(\frac{N_1}{N_3}\right)^2 \bullet \frac{R_o \bullet T_s}{8} \tag{30}$$

The rest of the transformer design is straightforward using the conventional (sometimes iterative) design steps of core selection, number of turns in primary and secondary, gapping, wire size selection etc.

In modes 2 and 4, the power transfer is from output to input with secondary side switches being modulated. The duty cycle to output relationship in these modes for DCM operation is given by :

$$\frac{|V_o|}{|I_o|} = \frac{2 \bullet L_{sec}}{D^2 \bullet T_s} \tag{31}$$

where $|V_o|$ and $|I_o|$ are the magnitudes of slowly varying sinusoidal output voltage and current respectively and can be assumed to be constant for a switching cycle. With a highly reactive load, the converter operates in modes 2 and 4 for substantial periods of time. Under these circumstances, if the ratio $|V_o|/|I_o|$ falls below the level given by the above equation, the duty cycle limit is reached and

the circuit is unable to transfer power at a rate required by the load, resulting in some distortion of the output waveform. One way to alleviate this behavior is to reduce the magnetizing inductance in the secondary. By selecting the turns ratios to correspond to the DC offset as described in step 2, the output voltage distortion is minimized.

Control Circuit Considerations

The control circuit required for the four quadrant flyback converter has to support all four modes of operation and has to be able to handle transitions from one mode to the other smoothly. While a discrete implementation is possible, the complexity of such an approach can be overwhelming due to precision timing requirements and multiple functionalities required. The converter implementation can be greatly simplified by using Unitrode's source ringer controller IC, the UCC3750.

Figure 7 shows the block diagram of the UCC3750. The UCC3750 provides complete control and drive solution for the four-quadrant flyback topology. It provides controls for switches Q1-Q3 with intelligent logic circuits to detect appropriate mode of operation and direct the PWM and rectification signals to appropriate switch. It also contains a crystal derived low frequency sine wave reference which can be programmed to 3 different frequencies with a single crystal. The sine-wave reference has versatility to accept external clocks instead of crystal and also to accept an externally generated sine wave. The IC operates from a single 5V bias supply and has the capability to generate a higher charge-pump voltage (VCP) to drive the MOSFETs. It contains internal 3V and 7.5V references, a summing amplifier (AMP1), an error amplifier (AMP2), programmable AC and DC current limits and a triangular clock oscillator. More details about the UCC3750 operation are available in the device datasheet which also contains pin descriptions and a detailed application section.

UCC3750 Interface Signals

The UCC3750 provides a number of interface signals which allow easy incorporation of the ring generator into a phone distribution system. One of the output interface signals is the RGOOD signal which can be used to determine if the ring generator is providing a sinusoidal signal or not. This output goes low if the error amplifier saturates, indicating that the output is not able to track the reference signal.

The other key output signal is the SWRLY signal. This signal provides a pulse output that precedes the zero crossing of the sine-wave output by a fixed interval (5-8 ms). There are many uses of such a signal. One is to use it as a gating signal for external relay activation. When the phone goes off-hook and the need arises to switch that line

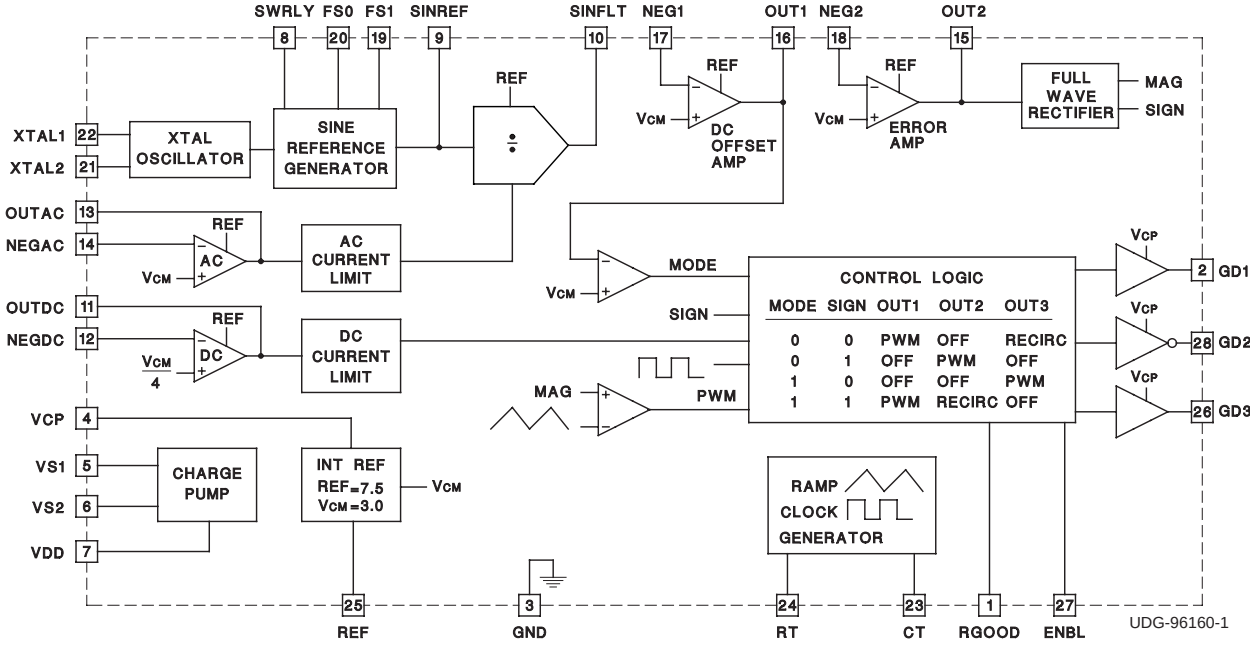

Figure 7. Block Diagram of the UCC3750

from the ring generator to the talk battery, it is best done at the point when the two voltages are equal to prevent arcing. This point happens to be the zero crossing of the sine wave reference. The SWRLY signal precedes the zero crossing to allow for the activation of the relay. For different output frequencies, the pulsewidth and the lead-time of the SWRLY are given in Table 4. The timings given in Table 4 are accurate for a 32 kHz crystal and for the zero crossing of the SINREF output. Due to the filtering of the SINREF before being applied to the error amplifier and the feedback loop delays, the actual output voltage may crossover at a different point than the SINREF signal. However, these delays are much smaller compared to the designed delay times (in ms) to have an appreciable impact on the circuit operation. Another use of the SWRLY signal is for generating handshake signal such as SYNC signals or Message Waiting signals. The SWRLY signal provides an accurate, low frequency timing base that can be used to derive system specific handshake signals. These signals can also be brought back to control the UCC3750 to meet specific output signal shaping requirements.

Table IV. SWRLY Pulsewidth and Lead Time

Frequency (Hz)	SWRLY Lead Time (ms)	SWRLY Pulsewidth (ms)
20	7.8125	1.5625
25	6.25	1.25
50	5.625	0.625

Finally, if the UCC3750 is used for single line ringing applications, its output can be cadenced on and off by using the ENABLE pin to input the cadencing signal. Any external power management signals requiring sequencing and/or shutdown can also be channeled into the ENABLE pin with appropriate buffering.

Summing and Error Amplifier Configuration

In order to program the output voltage for the ring generator, the summing amplifier and the error amplifier of the UCC3750 need to be configured for required DC gain. (See Fig 8.) Depending on the output voltage requirements and the system configuration selection, there are three approaches available for programming the error amplifier components. Typically, the ring generator output voltage is some combination of a DC offset voltage and a sinusoid which is amplified from the sine-wave reference signal (V_{AC}) generated by the UCC3750.

Approach A. No DC Offset (VB=0) [$V_O = k2 \bullet V_{AC}$]. In this approach, the required output voltage is a sinusoidal signal with no DC offset. As indicated, only a gain from the sinusoidal reference (V_{AC}) needs to be programmed. This approach is used when the ring generator output is cascaded with a DC voltage that is already available.

Approach B. Programmable DC offset (αVB) [V_O= k1•VB + k2•V_{AC}]. The UCC3750's capability to make the ring generator output voltage completely programmable is fully exploited with this approach. By providing 2 separate gains for the AC and DC programming signals through the error amplifier, the DC offset and AC amplitude can be independently set at the desired levels with the added flexibility of changing the offset voltage by changing an input voltage level (VB).

Approach C. Fixed DC Offset [VB =0, $V_O = V_{OS} + k2 \bullet V_{AC}$]. The requirement for a DC offset voltage is predetermined and fixed in some applications. In this case, the requirement of a programming voltage (VB) for setting the offset voltage can be done away with and the resistor values can be selected to provide a fixed DC offset (V_{OS}).

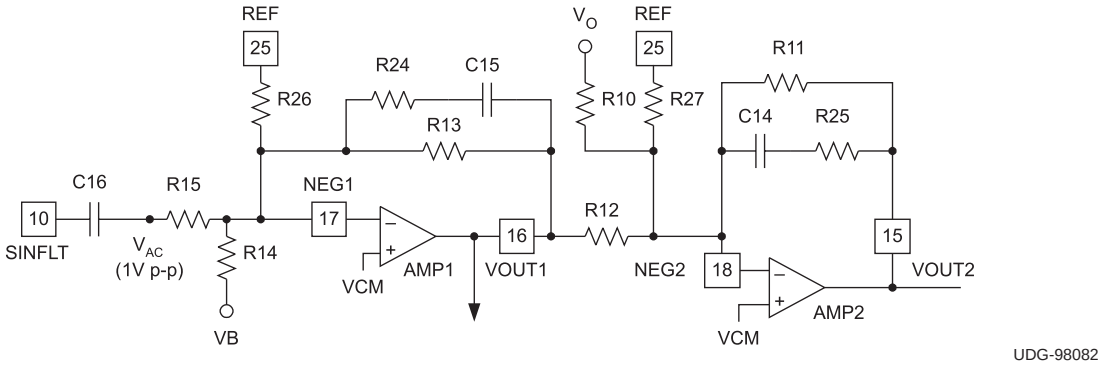

Figure 8. Summing Amplifier and Error Amplifier Configuration

A step-by-step procedure for selecting the error amplifier components for all the 3 approaches is provided below. Except for step 2, all other steps are common to all the 3 approaches. For step 2, the distinct procedures for approaches A-C are listed as steps 2A-2C. Equations 32-36 give formulas for the amplifier setup.

For $R_{26} = 1.5 \bullet R_{14}$; (32) can be simplified to:

$$V_{out1} = V_{CM} - \frac{R_{13}}{R_{14}} \bullet VB - \frac{R_{13}}{R_{15}} \bullet V_{AC} \quad (33)$$

For $R_{27} = 1.5 \bullet R_{10}$, (34) can be simplified to:

$$V_O = \frac{R_{10} \bullet R_{13}}{R_{12} \bullet R_{14}} \bullet VB + \frac{R_{10} \bullet R_{13}}{R_{12} \bullet R_{15}} \bullet V_{AC} \quad (35)$$

For $VB = V_{OS}$:

$$R_{10} \bullet R_{13} = R_{12} \bullet R_{14} \quad (36)$$

Step 1. Select R_{15} and C_{16}. As indicated in equation (35), the AC gain from SINFLT to V_O is inversely proportional to R_{15}. Thus, R_{15} should be chosen to be as low as possible. However, R_{15} and C_{16} form a high pass (DC blocking) filter with very low frequency cut-off in order to allow the ring frequency through. As a result, a low value of R_{15} will necessitate a high value of C_{16}. Based on component availability and output requirements, the resolution of this trade-off (low R vs. low C) will vary. In order to get a 5Hz cut-off a 15k resistor and a 2.2μF are chosen.

Step 2. The next step is to select R_{13} and R_{14} so that maximum amplification is attained from the first amplifier without saturating it. The amplifier output range is from 0.7V to 5.3V, V_{CM} = 3V and V_{AC} = 0.5V.

2A. For V_{OS}=0, select R_{13} such that the ratio of R_{13} to R_{15} is at or below 4.5. This constraint follows from equation (33) and assumes that R_{26}=1.5 • R_{14}. In this case, particular values of R_{14} and R_{26} are not very critical as they only provide a DC bias for the first amplifier. They should be chosen to achieve moderate bias levels. For the present example, R_{13} is selected to be 60k.

2B. For a programmable DC offset in the range of –48V, having VB equal to the desired offset voltage (k1=1) leads to difficult trade-offs in component value selections. For example, from equations (35) and (36), the AC gain from the sine wave reference to the output is given by (R_{14}/R_{15}). With R_{15} already chosen using the trade-off in step 1, the value of R_{14} can become very large for systems with high output voltage requirements. As a result, the ratio of R_{10} to R_{12} also becomes large, leading to a small value of R_{12} or a large value of R_{10}, both options result in non-optimal performance. Alternatively, a resistive divider can be used to scale down the offset voltage before applying it to VB. For example, a 1:10 scaling would result in VB=–4.8V for V_{OS} = –48V. The ratio:

$k1 = \left[\frac{(R_{10} \bullet R_{13})}{(R_{12} \bullet R_{14})}\right] = 10$ in this case. With this arrangement, R_{13} and R_{14} can be more optimally chosen. Using equation (35) and required AC gain (k2), the value of ($R_{10} \cdot R_{13}/R_{12}$) can be determined. Substituting this value for k1, the value of R_{14} is derived. R_{13} should be selected so that the output of the first amplifier provides maximum swing without saturating for all possible values of VB. The value of R_{26} equals 1.5•R_{14}.

For example, for an 85V AC output, Vo–pk =120 V, k2 = 120/0.5 = 240. With R_{15}=15k, ($R_{10} \bullet R_{13}/R_{12}$) = k2·$R_{15}$ = 3.6M. For k1=10, R_{14} becomes 360k. Putting these values into equation (33) and solving for R_{13} with V_{out1}=5.3V, V_{AC} = –0.5V and VB =–4.8V yields R_{13} = 49k.

2C. For a fixed, negative DC offset, R_{26} can be removed and R_{14} wired to ground (VB=0). The output voltage then becomes:

$$V_O = \left(\frac{R_{10} \bullet R_{13}}{R_{12} \bullet R_{14}}\right) \bullet V_{CM} + \left(\frac{R_{10} \bullet R_{13}}{R_{12} \bullet R_{15}}\right) \bullet V_{AC} \quad (37)$$

$$V_{out1} = \left(1 + \frac{R_{13}}{R_{14}} + \frac{R_{13}}{R_{26}}\right) \bullet V_{CM} - \frac{R_{13}}{R_{26}} \bullet REF - \frac{R_{13}}{R_{14}} \bullet V_B - \frac{R_{13}}{R_{15}} \bullet V_{AC} \quad (32)$$

$$V_O = \left(1 + \frac{R_{10}}{R_{27}} + \frac{R_{10}}{R_{12}}\right) \bullet V_{CM} - \frac{R_{10}}{R_{27}} \bullet REF - \frac{R_{10}}{R_{12}} \bullet V_{out1} \quad (34)$$

Again, for a required output AC level, k2 can be calculated. With k2 and R_{15} known, the value of (R_{10}•R_{13}/R_{12}) is determined, in the present example, it is 3.6M. The value of R_{14} falls out from the required offset V_{OS} and the first part of equation given above. If V_{OS} = –48V, R_{14} can be calculated to be 225k for the continuing example. The output voltage of the first amplifier in this approach is given by:

$$V_{out1} = \left(1+\frac{R_{13}}{R_{14}}\right) \bullet V_{CM} - \left(\frac{R_{13}}{R_{15}}\right) \bullet V_{AC} \quad (38)$$

Again, R_{13} can be calculated to get the maximum swing out of the summing amplifier (AMP1) without saturating it, in this case it also turns out to be 49k.

Step 3. Once R_{13} and R_{15} are selected, R_{10} and R_{12} are selected next. From step 2, the value of R_{10}/R_{12} is easily calculated to be (k2•R_{15}/R_{13}). For k2=240, the value of R_{10}/R_{12} equals 60 for approach A and 73.5 for approaches B and C in the given example. These ratios could be even higher if the choice of R_{13}–R_{15} is non-optimal or if a higher output voltage is required. The individual values of R_{10} and R_{12} can be somewhat arbitrarily chosen as long as they satisfy the ratio and the bias currents through the two are neither too low nor too high. The value of R_{10} may also be dictated by feedback loop considerations addressed in the next section. The selected values are R_{12} = 3.3k and R_{10} = 200k.

The value of R_{27} should always be 1.5•R_{10} for proper DC biasing of AMP2. The filter around AMP1 (consisting of R_{24}, C_{15}) can provide a high frequency noise pole if necessary.

Feedback Loop Compensation

The load behavior for the ring generator is different from a typical power supply load, which can be assumed to be resistive. The capacitive coupling introduces an integrator at the origin and a low frequency zero in the power stage gain equation. The resultant open loop power stage gain equation is given as:

$$G_d(s) = G_{lf} \bullet \frac{s_{z1}}{s} \bullet \frac{\left(1+\frac{s}{s_{z1}}\right)}{\left(1+\frac{s}{s_{p1}}\right)} \bullet \left(1+\frac{s}{s_{z2}}\right) \quad (39)$$

Where:

$$G_{lf} = V_{in} \bullet \sqrt{\frac{0.4 \bullet R_l \bullet T_s}{L_p}} \quad (40)$$

$$s_{z1} = \frac{1}{R_l \bullet C_l} \quad (41)$$

$$s_{p1} = \frac{2}{R_l \bullet \left(\frac{C_l \bullet C_o}{C_l + C_o}\right)} \quad (42)$$

$$s_{z2} = \frac{1}{R_c \bullet C_o} \quad (43)$$

Using the power stage gain and the required crossover frequency, the compensation components can be calculated with conventional loop compensation techniques. The feedback loop should be designed to provide adequate phase margin at the crossover frequency. The error amplifier gain for the configuration in Figure 8 is given by (equation 44):

This configuration can be modified by replacing R_{11} with a capacitor to give a pole at origin. That configuration also provides a high frequency pole for noise filtering. The location of the zero does not change.

$$G_{vea}(s) = \left(\frac{R_{11}}{R_{10}}\right)\left(\frac{\left(1+s \bullet R_{24} \bullet C_{15}\right)}{\left(1+s \bullet C_{14} \bullet \left[R_{11}+R_{25}\right]\right)}\right) \quad (44)$$

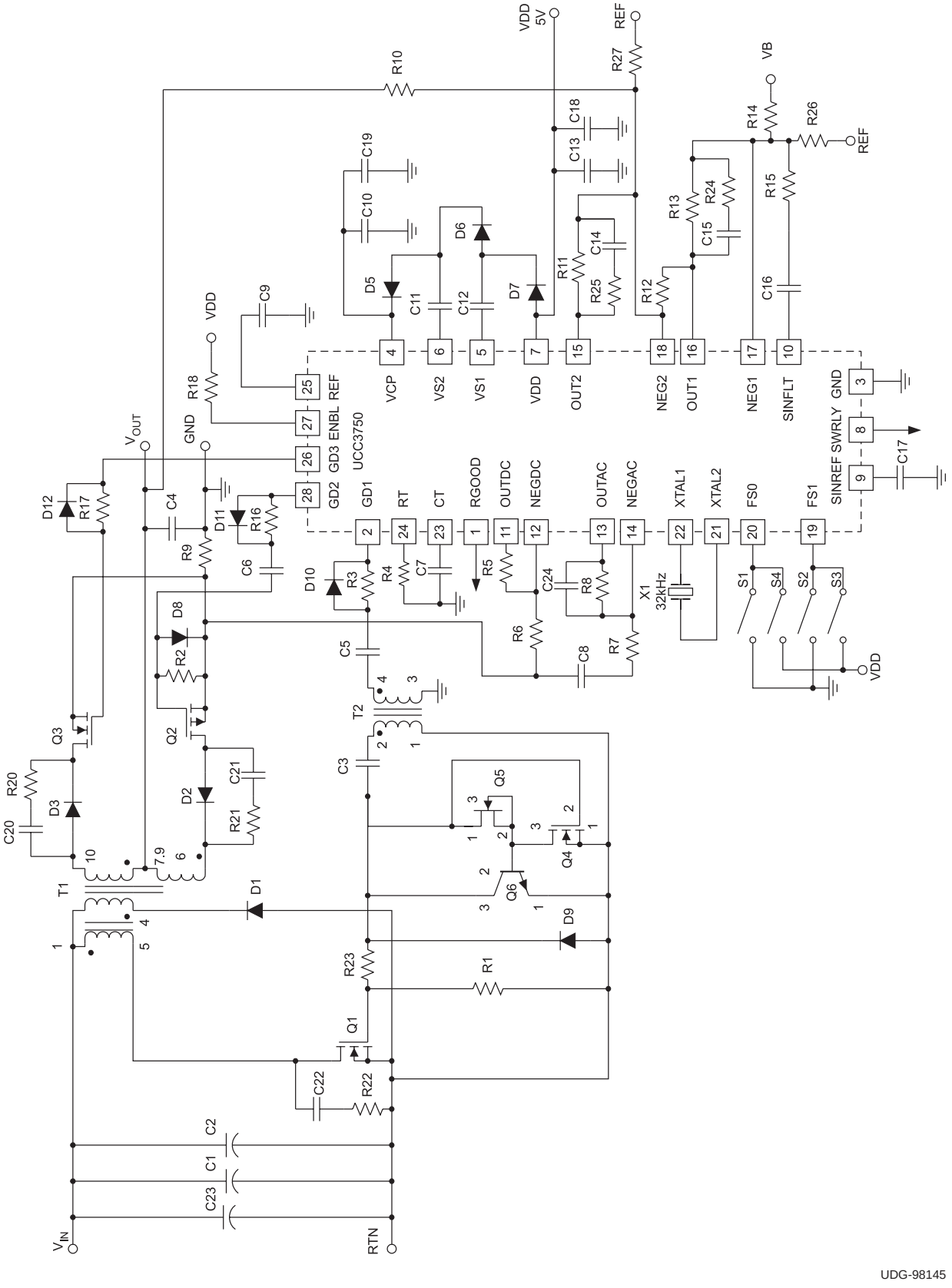

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Figure 9. UCC3750 Detailed Application Circuit Schematic

Circuit Implementation and Results

Using the design guidelines provided above, a four-quadrant flyback ring generator for 15 REN, $85V_{AC}$ output was designed and built. The circuit schematic of the designed converter is shown in Figure 9. The selection of power semiconductors and the transformer design followed the guidelines in Steps 4 and 5 respectively. The transformer used for the design is Coiltronics CTX08-13484 with primary inductance of 60μH. Values of critical circuit components are summarized in Table 5. The performance of the circuit was verified over different operating conditions. The efficiency was measured to be 81% for a 48V input and a 10 REN load. The output voltage and current waveforms are shown in Figure 10. The output voltage shows low harmonic content under normal load conditions. Under highly reactive loads, it can show some distortion near mode crossings. The distortion can be reduced by redesigning the transformer to have a lower magnetizing inductance with the associated penalty of higher peak currents and lower efficiency.

Table V.
Critical Circuit Components Selected Using Design Steps

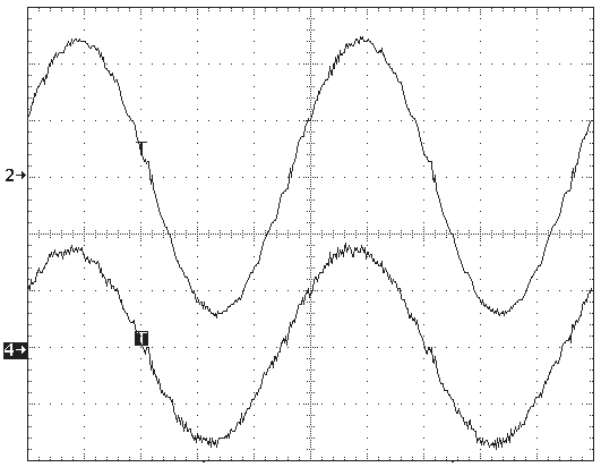
Component (As shown in Figure 9)	**Description**
D1, D2, D3	BYV26C, 600V, 1A
Q1	IRF640, 200V, 0.18Ω, n-channel FET
Q2	MTP2P50, 500V, p-channel FET
Q3	IRF840, 500V, 0.85Ω n-channel FET
R10	200k
R11	1M
R12	3.32k
R13	61.9k
R14	374k
R15	15k
R26	560k
R27	300k
R5, R6	30k,10k
R9	1Ω, 1W sense resistor
T1	1:1:0.2:0.2 Turns ratio, 60μH Lp
T2	Low Lm, pulse transformer

Alternative Topology Implementations

The circuit shown in Figure 9 provides input to output isolation and uses a p-channel FET for Q2. In many applications however, isolation is not required. The circuit implementation can then be simplified by removing the gate drive transformer T2. This type of implementation is captured in Figure 11 where a non-isolated –48V input ring generator is depicted. The IC is referenced to the lowest voltage (–48V) and needs a 5V bias with respect to that voltage to operate. For non-isolated applications, this is easily derived using a resistive divider or a linear regulator.

In applications where the ring generator is designed as a module with isolation, other means of generating the bias voltage on the secondary are required. The most optimal way is to design a small flyback regulator for this purpose.

Another alternative that can be considered for the four-quadrant flyback converter is the selection of the switch Q2. The main reason for selecting a p-channel switch is to be able to drive it directly from the UCC3750. However, in many cases, the performance and selection available for p-channel MOSFETs are inferior to the n-channel alternatives. The n-channel switch requires an isolated/floating gate driver interface to the UCC3750. As shown in Figure 12, this is easily accomplished using a small pulse transformer and a few passive components.



Time Scale: 10.0 ms/div
Upper Waveform: V_{OUT} (50V/div)
Lower Waveform: I_{OUT} (100mA/div)

Figure 10. Output Voltage and Current Waveforms

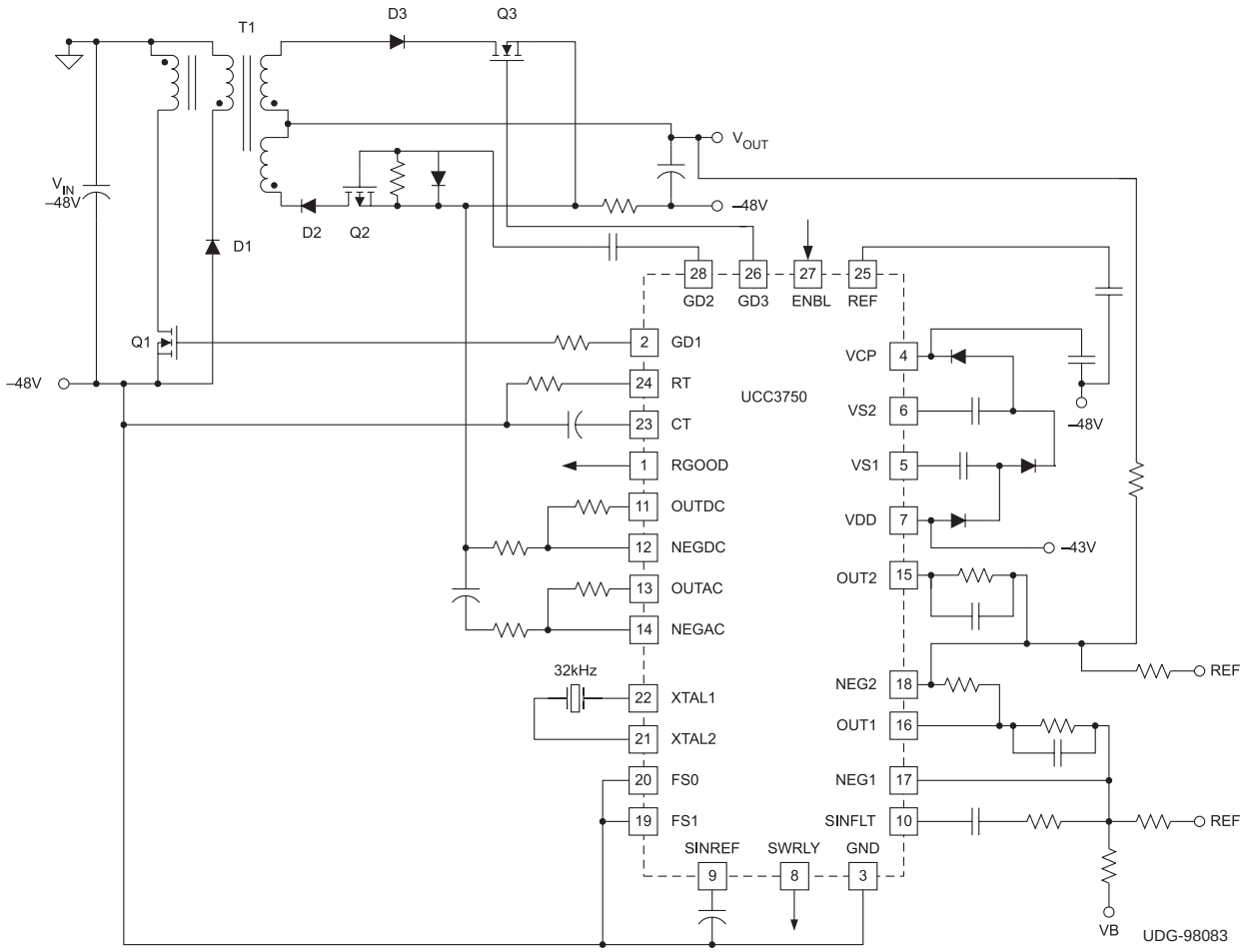


Figure 11. Non-isolated Ring Generator Implementation

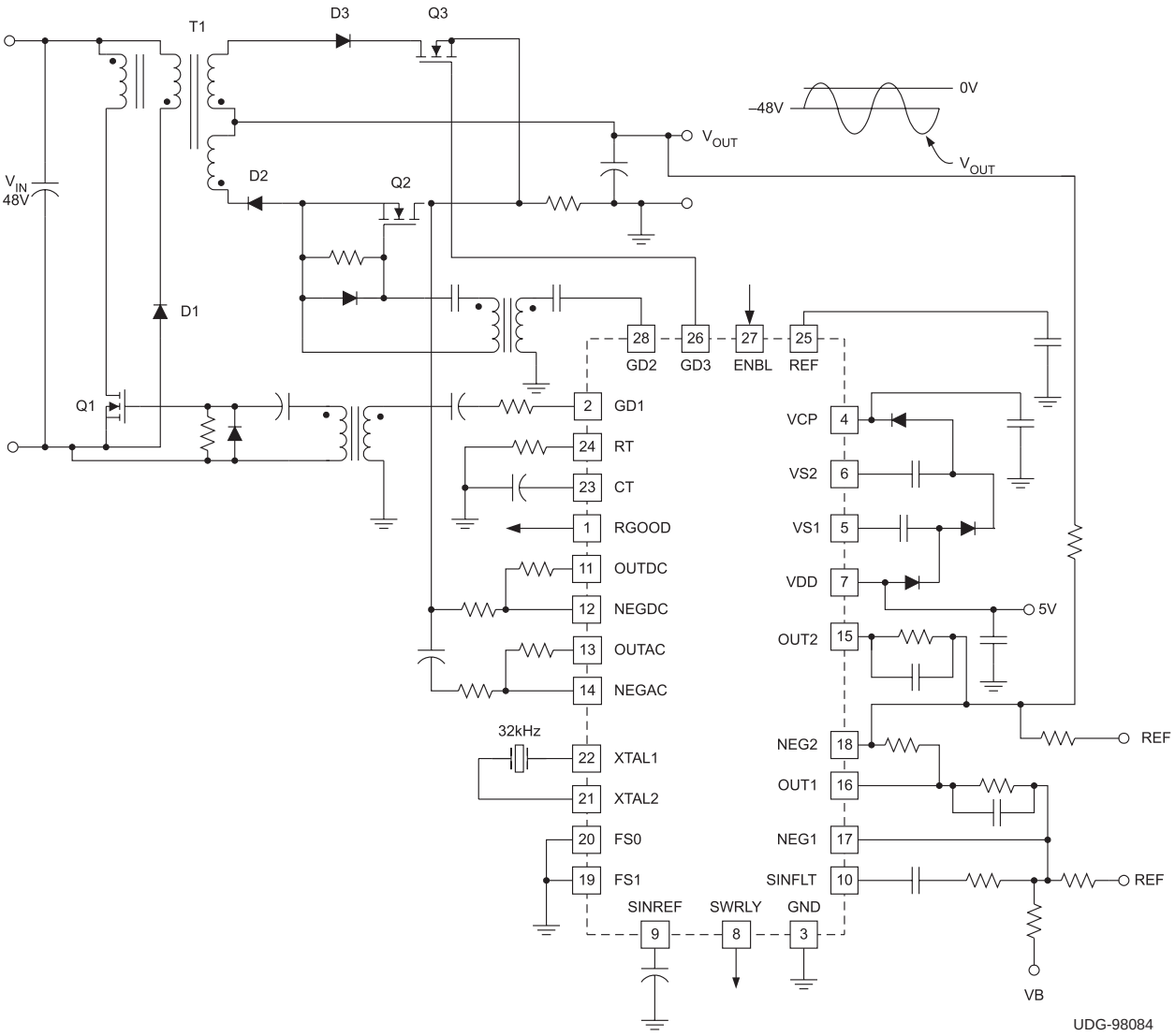


Figure 12. Alternative Implementation — N-channel Q2

Conclusions

A topology for generating low frequency, high voltage AC outputs from DC inputs (ideally suited for ring generator applications) was introduced in this application note. This topology, the four-quadrant flyback converter, is analyzed and a step-by-step design procedure is described. A new control IC, the UCC3750, provides all the control signals required for the four-quadrant flyback converter. Details of setting up the UCC3750 to achieve optimum performance are provided.

References

Following references also provide useful information about the topology and the UCC3750.

[1] Jim Walker, "*Four Quadrant Amplifier Based on the Flyback Topology*", APEC '95, pp. 947-951.

[2] Dhaval Dalal, "*A Unique Four quadrant flyback converter*", Unitrode Power Supply Design Seminar 1997-98, Topic 5, SEM 1200.

[3] UCC3750 Datasheet (revision 7/97 or later).

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