Application Report
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Frequency Dithering with the UCC28180 and TLV3201

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ABSTRACT

For some power supplies, even after careful considerations throughout the design cycle, the issue of Electromagnetic Interference (EMI) still remains. Use of Frequency Dithering is an effective and simple way to pass EMC compliance testing. This application note provides a simple circuit to implement frequency dithering for the UCC28180.

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1 Introduction

One of the greatest challenges in designing switching power supplies is limiting its Electromagnetic Interference (EMI) with other electronics. In addition to layout techniques to minimize high di/dt current loop areas and snub high dv/dt nodes, extensive filtering, slowing switching edges, and shielding, dithering the pulse width modulator (PWM) frequency has proven to be an effective way to reduce EMI by changing it from narrowband to broadband. To demonstrate how to design such a dithering circuit, this application note shows a simple example of using a TLV3201 comparator to add dither function to a UCC28180 PFC controller. The circuit used to dither the frequency is accomplished by taking advantage of the UCC28180's internal oscillator.

2 Typical PFC converter with UCC28180

Figure 1 is a schematic of a 360W PFC converter with UCC28180 that was designed for a universal input voltage. This application is similar to many PFC converters that use a pulse width modulator (PWM) to control the power converter. UCC28180 is a wide range programmable switching frequency PFC controller by connecting a resistor from FREQ (pin4) to ground, so a dithering circuit can be connected to FREQ (pin4) to dither the switching frequency.

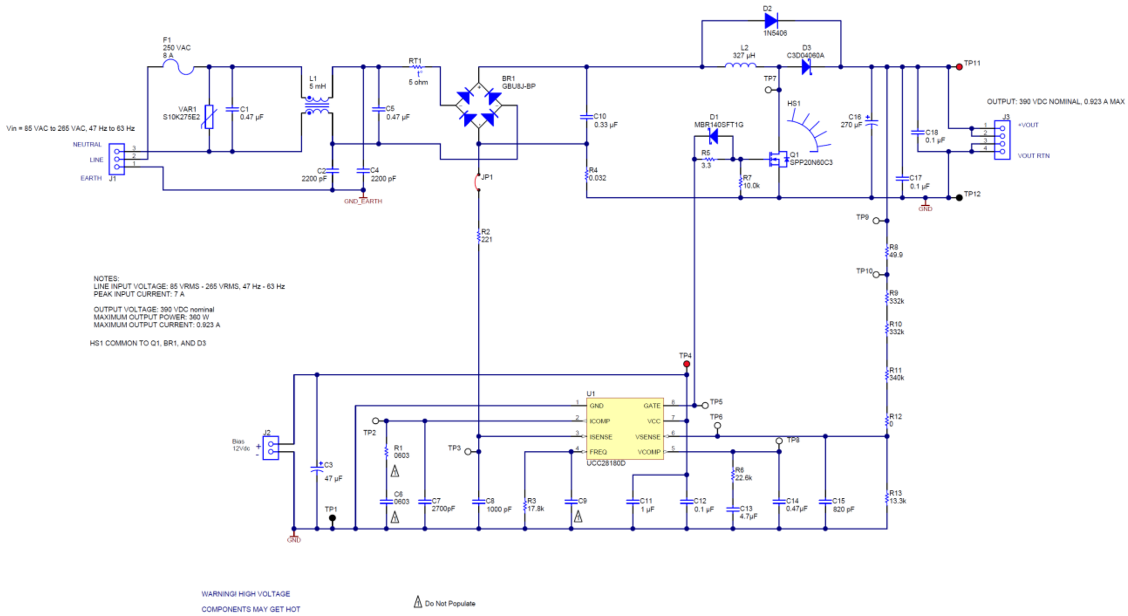


Figure 1. 360W PFC converter with UCC28180

3 Internal PWM oscillator

Figure 2 shows a functional block diagram of the internal circuit that generates the oscillator signal of the UCC28180. The switching frequency is set up by connecting R1 to the FREQ pin. Oscillator gets current signal I1, the final switch frequency is proportional to I1.

The switching frequency is defined as:

$$f = 1.5*1417/RT \qquad (1)$$

This is a simplified version of the equation shown in the datasheet.

Where f is in kHz, RT is in kΩ

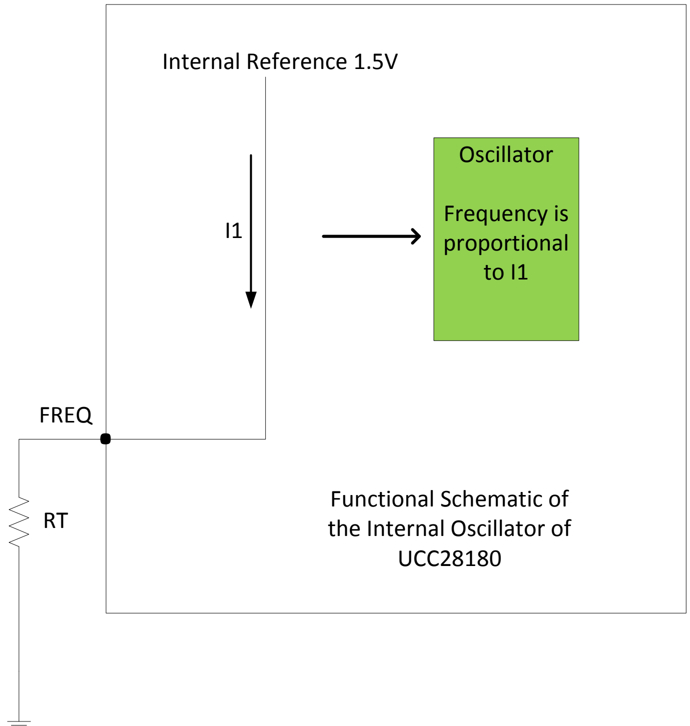


Figure 2. Internal oscillator of UCC28180

4 Sample Circuit used for Dithering the PWM Oscillator Frequency

A typical circuit to apply frequency dithering function is shown in Figure 3 below:

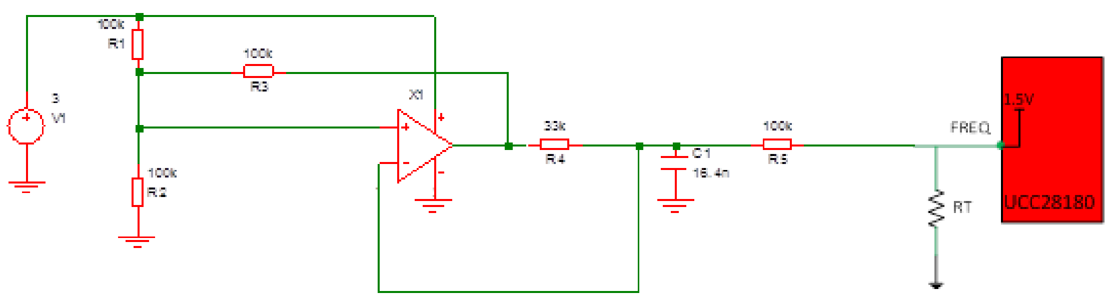


Figure 3. Typical Dither Circuit with UCC28180 and TLV3201

For the UCC28180, the switching frequency is set by the resistor value at the FREQ pin, the FREQ pin itself has an internal 1.5V source and the current out of the FREQ pin determines the switching frequency of the controller, as shown in Figure 2.

4.1 frequency dithering variation goal with UCC28180

In this example, 65 kHz is selected as the central switching frequency of the UCC28180. We will choose an effective dithering magnitude of ±7kHz, and dithering rate of 2 kHz. Because central switch frequency is 65 kHz and dithering magnitude is ±7kHz, so the maximum switch frequency is 72kHz and the minimum switch frequency is 58kHz.

4.2 components calculation of sample circuit

Based on equation (1):

RT=1.5*1417/65=32.7(kΩ)

So the current out of FREQ pin is: I1=1.5V/32.7kΩ=45.87µA

Dithering current out of FREQ pin is: ΔI=±(7kHz/65kHz)×45.87 µA=±4.94 µA

The dithering current comes from the external frequency dithering circuit.

Select R5=100kΩ, the value of R5 affects frequency dithering magnitude.

The ripple voltage of C1 is: 4.94 µA×100kΩ=0.494V.

The voltage of C1 is 1.5V±0.494V, the minimum voltage of C1 is 1.006V; the maximum voltage of C1 is 1.994V, as shown in Figure 4.

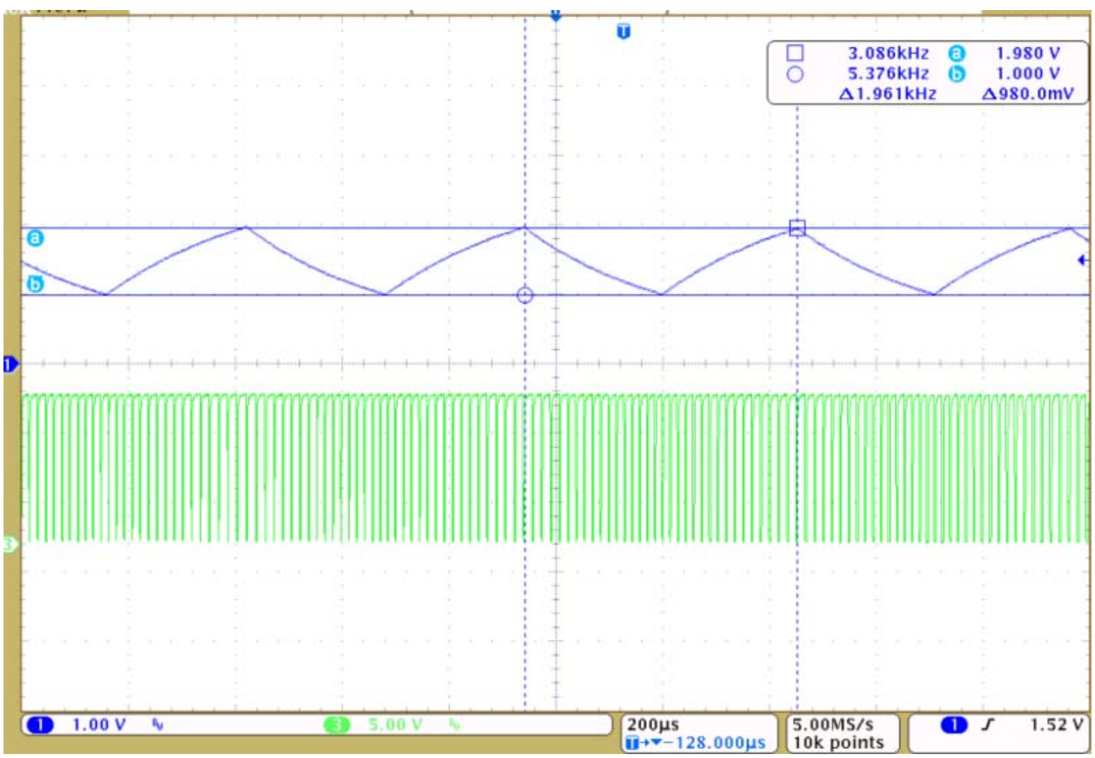


Figure 4. Voltage waveform of C1 of frequency dithering circuit , Ch3 is PWM

A 3V bias voltage is needed for frequency dithering circuit to get symmetrical dithering, because the voltage of FREQ pin is 1.5V. If bias voltage is selected to be 5V, the frequency dithering circuit would not be symmetrical, it is better to select 3V as bias voltage of frequency dithering circuit to get best EMC performance.

R4 limits charge and discharge current for C1, and time factor of R4 and C1 determines dithering rate

A. **Upon initial power-up, the voltage of C1 is 0 V, so the voltage at the non-inverting pin is larger than the inverting pin, the output of the comparator switches high to 3V.**

So the voltage of R2 is VR2:

$$VR2 = 3V \times \left(\frac{R2}{R2 + R1 // R3} \right) = 1.994V \qquad (2)$$

The output voltage of comparator charges C1 through R4, increasing voltage at the inverting pin of comparator.

B. **When voltage of C1 is larger than 1.994V, the output voltage of comparator switches low to 0V.**

So the voltage of R2 is VR2:

$$VR2 = 3V \times \left(\frac{R2 // R3}{R1 + R2 // R3} \right) = 1.006V \qquad (3)$$

C. The output voltage of comparator discharges C1 through R4
Once the inverting (-) pin is discharged below the 1.006V threshold, the output voltage of comparator switches high to 3V again, and charges C1 through R4 again, and the process repeats.

We select R2=100kΩ

Solve R1 and R2 from equation (2) and (3):

R1=100 kΩ, R3=100 kΩ

The actual selection is: R1=100 kΩ, R2=100 kΩ, R3=100 kΩ

From 4.1 and 4.2, the modulating signal will change from 1.006V to 1.994V and back again. With a dithering frequency of 2kHz, the dithering cycle period is T=500µs. So that the RC time constant of R4 and C1 is equal to the dithering cycle period.

Select R4=33kΩ because R4 is much smaller than R5

So $$C1 = \frac{T}{R4} = 15.2nF \quad (4)$$

Therefore we select 2pcs standard 8.2nF cap in parallel to be the charge/discharge cap (C1) to set the modulating frequency.

4.3 Final components selection

Final components selection is:

R1=100 kΩ, R2=100 kΩ, R3=100 kΩ, R4=33 kΩ, R5=100 kΩ, C1=8.2nF×2

5. Circuit Performance

Using the components value selection in 4.3 above, the following waveform in Figure 5 was observed at C1:

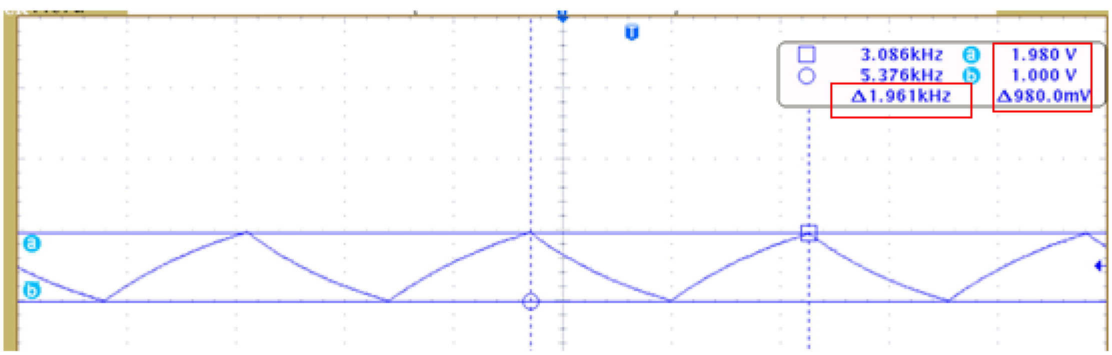


Figure 5. Actual hardware-tested of C1

From Figure 5, we can see 0.98V, 1.961kHz modulation signal, which is very close to our design goals.

PWM signal of UCC28180 with frequency dithering can be observed below in Figure 6:

CH1 = voltage of C1, CH3 = PWM signal of UCC28180

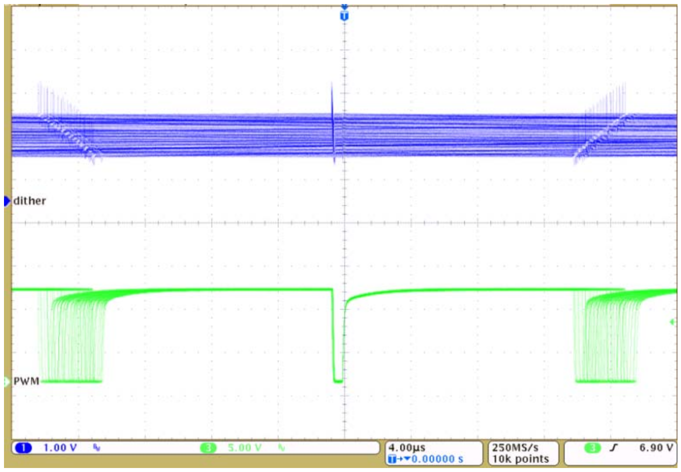


Figure 6. PWM signal of the UCC28180 with dithering added

Figures 7 to 9 show the frequency is varying above and below the 65kHz center frequency.

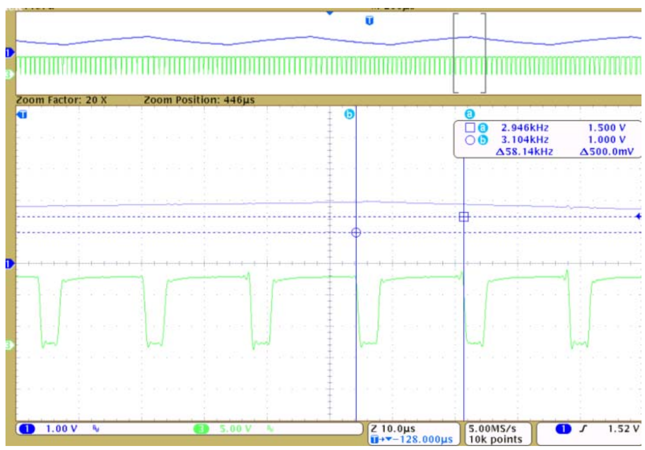


Figure 7. PWM signal of the UCC28180 with dithering added (minimum frequency is 58kHz)

CH3 = PWM signal of UCC28180, CH1 = voltage of C1

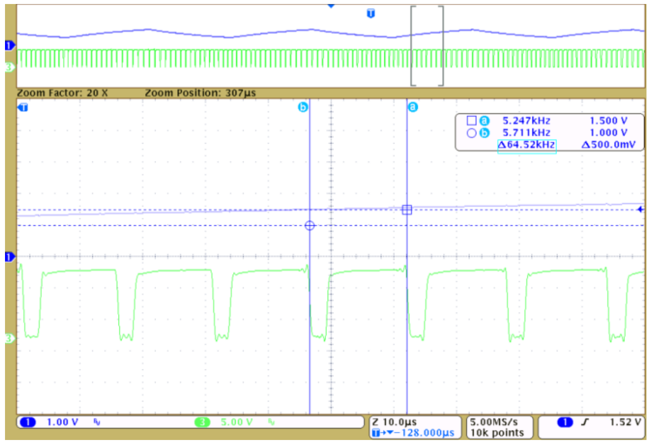


Figure 8. PWM signal of the UCC28180 with dithering added (central frequency is 65kHz)

CH3 = PWM signal of UCC28180, CH1 = voltage of C1

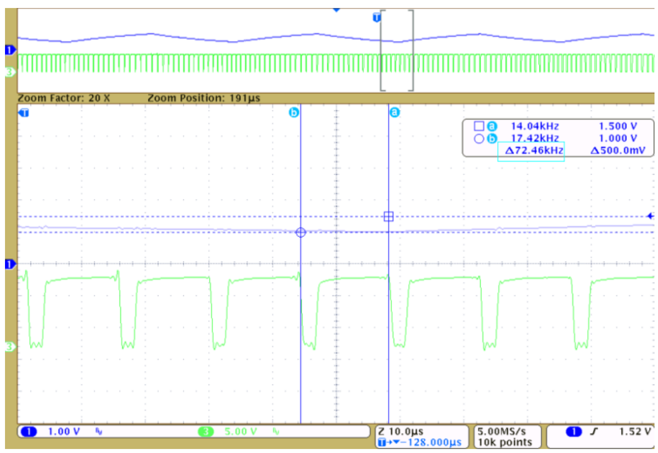


Figure 9. PWM signal of the UCC28180 with dithering added (maximum frequency is 72.5kHz)

CH3 = PWM signal of UCC28180, CH1 = voltage of C1

6. System performance with dithering circuit

6.1 PFC ramp up with dithering circuit

CH1 = voltage of C1, CH2=Iin, CH3=PWM signal of UCC28180, CH4=Vout of PFC

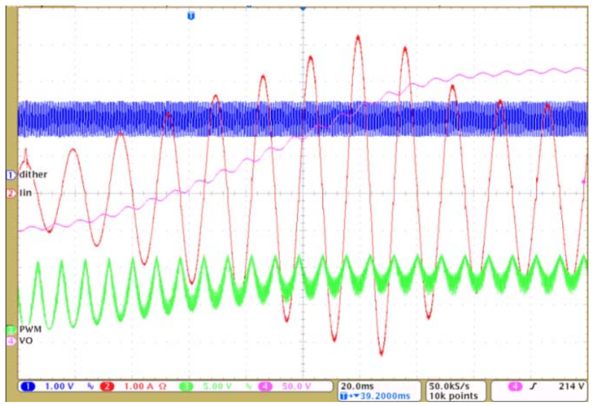
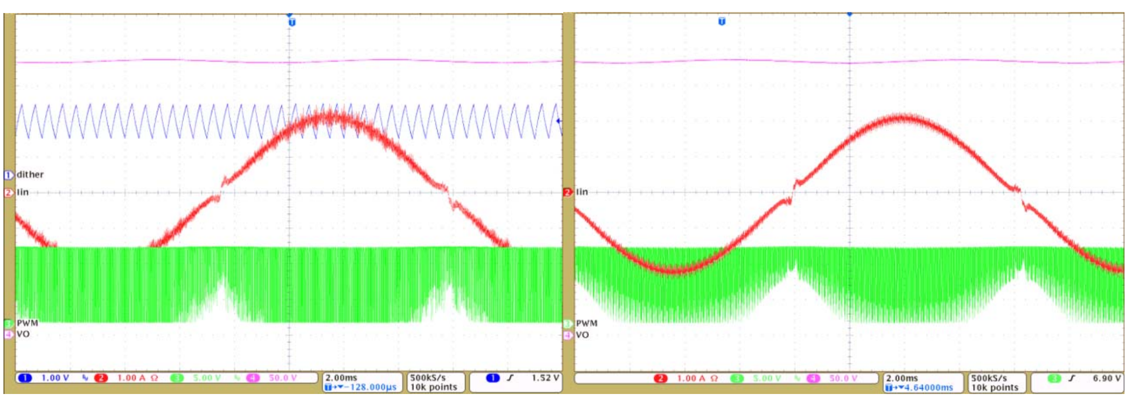


Figure 10.Ramp up with dithering circuit under Vin=110Vac/60Hz, 380V×0.4A load

6.2 THD comparison with dithering to without dithering

	Vout	Iout	With dithering THD	without dithering THD
110V/60Hz	380V	0.2A	5.90%	5%
		0.4A	3.90%	3.43%
230V/50Hz	380V	0.2A	19.58%	18.90%
		0.4A	6.04%	5.50%



a. Vin=110Vac/60Hz, 380V×0.4A load with dithering circuit b. Vin=110Vac/60Hz, 380V×0.4A load without dithering circuit

Figure 11. Input current with and without dithering circuit

The system performance is not changed a lot with frequency dithering circuit. Ramp up is not changed with frequency dithering circuit, iTHD is a litter worse, but still good.

7. Conclusions

The frequency dithering technique is used in industry to reduce EMI. This Application Note shows how to design a circuit using the TLV3201 comparator to dither the switching frequency of a UCC28180 PFC controller. It has been seen that with just a few simple components, the current out of the FREQ pin of the controller can be varied to spread the frequency spectrum of converter, which in turn will spread the EMI emissions to lower the narrowband energy amplitude for EMC/I compliance.

References

1. *"PFC Pre-Regulator Frequency Dithering Circuit", Mike O'loughlin, Texas Instruments' Literature No. SLUA424A, May 2007*
2. *"Frequency Dithering With the UCC28950 and TLV3201", John Stevens, Texas Instruments' Literature No. SLUA646, May 2012*