User's Guide

TPS40100 Buck Controller Evaluation Module User's Guide

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1 Introduction

The TPS40100EVM-001 evaluation module (EVM) is a synchronous buck converter that provides a fixed 3.3-V output up to 10 A from a 12-V input bus. The EVM is designed to start up from a single input supply with no additional bias voltage required. The module uses a TPS40100 midrange input synchronous buck controller.

2 Description

The TPS40100EVM-001 is designed to use a regulated 12-V ±10% (10.8 V–13.2 V) bus to produce a regulated 3.3-V output at up to 10 A of load current. The EVM is designed to demonstrate the TPS40100 in a typical regulated bus to low-voltage application while providing a number of test points to evaluate the performance of the TPS40100. The EVM includes features to demonstrate voltage tracking, margin up/down, enable/disable, and power good. A synchronization pin is provided to allow the EVM to be synchronized to an external clock.

2.1 Applications

- Non-isolated medium current point of load and low voltage bus converters
- Merchant power modules
- Networking equipment
- Telecommunications equipment
- DC power distributed systems

2.2 Features

- 10.8-V to 13.2-V input range
- 3.3-V fixed output
- 10-A_{DC} steady state output current
- Output margin up and down support
- Tracking voltage input to support simultaneous sequencing
- Power-good indicator
- Frequency synchronization input
- Remote sensing scheme
- 380-kHz switching frequency
- Single main switch MOSFET and single synchronous rectifier MOSFET
- Single component side, surface mount design on a 3.0-inch × 3.25-inch evaluation board
- Four layer PCB with all components on top side
- Convenient test points for probing critical waveforms
- Test points for full loop analysis as well as control to output

2.2.1 Using Remote Sense (J3)

The TPS40100EVM-001 provides the user with remote sense capabilities. Remote sense is used to provide more accurate load regulation by compensating for losses over terminal connections and load wire resistance.

When remote sense is used properly, the converter will regulate the voltage at the point where sense connections are placed. These remote sense connections are usually placed at the intended load. As the load is increased the direct output of the converter will rise to compensate for IR losses.

CAUTION

Long wiring connections can cause the converter to act irregularly. This can show up as pulse width jitter or an oscillatory effect on the ripple voltage. If this condition occurs, check the setup and make adjustments. Please see Section 5.3.2.

2.2.2 Simultaneous Tracking (J3)

The EVM is equipped to provide the ability to demonstrate the tracking feature of the TPS40100. In addition, the module can be configured to have multiple TPS40100EVMs track. The voltage tracking function allows the TPS40100 to track an external ramp (provided on EVM). This tracking feature allows single or multiple modules to track an external ramp in order to comply with the demands of many microprocessor and memory applications. Please see Section 5.3.3.

2.2.3 Enable (SW2)

The EVM is equipped with an enable/disable switch. Please see Section 5.3.4. Closing S1 will disable the device by pulling the UVLO pin of the TPS40100 low. Opening the S1 will enable the device, provided that the appropriate input voltage is present. J3 pin 4 is an enable monitor pin that provides a connection for user observation.

2.2.4 Margin Up/Down (J4)

The margin up and down feature of the EVM provides the user with the ability to trim or margin the output of the converter up/down by 3% or 5%. The EVM is equipped with convenient jumper settings to give the user the ability to trim the output voltage. Please see Section 5.3.5 for more detailed test setup information.

2.2.5 Power Good (J1)

The EVM contains a power-good pin to provide the user with a “power ok” signal. This pin is pulled up through a resistor to the 5VBP pin of the TPS40100. If any of the following conditions occur, the power-good pin will pull low.

- Soft start is active (V_{SS} < 3.5 V).
- Tracking is active ($V_{trackout}$ > .7 V).
- V_{FB} < 0.61 V
- V_{FB} > 0.77 V
- V_{UVLO} < 1.33 V
- Overcurrent condition exists
- Die temperature is greater than 165°C.

This pin can be monitored with an oscilloscope to observe its behavior. Please see Section 5.3.6.

2.2.6 Synchronization (J1)

Two TPS40100-EVM can be synchronized to an external clock source of a higher frequency than that of the free running PWM clock. This is a feature that can aid with input filter design. It is recommended that the synchronization frequency be no more than 120% of the free running frequency. The EVM is configured to a switching frequency of 370 kHz, so the external frequency into the synchronization pin should be no more than 470 kHz. Please see Section 5.3.6.

3 Electrical Performance Specifications

Table 3-1. TPS40100EVM-001 Electrical and Performance Specifications

Parameter	Notes and Conditions		Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Input voltage range			10.8		13.2	V
Max input current	V_{IN} = 10.8 V, I_{OUT} = 10 A			3.5		A
No-load input current	V_{IN} = 13.2 V, I_{OUT} = 0 A			100		mA
OUTPUT CHARACTERISTICS						
Output voltage			3.22	3.30	3.39	V
Output voltage	Line regulation (10.8 V < V_{IN} < 13.2 V, I_{OUT} = 5 A)				1%	
Regulation	Load regulation (0 A < I_{OUT} < 10 A, V_{IN} = 12 V)				1%	
Output voltage ripple	V_{IN} = 13.2 V, I_{OUT} = 10 A			25		mVpp
Output load current			0		10	A
Output over current				15		A
SYSTEM CHARACTERISTICS						
Switching frequency			350	380	410	kHz
Full load efficiency	V_{OUT} = 3.3 V, I_{OUT} = 10 A	V12V_IN = 10.8 V		93.9		
		V12V_IN = 12 V		93.5%		
		V12V_IN = 13.2 V		93.4%		

4 Schematic

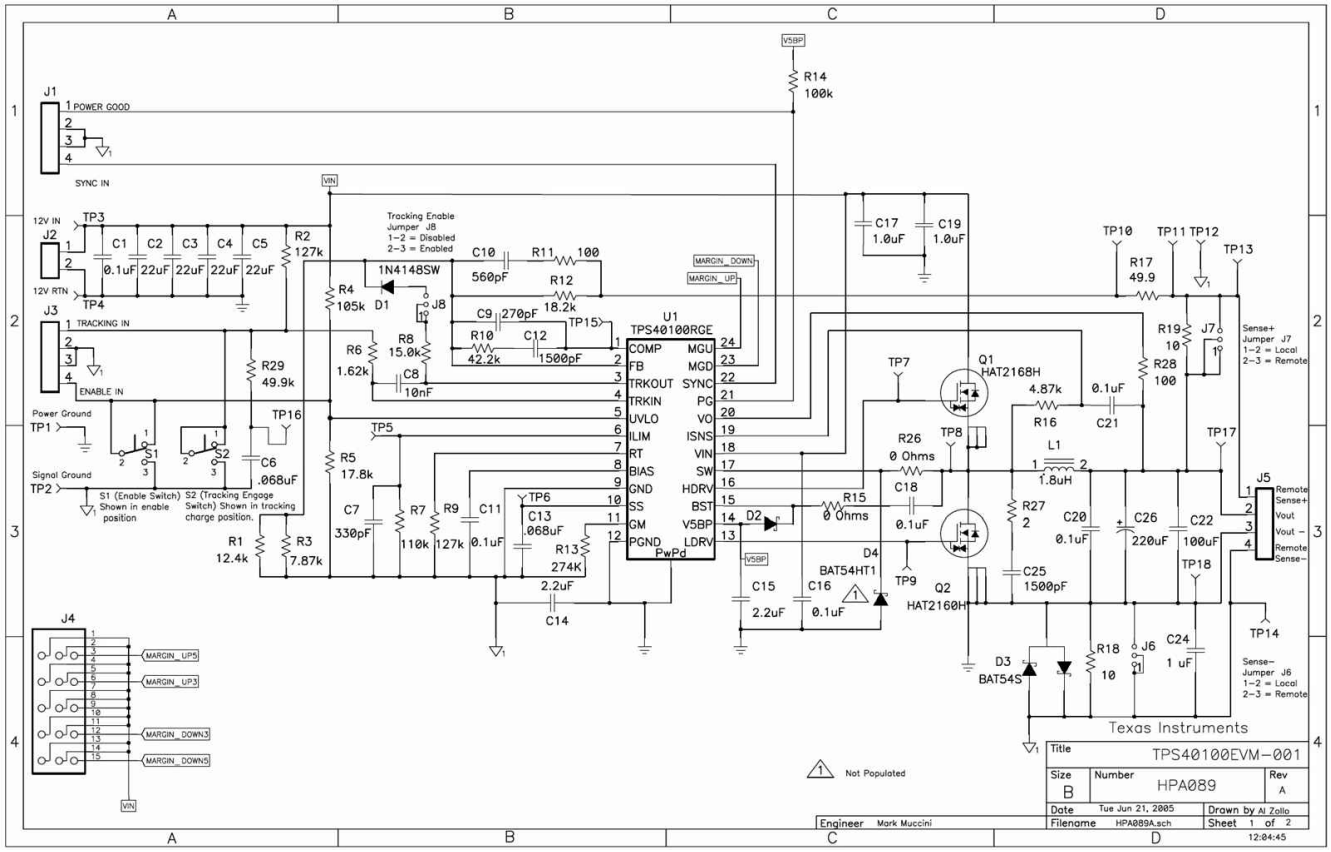
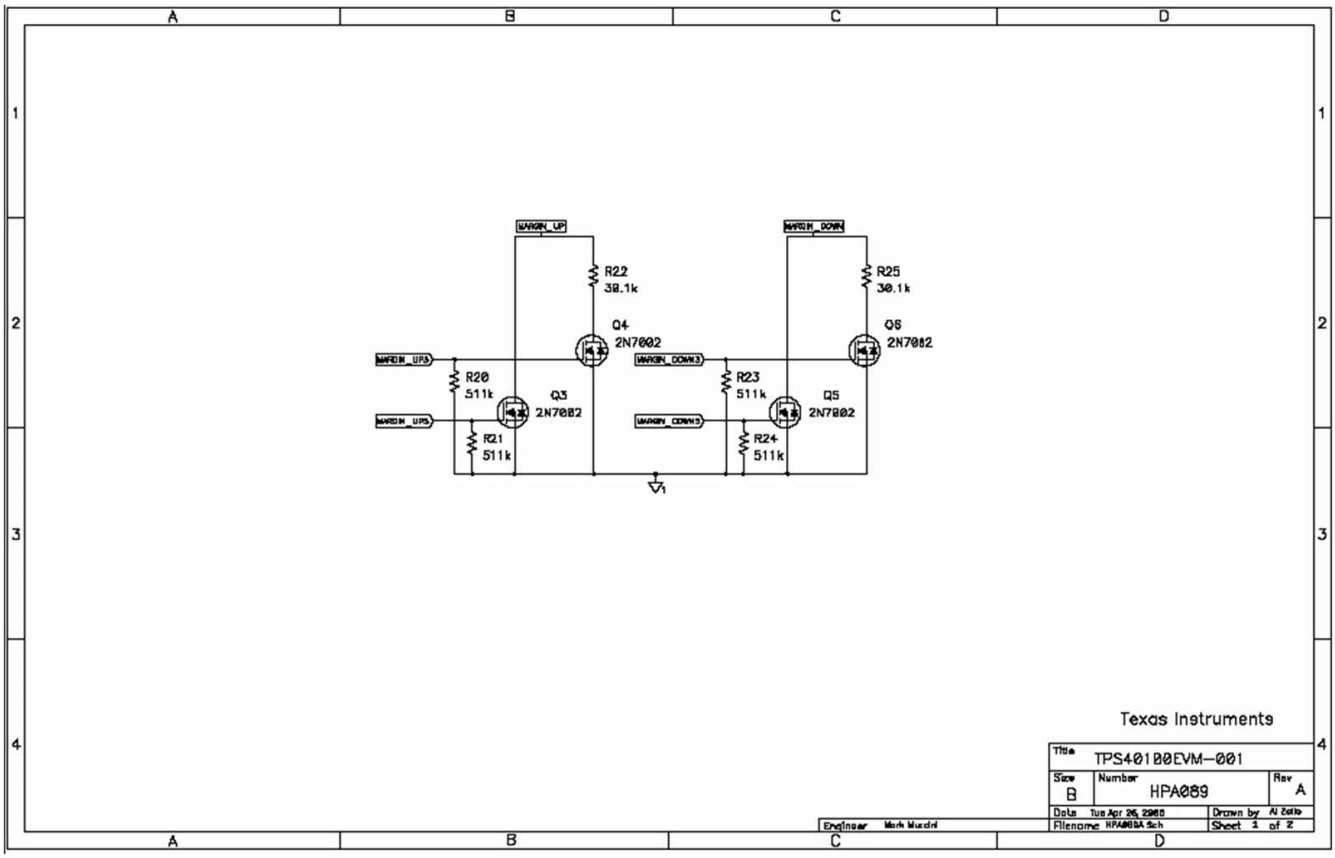


Figure 4-1. TPS40100EVM-001 Power Stage/Control Schematic



Note

Component values are for reference only.

Figure 4-2. TPS40100EVM-001 Margin Control

5 Test Setup

5.1 Equipment

5.1.1 Voltage Source (V_{IN})

The input voltage source (V_{IN}) should be a 0-V to 15-V variable DC source capable of 5 A_{DC}. Connect VIN to J2 as shown in Figure 5-2.

5.1.2 Meters

- Ammeter1: 0 A to 5 A_{DC}, ammeter
- Voltmeter1: VIN, 0-V to 15-V voltmeter
- Voltmeter2: VIN, 0-V to 5-V voltmeter

5.1.3 Loads (LOAD1)

The output load (LOAD1) should be an electronic constant current mode load capable of 0 A_{DC} to 10 A_{DC} at 3.3 V.

5.1.4 Recommended Wire Gauge

VIN to J2

The connection between the source voltage, V_{IN}, and J2 of EVM can carry as much as 5 A_{DC}. The minimum recommended wire size is AWG #16. Shorter lengths of input wire will aid in reducing inductance and provide better overall performance.

J5 to LOAD1 (Power Pins 2 and 3)

The power connection between J5 of EVM and LOAD1 can carry as much as 10 A_{DC}. It is recommended that the user use AWG#16 wire. It is recommended that the load wires be kept as short as possible. This will aid in performance, most notably in transient response.

J2 to LOAD1 (Remote Sense)

If remote sense is to be used, ensure that J6 and J7 are in the remote sense enable position (shunt pins 1 and 2).Load wires and sense wires should be kept less than six inches to ensure proper functionality. The remote sense wires connecting J5 (pins 1 and 4) and LOAD1 carry less than 1 A_{DC}. The minimum recommended wire size is AWG #22 with the total length of less than six inches long.

5.1.5 Other

Fan

This evaluation module includes components that can get hot to the touch. A small fan capable of 200–400 LFM is required to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended while powered or probed while the fan is not running.

Oscilloscope

A 60-MHz or faster oscilloscope can be used to monitor many points on the EVM. For output ripple voltage measurements, the Oscilloscope should be set for the following to take output ripple measurements:

- 20-MHz bandwidth limiting
- 1-MW impedance
- AC coupling
- 1-ms/division horizontal resolution
- 10-mV to 20-mV/division vertical resolution

Function Generator

A function generator capable of sourcing a 0-V to 5-V square wave at frequencies past 400 Khz.

5.2 Equipment Setup

5.2.1 Initial EVM Jumper and Switch Settings

Figure 5-2 is the basic test setup recommended for evaluating the TPS40100EVM-001. The EVM is shipped with the following in the default position:

- The enable switch (S1) is open across pins 2 and 3. This is the enable position.
- The tracking enable jumper (J8) has shunt positioned across pins 1 and 2, disabling the tracking feature.
- The tracking engage switch (S2) is open across pins 2 and 3. This enables the tracking ramp to charge.
- Remote sense jumpers (J6 and J7) have shunts positioned across pins 2 and 3, enabling local connector sensing.
- Margin shunts positioned in the margin disable position.

5.2.2 Procedure

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM. An electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the DC input source, VIN, it is advisable to limit the source current to 5.0 A maximum. Make sure VIN is initially set to 0 V and connected as shown in Figure 5-2.
3. Connect an ammeter between the positive output of the input supply and the positive input of the EVM (J2, Pin 1).
4. Connect voltmeter #1 to TP3 and TP4. These are the EVM input supply monitoring points.
5. Connect LOAD1 to J5. Set LOAD1 to constant current mode to sink 0 A_{DC} before input voltage is applied.
6. Connect voltmeter #2 across TP13 and TP14. This is the EVM output supply monitoring point. This configuration is local sensing.
7. Remove the oscilloscope probe jacket and position the probe as shown in Figure 5-1. TP17 and TP18 are implemented to provide the user with the means to achieve good noise immune measurements of ripple voltage and transient response.

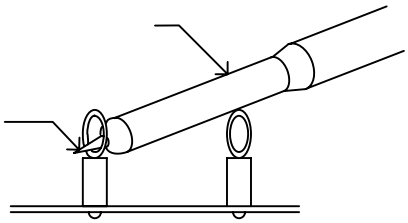


Figure 5-1. Probe Position for Ripple Measurement

8. Place a fan as shown in Figure 5-2 and turn it on, making sure air is flowing across the EVM.

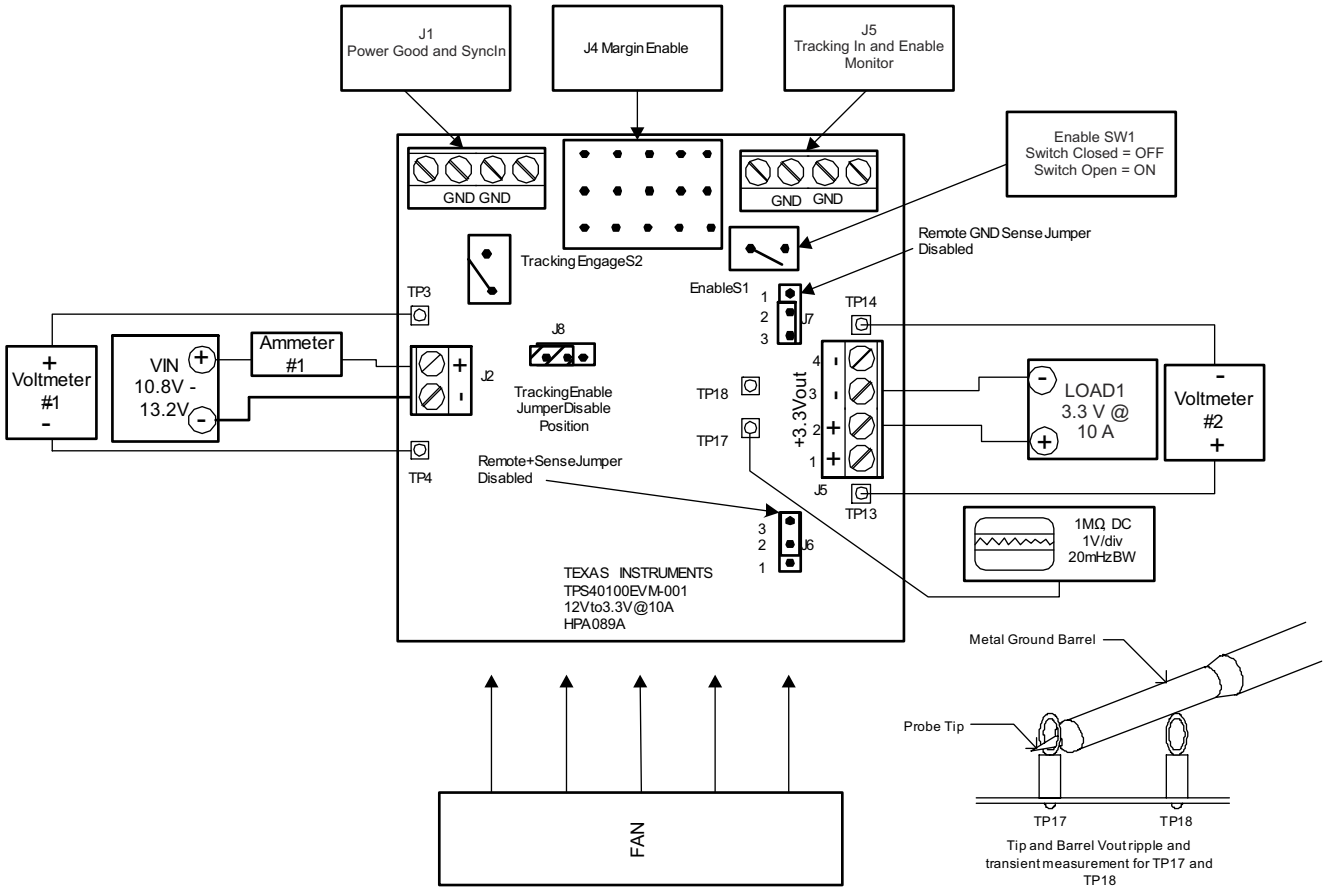


Figure 5-2. TPS40100EVM-001 Recommended Test Setup

5.2.3 Start-Up and Shutdown Procedure

1. Increase VIN (V1) from 0 V to 12 V_{DC}.
2. Observe that V_{OUT} has risen to its nominal voltage.
3. Vary LOAD1 from 0 A_{DC}–10 A_{DC}.
4. Vary VIN from 10.8 V_{DC} to 13.2 V_{DC}.
5. Decrease LOAD1 to 0 A.
6. Decrease VIN to 0 V.

5.2.4 Equipment Shutdown

1. Shut down the oscilloscope.
2. Shut down LOAD.
3. Shut down VIN.
4. Shut down the fan.

5.3 Other Tests

5.3.1 Adjusting Output Voltage (R1 and R3)

The regulated output voltage can be adjusted by changing the values of the feedback resistors, R1 and R3. R19 and R17 are located in the feedback to provide the user with positive remote sense and the ability to perform loop analysis with a frequency/gain analyzer. Resistors R12 and the parallel combination of R1 and R3 are the dominant resistors associated with setting the output voltage. The following are the equations associated for establishing the output voltage.

$$R_{PARALLEL} = \frac{R1 \times R3}{R1 + R3} \quad (1)$$

$$V_{OUT} = V_{REF}\left[\frac{R12 + R17}{R_{PARALLEL}} + 1\right] \quad (2)$$

$$R_{PARALLEL} = \left[\frac{V_{REF}}{V_{OUT} - V_{REF}}\right] \times \left(R17 + R12\right) \quad (3)$$

where

- V_{VREF} = 0.690 V
- R17 = 49.9 Ω
- R12 = 18.2 kΩ

R1//R3 can be adjusted to provide user defined output voltages. Table 5-1 contains values for R1//R3 to generate popular output voltages.

Table 5-1. Adjusting V_{OUT} with R1/R3

VOUT	R1//R3 ($R_{PARALLEL}$)	R1	R3
3.3 V	4.82 k	12.4 k	7.87 k
2.5 V	6.95 k	7.15 k	237 k
2.2 V	8.33 k	8.66 k	205 k
2.0 V	9.61 k	10.0 k	237 k
1.8 V	11.34 k	12.1 k	178 k
1.5 V	15.55 k	16.2 k	365 k
1.2 V	24.69 k	26.1 k	422 k

5.3.2 Remote Sense Test Setup

In order for the remote sense feature of the TPS40100EVM-001 to function properly, it is essential that the test setup be configured correctly. Use the following steps to set up the remote sense:

1. Ensure that the remote sense jumpers J7 and J8 are shunted across pins 1 and 2.
2. Connect load wires with a maximum length of six inches from pin 2 of J5 (+Vout) to the positive terminal of the load. Connect the same length of wire from pin 3 of J5 (RTN) to the negative terminal of the load. Be sure to properly gauge the load wires for 10 A. AWG#16 is recommended.
3. Connect a sense wire from J5 pin 1 to the positive terminal of the load. This is the +senseline. Be sure to not exceed six inches in length. AWG#22 wire is recommended.
4. Connect a sense wire from J5 pin 4 to the negative terminal of the load. This is the –sense line. Be sure to not exceed six inches in length. AWG#22 wire is recommended.
5. Monitor voltage at TP13 and TP14 using a voltmeter. This will be the regulated voltage at the load.
6. Monitor voltage at J5 pins 2 and 3. This is the voltage at the output connector. This voltage will increase based on the load.
7. Set load to 0 A, constant current. Both monitoring points should read very close to the same value.
8. Increase the load gradually and observe the difference in voltages present at the monitoring points. The set voltage (3.3 V) will be regulated at the load; this will be noted at TP13 and TP14. The direct output of the converter (J5 pins 2 and 3) will read a higher voltage. As IR losses increase over load wires and terminals, the direct output of the converter will compensate by raising the voltage to keep within regulation at the load.

CAUTION

Long distance runs from the output of the converter and the load will cause erratic behavior. This can show up as pulse width jitter or an oscillatory effect on the ripple voltage. If this condition occurs, check the setup and make adjustments. Please see Figure 5-3 for test setup.

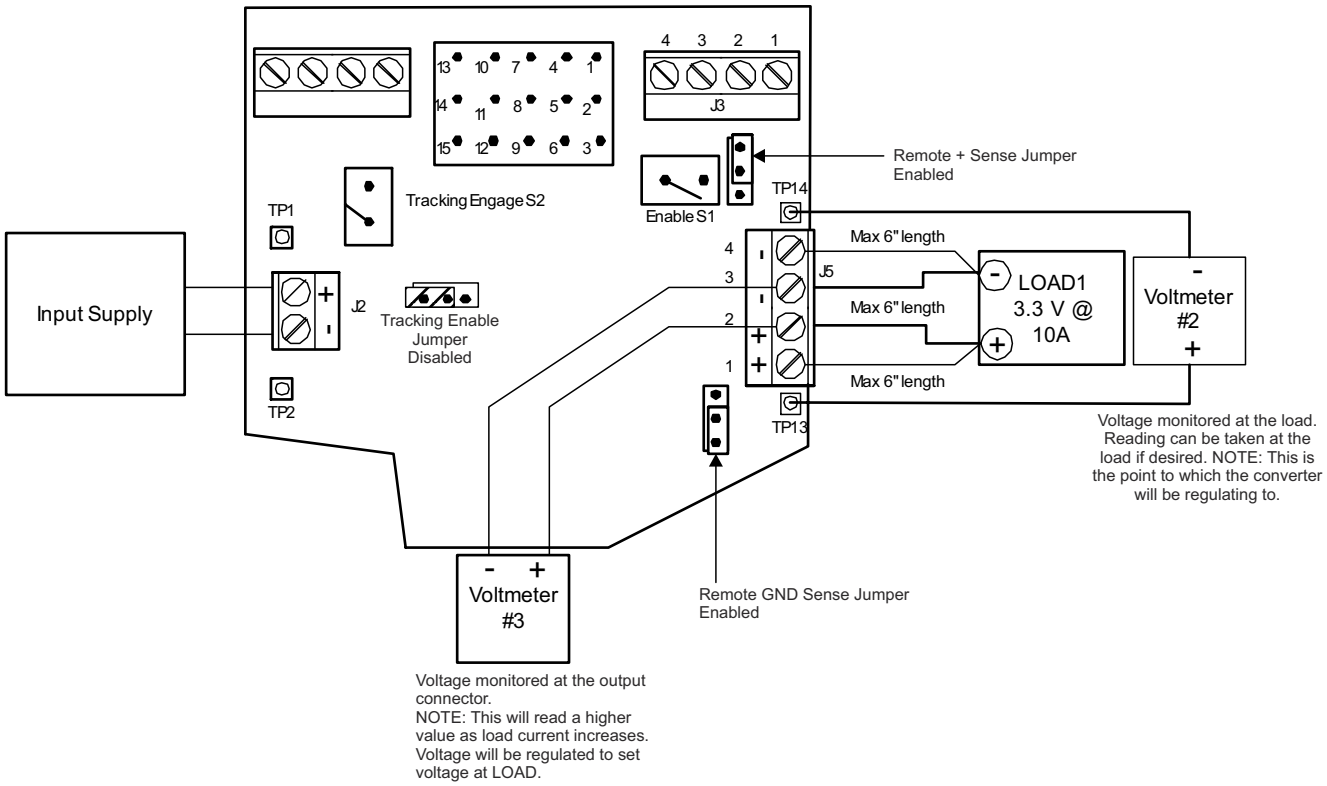


Figure 5-3. TPS40100EVM-001 Recommended Remote Test Setup

5.3.3 Voltage Tracking Test Setup

The following procedure is for a single EVM demonstration of the track function. Please see Figure 5-4.

1. Shunt pins 2 and 3 of J8 (tracking enable jumper).
2. The tracking engage switch (S2) should be in the closed position.
3. Connect an oscilloscope probe to the TRACKING IN pin (J3 pin 1) and VOUT (TP 17 and 18).
4. Connect the load to the output of the EVM and set from 1 A–10 A (User selectable).
5. Power on the EVM with an input voltage of 10.8 V–13.2 V (Allow for SS voltage to reach 3.5 V to ensure proper tracking performance or wait one to two seconds).
6. Open the Tracking Engage Switch (S2) (Shorting pins 1 and 2 open) and observe how VOUT tracks the TRACKING IN pins rising voltage. Waveforms should be simultaneous.
7. Close the Tracking Engage (S2) (Shorting pins 2 and 3 open) and observe how VOUT tracks the TRACKING IN pins falling voltage. Waveforms should be simultaneous.

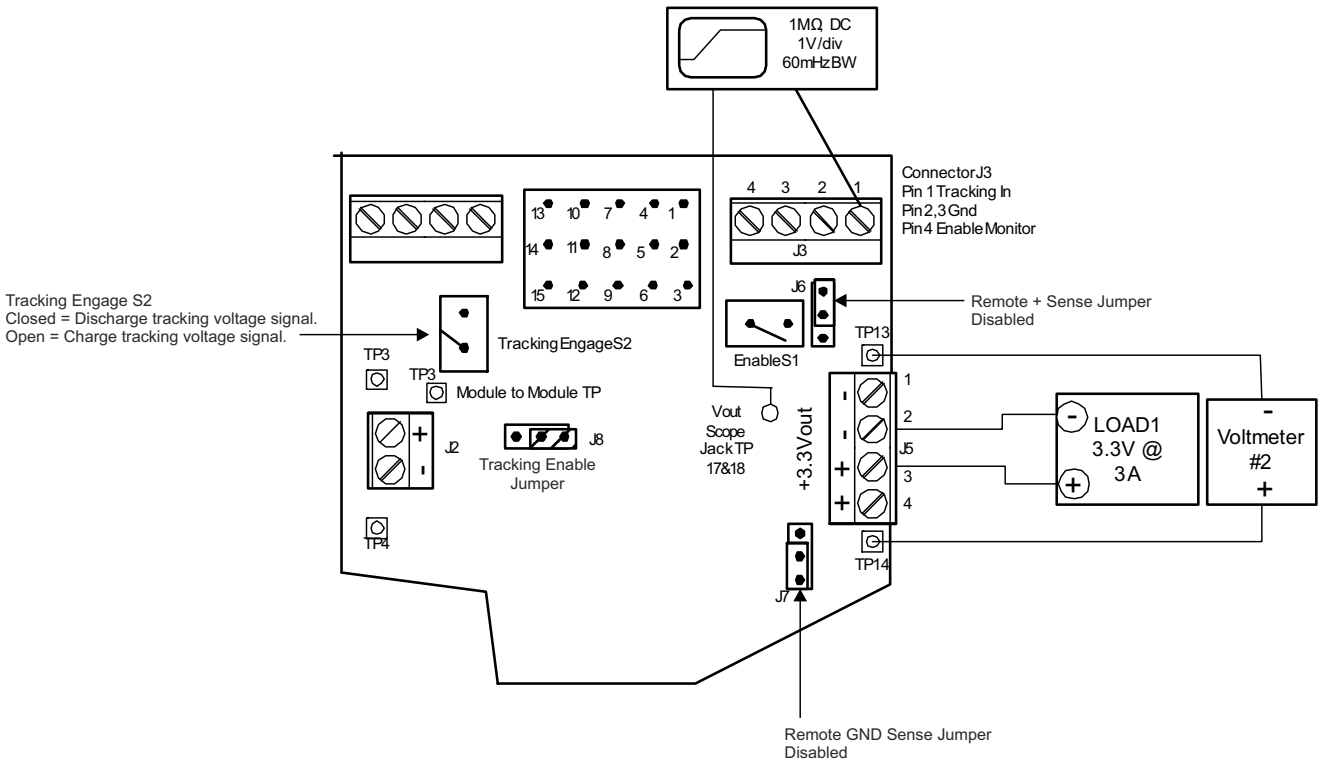


Figure 5-4. TPS40100EVM-001 Single EVM Tracking Test Setup

5.3.3.1 Single Unit Tracking (Charge)

- Channel 1 (+ 3.3 V_{OUT})
- Channel 4 (Tracking In)
- V_{IN} = 12 V
- I_{OUT} = 10 A

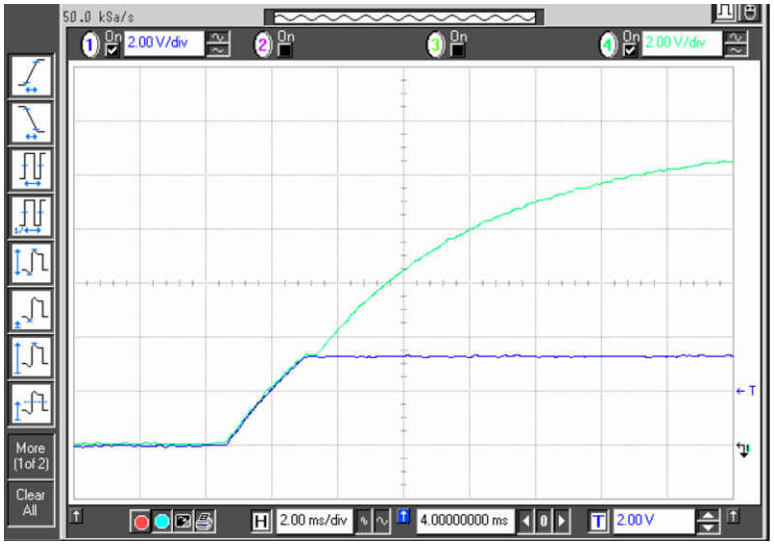


Figure 5-5. Single EVM Tracking Charging Ramp

5.3.3.2 Single Unit Tracking (Discharge)

- Channel 1 (+ 3.3 V_{OUT})

- Channel 4 (Tracking In)
- V_{IN} = 12 V
- I_{OUT} = 10 A

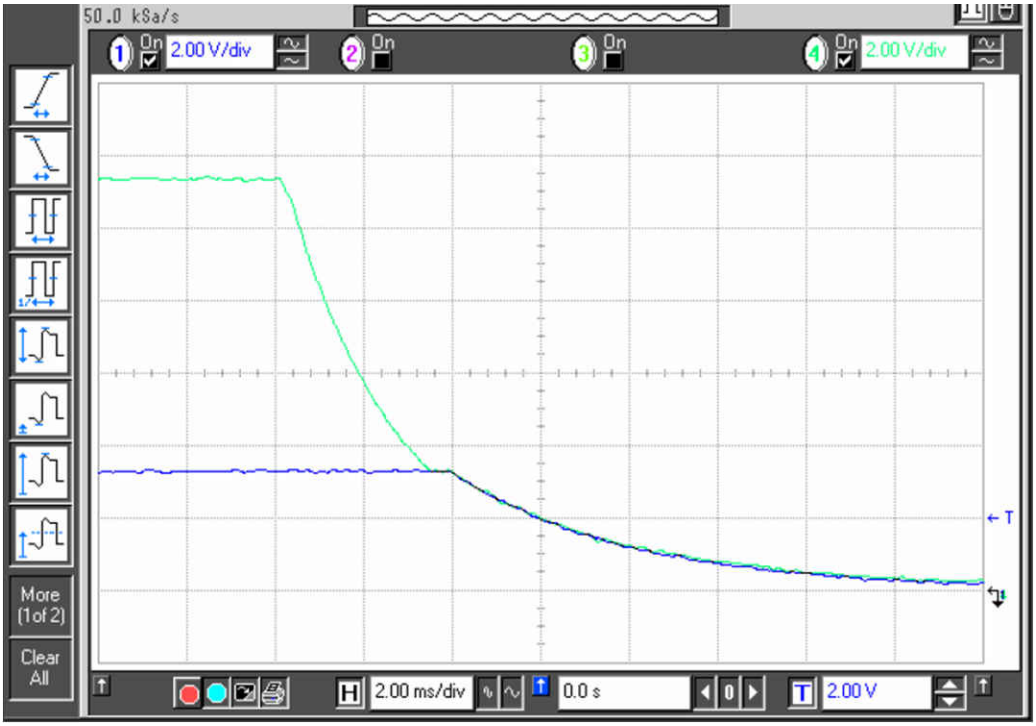


Figure 5-6. Single EVM Tracking Discharging Ramp

To demonstrate multiple EVM (2 modules) tracking, the following procedure must be followed to ensure proper functionality. The second TPS40100 EVM should be configured to a different output voltage.

1. Shunt pins 2 and 3 of the Tracking Enable Jumper (J8) for both modules.
2. Connect J3 pin 1 of each EVM.
3. Connect TP16 of each EVM. This is the module to module test point. This allows either module to be the control EVM through S2.
4. The Tracking Engage Switch (S2) should be in the closed (shorting pins 2 and 3) position on the control EVMs.
5. Connect an oscilloscope probe to the TP17 and 18 of both modules and pin 1 of J3 of one of the modules. Modules should have a common input voltage and return.
6. Remote sense jumpers (J6 and 7) should have pins 2 and 3 shunted, activating local output sensing.
7. Apply an input voltage of 10.8 V to 13.2 V.
8. Allow the SS voltage to reach 3.5 V.
9. Open the control EVM Tracking Engage Switch (S2) (Opening pins 2 and 3) and observe the monitored points (Both EVM outputs and the tracking in voltage. Output voltage should follow the tracking in voltage until reaching the regulation point).
10. Close the Tracking Engage Switch (S2) (Shorting pins 2 and 3) of the control EVM and observe the monitored points (Both EVM outputs and the tracking in voltage). Falling waveforms should be coincidal.

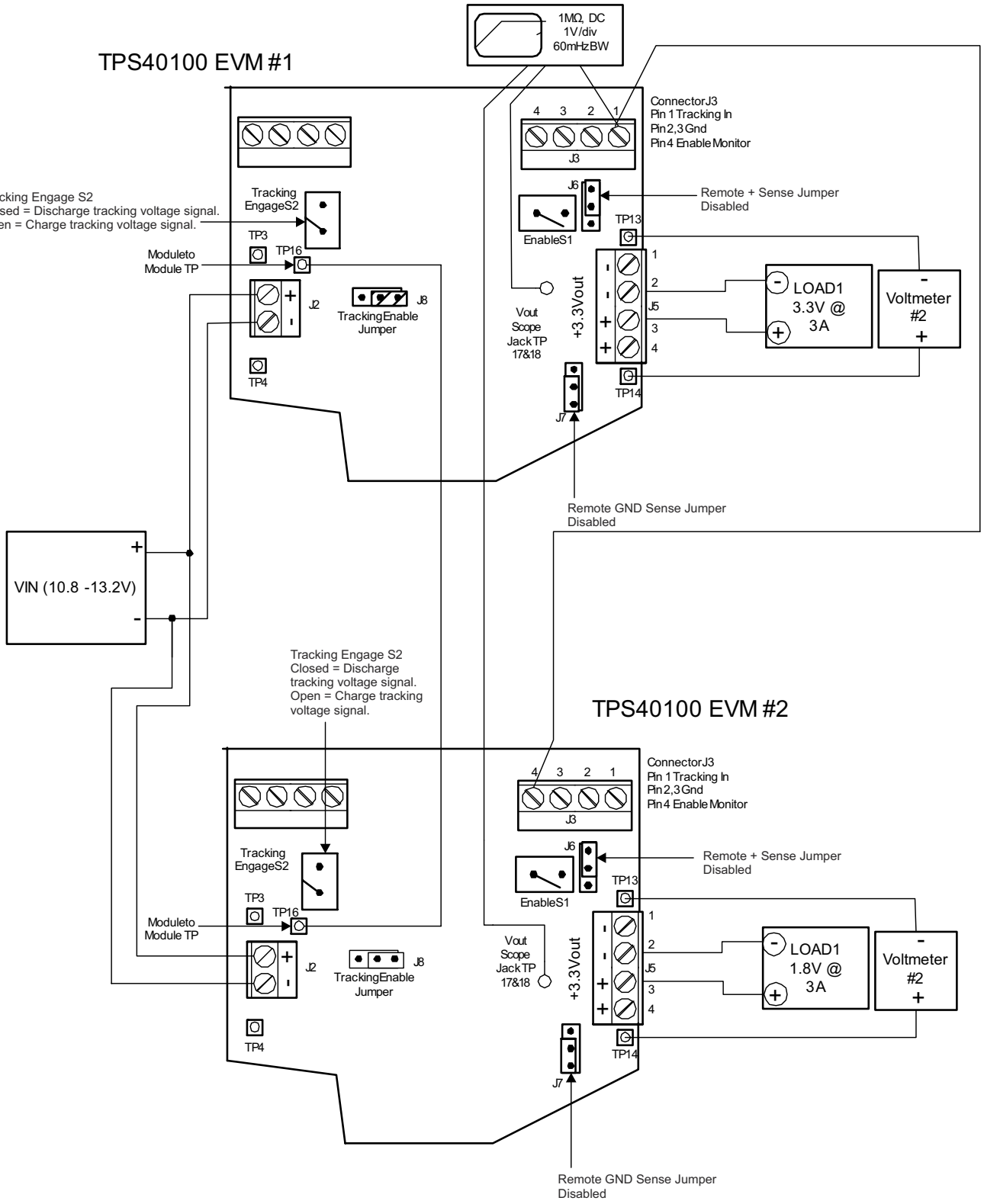


Figure 5-7. TPS40100EVM-001 Dual EVM Tracking Test Setup

5.3.4 Enable and Disable Test Setup

To begin testing, set up the EVM according to Section 5.2.2. The switch (ENABLE S1) provides the ability to enable and disable the device. Please see Figure 5-8 for illustration. Closing S1 will disable the device by pulling the UVLO pin of the TPS40100 low. Opening S1 will enable the device, providing that the appropriate input voltage is present. J3 pin 4 is an enable monitor pin providing a connection for user observation.

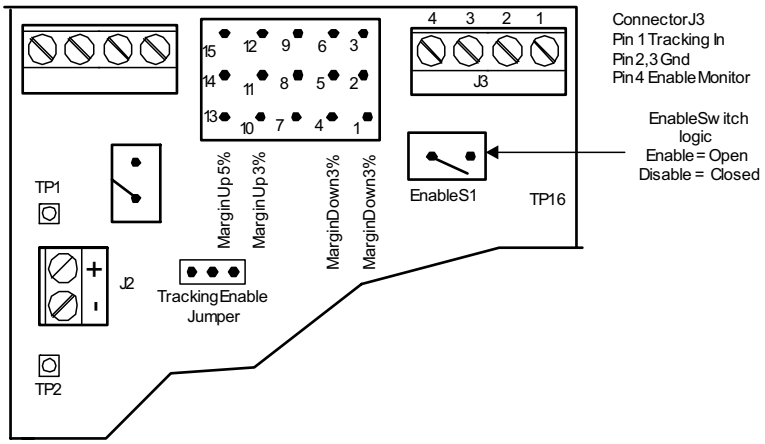


Figure 5-8. TPS40100EVM-001 Enable Test Setup

5.3.4.1 Power-On Enable

- Channel 1 (+ 3.3 V_{OUT})
- Channel 3 (Power good)
- Channel 4 (SS)
- V_{IN} = 12 V
- I_{OUT} = 10 A

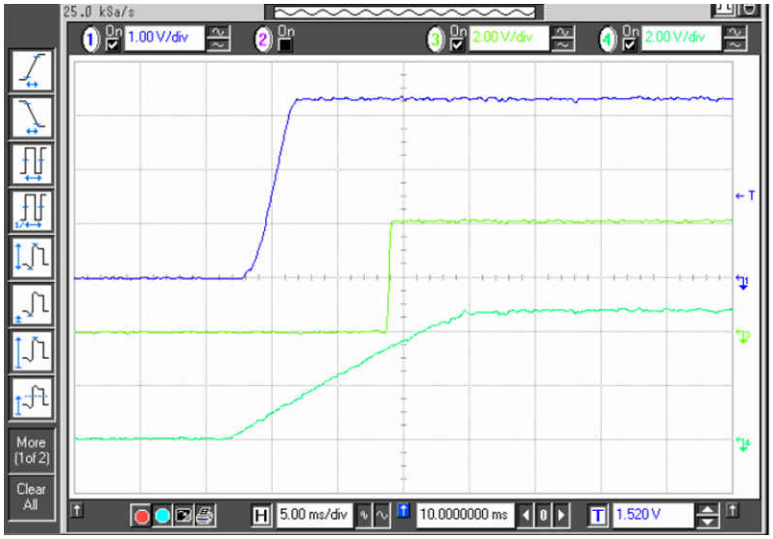


Figure 5-9. Power On from Enable

5.3.5 Margin Test Setup

To begin testing, set up the EVM according to Figure 5-2. Choose the desired margin level. Connector J4 pins 3, 6, 12, and 15 are designated pins that can be connected to adjacent VIN pins (2, 5, 11, and 14) of J4 to enable the desired margin level. Please see Figure 5-10. For example, to margin the unit up 5%, connect a jumper across pins 2 and 3 of J4.

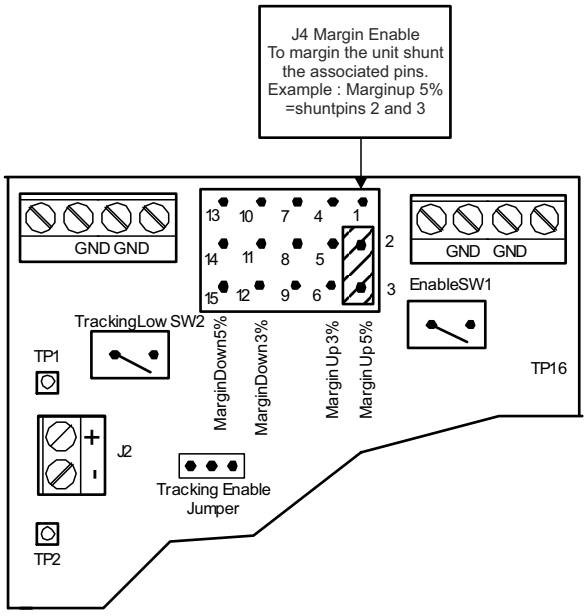


Figure 5-10. TPS40100EVM-001 Margin Test Setup

5.3.5.1 Margin Up 5%

- Channel1 V_{OUT} (looking at transition of voltage 165 mV)
- Channel 2 corresponding margin pin
- V_{IN} = 12 V
- I_{OUT} = 10 A

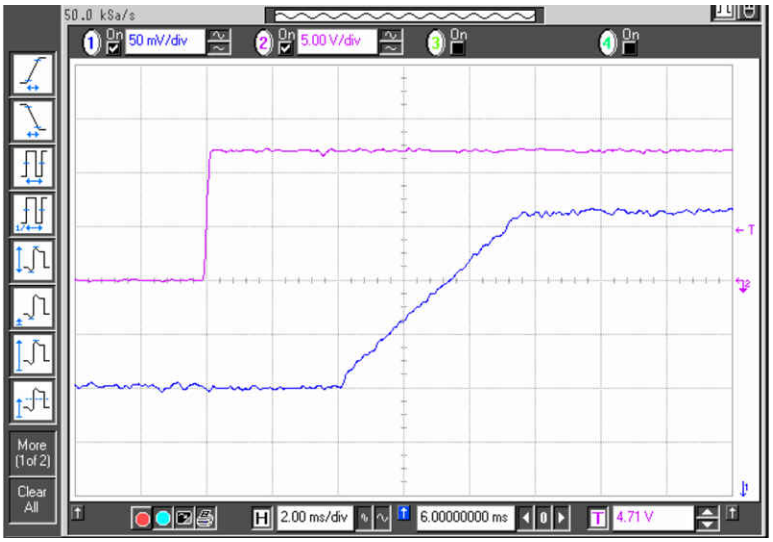


Figure 5-11. Margin Up 5%

5.3.6 Power Good and Synchronization Test Setup

The TPS40100EVM-100 has the ability to be synchronized to an external clock. To begin testing, set up the EVM according to Figure 5-2. Connector J1 contains both the power-good pin and sync-in pin. Power good can be monitored for its steady state response with a DMM or with an oscilloscope to illustrate its dynamic response. The power-good voltage swing will range from 0 V– 4.5 V depending on the condition of the output. A low on this pin dictates a power fault and a high (4.5 V) conveys “power ok.”

Pin 4 of J1 is the input for an external clock frequency. To test, set up a function generator to provide a squarewave at a frequency of above 410 kHz and below 480 kHz. The function generator should be set to provide a 0-V to 5-V square wave with a 50% duty cycle. Once power is applied to the EVM, apply the external

clock to the sync-in pin and observe the gate drive of the low-side MOSFET (Q2). This should be measured using an oscilloscope measuring at TP7. Gate drive pulse will coincide with external clock frequency. Please see Figure 5-12.

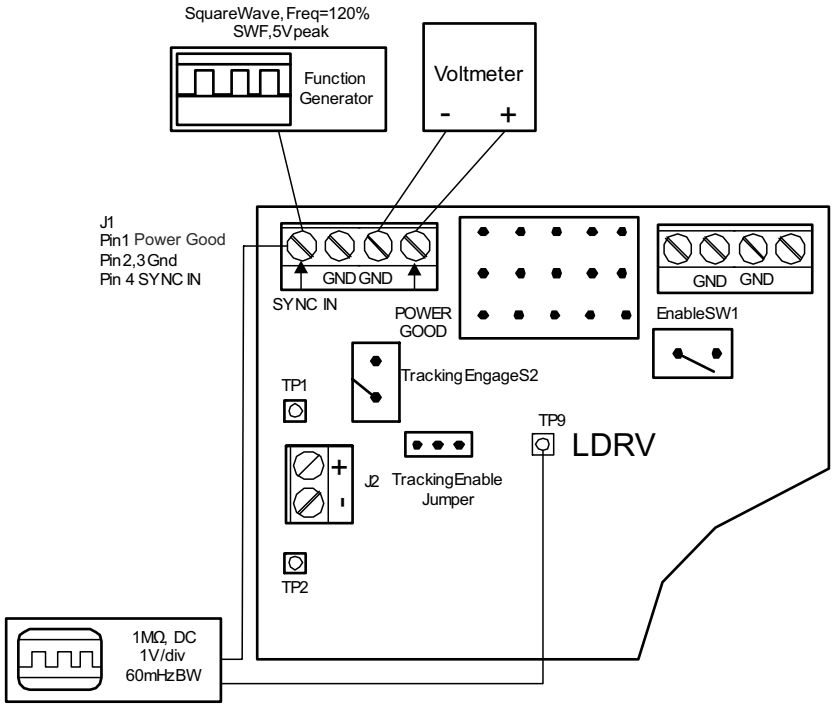


Figure 5-12. TPS40100EVM-001 Power Good and Synchronization Test Setup

5.3.6.1 Synchronization

- Channel 1 switch node voltage
- Channel 2 external clock signal
- V_{IN} = 12 V
- I_{OUT} = 10 A

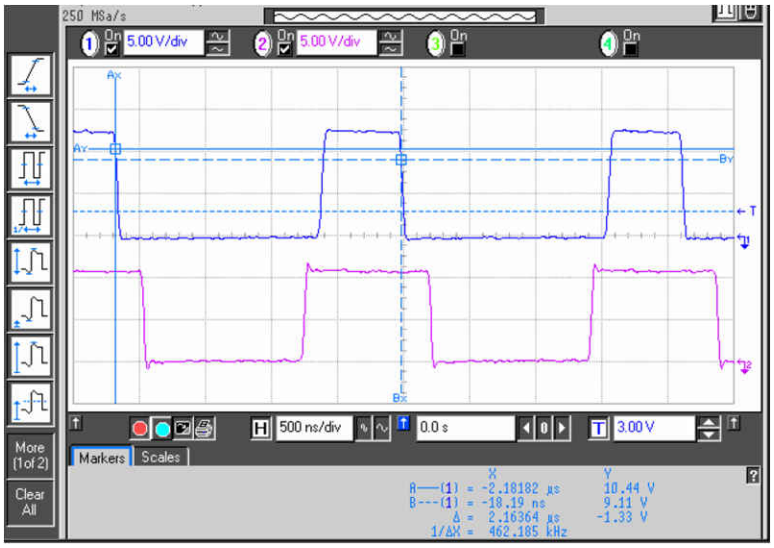


Figure 5-13. Synchronization

6 TPS40100EVM Typical Performance Data and Characteristics Curves

Figure 6-1 through Figure 6-3 present typical performance curves for the TPS40100EVM-001. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and can differ from actual field measurements.

6.1 Efficiency

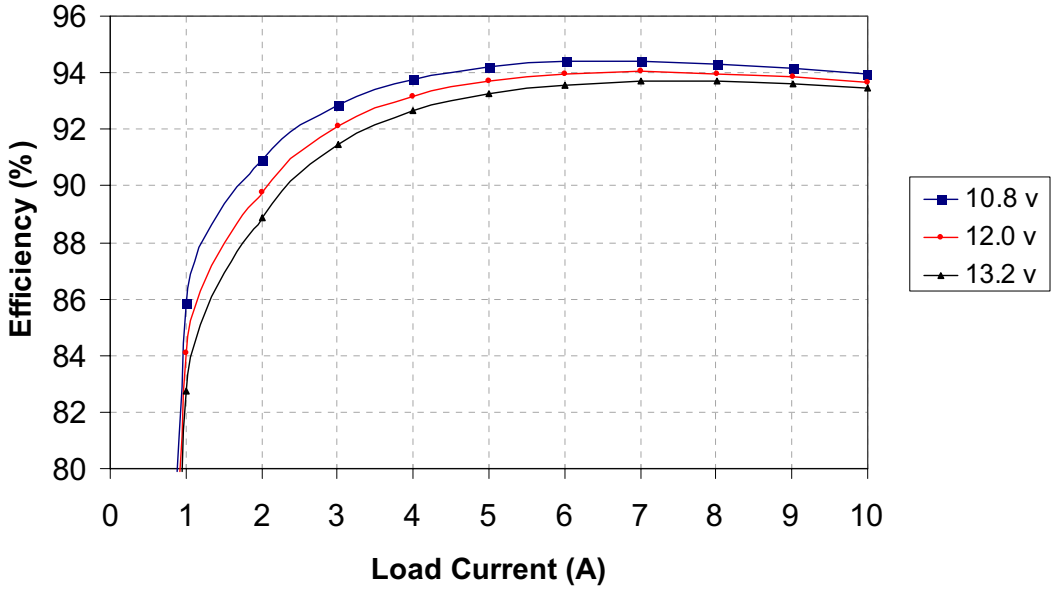


Figure 6-1. TPS40100EVM-001 Efficiency
V_{12V_IN} = 10.8 V–13.2 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A–10 A

6.2 Line and Load Regulation

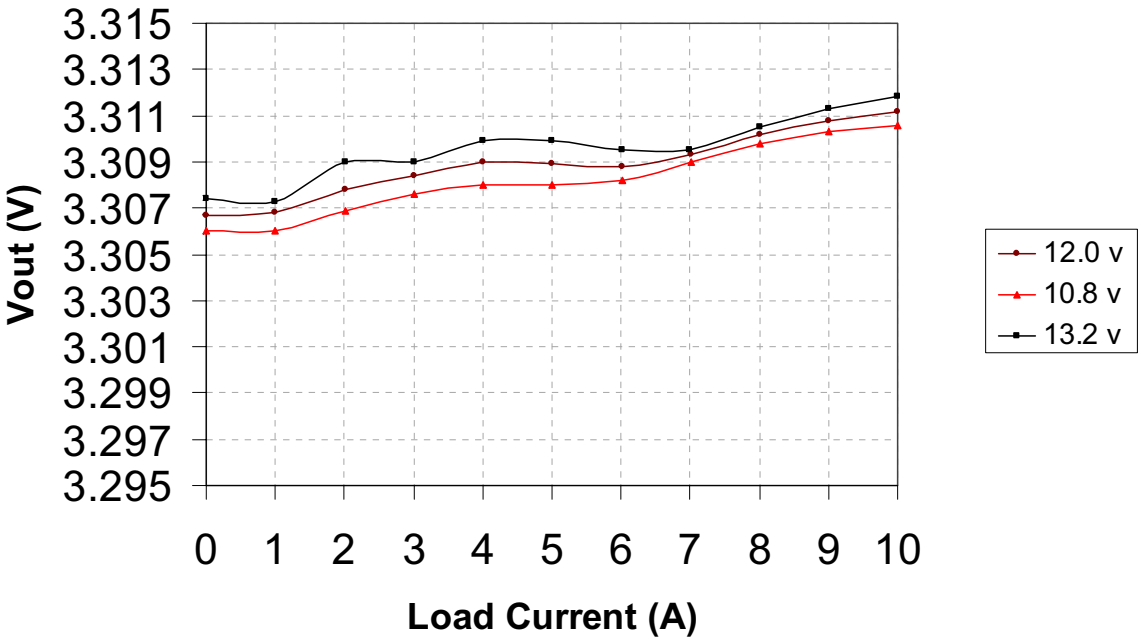


Figure 6-2. TPS40100EVM-001 Line Regulation
I_{OUT} = 10 A, V_{IN} = 10.8 V–13.2 V

6.3 Loop Stability

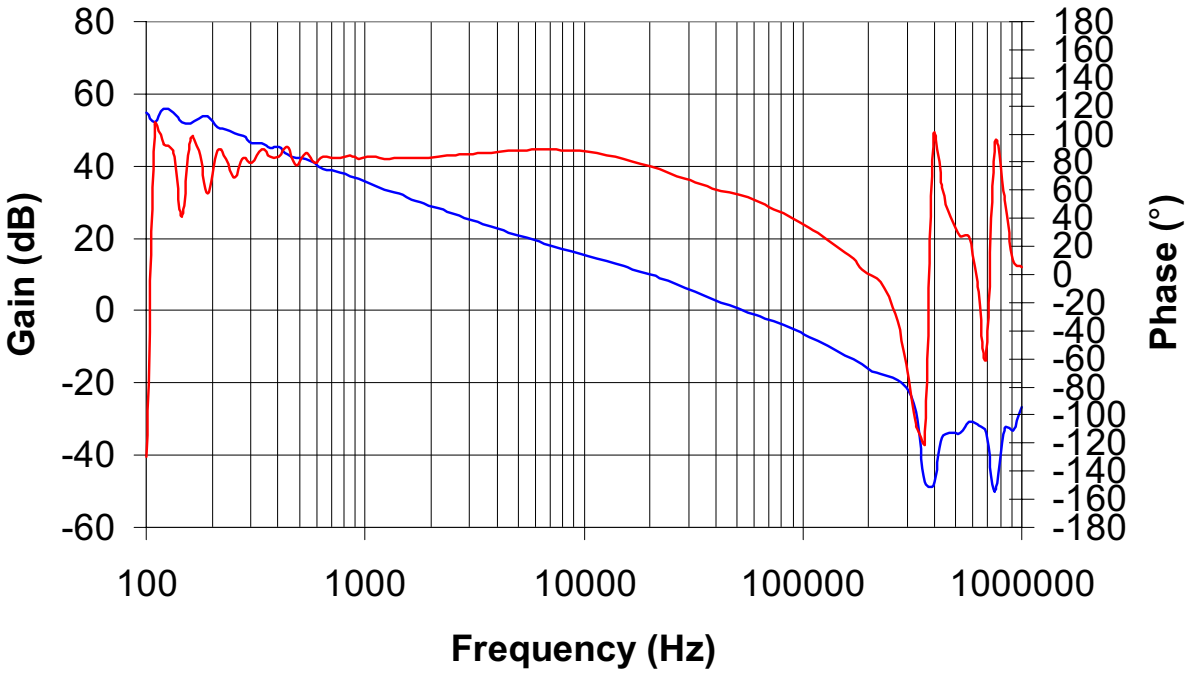


Figure 6-3. TPS40100EVM-001 Loop Response
V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 10 A

7 EVM Assembly Drawings and Layout

Figure 7-1 through Figure 7-6 show the design of the TPS40100EVM-001 printed circuit board. The EVM has been designed using a 4-layer, 2-oz copper-clad 3.0-inch × 3.25-inch circuit board with most of the components on the top side to allow the user to easily view, probe, and evaluate the TPS40100 control IC in a practical application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

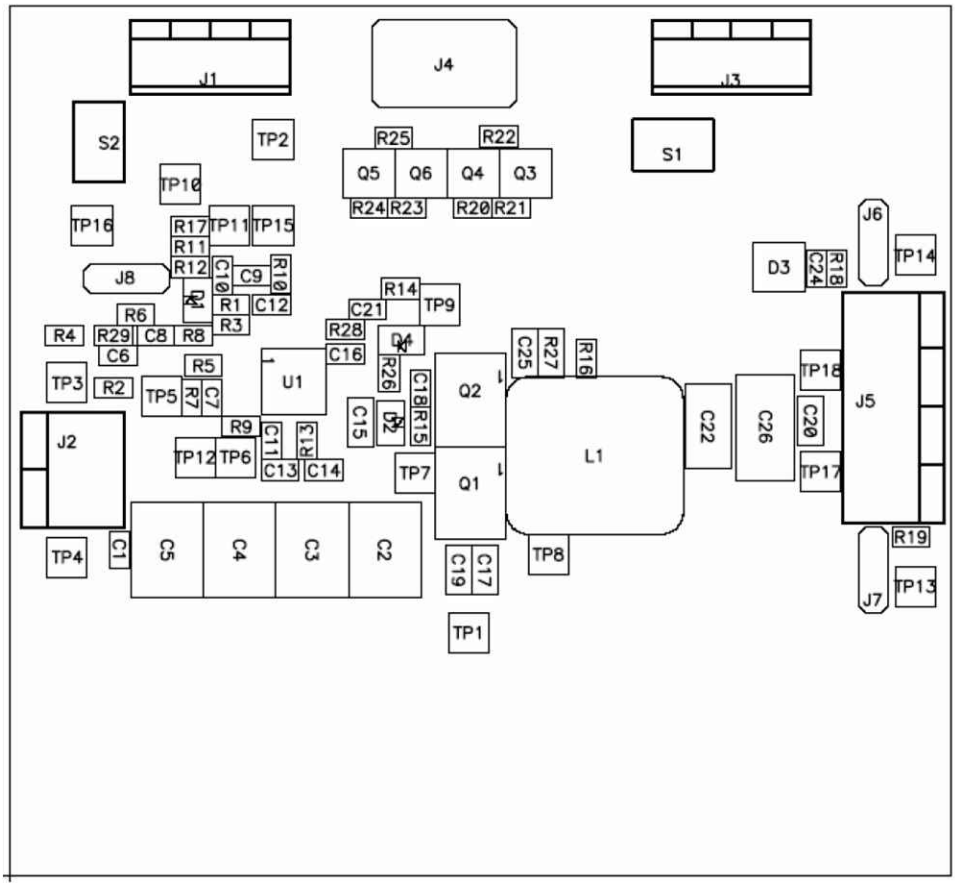


Figure 7-1. TPS40100EVM-001 Component Placement (Viewed from Top)

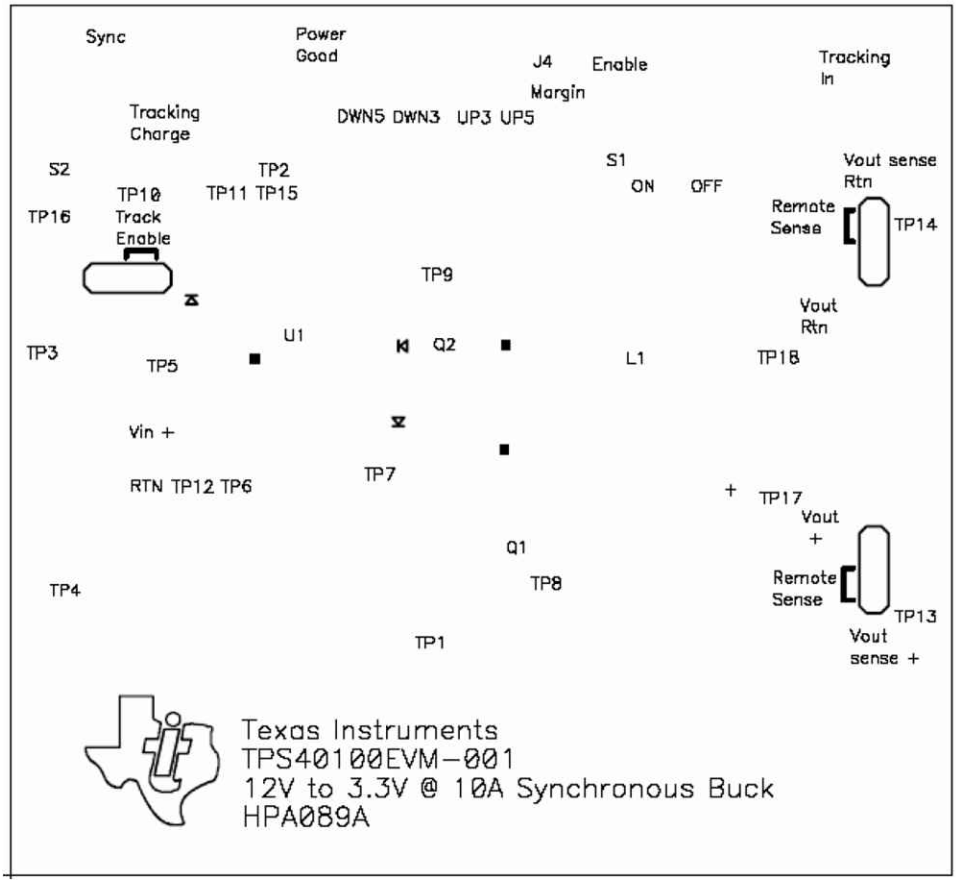


Figure 7-2. TPS40100EVM-001 Silkscreen (Viewed from Top)

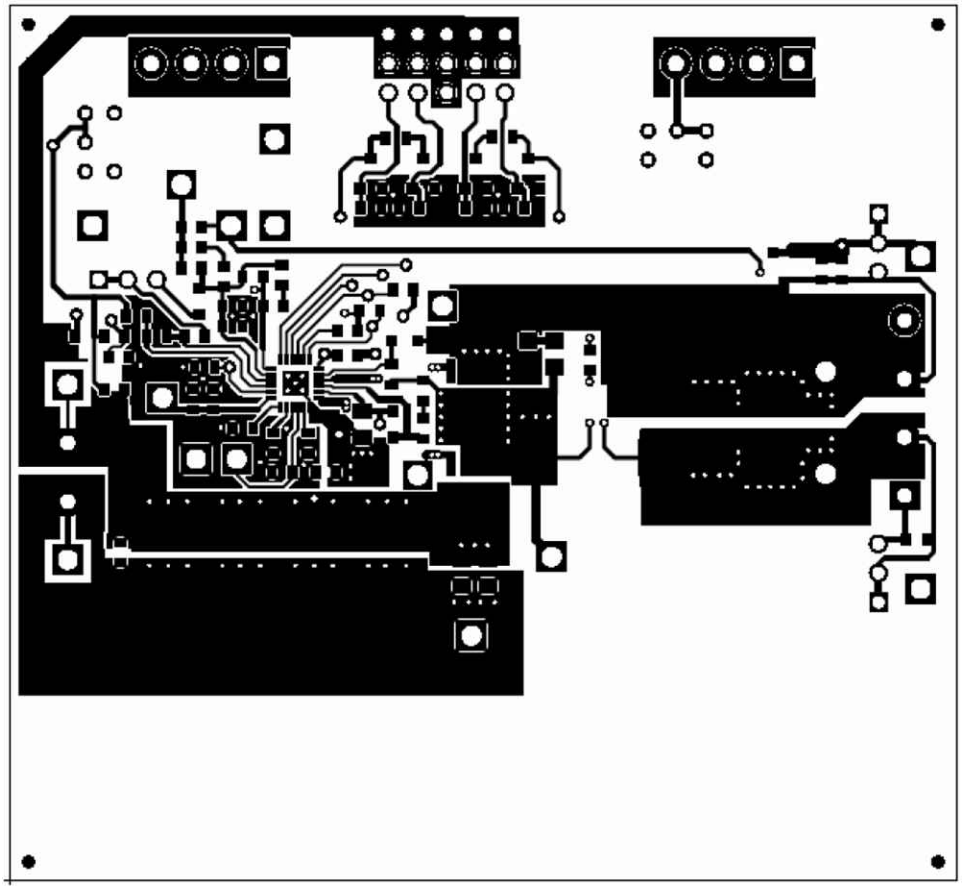


Figure 7-3. TPS40100EVM-001 Top Copper (Viewed from Top)

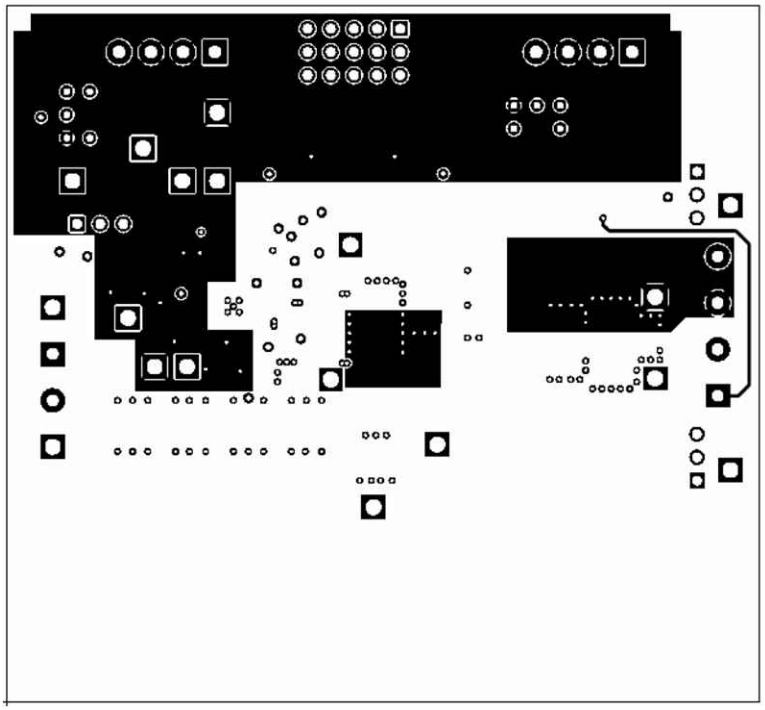


Figure 7-4. TPS40100EVM-001 Layer 2 (X-Ray View from Top)

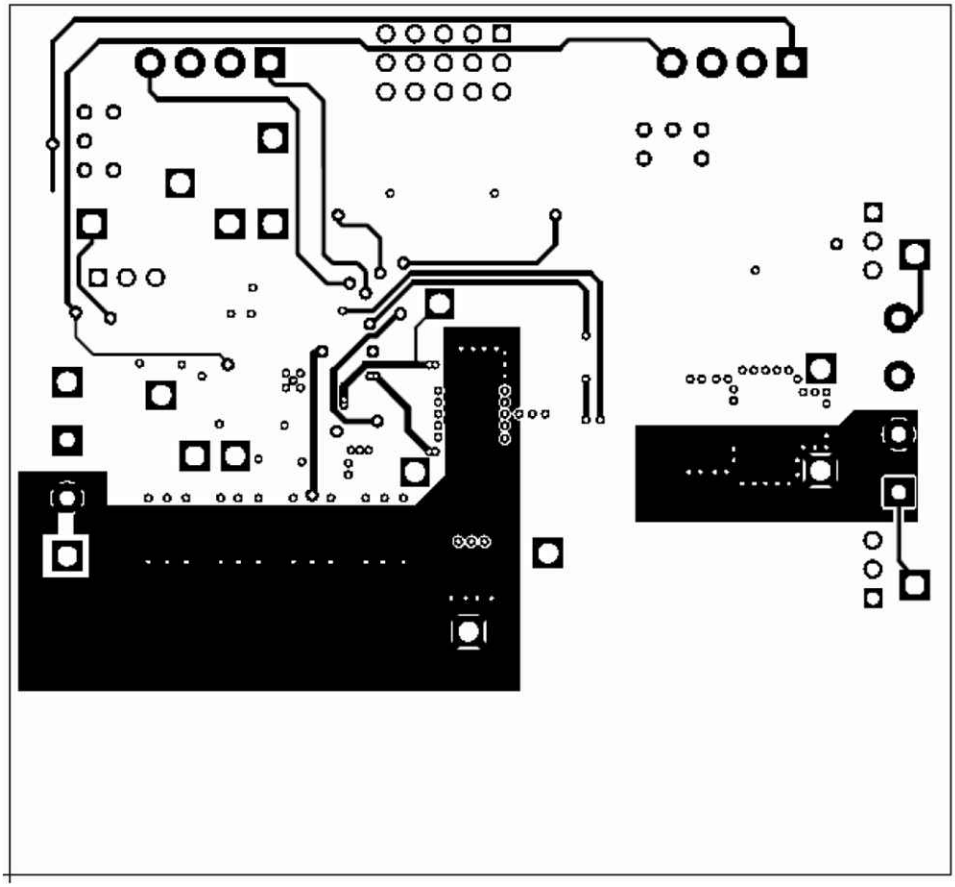


Figure 7-5. TPS40100EVM-001 Layer 3 (X-Ray View from Top)

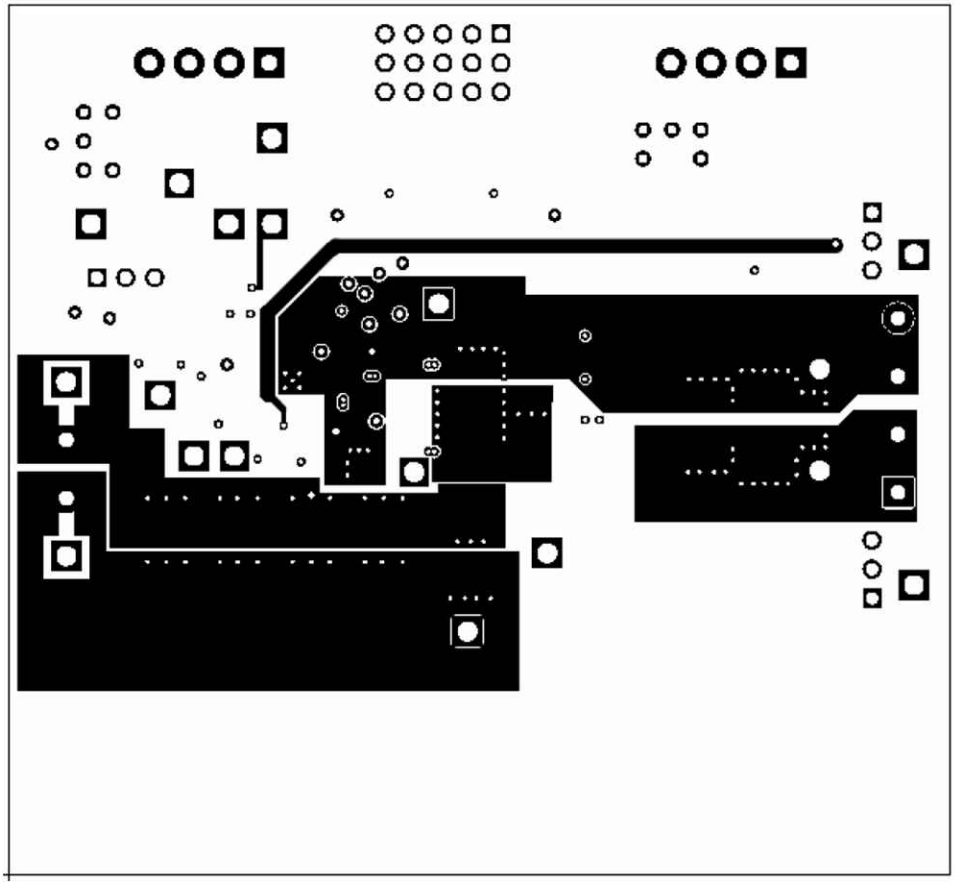


Figure 7-6. TPS40100EVM-001 Bottom Copper (X-Ray View from Top)

8 List of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
5	C1, C11, C16, C18, C21	0.1 µF	Capacitor, Ceramic, 0.1 µF, 50 V, X7R, 10%	603	Std	Std
1	C10	560 pF	Capacitor, Ceramic, 560 pF, 50 V, X7R, 20%	603	Std	Std
1	C12	1500 pF	Capacitor, Ceramic, 1500 pF, 50 V, X7R, 20%	603	Std	Std
1	C14	2.2 µF	Capacitor, Ceramic, 2.2 µF, 10 V, X7R, 20%	603	Std	Std
1	C15	2.2 µF	Capacitor, Ceramic, 2.2 µF, 16 V, X7R, 20%	805	C2012X7R1C225M	TDK
2	C17, C19	1.0 µF	Capacitor, Ceramic, 1.0 µF, 25 V, X7R, 20%	805	C2012X7R1E105M	TDK
4	C2–C5	22 µF	Capacitor, Ceramic, 22 µF, 16 V, X7R, 20%	2220	C5750X7R1C226M	TDK
1	C20	0.1 µF	Capacitor, Ceramic, 0.1 µF, 6.3 V, X5R, 10%	805	C2012X5R0J226K	TDK
1	C22	100 µF	Capacitor, Ceramic, 100 µF, 6.3 V, X5R, 20%	1812	Std	Std
1	C24	1.0 µF	Capacitor, Ceramic, 1.0 µF, 50 V, X7R, 20%	603	Std	Std
1	C25	1500 pF	Capacitor, Ceramic, 1500 pF, 50 V, X7R, 10%	805	Std	Std
1	C26	220 µF	Capacitor, POSCAP, 220 µF, 10 V, 12 mΩ, 20%	7343(D)	10TPB220M	Sanyo
2	C6, C13	.068 µF	Capacitor, Ceramic, 0.068 µF, 25 V, X7R, 10%	603	Std	Std
1	C7	330 pF	Capacitor, Ceramic, 330 pF, 50 V, X7R, 10%	603	Std	Std
1	C8	10 nF	Capacitor, Ceramic, 10 nF, 50 V, X7R, 10%	603	Std	Std
1	C9	270 pF	Capacitor, Ceramic, 270 pF, 50 V, X7R, 10%	603	Std	Std
1	D1	1N4148SW	Diode, Switching, 75 V, 200 mA, 200 mW	SOD- 323	1N4148WS-7	Diode Inc
1	D2	SDM10K45-7	Diode, Schottky, 200 mA, 45 V	SOD-323	SDM10K45-7	Diodes Inc
1	D3	BAT54S	Diode, Dual Schottky, 200 mA, 30 V	SOT23	BAT54S	Zetex
1	D4	BAT54HT1	Diode, Schottky, 200 mA, 30 V	SOD323	BAT54HT1	On Semiconductor
2	J1, J3	ED1516	Terminal Block, 4 pin, 6 A, 3.5 mm	0.55 × 0.25	ED1516	OST
1	J2	ED1609-ND	Terminal Block, 2 pin, 15 A, 5.1 mm	0.40 × 0.35 × 0.100	ED1609	OST
1	J4		Header, 3 × 5 pin, 100-mil spacing	5 × 3 × 0.80	STD	STD
1	J5		Terminal Block, 4 pin, 15 A, 5.1 mm	0.35	ED2227	OST
3	J6–J8		Header, 3 pin, 100-mil spacing, (36-pin strip)	0.100 × 3	PTC36SAAN	Sullins
1	L1	1.8 µH	Inductor, SMT, 1.8 µH, 16 A, 3.19 mΩ	0.512 × 0.55 inch	744318180/LF	Wurth Elektronik
0	L1 (Second source only)	1.9 µH	Inductor, SMT, 1.9 µH, 20 A, 3.00 mΩ	0.512 × 0.551 inch	PG0077.202	Pulse Engineering

Count	RefDes	Value	Description	Size	Part Number	MFR
1	Q1	HAT2168H	Mosfet, N-Ch, Vds 30 V, Rds 7.9 mΩ, Id 30 A	LFPAK	HAT2168H	Hitachi
1	Q2	HAT2160H	Mosfet, N-Ch, Vds 20 V, Rds 2.6 mΩ, Id 60 A	LFPAK	HAT2160H	Hitachi
4	Q3–Q6	2N7002	MOSFET, N-ch, 60 V, 115 mA, 1.2 Ω	SOT23	2N7002DICT	Vishay-Liteon
1	R1	12.4 k	Resistor, Chip, 12.4 kΩ, 1/16-W,1%	603	Std	Std
1	R10	42.2 k	Resistor, Chip, 42.2 kΩ, 1/16- W, 1%	603	Std	Std
1	R11	100	Resistor, Chip, 100 Ω, 1/16-W, 1%	603	Std	Std
1	R12	18.2 k	Resistor, Chip, 18.2 k Ohms, 1/16-W, 1%	603	Std	Std
1	R13	274 k	Resistor, Chip, 274 kΩ, 1/16-W, 1%	603	Std	Std
1	R14	100 k	Resistor, Chip, 100 kΩ, 1/16-W, 1%	603	Std	Std
2	R15,R26	0	Resistor, Chip, 0 Ω, 1/16-W, 1%	603	Std	Std
1	R16	4.87 k	Resistor, Chip, 4.87 kΩ, 1/16- W, 1%	603	Std	Std
1	R17	49.9	Resistor, Chip, 49.9 Ω, 1/16-W, 1%	603	Std	Std
2	R18, R19	10	Resistor, Chip, 10.0 Ω, 1/16-W,1%	603	Std	Std
1	R2	127 k	Resistor, Chip, 127 kΩ, 1/16-W,1%	603	Std	Std
4	R20– R24	511 k	Resistor, Chip, 511 kΩ, 1/16-W,1%	603	Std	Std
2	R22, R25	30.1 k	Resistor, Chip, 30.1 kΩ, 1/16-W, 1%	603	Std	Std
1	R27	2	Resistor, Chip, 2 Ω, 1/10W, 1%	805	Std	Std
1	R28	100	Resistor, Chip, 100 Ω, 1/16-W,1%	603	Std	Std
1	R29	49.9 k	Resistor, Chip, 49.9 kΩ, 1/16-W, 1%	603	Std	Std
1	R3	7.87 k	Resistor, Chip, 7.87 kΩ, 1/16-W, 1%	603	Std	Std
1	R4	105 k	Resistor, Chip, 105 kΩ, 1/16-W,1%	603	Std	Std
1	R5	17.8 k	Resistor, Chip, 17.8 kΩ, 1/16-W, 1%	603	Std	Std
1	R6	1.62 k	Resistor, Chip, 1.62 kΩ, 1/16-W, 1%	603	Std	Std
1	R7	110 k	Resistor, Chip, 110 kΩ, 1/16-W, 1%	603	Std	Std
1	R8	15.0 k	Resistor, Chip, 15.0 kΩ, 1/16-W, 1%	603	Std	Std
1	R9	127 k	Resistor, Chip, 127 kΩ, 1/16-W, 1%	603	Std	Std
2	S1, S2		Switch, ON-ON Mini Toggle (Initial switch position closed shorting pins 1 and 2)	0.28 inch × 0.18 inch	G12AP	NKK

Count	RefDes	Value	Description	Size	Part Number	MFR
5	TP1, TP2, TP4, TP12, TP14	5011	Test Point, Black, Thru Hole	0.125 × 0.125	5011	Keystone
2	TP3, TP13	5010	Test Point, Red, Thru Hole	0.125 × 0.125	5010	Keystone
1	—	(Remote Sense –)	Shunt, 100-mil, Black (Initial Placement Across Pins 2, 3 of J6)	0.1	929950-00	3M
1	—	(Remote Sense +)	Shunt, 100-mil, Black (Initial Placement Across Pins 2, 3 of J7)	0.1	929950-00	3M
1	—	(Tracking Enable)	Shunt, 100 mil, Black (Initial Placement Across Pins 1, 2 of J8)	0.1	929950-01	3M
4	—	margin	Shunt, 100-mil, Black (Initial Placement Across Pins (1, 2) (4, 5) (7, 8) (10, 11) (13, 14) of connector J4)	0.1	929950-00	3M
11	TP18	5012	TestPoint, White, Thru Hole	0.125 × 0.125	5012	Keystone
1	U1	TPS40100RGE	IC,Midrange Input Synchronous Buck Controller	QFN-24	TPS40100RGE	TI
1			PCB,3.25 inch × 3.0 inch × 0.062 inch		EVM	Any

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2005) to Revision A (March 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated the user's guide title.	2

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