TEXAS INSTRUMENTS

*User's Guide*
*SLUUAT5–March 2014*

# *TPS92602 Evaluation Module (EVM)*

The TPS92602EVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS92602-Q1 two-channel high-side current-sense dc-dc MOSFET controller. The TPS92602-Q1, designed to drive automotive high-brightness light-emitting diodes (LEDs), features a wide input-voltage range (4.5 V to 40 V), high-side current sense, a precision reference, switching-frequency synchronization, analog dimming, PWM dimming, and full diagnostics including high-side current (LED current) available as analog output, open-LED and short-to-GND detection, and shorted-output protection.

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# 1 Detailed Description

## 1.1 Description

The TPS92602-Q1 is a dual-channel LED driver. The basis for each independent driver is a peak-current-mode boost controller. Each controller has a current feedback loop with high-side current-sensing shunt and a voltage-feedback loop with an external resistor-divider network. Each controller has two independent feedback loops, a current-feedback loop with high-side current-sensing shunt and a voltage-feedback loop with an external resistor-divider network. The controller delivers a constant output voltage or a constant output current. The connected load determines whether the board is regulating a constant output current (if current set point is reached earlier than voltage set point) or a constant output voltage (if the voltage set point is reached first, for example in an open-load condition).

Each controller supports all typical topologies like boost, boost to battery, SEPIC, or flyback.

Uses for the high-side PMOS FET driver are for PWM dimming of the LED string and for cutoff in case of an external short circuit to GND in order to protect the circuit.

## 1.2 Typical Applications

This converter design describes an application of the TPS92602-Q1 as an LED driver for the boost and boost-to-battery applications. For applications with a different input voltage range or different output voltage range, see the TPS92602-Q1 data sheet (SLUSBP5).

## 1.3 Features

### 1.3.1 Connector Description

This section describes the connectors, jumpers, and test points on the EVM and how to properly connect, set up, and use the TPS92602EVM.

### 1.3.2 J_VBAT1, J_VBAT2

J_VBAT1 is the CH1 input and J_VBAT2 is the CH2 input.

### 1.3.3 J-PGND

J_PGND is a common GND for the input.

### 1.3.4 J_B1_OUT, J_B2_OUT

J_B1_OUT is the output of CH1; connect LED+ to this connector. J_B2_OUT is output of CH2; connect LED+ to this connector.

### 1.3.5 J_B1_GND, J_B2_GND

J_B1_GND is the output GND of CH1; connect LED– to this connector. J_B2_OUT is the output GND of CH2; connect LED– to this connector.

### 1.3.6 CN1, CN3

CN1 is the PWM input for CH1 and CN3 is the PWM input for CH2.

### 1.3.7 CN2, CN4

CN2 is the output of DIAG1 and CN4 is the output of DIAG2.

### 1.3.8 P1

Jumper for TPS92602-Q1 VIN; connect it before power on.

### 1.3.9 P2

Jumper for TPS7A6650-Q1 Vin; connect it when in need of an LDO in the EVM to generate 5 V for Ictrl and PWM.

### 1.3.10 P3

Jumper for TPS7A6650-Q1 Vout; connect it when in need of an LDO in the EVM to generate 5 V for Ictrl and PWM.

### 1.3.11 P4

Connect P4 terminal 1 with P4 terminal 2 to enable the TPS7A6650-Q1, and connect P4 terminal 2 with P4 terminal 3 to disable the TPS7A6650-Q1.

### 1.3.12 P_RT

Connect P_RT terminal 1 with P_RT terminal 2 to set the RT resistor as 20 kΩ, or input PWM on P_RT terminal 2 for direct frequency synchronization.

The switching frequency is adjustable over a range from 100 kHz to 600 kHz by placing a resistor on the RT terminal. The RT terminal voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 1 or Figure 5. To reduce the solution size, one would typically set the switching frequency as high as possible, but consider tradeoffs of the supply efficiency, maximum input voltage, and minimum controllable on-time.

$$R_{(RT)}[k\Omega] = \frac{12.5\ MHz \times 1\ k\Omega}{f_{(OSC)}[MHz]} \tag{1}$$

One can also use the RT terminal to synchronize the controllers to an external system clock, over a range from 100 kHz to 600 kHz. Use this synchronization feature by applying a square wave to the RT terminal. The square wave must transition lower than 0.8 V and higher than 2 V on the RT terminal and have an on-time greater than 70 ns and an off-time greater than 70 ns. The synchronization frequency range is 100 kHz to 600 kHz. The rising edge of GDRV1 synchronizes with the falling edge of the RT terminal signal.

Leaving the RT terminal open or shorted to ground, with no external system clock signal present, disables both boost controllers and switches off both PWM dimming FETs. In order to recover from this global failure state, (for example, after removal of the failure condition on the RT terminal) there must be one global disable-and-enable cycle (active shutdown by pulling both P_PWMx terminals low for $t > t_{(CH\_OFF)}$, and setting one or both PWMINx terminals high for $t > t_{(CH\_ON)}$).

### 1.3.13 P_PWM1, P_PWM2

Connect P_PWM1 terminal 1 with P_PWM1 terminal 2 to set the CH1 PWM dimming duty cycle to 100%, connect P_PWM1 terminal 2 with P_PWM1 terminal 3 to disable CH1, or input PWM directly to P_PWM1 terminal 2 to control the dimming duty cycle. Connect P_PWM2 terminal 1 with P_PWM2 terminal 2 to set the CH2 PWM dimming duty cycle to 100%, connect P_PWM2 terminal 2 with P_PWM2 terminal 3 to disable CH2, or input PWM directly to P_PWM2 terminal 2 to control the dimming duty cycle.

In order to change the brightness of an LED string to a certain luminosity without affecting the lighting color of the LED, it is necessary to use PWM dimming topology. Turning the LEDs ON and OFF at a certain frequency with a certain duty cycle reduces the brightness without changing the LED current (so not affecting the color).

The integrated high-side PMOS-FET gate driver turns the LED string ON and OFF following the supplied signal frequency and duty cycle on the PWMIN terminal. During the OFF time of the FET, the internal control loop stops, and the device stores the value of the compensation network by disconnecting the amplifier internally. This technique allows the fastest recovery of the regulator during the following on-time, as the control loop restarts from the point at which it stopped. The average LED current during the on-time is almost the same as the LED current with no PWM dimming (the duty cycle is 100%). For very low duty cycles, the time for the controller to ramp up the inductor current from 0 A is more significant relative to the overall on-time, leading to lower average current. So for very low duty cycles, the relation between average current and duty cycle is no longer linear.

Maintaining a minimum on-time is necessary in order for PWM dimming to operate in the linear region of its transfer function. Because of the disabled state of the controller during dimming, the PWM pulse must be long enough that the energy intercepted from the input is greater than or equal to the energy being put into the LEDs. For boost and boost-to-battery topologies, the minimum on-time (in seconds) for which the PWM dimming operates in the linear region is given by:

$$t_{(PWMON\_MIN)} = \frac{2 \times I_{(LED)} \times V_{(out)} \times L}{V_{(in)}^{2}} \quad (2)$$

In order to ensure that the applied dimming-pulse duration matches with the effective dimming-pulse duration, TI recommends synchronizing the dimming pulses with the switching clock of the boost converter. Choose an external inductor and output capacitors according to the requirements for the minimum duty cycle.

### 1.3.14 P1, P_VBAT1 and P_VBAT2

Connect P1, P_VBAT1, and P_VBAT2 as necessary to meet the input requirements for VIN on the TPS92602-Q1.

### 1.3.15 TP_AGND1, TP_AGND2

Test points for AGND1 and AGND2

### 1.3.16 TP_B1, TP_B2

Test points for CH1 and CH2 GND

### 1.3.17 TP_COMP1, TP_COMP2

Test points for the COMP1 and COMP2 terminals

### 1.3.18 TP_DIAG1, TP_DIAG2

Test points for the DIAG1 and DIAG2 terminals

In regular operation mode, an external microcontroller can measure the actual output current of the controller by sensing the voltage at the DIAGx terminal. A DIAGx terminal voltage between 0.2 V and 2.85 V represents in a linear relation the output current measured by the current-sense block over the external shunt resistor. Parameter DIAGfactor gives the scale factor of typically 16 (TPS92601-Q1 or TPS92602-Q1 with 150-mV full-scale current-sense voltage) or 8 (TPS92601A-Q1 or TPS92602A-Q1 with 300-mV full-scale current-sense voltage). Figure 1 shows the relation between the DIAGx terminal voltage and the current-sense voltage.

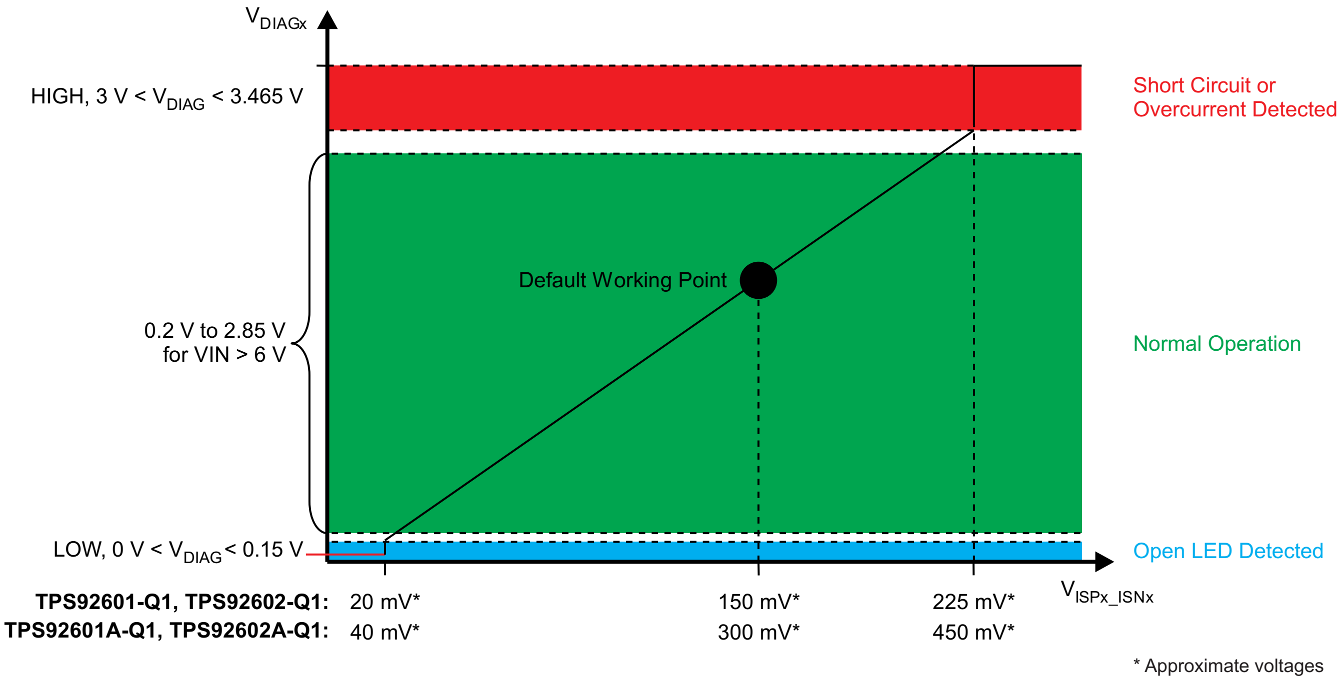



**Figure 1. DIAGx Terminal Function**

### 1.3.19 TP_ICTRL1, TP_ICTRL2

Test points for the ICTRL1 and ICTRL2 terminals. Adjust R12 and R27 to set the ICTRL voltage. An analog voltage applied to the ICTRLx terminal allows changing the output current for each channel on the fly from 10% to 100% of full scale. Typically, this approach is used to:

- Reduce the default current in a narrow range to adjust to different binning classes of LEDs
- Reduce the current at high temperatures (protect LEDs from overtemperature)
- Reduce the current at low input voltages (for example, cranking-pulse breakdown of the supply)

Implementing this analog dimming function is possible with an analog approach [discrete resistor and negative-temperature-coefficient (NTC) network] or with a more flexible approach by using a microcontroller. In order to simplify the analog implementation, the device clamps the maximum voltage at the ICTRLx terminal internally at 1.5 V. So, applying any higher voltage has no effect on the output current (which sticks to its current set point at 100% of full scale, that is, approximately 150 mV or 300 mV drop at the external current-shunt resistor).

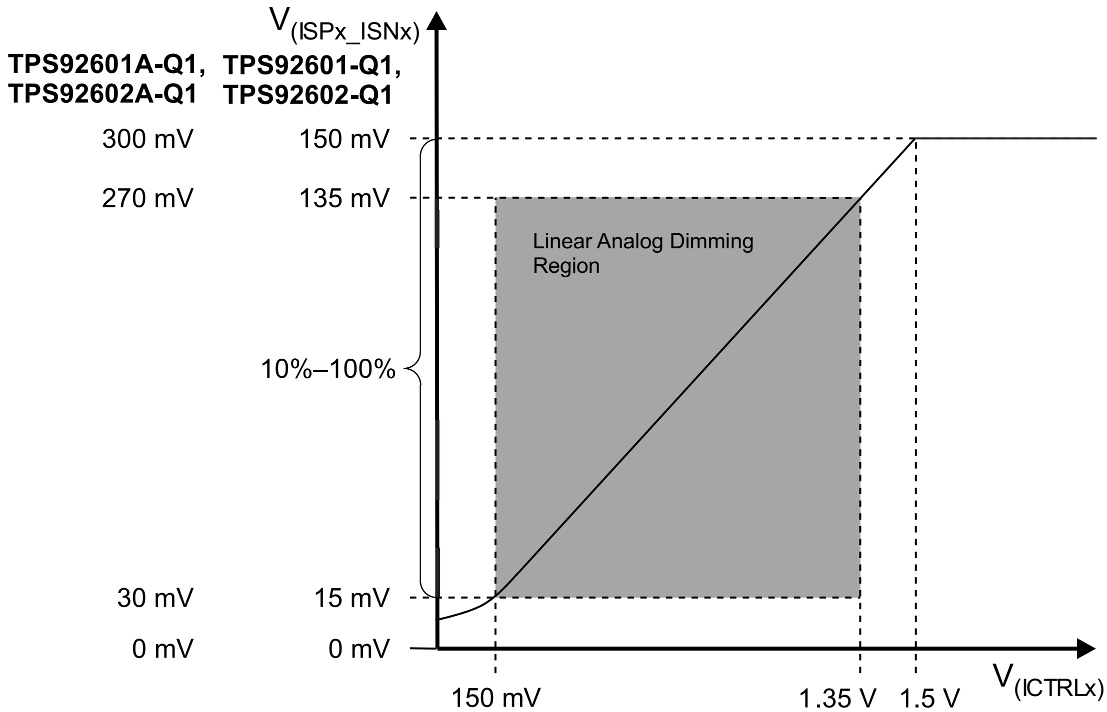



**Figure 2. Analog Dimming – ICTRLx Terminal**

### 1.3.20 TP_PWMIN1, TP_PWMIN2

Test points for the PWMIN1 and PWMIN2 terminals

### 1.3.21 TP_RT

Test point for the RT terminal

### 1.3.22 TP_VFB1, TP_VFB2

Test points for the VFB1 and VFB2 terminals. Adjust R032 and R102 to set the OVP voltage.

### 1.3.23 TP_VIN_D

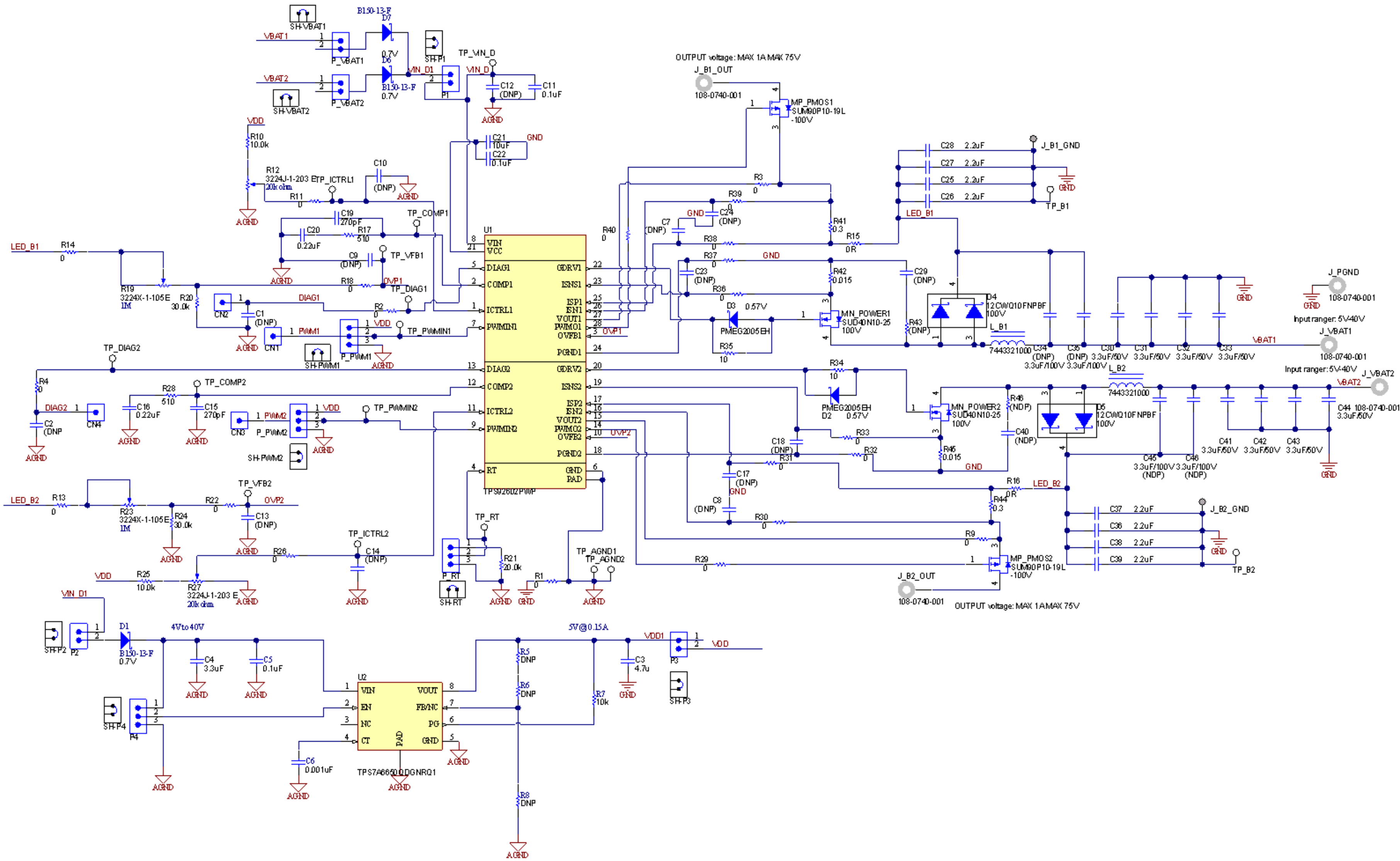
Test point for TPS92602-Q1 $V_{(VIN)}$

## 2 Electrical Performance Specifications

**Table 1. TPS926902EVM Electrical Performance Specifications**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | |
| Voltage range | | 5.86 | | 40 | V |
| Maximum input current | At $I_{(OUT)}$ = 500 mA | | 2.49 | | A |
| Undervoltage lockout level | Input rising | | 5.38 | | V |
| | Input falling | | 3.84 | | V |
| **WITH 10 LEDs IN SERIES** | | | | | |
| Output voltage, $V_{(OUT)}$ | At $I_{(OUT)}$ = 500 mA | | 27.4 | | V |
| Output load current, $I_{(OUT)}$ | $V_{(ICTRLx)}$ = 0 V to 1.5 V | 0 | 250 | 499.7 | mA |
| Output current regulation | Line regulation: input voltage = 8 V to 19 V | | 0.38% | | |
| Output current ripple | At $I_{(OUT)}$ = 500 mA | | 8.4 | | mApp |
| Overvoltage protection level | Output rising | | 36 | | V |
| **SYSTEMS CHARACTERISTICS** | | | | | |
| Switching frequency | | | 589 | | kHz |
| Efficiency | Input voltage = 12 V, Load = 10 LEDs at 500 mA | | 92.51% | | |
| PWM dimING frequency | | 200 | | 2000 | Hz |

# 3 Schematic


OUTPUT voltage: MAX 1A MAX 75V
J_B1_OUT
108-0740-001
MP_PMOS1
SUM90P10-19L
-100V
J_B1_GND
TP_B1
LED_B1
J_PGND
Input ranger: 5V-40V
J_VBAT1
J_VBAT2
MN_POWER1
SUD40N10-25
100V
MN_POWER2
D4
12CWQ10FNPBF
D5
L_B1
L_B2
7443321000
PMEG2005EH
U1
TPS92602PWP
VIN
VCC
DIAG1
COMP1
ICTRL1
PWMDIM1
DIAG2
COMP2
ICTRL2
PWMDIM2
RT
GDRV1
ISNS1
ISP1
ISN1
VOUT1
PWMO1
OVFB1
PGND1
GDRV2
ISNS2
ISP2
ISN2
VOUT2
PWMO2
OVFB2
PGND2
GND
PAD
TP_VIN_D
TP_ICTRL1
TP_COMP1
TP_VFB1
TP_DIAG1
TP_PWMIN1
TP_DIAG2
TP_COMP2
TP_PWMIN2
TP_VFB2
TP_ICTRL2
TP_RT
TP_AGND1
TP_AGND2
J_B2_GND
TP_B2
J_B2_OUT
MP_PMOS2
B150-13-F
SH-VBAT1
SH-VBAT2
P_VBAT1
P_VBAT2
SH-P1
SH-PWM1
SH-PWM2
SH-RT
SH-P2
SH-P3
SH-P4
4V to 40V
5V@0.15A
U2
TPS7A6650QDGNRQ1
VIN
EN
NC
CT
VOUT
FB/NC
PG
GND
PAD
AGND
VDD
VDD1
VIN_D1

# 4 Performance Data and Typical Characteristic Curves

## 4.1 Efficiency

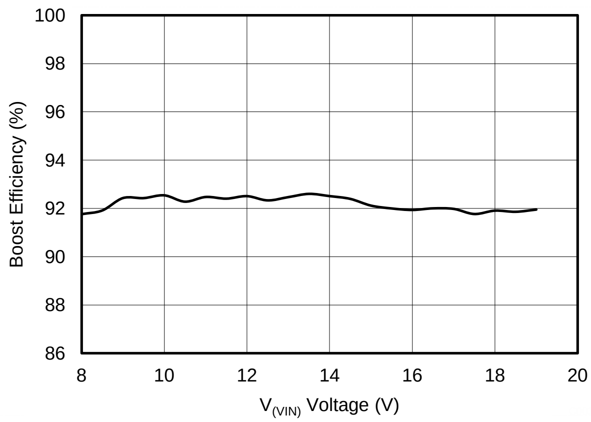



**Figure 3. Boost Efficiency versus Input Voltage**

## 4.2 Line Regulation

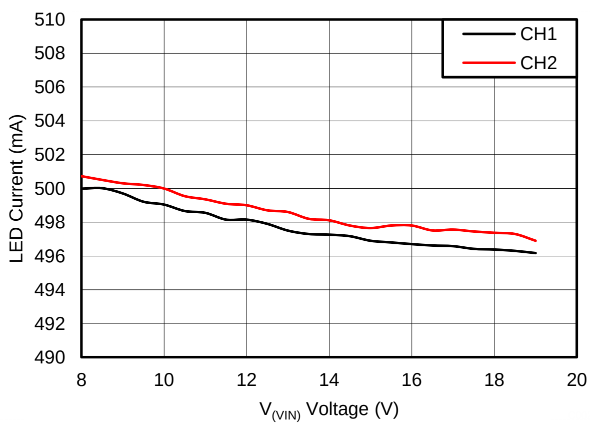



**Figure 4. Line Regulation**

## 4.3 Switching Frequency

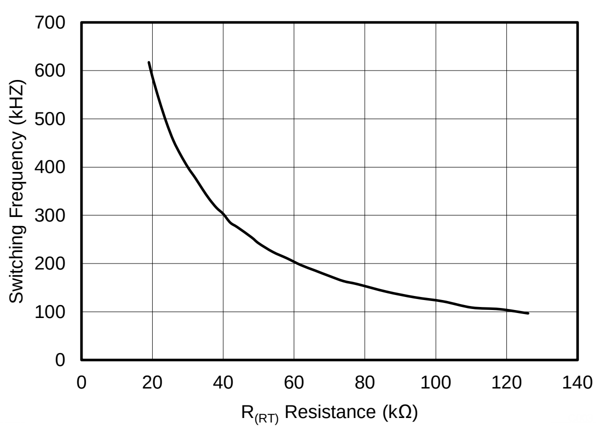



**Figure 5. Switching Frequency versus $R_{(RT)}$ Resistance**

### 4.4 Switch-Node Voltage and LED Current Ripple

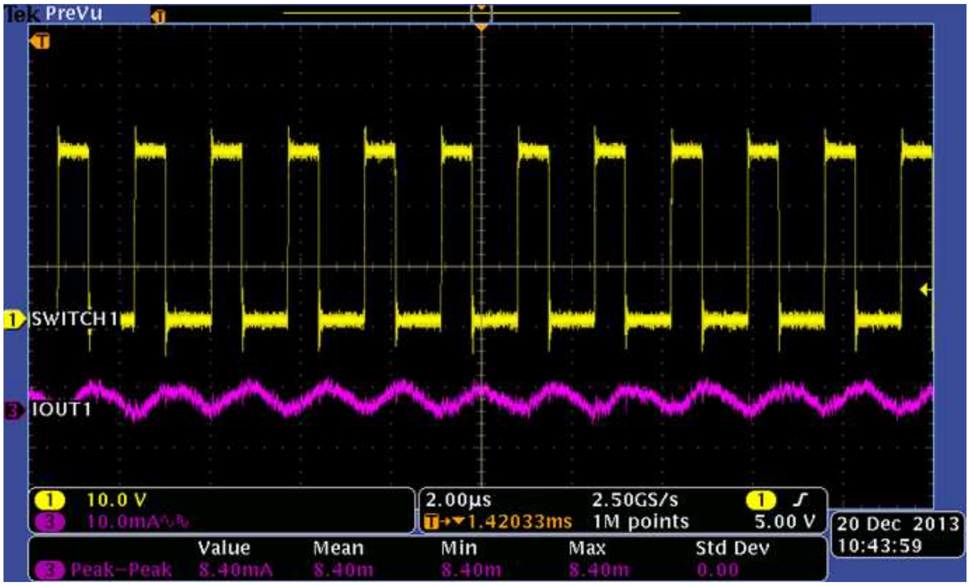



**Figure 6. Switching and LED Current Ripple When Iout = 500 mA**

**PWM Dimming**

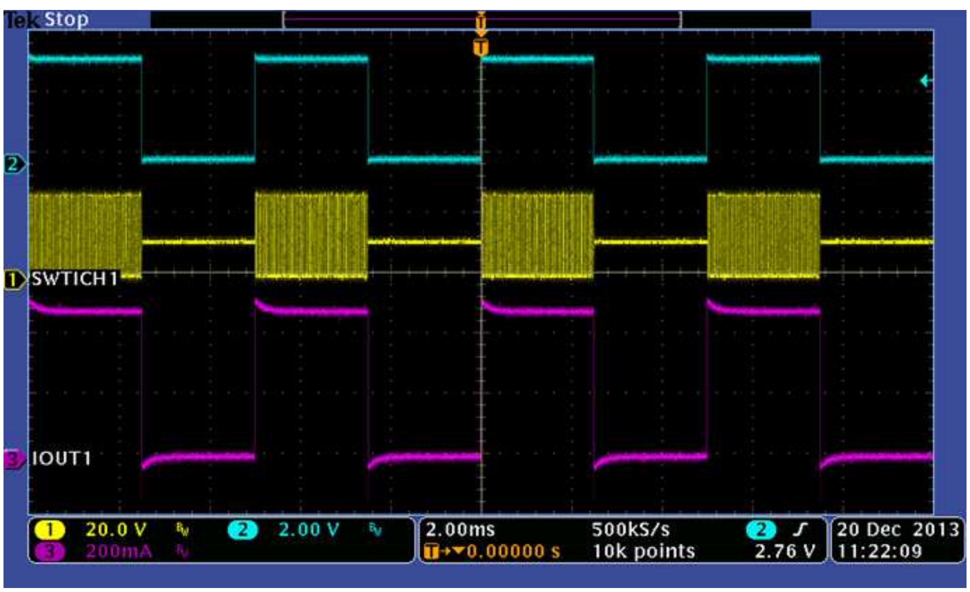



**Figure 7. PWM Dimming, $f_{PWM}$ = 200 Hz, Duty Cycle = 50%**

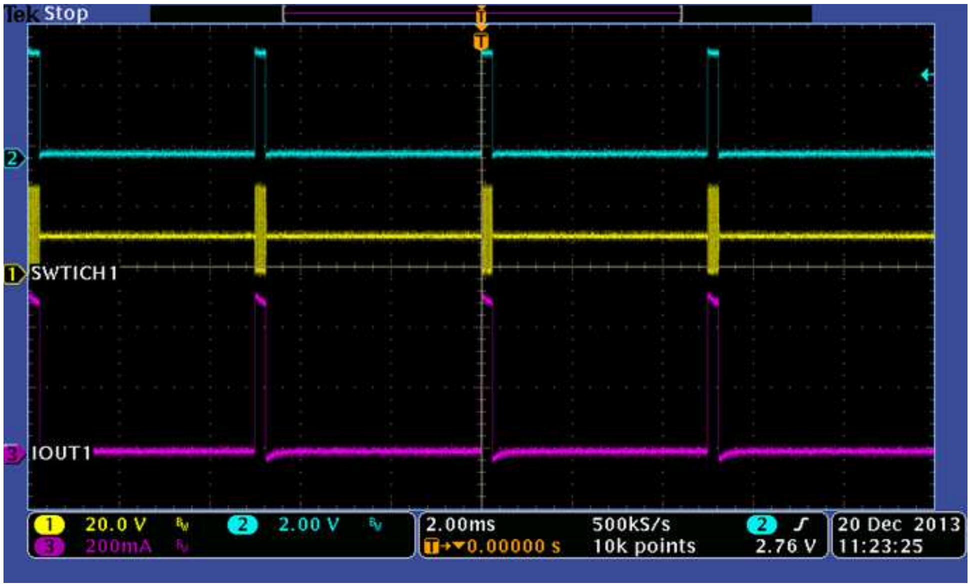



**Figure 8. PWM Dimming, $f_{PWM}$ = 200 Hz, Duty Cycle = 5%**

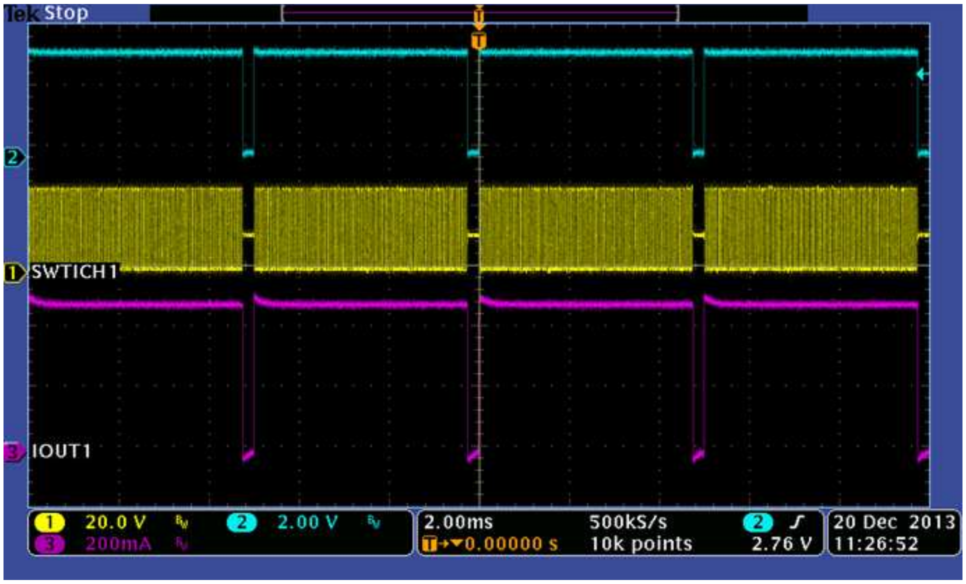



**Figure 9. PWM Dimming, $f_{PWM}$ = 200 Hz, Duty Cycle = 95%**

### 4.5 Start-Up and Shut-Down Response

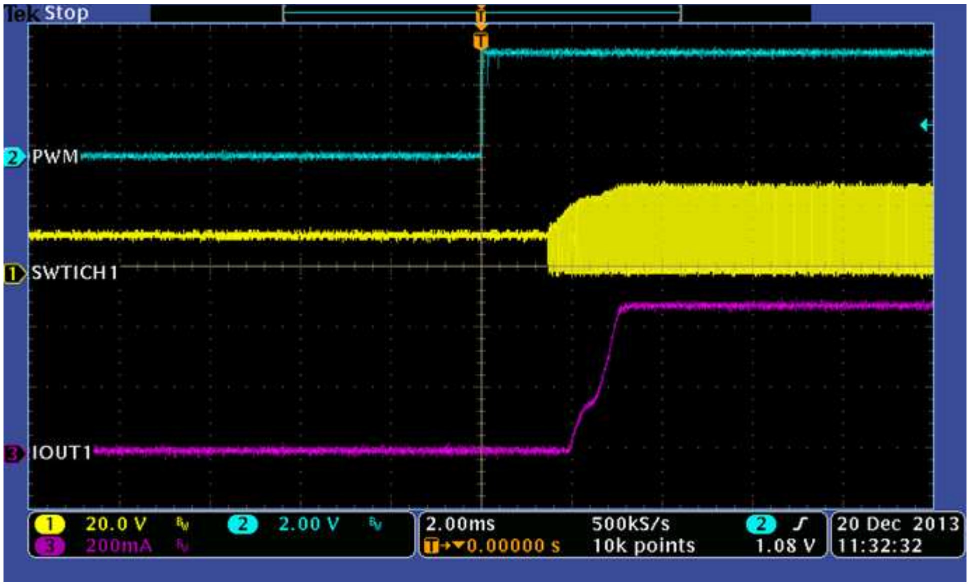



**Figure 10. Start-Up Waveform**

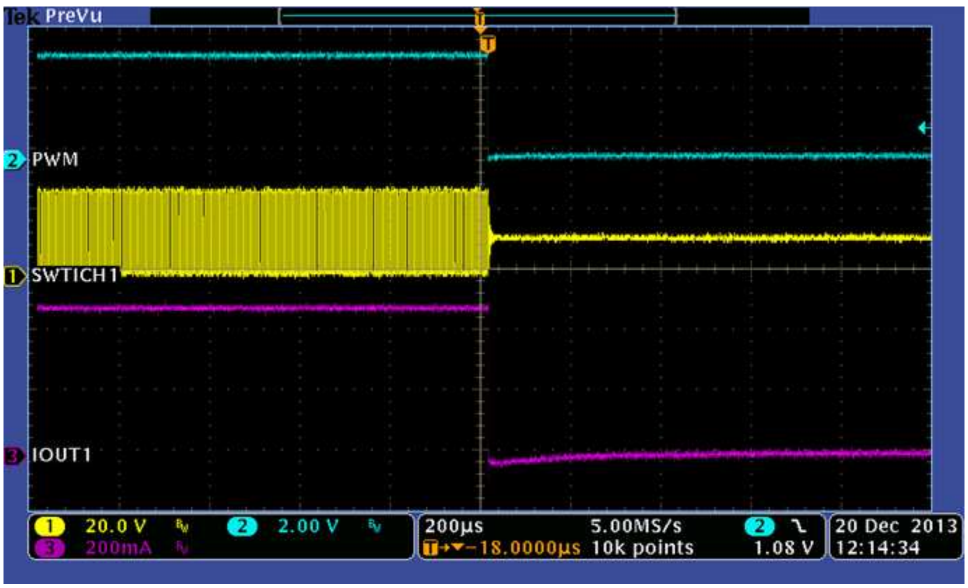



**Figure 11. Shut-Down Waveform**

## 4.6 Thermal Performance

Figure 12 and Figure 13 show the steady state thermal performance of the EVM under the following conditions: Load of 10 LEDs per channel, both channels working, $I_{(LED)}$ = 500 mA, $V_{(VIN)}$ = 12 VDC.

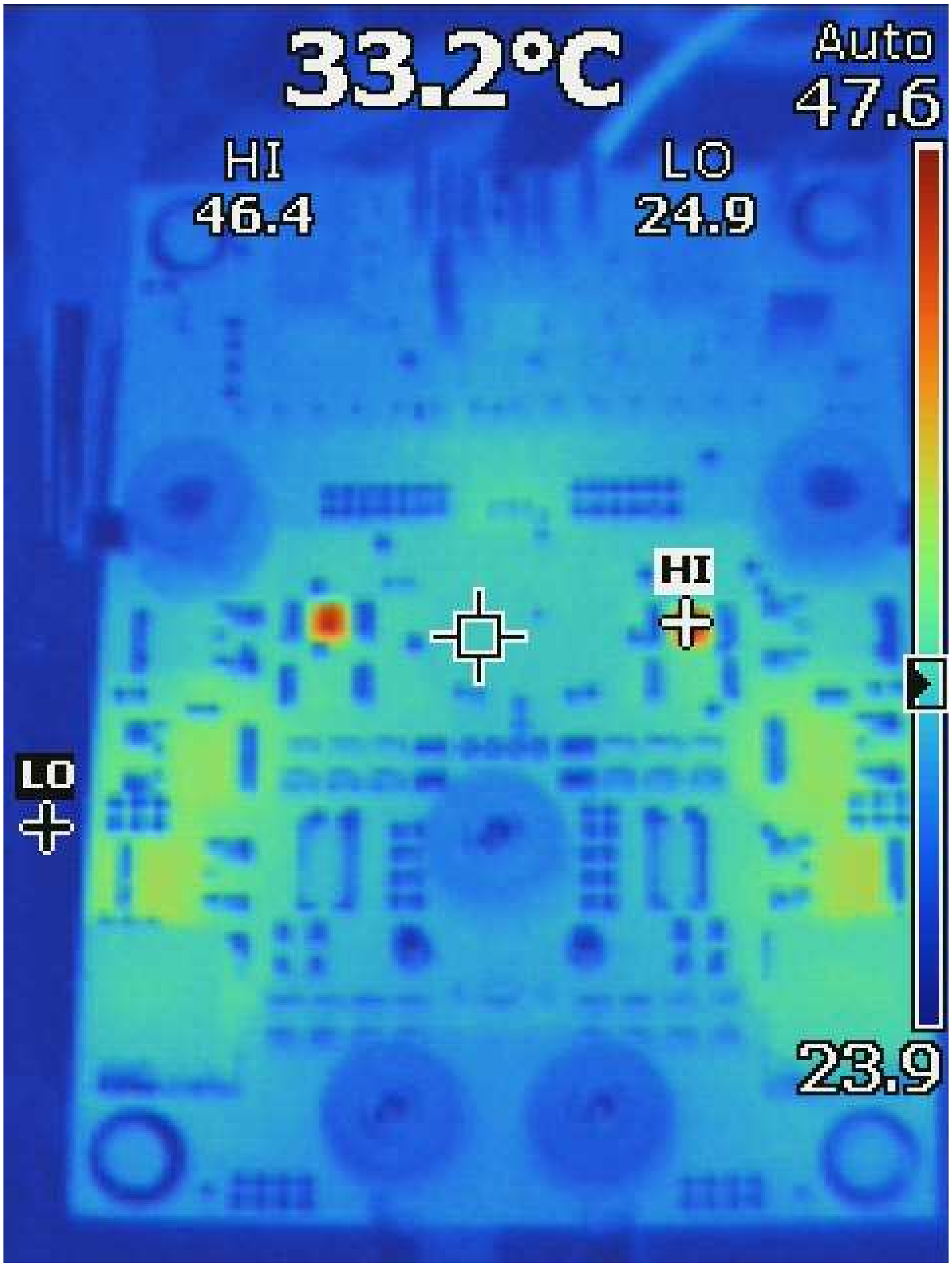



**Figure 12. Top Thermal Performance**

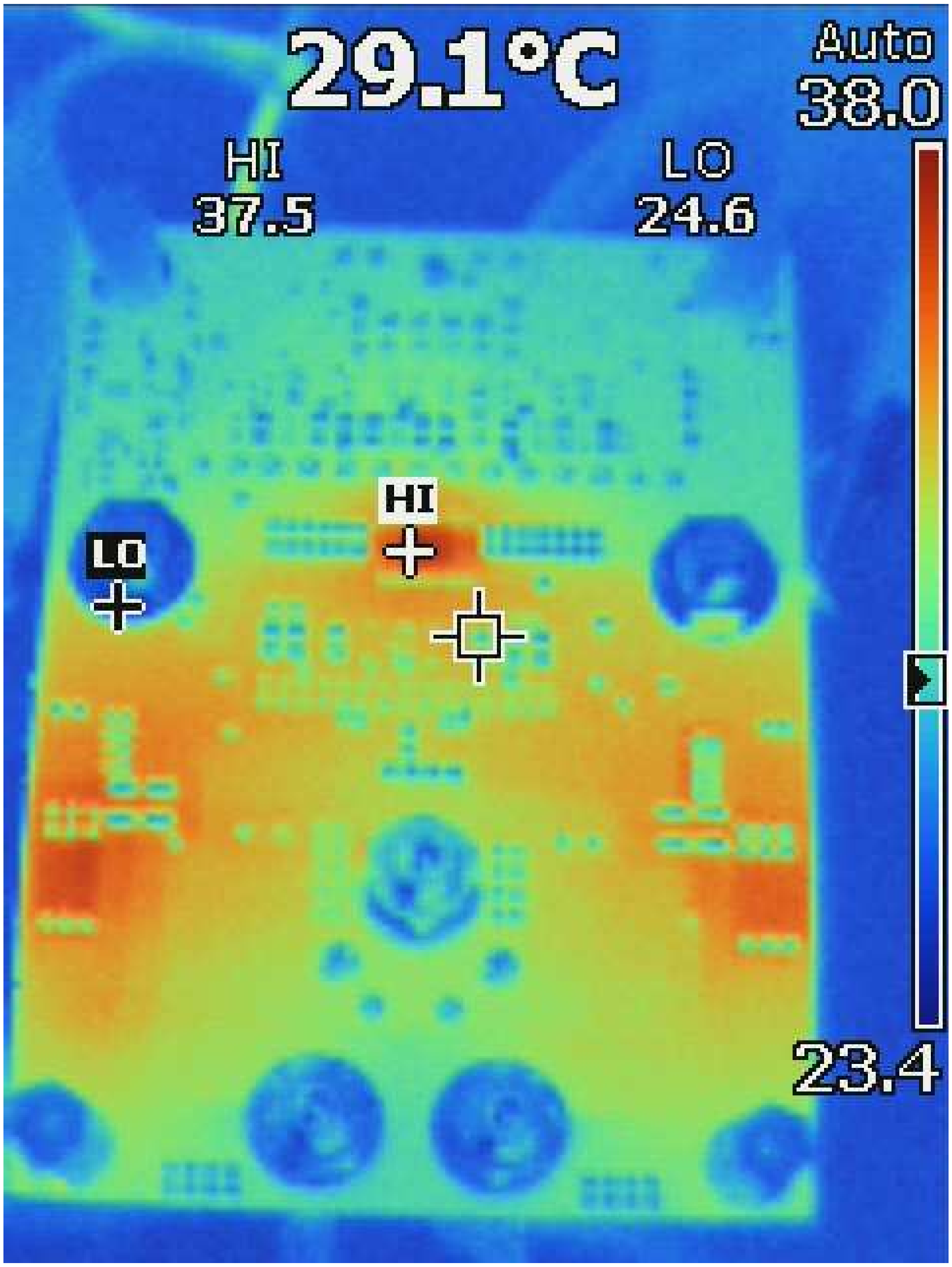



**Figure 13. Bottom Thermal Performance**

# 5 TPS92602EVM PCB Layout

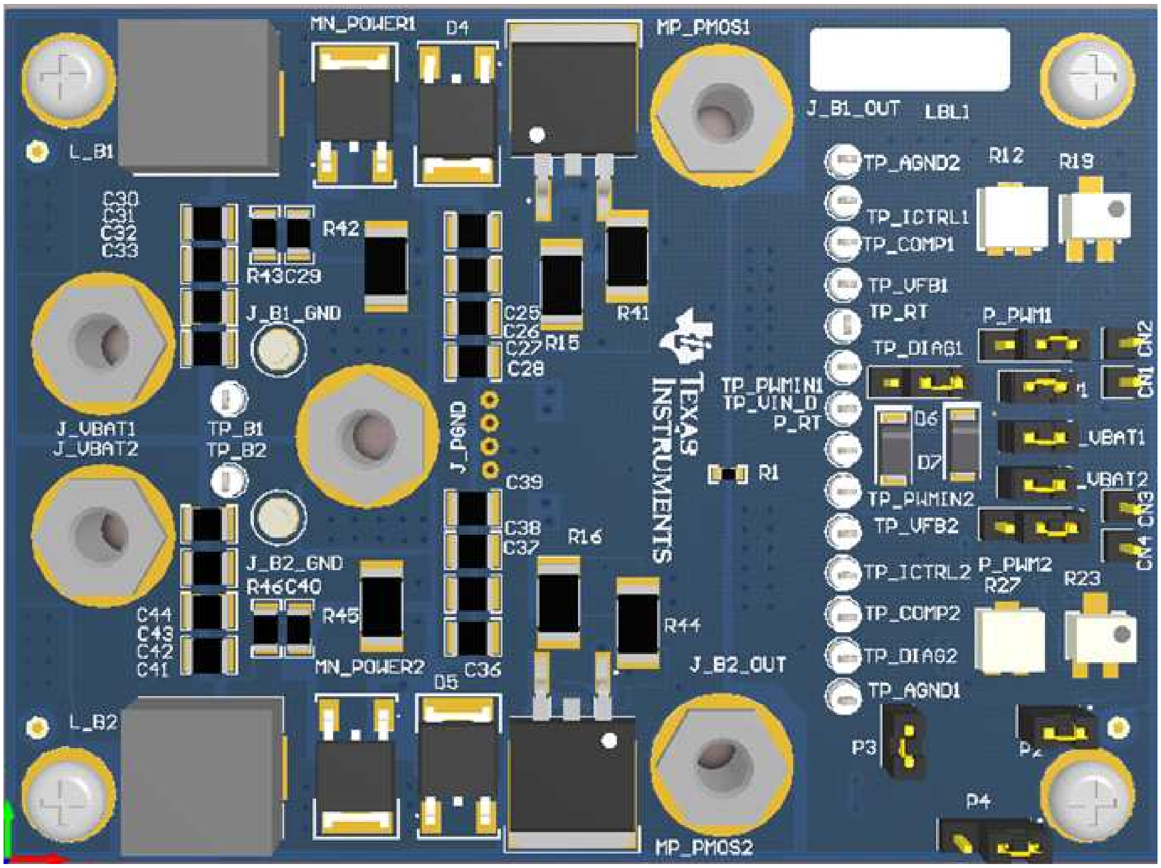



**Figure 14. 3D Board View**

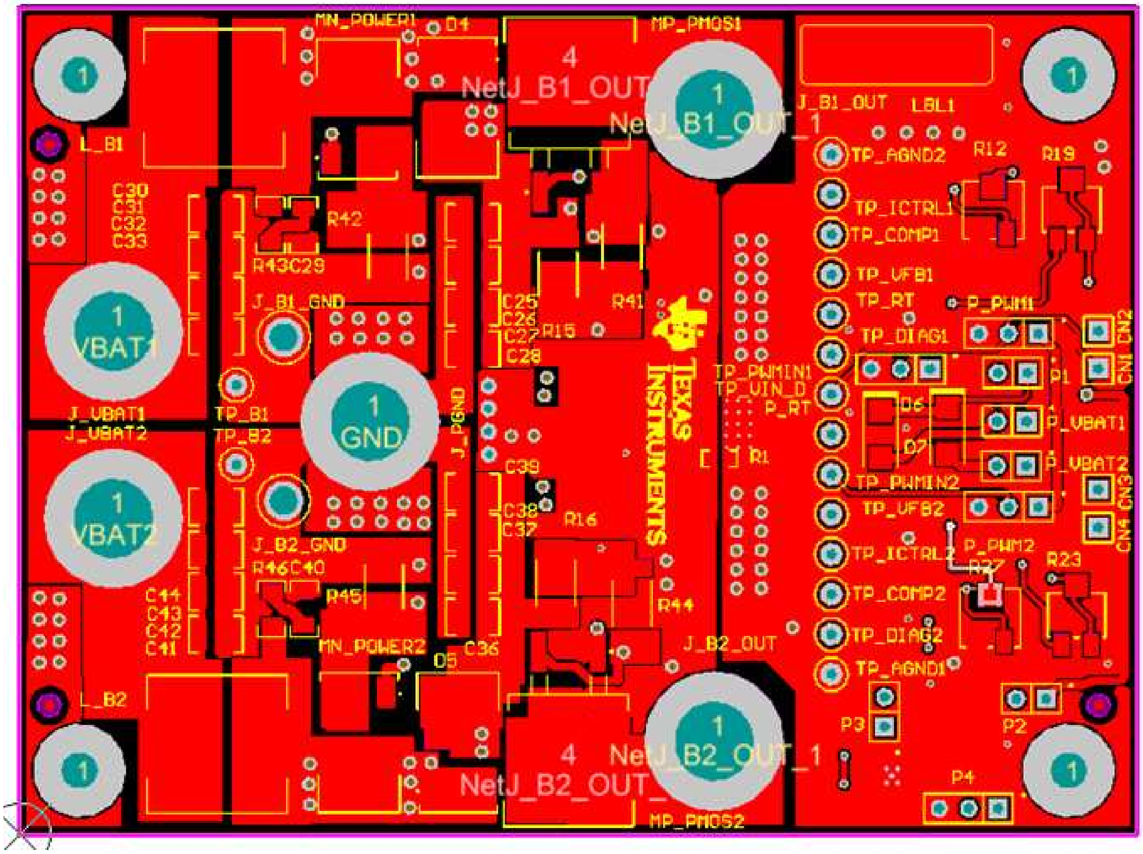


**Figure 15. PCB Top Layer**

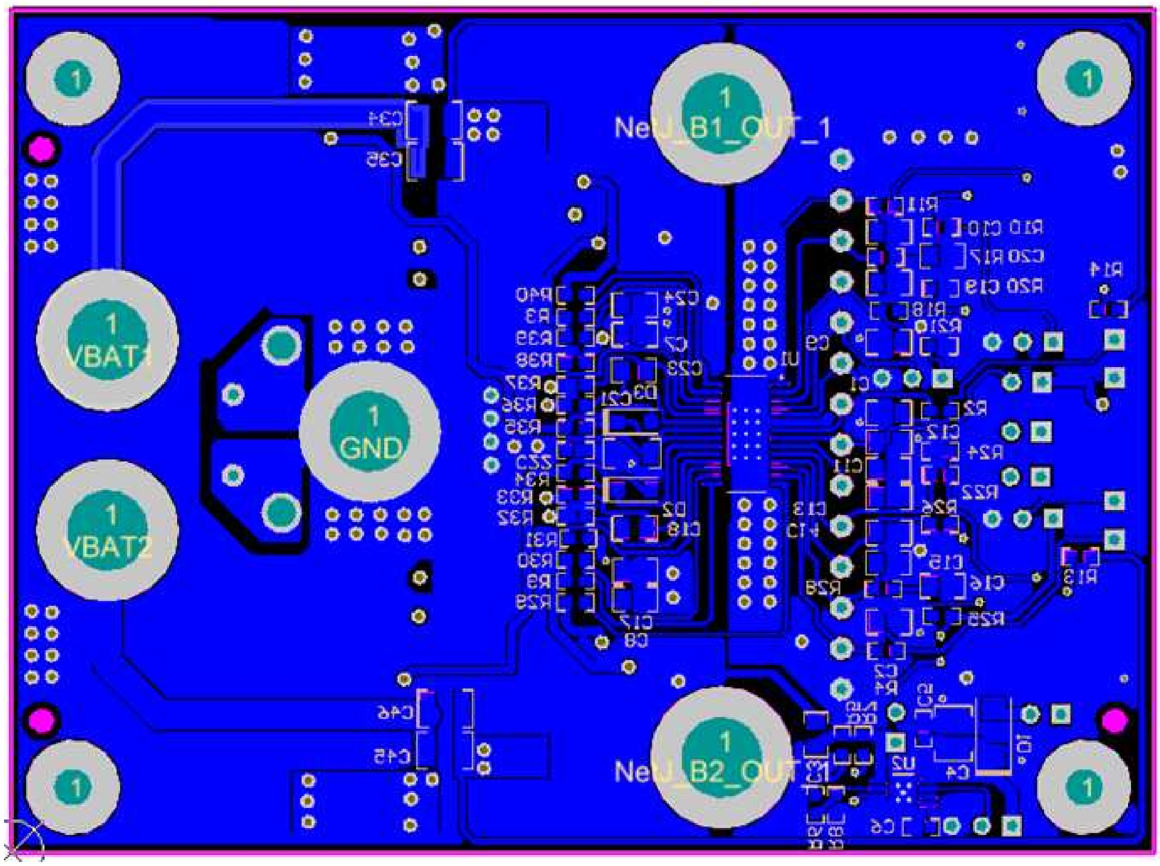



**Figure 16. PCB Bottom Layer**

# 6 Bill of Materials

**Table 2. Bill of Materials**

| Designator | Description | RoHS | Manufacturer | Part Number | Quantity |
|---|---|---|---|---|---|
| !PCB1 | Printed circuit board | O | Any | XX#### | 1 |
| C1, C2, C7, C8, C9, C10, C12, C13, C14, C17, C18, C23, C24 | NC | Y | AVX | NC | 0 |
| C3 | Capacitor, ceramic, 4.7-µF, 10-V, ±10%, X5R, 0805 | Y | AVX | 0805ZD475KAT2A | 1 |
| C4, C30, C31, C32, C33, C34, C35, C41, C42, C43, C44, C45, C46 | Capacitor, ceramic, 3.3-µF, 50-V, ±20%, X7R, 1210 | Y | TDK | C3225X7R1H335M | 13 |
| C5 | Capacitor, ceramic, 0.1-µF, 50-V, ±10%, X7R, 0603 | Y | MuRata | GRM188R71H104KA93D | 1 |
| C6 | Capacitor, ceramic, 1000-pF, 50-V, ±10%, C0G/NP0, 0603 | Y | AVX | 06035A102KAT2A | 1 |
| C11 | Capacitor, ceramic, 0.1-µF, 50-V, ±10%, X7R, 0805 | Y | AVX | 08055C104KAT2A | 1 |
| C15, C19 | Capacitor, ceramic, 270-pF, 50-V, ±5%, C0G/NP0, 0805 | Y | Kemet | C0805C271J5GACTU | 2 |
| C16, C20 | Capacitor, ceramic, 0.22-µF, 25-V, ±5%, X7R, 0805 | Y | AVX | 08053C224JAT2A | 22 |
| C21 | Capacitor, ceramic, 10-µF, 16-V, ±20%, X5R, 1206 | Y | TDK | C3216X5R1C106M | 1 |
| C22 | Capacitor, ceramic, 0.1-µF, 16-V, ±5%, X7R, 0603 | Y | AVX | 0603YC104JAT2A | 1 |
| C25, C26, C27, C28, C36, C37, C38, C39 | Capacitor, ceramic, 2.2-µF, 100-V, ±10%, X7R, 1210 | Y | Taiyo Yuden | HMK325B7225KN-T | 8 |
| C29, C40 | Capacitor, ceramic, 0.01-µF, 50-V, ±5%, C0G/NP0, 1206 | Y | TDK | C3216C0G1H103J | 2 |
| CN1, CN2, CN3, CN4 | Header, TH, 100-mil (2.54-mm), 1-pos, gold plated, 230 mil (5.84 mm) above insulator | Y | Samtec, Inc. | TSW-101-07-G-S | 4 |
| D1, D6, D7 | Diode, Schottky, 50-V, 1-A, SMA | Y | Diodes Inc. | B150-13-F | 3 |
| D2, D3 | Diode, Schottky, 60-V, 1-A, SOD-123F | Y | NXP Semiconductor | PMEG6010CEH,115 | 2 |
| D4, D5 | Diode, Schottky, 100-V, 12-A, DPAK | Y | Vishay-Semiconductor | 12CWQ10FNPBF | 2 |
| FID1, FID2, FID3 | Fiducial mark. There is nothing to buy or mount. | | N/A | N/a | 3 |
| H1, H2, H5, H6 | Standoff, hex, 0.5 inch (12.7 mm) L, No, 4-40 nylon | Y | Keystone | 1902C | 4 |
| H3, H4, H7, H8 | Machine screw, round, No. 4-40 × 1/4 inch (6.35 mm), nylon, Philips panhead | Y | B&F Fastener Supply | NY PMS 440 0025 PH | 4 |
| J_B1_GND, J_B2_GND | Terminal, turret, TH, double | Y | Keystone | 1502-2 | 2 |
| J_B1_OUT, J_B2_OUT, J_PGND, J_VBAT1, J_VBAT2 | Standard banana jack, uninsulated, 15-A | Y | Emerson Network Power | 108-0740-001 | 5 |
| LBL1 | Thermal transfer printable labels, 0.65 inch (16.5 mm) W × 0.2 inch (5.08 mm) H, 10,000 per roll | Y | Brady | THT-14-423-10 | 1 |
| L_B1, L_B2 | Inductor, shielded drum core, ferrite, 10-µH, 9-A, 0.0144-Ω, SMD | Y | Wurth Elektronik eiSos | 7443321000 | 2 |
| MN_POWER1, MN_POWER2 | MOSFET, N-ch, 100-V, 40-A, DPAK | Y | Vishay-Siliconix | SUD40N10-25 | 2 |

**Table 2. Bill of Materials (continued)**

| Designator | Description | RoHS | Manufacturer | Part Number | Quantity |
|---|---|---|---|---|---|
| MP_PMOS1, MP_PMOS2 | MOSFET, P-ch, –100-V, –17.2-A, DDPAK | Y | Vishay-Siliconix | SUM90P10-19L | 2 |
| P1, P2, P3, P_VBAT1, P_VBAT2 | Header, TH, 100-mil (2.54-mm), 2×1, gold plated, 230 mil (8.84 mm) above insulator | Y | Samtec, Inc. | TSW-102-07-G-S | 5 |
| P4, P_PWM1, P_PWM2, P_RT | Header, TH, 100-mil (2.54-mm), 3×1, gold plated, 230 mil (8.84 mm) above insulator | Y | Samtec, Inc. | TSW-103-07-G-S | 4 |
| R1, R2, R4, R9, R11, R18, R22, R26, R29, R30, R31, R32, R33, R36, R37, R38, R40 | Resistor, 0-Ω, 5%, 0.1-W, 0603 | Y | Rohm | MCR03EZPJ000 | 17 |
| R3, R13, R14, R39 | Resistor, 0-Ω, 5%, 0.1-W, 0603 | Y | Panasonic | ERJ-3GEY0R00V | 4 |
| R5 | Resistor, 0 Ω, 5%, 0.1W, 0603 | Y | Vishay-Dale | CRCW06030000Z0EA | 1 |
| R6 | Resistor, 1.87-kΩ, 1%, 0.1-W, 0603 | Y | Vishay-Dale | CRCW06031K87FKEA | 1 |
| R7 | Resistor, 10 kΩ, 5%, 0.1-W, 0603 | Y | Vishay-Dale | CRCW060310K0JNEA | 1 |
| R8 | Resistor, 8.2 kΩ, 5%, 0.1 W, 0603 | Y | Vishay-Dale | CRCW06038K20JNEA | 1 |
| R10, R25 | Resistor, 10 kΩ, 1%, 0.1 W, 0603 | Y | Vishay-Dale | CRCW060310K0FKEA | 2 |
| R12, R27 | Trimmer, 20-kΩ, 0.25-W, SMD | Y | Bourns | 3224J-1-203 E | 2 |
| R15, R16 | Resistor, 0.003-Ω, 1%, 1-W, 2512 | Y | CTS Resistor | 73M1R003F | 2 |
| R17, R28 | Resistor, 510-Ω, 1%, 0.1-W, 0603 | Y | Yageo America | RC0603FR-07510RL | 2 |
| R19, R23 | Trimmer, 1-MΩ, 0.25-W SMD | Y | Bourns | 3224X-1-105E | 2 |
| R20, R24 | Resistor, 30-k Ω, 0.1%, 0.1-W, 0603 | Y | Susumu Co Ltd | RG1608P-303-B-T5 | 2 |
| R21 | Resistor, 20-k Ω, 1%, 0.1-W, 0603 | Y | Vishay-Dale | CRCW060320K0FKEA | 1 |
| R34, R35 | Resistor, 10-Ω, 5%, 0.1-W, 0603 | Y | Vishay-Dale | CRCW060310R0JNEA | 2 |
| R41, R44 | Resistor, 0.3-Ω, 1%, 2-W, 2512 | Y | Stackpole Electronics Inc | CSRN2512FKR300 | 2 |
| R42, R45 | Resistor, 0.015-Ω, 1%, 2-W, 2512 | Y | Stackpole Electronics Inc | CSRN2512FK15L0 | 2 |
| R43, R46 | Resistor, 51-Ω, 1%, 0.25-W, 1206 | Y | Yageo America | RC1206FR-0751RL | 2 |
| SH-P1, SH-P2, SH-P3, SH-P4, SH-PWM1, SH-PWM2, SH-RT, SH-VBAT1, SH-VBAT2 | Shunt, 100-mil (2.54-mm), gold plated, black | Y | 3M | 969102-0000-DA | 9 |
| TP_AGND1, TP_AGND2, TP_B1, TP_B2, TP_COMP1, TP_COMP2, TP_DIAG1, TP_DIAG2, TP_ICTRL1, TP_ICTRL2, TP_PWMIN1, TP_PWMIN2, TP_RT, TP_VFB1, TP_VFB2, TP_VIN_D | Test point, TH, miniature, white | Y | Keystone | 5002 | 16 |
| U1 | Automotive headlight LED driver, 2-channel, PWP0028F | Y | Texas Instruments | TPS92602QPWPRQ1 | 1 |
| U2 | High-voltage ultralow-Iq low-dropout regulator, DGN0008D | Y | Texas Instruments | TPS7A6650QDGNRQ1 | 1 |

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