User's Guide

TPS562202 Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS562202 as well as support documentation for the TPS562202EVM evaluation module. Included are the performance specifications, board layout, schematic, and the bill of materials of the TPS562202EVM.

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Trademarks

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1 Introduction

The TPS562202 is a single, adaptive on-time, D-CAP2™ mode, synchronous buck converter requiring a very low external component count. The D-CAP2 control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal 580 KHz and enters Advanced Eco-mode in light load conditions. The high-side and low-side switching MOSFETs are incorporated inside the TPS562202 package along with the gate-drive circuitry. The low drain-to-source on-resistance of the MOSFETs allows the TPS562202 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The TPS562202 dc/dc synchronous converter is designed to provide up to a 2-A output from an input voltage source of 4.3 V to 17 V. The output voltage range is from 0.804 V to 7 V. Rated input voltage and output current ranges for the evaluation module are given in Table 1-1.

The TPS562202EVM evaluation module (EVM) is a single, synchronous buck converter providing 1.05 V at 2 A from 4.3-V to 17-V input. This user's guide describes the TPS562202EVM performance.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS562202EVM	V_{IN} = 4.3 V to 17 V	0 A to 2 A

2 Performance Specification Summary

A summary of the TPS562202EVM performance specifications is provided in Table 2-1. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 1.05 V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2-1. Performance Specifications Summary

SPECIFICATIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		4.3	12	17	V
Output voltage set point			1.05		V
Operating frequency	V_{IN} = 12 V, I_O = 2 A		580		kHz
Output current range		0		2	A
Overcurrent limit	V_{IN} = 12 V, L_O = 2.2 µH		3.1		A
Output ripple voltage	V_{IN} = 12 V, I_O = 2 A		20		mV_{PP}

3 Modifications

These evaluation modules are designed to provide access to the features of the TPS562202. Some modifications can be made to this module.

3.1 Output Voltage Setpoint

To change the output voltage of the EVMs, it is necessary to change the value of resistor R4. Changing the value of R4 can change the output voltage. The value of R4 for a specific output voltage can be calculated using Equation 1.

$$R_4 = \frac{R_6 \times (Vout - 0.804V)}{0.804V} \quad (1)$$

Table 3-1 lists the R4 values for some common output voltages. Note that the values given in Table 3-1 are standard values and not the exact value calculated using above equation.

Table 3-1. Output Voltages

OUTPUT VOLTAGE (V)	R4 (kΩ)	R6 (kΩ)	TYP L1 (µH)	C5+C6+C7 (µF)			CFF (pF)
				MIN	TYP	MAX	
0.85	0.55	10.0	2.2	20	44	110	
0.9	1.2	10.0	2.2	20	44	110	

Table 3-1. Output Voltages (continued)

OUTPUT VOLTAGE (V)	R4 (kΩ)	R6 (kΩ)	TYP L1 (µH)	C5+C6+C7 (µF)			CFF (pF)
				MIN	TYP	MAX	
1.0	2.4	10.0	2.2	20	44	110	
1.05	3	10.0	2.2	20	44	110	
1.2	4.9	10.0	2.2	20	44	110	
1.5	8.6	10.0	2.2	20	44	110	
1.8	12.3	10.0	2.2	20	44	110	
2.5	21	10.0	3.3	20	44	110	
3.3	31	10.0	3.3	20	44	110	10-220
5.0	52	10.0	4.7	20	44	110	10-220
6.5	70.5	10.0	4.7	20	44	110	10-220

4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS562202EVM. The section also includes test results typical for the evaluation modules: start-up, shut-down, output voltage ripple, input voltage ripple, and load transient response.

4.1 Input/Output Connections

The TPS562202EVM is provided with input/output connectors and test points as shown in Table 4-1. Figure 4-1 shows connectors and jumpers placement on TPS562202EVM board.

A power supply capable of supplying 2 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 2 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP2 provides a place to monitor the V_{IN} input voltages with TP6 providing a convenient ground reference. TP3 is used to monitor the output voltage with TP10 as the ground reference.

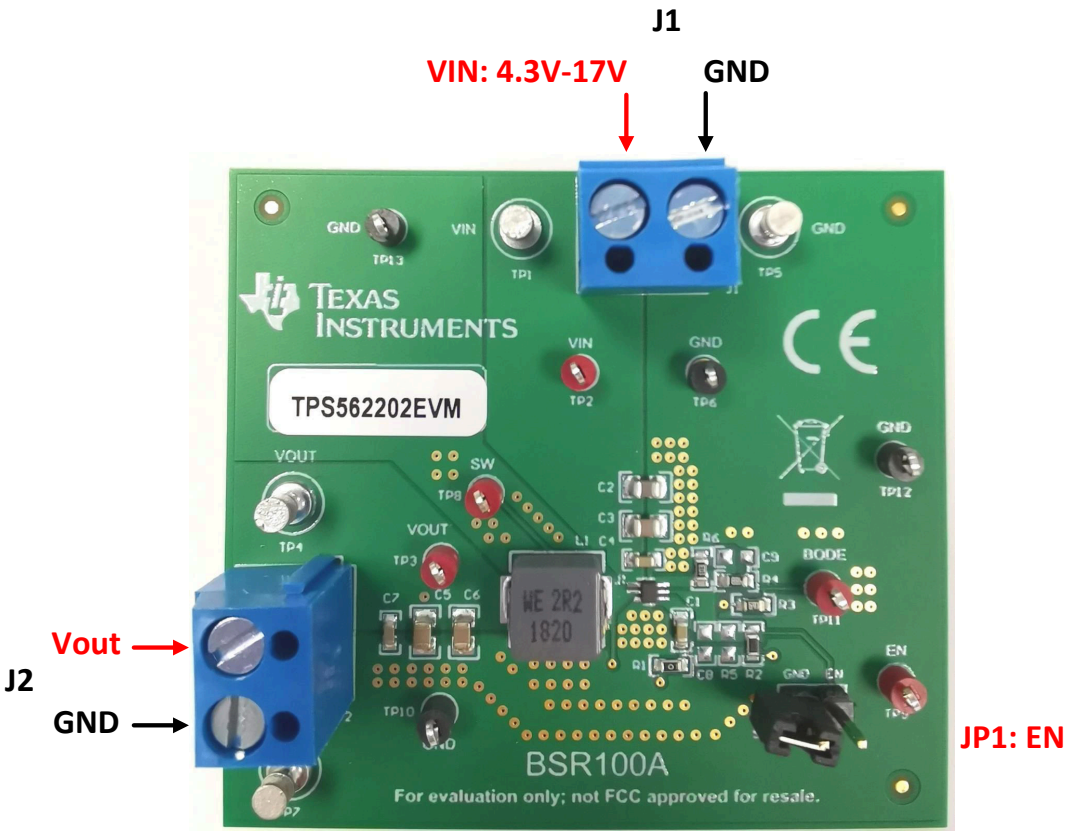

Figure 4-1. TPS562202EVM Connectors and Jumpers Placement

Table 4-1. Connection and Test Points

REFERENCE DESIGNATOR	FUNCTION
J1	V_{IN} (see Table 1-1 for V_{IN} range)
J2	V_{OUT}, 1.05 V at 2-A maximum
JP1	EN control. Shunt EN to GND to disable
TP1	V_{IN} positive power point
TP2	V_{IN} positive monitor point
TP3	V_{OUT} positive monitor point
TP4	V_{OUT} positive power point
TP5, TP7	GND power point
TP6, TP10, TP12,TP13	GND monitor point
TP8	Switch node test point
TP9	EN test point
TP11	Test point for loop response measurements

4.2 Start-Up Procedure

1. Ensure that the jumper at JP1 (Enable control) pins 1 and 2 are covered to shunt EN to GND, disabling the output.
2. Apply appropriate V_{IN} voltage to VI (J1-2) and GND (J1-1).
3. Move the jumper at JP1 (Enable control) pins 1 and 2 (EN and GND) to enable the output.

4.3 Start-Up

The TPS562202EVM start-up waveform relative to V_{IN} is shown in Figure 4-2.

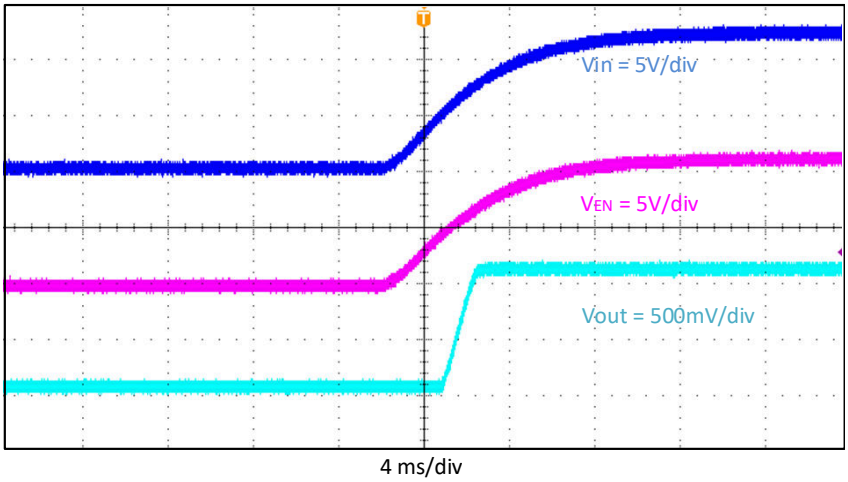

Figure 4-2. Start-Up Relative to V_{IN}, I_{OUT} = 2 A

The TPS562202EVM start-up waveform relative to enable (EN) is shown in Figure 4-3.

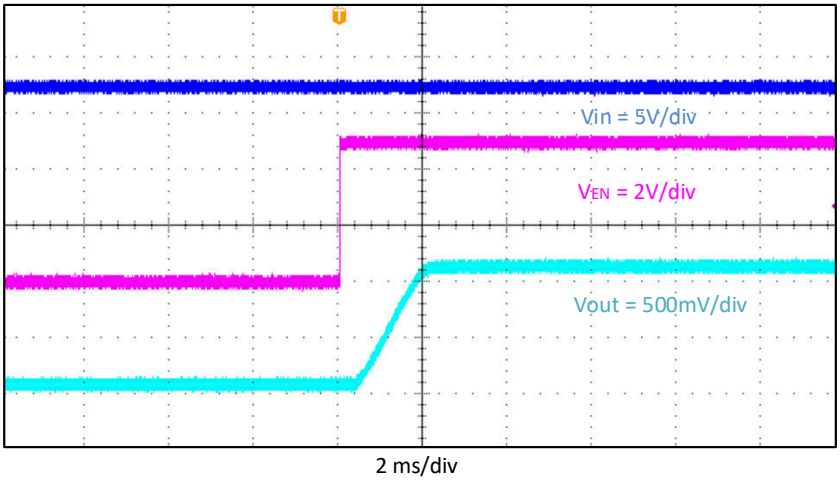

Figure 4-3. Start-Up Relative to EN, I_{OUT} = 2 A

4.4 Shut-Down

The TPS562202EVM shut-down waveform relative to V_{IN} is shown in Figure 4-4.

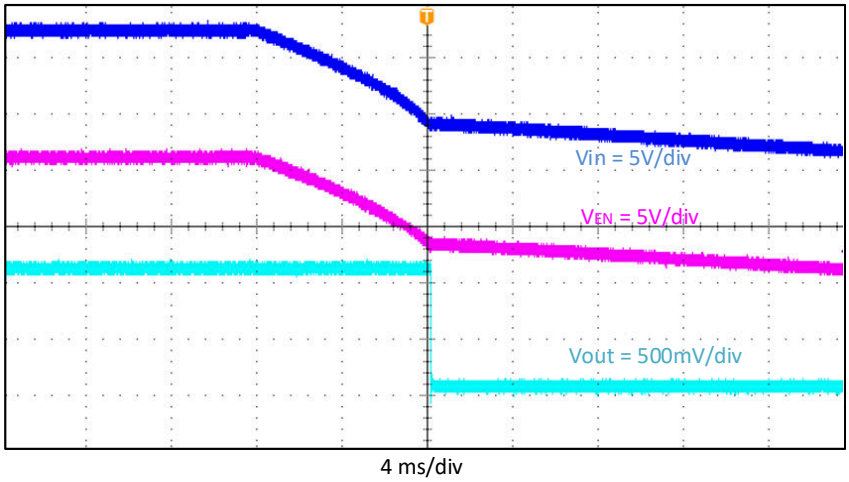

Figure 4-4. Shut-Down Relative to V_{IN}, I_{OUT} = 2 A

The TPS562202EVM shut-down waveform relative to EN is shown in Figure 4-5.

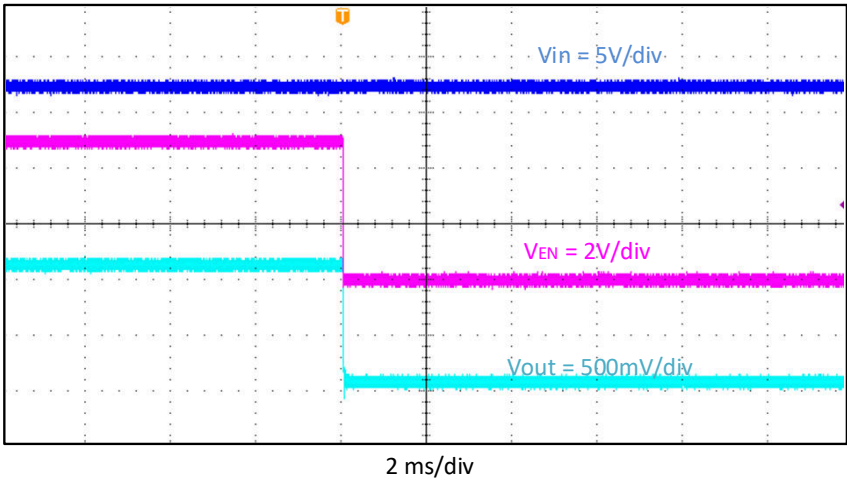

Figure 4-5. Shut-Down Relative to EN, I_{OUT} = 2 A

4.5 Output Voltage Ripple

The TPS562202EVM output voltage ripple is shown in Figure 4-6 and Figure 4-7. The output currents are as indicated.

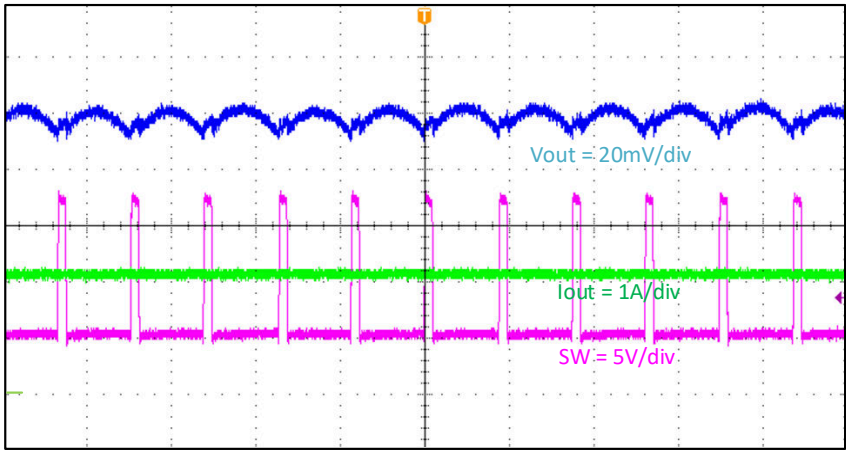

Figure 4-6. Output Voltage Ripple, I_{OUT} = 2 A

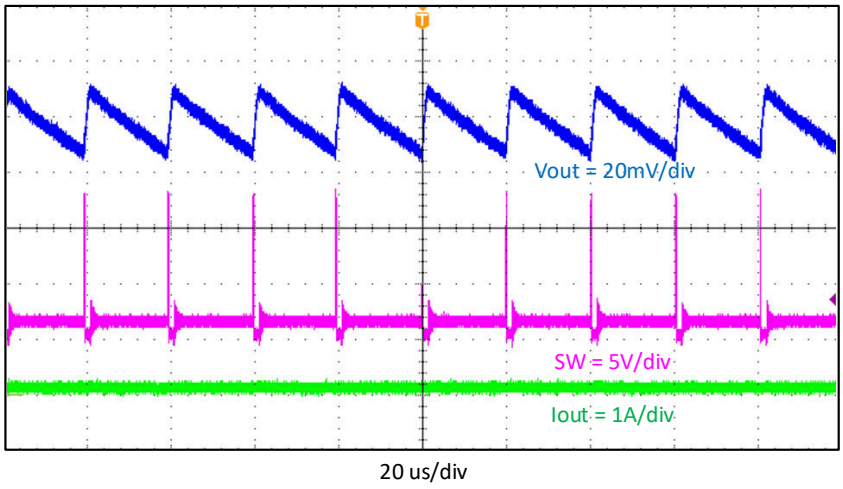

Figure 4-7. Output Voltage Ripple, I_{OUT} = 10 mA

4.6 Input Voltage Ripple

The TPS562202EVM input voltage ripple is shown in Figure 4-8. The output current is as indicated.

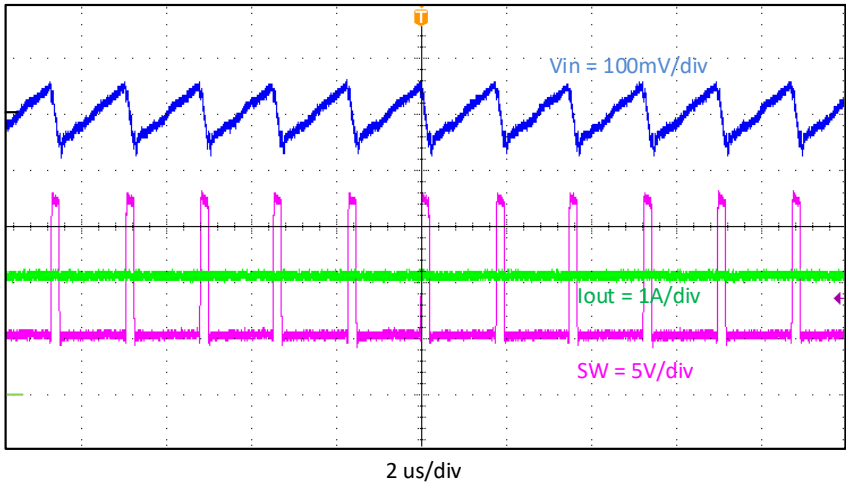

Figure 4-8. Input Voltage Ripple, I_{OUT} = 2 A

4.7 Load Transient Response

The TPS562202EVM response to load transient is shown in Figure 4-9. The current steps are indicated in Figure 4-9. The loading step slew rate is 2.5 A/µs. Total peak-to-peak voltage variation is as shown.

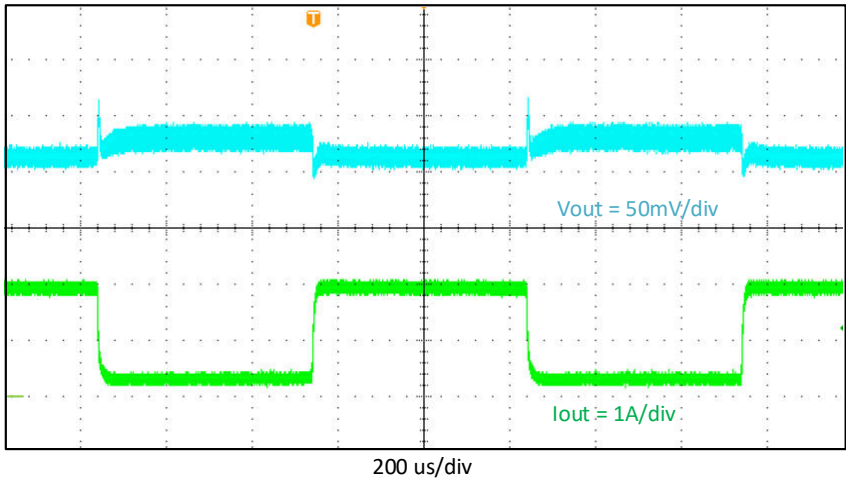

Figure 4-9. Load Transient Response, 10% to 90% (0.2 A - 1.8 A) Load Step

5 Board Layout

This section provides a description of the TPS562202EVM, board layout, and layer illustrations.

5.1 Layout

The board layout for the TPS562202EVM is shown in Figure 5-1, Figure 5-2, and Figure 5-3. The top layer contains the main power traces for VIN, VOUT, and ground. The top layer also has the connections for the pins of the TPS562202 and a large area filled with ground. Most of the signal traces are also located on the top side. The input decoupling capacitors, C2, C3, and C4 are located as close to the IC as possible. The input and output connectors, test points, and all of the components are located on the top side. The bottom layer is a ground plane along with the switching node copper fill, signal ground copper fill, and the feedback trace from the point of regulation to the top of the resistor divider network. Both the top layer and bottom layer use 2-oz copper thickness.

Figure 5-4 and Figure 5-5 are the TPS562202EVM board top view and bottom view, respectively.

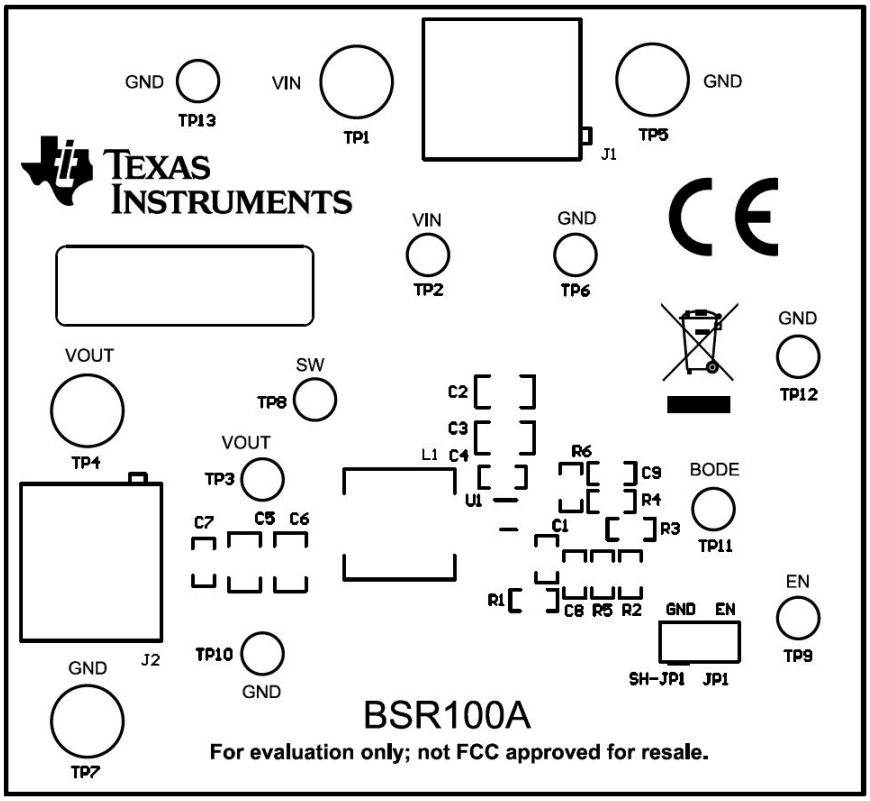

Figure 5-1. TPS562202EVM Top Assembly

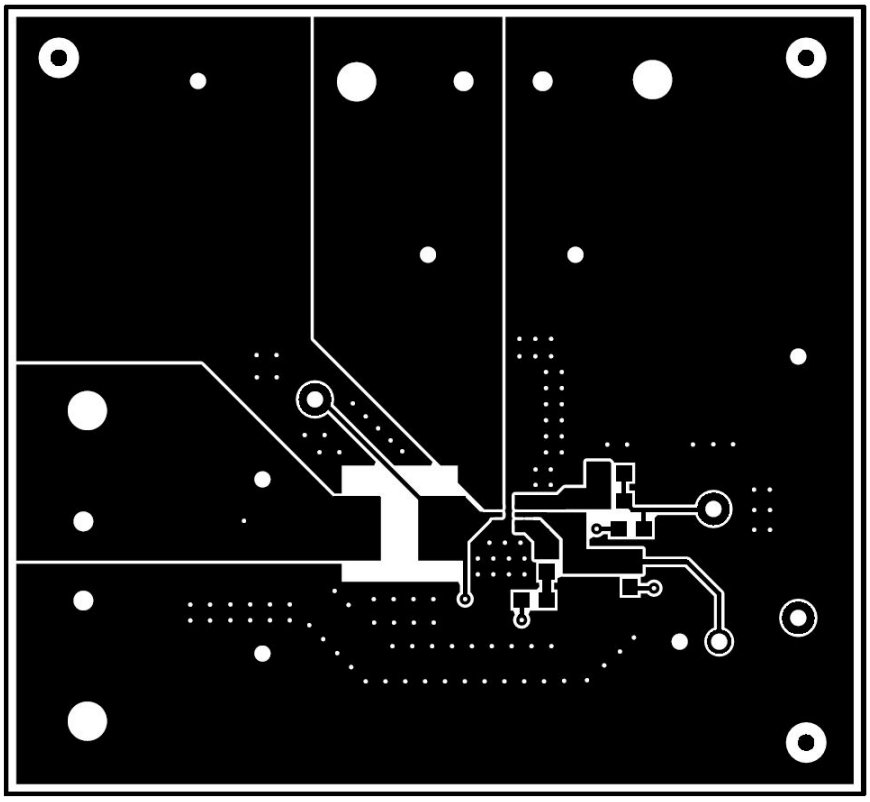

Figure 5-2. TPS562202EVM Top Layer

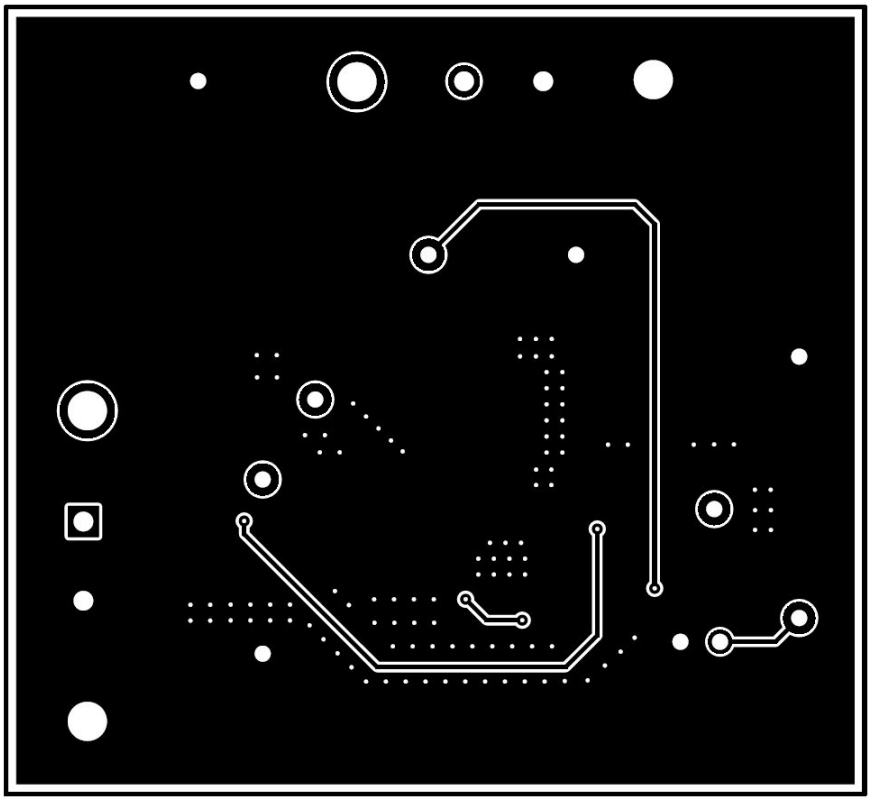

Figure 5-3. TPS562202EVM Bottom Layer

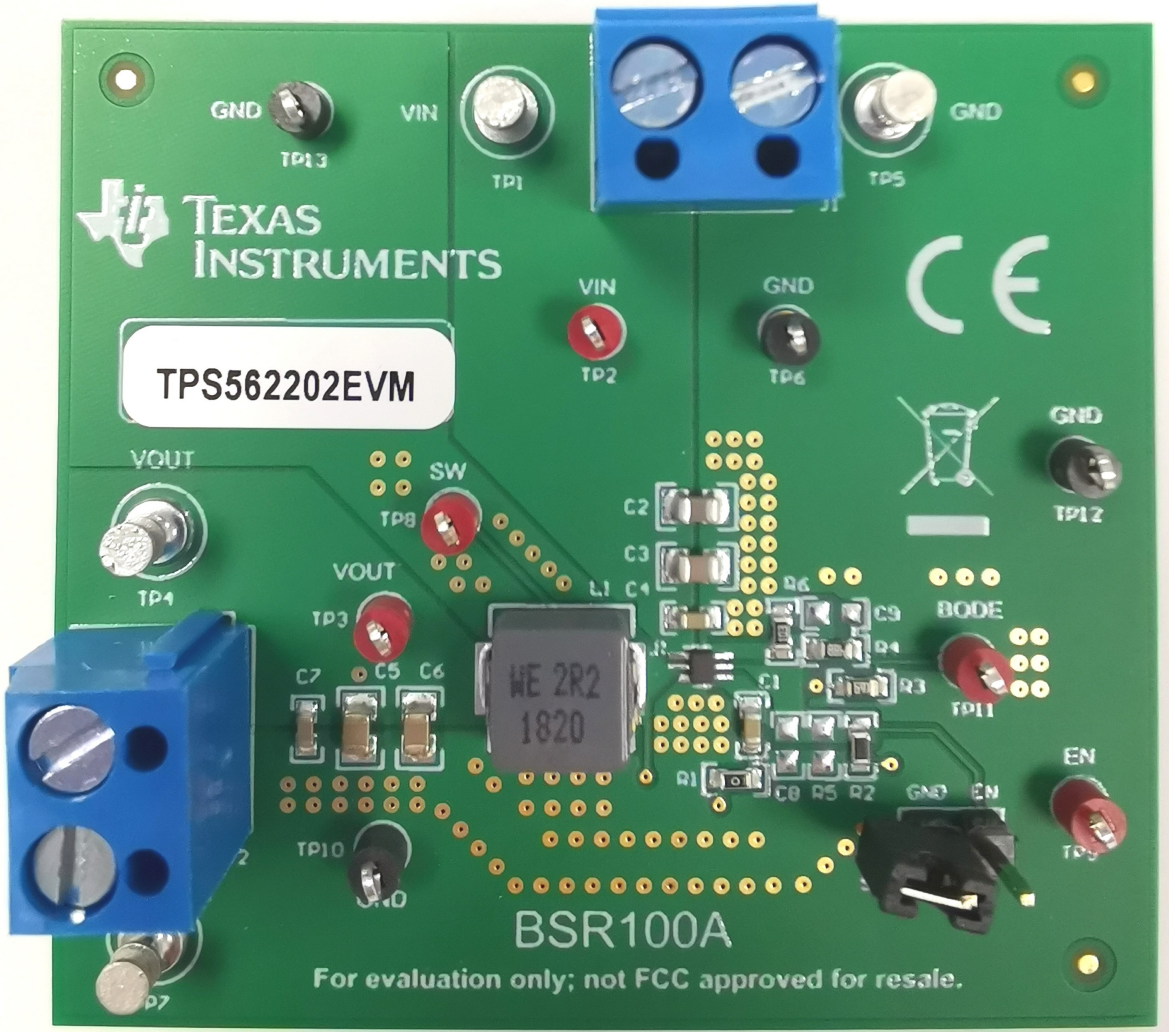

Figure 5-4. TPS562202EVM Board Top View

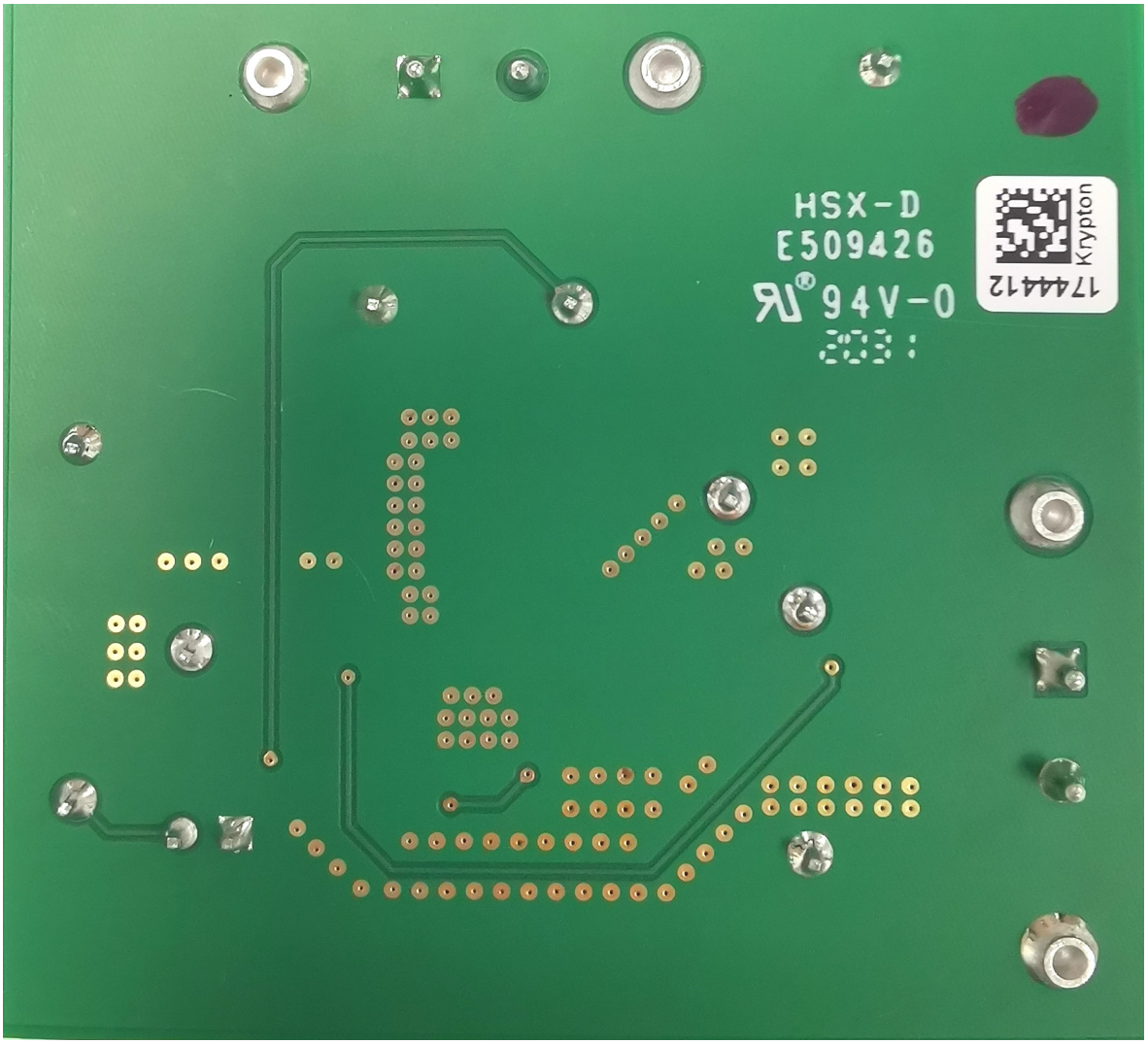

Figure 5-5. TPS562202EVM Board Bottom View

6 Schematic, Bill of Materials, and Reference

6.1 Schematic

Figure 6-1 is the schematic for the TPS562202EVM.

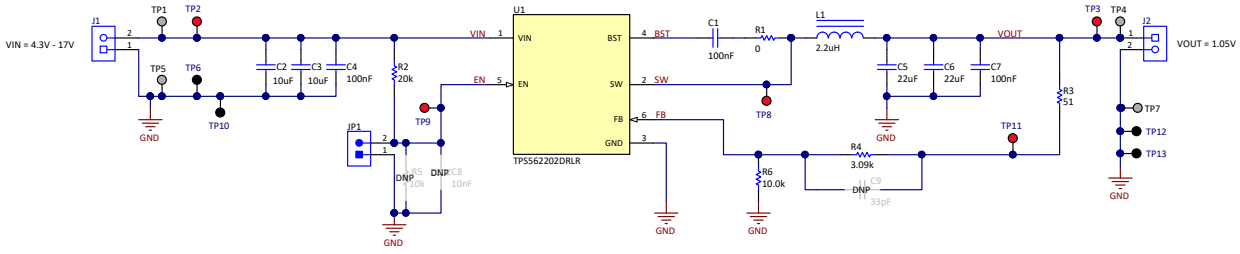

Figure 6-1. TPS562202EVM Schematic Diagram

6.2 Bill of Materials

Table 6-1. Bill of Materials

DES	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
!PCB1	1	Printed Circuit Board	BSR100	Any
C1, C4,C7	3	Capacitor, ceramic, 0.1 µF, 25 V, ±10%, X7R, 0603	C1608X7R1E104K080AA	TDK
C2, C3	2	Capacitor, ceramic, 10 µF, 25 V, ±20%, X5R, 0805	GRM21BR61E106MA73L	MuRata
C5, C6	2	Capacitor, ceramic, 22 µF, 10 V, ±20%, X5R, 0805	GRM21BR61A226ME44L	MuRata
J1, J2	2	Terminal block, 5.08 mm, 2x1, Brass, TH	ED120/2DS	On-Shore Technology
JP1	1	Header, 100 mil, 2 x 1, tin, TH	PEC02SAAN	Sullins Connector Solutions
L1	1	Inductor, shielded drum core, powdered iron, 2.2 µH, 7.5 A, 0.0112 Ω, SMD	74437349022	Wurth Elektronik
LBL1	1	Thermal transfer printable labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady
R1	1	Resistor, 0 Ω, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06030000Z0EA	Vishay-Dale
R2	1	Resistor, 20 kΩ, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060320K0JNEA	Vishay-Dale
R3	1	Resistor, 51 Ω, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060351R0JNEA	Vishay-Dale
R4	1	Resistor, 3.09 kΩ, 1%, 0.1 W, 0603	RC0603FR-073K09L	Yageo
R6	1	Resistor, 10.0 kΩ, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310K0FKEA	Vishay-Dale
SH-JP1	1	Shunt, 100 mil, gold plated, black	SNT-100-BK-G	Samtec
TP1, TP4, TP5, TP7	4	Terminal, turret, TH, double	1502-2	Keystone
TP2, TP3, TP8, TP9, TP11	5	Test point, miniature, red, TH	5000	Keystone
TP6, TP10, TP12, TP13	4	Test Point, miniature, black, TH	5001	Keystone
U1	1	4.3-V to 17-V Input, 2-A Synchronous Buck Converter, DRL0006A (SOT-5X3-6)	TPS562202DRLR	Texas Instruments
C8	0	Capacitor, ceramic, 0.01 µF, 50 V, ±10%, X7R, 0603	C1608X7R1H103K080AA	TDK
C9	0	Capacitor, ceramic, 33 pF, 100 V, ±5%, C0G/NP0, 0603	GRM1885C2A330JA01D	MuRata
R5	0	Resister, 10 kΩ, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310K0JNEA	Vishay-Dale

6.3 Reference

1. *TPS562202 4.3 V to 17 V Input, 2-A Synchronous Step-Down Voltage Regulator in SOT563* data sheet (SLUSE28)

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2020) to Revision A (April 2021) **Page**

- Updated user's guide title..... 3

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