BQ76905

Technical Reference Manual

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Read This First

About This Manual

This technical reference manual (TRM) discusses the modules and peripherals of the BQ76905 device, and how each is used to build a complete battery pack monitor and protection solution. For details on the hardware device features and electrical specifications, see the *BQ76905 2-Series to 5-Series High Accuracy Battery Monitor and Protector for Li-Ion, Li-Polymer, LiFePO$_4$ (LFP), and LTO Battery Packs*.

Battery Notational Conventions

The following notation is used if commands, subcommands, and data memory values are mentioned within a text block:

- Commands and subcommands: *italics* with parentheses and no breaking spaces; for example, *Battery Status()*
- Data memory: *italics*, **bold**, and breaking spaces; for example, ***Power Config***
- Register bits and flags: *italics* and brackets; for example, *[SCD]*
- Data memory bits: *italics* and **bold**; for example, ***[FET_EN]***
- Modes and states: ALL CAPITALS; for example, DEEPSLEEP

Trademarks

Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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Chapter 1

Introduction

The Texas Instruments BQ76905 provides a highly integrated, high accuracy battery monitor and protector for 2-series to 5-series Li-Ion, Li-Polymer, and $LiFePO_4$ battery packs. Each device includes a high accuracy monitoring system, a highly configurable protection subsystem, and support for host controlled cell balancing. Integration includes low-side protection NFET drivers, a programmable LDO for external system use, and an I^2C host communication interface supporting up to 400-kHz operation with optional CRC. Device features include:

- Battery monitoring capability for 2-series to 5-series cells
- Integrated low-side drivers for NFET protection with optional autonomous recovery
- Extensive protection suite including voltage,temperature, current, and internal diagnostics
- 16-bit delta-sigma voltage ADC
  - High accuracy cell voltage measurement of 5 mV (typical)
- Dedicated 16 / 24-bit delta-sigma coulomb counter ADC
- – High-accuracy current measurement with low input offset error
  - Wide-range current applications (±200 mV measurement range across sense resistor)
  - 48-bit accumulated charge integrator with timer
- Host-controlled cell balancing
- Multiple power modes (typical battery pack operating range conditions)
  - NORMAL mode: 30 µA to 180 µA
  - SLEEP mode: 10 µA
  - DEEPSLEEP mode: 5 µA
  - SHUTDOWN Mode: 1 µA
- High voltage tolerance of 45 V on cell connect and select additional pins
- Support for temperature sensing using internal sensor and external thermistor
- Integrated one-time-programmable (OTP) memory for device settings, programmed by TI
- 400-kHz I^2C serial communications with optional CRC support
- Programmable LDO for external system usage

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2.1 Overview

The BQ76905 product is a highly integrated, accurate battery monitor and protector for 2-series to 5-series Li-Ion, Li-Polymer, $LiFePO_4$ (LFO), and LTO battery packs. A high accuracy voltage, current, and temperature measurement provides data for host-based algorithms and control. A feature-rich and highly configurable protection subsystem provides a wide set of protections which can be triggered and recovered completely autonomously by the device or under full control of a host processor. Integrated FET drivers drive low-side charge and discharge protection NFETs. A programmable LDO is included for external system use, with voltage programmable to 1.8 V, 2.5 V, 3.0 V, 3.3 V, or 5.0 V, capable of providing up to 20 mA.

The BQ76905 device includes one-time-programmable (OTP) memory which TI programs to configure default device operation settings, for systems where a host processor is not available to configure the device. A 400-kHz I^2C communication interface and ALERT interrupt output enable communication with a host processor. The device includes support for one external thermistor as well as an internal die temperature measurement. Figure 2-1 shows the BQ76905 block diagram.

2.2 Functional Block Diagram

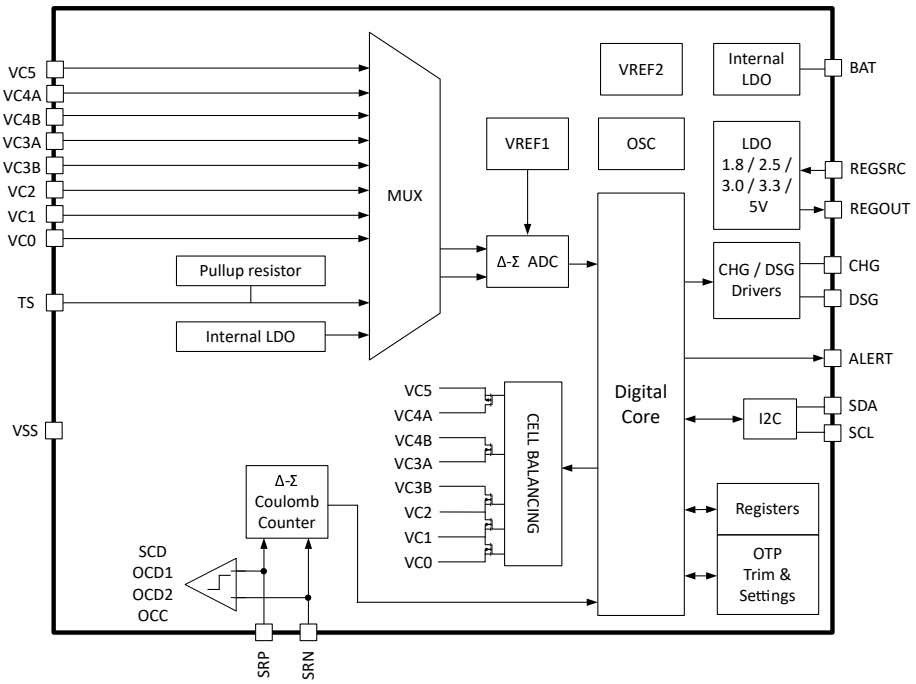

Figure 2-1. BQ76905 Block Diagram

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Chapter 3

Device Configuration

3.1 Direct Commands and Subcommands

The BQ76905 device includes support for direct commands and subcommands. The direct commands are accessed using a 7-bit command address that is sent from a host through the device serial communications interface and either triggers an action, or provides a data value to be written to the device, or instructs the device to report data back to the host. Subcommands are additional commands that are accessed indirectly using the 7-bit command address space and provide the capability for block data transfers.

When a subcommand is initiated, a 16-bit subcommand address is first written to the 7-bit command addresses 0x3E (lower byte) and 0x3F (upper byte). The device initially assumes a read-back of data is needed and auto-populates existing data into the 32-byte transfer buffer (which uses 7-bit command addresses 0x40–0x5F), and writes the checksum for this data into address 0x60. If the host instead intends to write data into the device, the host overwrites the new data into the transfer buffer, a checksum for the data into address 0x60, and the data length into address 0x61.

As soon as address 0x61 is written, the device checks the checksum written into 0x60 with the data written into 0x40-0x5F, and if this is correct, it proceeds to transfer the data from the transfer buffer into the device's memory. The checksum is the 8-bit modulo-256 sum of the subcommand bytes (0x3E and 0x3F) and the bytes used in the transfer buffer, then the result is bitwise inverted. The verification cannot take place until the data length is written, so the device realizes how many bytes in the transfer buffer are included. The data length must be written last, after the checksum has been written (they do not need to be written together as a word).. The data length includes the two bytes in 0x3E and 0x3F, the two bytes in 0x60 and 0x61, and the length of data in the transfer buffer. Therefore, if the entire 32-byte transfer buffer is used, the data length is 0x24.

When the data length in 0x61 is read, the device automatically increments the address presently in 0x3E and 0x3F by 0x0020, and populates the transfer buffer with new readback data. This allows large portions of data memory to be read by continuous reading of the address space 0x40 to 0x61. If the host attempts to read the transfer buffer data starting at 0x40 while the device is still loading the data into the transfer buffer, the device clock stretches the I2C read transaction until the data is available.

Some subcommands are only used to initiate an action and do not involve sending or receiving data. In these cases, the host can simply write the subcommand into 0x3E and 0x3F, it is not necessary to write the length and checksum or any further data. Note that if an auto-incremented address corresponds to a subcommand that does not involve data, the auto-incrementing does not cause that subcommand to be initiated.

The commands supported in the device are described in Commands and Subcommands. Single-byte commands are direct commands, while two-byte commands are subcommands. Data formats are described in Data Formats.

The most efficient approach to read the data from a subcommand (to minimize bus traffic) is shown below:

1. Write lower byte of subcommand to 0x3E.
2. Write upper byte of subcommand to 0x3F.
3. Read back the subcommand from 0x3E and 0x3F, which echoes back the subcommand address sent in steps 1 and 2 (or the auto-incremented address from step 6).
4. Read buffer starting at 0x40 for the expected length (reading the full 32 bytes is also acceptable).
5. Read the checksum at 0x60 and verify it matches the data read over the length specified by the subcommand.

6. If auto-incrementing is desired, read the data length at 0x61, at which point the device increments the address in 0x3E and 0x3F by 32 and repopulate the buffer with the next 32 bytes of data, then go to step 2.

Note

0x61 provides the length of the buffer data plus 4 (that is, length of the buffer data plus the length of 0x3E and 0x3F plus the length of 0x60 and 0x61).

The checksum is calculated over 0x3E, 0x3F, and the length of buffer data specified by the subcommand, it does not include the checksum or length in 0x60 and 0x61.

Write command or subcommand bits denoted RSVD_0 only as a "0". Write bits denoted RSVD_1 only as a "1".

3.2 Configuration Using OTP or Registers

The BQ76905 device includes Data Memory registers with values stored in digital logic, as well as one-time programmable (OTP) memory, which holds device trim information and default settings for registers. At initial power-up or after a reset, the device loads the OTP settings into registers, which are used by the device logic during operation. The device can also perform a reset on demand if the *0x0012 RESET()* subcommand is sent.

The OTP memory is written by TI during device manufacturing and cannot be modified by the customer. A customized OTP configuration can be developed and programmed into a custom device by TI, depending on business terms. For example, with the appropriate OTP configuration the device can power up, load settings from OTP, and operate autonomously without needing host processor support. If interested in this option, please contact TI for further discussion.

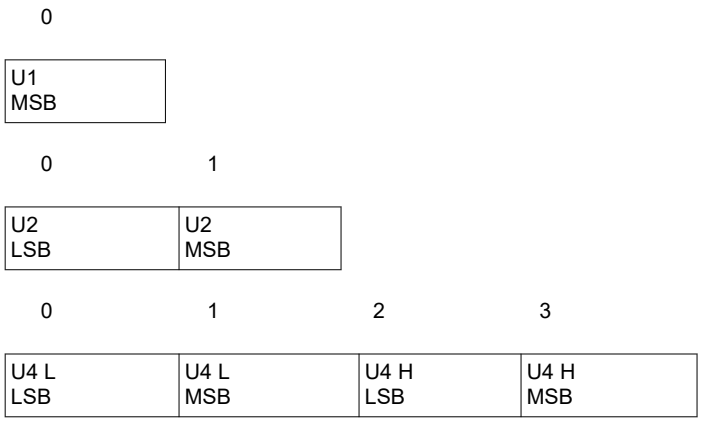
For other cases, a host processor generally initializes registers after power up or reset, but registers need to be re-initialized after each power cycle or reset of the device. Register values are preserved while the device is in NORMAL, SLEEP, or DEEPSLEEP modes. If the device enters SHUTDOWN mode or a reset occurs, all register memory is cleared, and the device returns to the default parameters when powered again. Even if TI has provided a device with a customized OTP, the customer can still modify register values in system after power-up, in case a different setting is required.

The OTP memory also includes a digital signature, which is stored in OTP. When the device is first powered or after a reset, it reads the OTP settings and check that the signature matches that stored, to provide robustness against bit errors in reading or corruption of the memory. If a signature error is detected, the device enters SHUTDOWN mode.

3.3 Data Formats

3.3.1 Unsigned Integer

Unsigned integers are stored without changes as 1-byte, 2-byte, or 4-byte values in little endian byte order.



3.3.2 Integer

Integer values are stored in 2's-complement format in 1-byte, 2-byte, or 4-byte values in little endian byte order.

0
I1 MSB

0	1
I2 LSB	I2 MSB

0	1	2	3
I4 L LSB	I4 L MSB	I4 H LSB	I4 H MSB

3.3.3 Hex

Bit register definitions are stored in unsigned integer format.

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Chapter 4

Device Security

The BQ76905 device includes two security modes: SEALED and FULLACCESS, which can be used to limit the ability to view or change settings.

In SEALED mode, most data and status can be read using commands and subcommands, but only selected settings can be changed. Data memory settings cannot be read or changed directly.

FULLACCESS mode includes SEALED mode functionality, adds the ability to execute additional subcommands, and provides capability to read and modify all device settings.

Selected settings in the device can be modified while the device is in operation through supported commands and subcommands, but in order to modify all settings, the device must enter CONFIG_UPDATE mode, which stops device operation while settings are being updated. After the update is completed, device operation is restarted using the new settings. CONFIG_UPDATE mode is only available in FULLACCESS mode.

The BQ76905 device implements a key-access scheme to move from SEALED to FULLACCESS mode. A unique set of keys must be sent to the device through the subcommand address (0x3E and 0x3F). The keys must be sent consecutively to 0x3E and 0x3F, with no other data written between the keys. Do not set the two keys to identical values, and it is recommended to not use keys which are identical to subcommand addresses. When in SEALED mode, the *0x12 Battery Status()[SEC1, SEC0]* bits are set to [1, 1]. When the FULLACCESS keys are correctly received by the device, the bits are set to [0, 1]. The state [0, 0] is not valid and only indicates that the state has not yet been loaded. The state [1, 0] is also not valid.

The FULLACCESS keys are stored in data memory in ***Security:Full Access Key Step 1*** and ***Security:Keys:Full Access Key Step 2***. The access keys are changed during operation using the *0x0035 SECURITY_KEYS()* subcommand. This subcommand enables a R/W of the 2 key words (4 bytes). Each word is sent in little endian order using this subcommand.

When using the codes by writing them to 0x3E and 0x3F, they must be sent in little endian order; therefore, if 0x1234 and 0x5678 are written as the FULLACCESS codes to *0x0035 SECURITY_KEYS()*, then to unseal requires writing 0x34 and 0x12 to 0x3E and 0x3F, followed by writing 0x78 and 0x56 to 0x3E and 0x3F. The two codes must be written within 5 s of each other to succeed.

To read the keys (only available in FULLACCESS mode, assume for example the keys are 0x1234 0x5678):

1. Write 0x35 and 0x00 to 0x3E and 0x3F
2. Read back 4 bytes from the transfer buffer at 0x40–0x43 (for example, 0x34 0x12 0x78 0x56).

To write the keys (only available in FULLACCESS mode):

1. Write 0x35 and 0x00 to 0x3E and 0x3F.
2. Write the data in little endian format to the transfer buffer at 0x40–0x43 (for example, 0x34 0x12 0x78 0x56).
3. Write the checksum to 0x60. The checksum is calculated by inverting the modulo-256 sum of the data and command bytes (for example, 0xB6).
4. Write the length of 0x08 to 0x61. The length includes the command, data, checksum, and length bytes.

To set the device into SEALED mode when initially powering up, the ***Security:Security Settings[SEAL]*** configuration bit must be programmed into OTP. During operation, a device in FULLACCESS mode can be put into SEALED mode by sending the *0x0030 SEAL()* subcommand.

The BQ76905 device includes additional means to limit further modification of device settings. If the ***Security:Security Settings[LOCK_CFG]*** configuration bit is set, the data memory settings can no longer be modified when the device exits CONFIG_UPDATE mode. If the ***Security:Security Settings[PERM_SEAL]*** bit is set, the device cannot be unsealed after it has been sealed. If these bits are not set in OTP, the settings are lost on a full reset and the device is again able to unseal and modify data memory.

5.1 Voltage Measurement

The BQ76905 device integrates a voltage ADC which is multiplexed between measurements of cell voltages, an internal temperature sensor, the TS pin, and also performs measurements of the voltage at the VC5 pin, the internal 1.8-V LDO (REG18) voltage, and the VSS rail (for diagnostic purposes). The BQ76905 device supports measurement of individual differential cell voltages in a series configuration, ranging from 2 series cells to 5 series cells. Each cell voltage measurement is a differential measurement of the voltage between two adjacent cell input pins, such as VC1-VC0, VC2-VC1, and so forth. The cell voltage measurements are processed based on trim corrections, and then reported in 16-bit resolution using units of 1 mV. The cell voltage measurements can support a recommended voltage range from -0.2 V to 5.5 V. The voltage ADC saturates at a level of 5 × VREF1 (approximately 5.98 V) when measuring cell voltages, although for best performance it is recommended to stay at a maximum input of 5.5 V.

The 16-bit cell and VC5 (Stack), VSS pin, and REG18 voltage measurements are available by using the commands listed below.

Table 5-1. Commands to Read 16-Bit Voltage Measurements

Command	Name	Unit
0x14 and 0x15	Cell 1 Voltage	mV
0x16 and 0x17	Cell 2 Voltage	mV
0x18 and 0x19	Cell 3 Voltage	mV
0x1A and 0x1B	Cell 4 Voltage	mV
0x1C and 0x1D	Cell 5 Voltage	mV
0x22 and 0x23	REG18 Voltage	16-bit ADC codes
0x24 and 0x25	VSS Voltage	16-bit ADC codes
0x26 and 0x27	Stack (VC5 pin) voltage	1 mV (unsigned)
0x28 and 0x29	Int Temperature	°C
0x2A and 0x2B	TS Measurement	16-bit ADC codes

5.1.1 Voltage Measurement Schedule

Overview

The voltage ADC and associated mux operates on a measurement loop in order to implement all its required measurements. The schedule is different in NORMAL versus SLEEP mode (there are no measurements in DEEPSLEEP or SHUTDOWN modes).

NORMAL Mode Scheduling

The measurement loop in NORMAL mode consists of a fast ADSCAN loop, which consists of up to 6 separate measurement slots. The width of the measurement slots is independently programmable based on the category of measurement - cell voltage measurement vs other measurements. By programming the width of the slot, the effective resolution of the ADC conversion changes with it. The slot width is programmable as 366 µs (fastest but lowest resolution), 732 µs, 1.46 ms, or 2.93 ms (slowest but highest resolution). The schedule of

conversions while in NORMAL mode is described in the tables below. If a device is configured to use fewer than the maximum number of supported series cells (such as the device being used in a 3s system), the schedule is shortened accordingly. This results in the number of slots in an ADSCAN in NORMAL mode being (number of cells used) + 1.

Table 5-2. NORMAL Mode Voltage ADC ADSCAN Measurement Loop (setup for a 5s configuration)

Slot Number	Selected Input
0	Cell-1 Voltage
1	Cell-2 Voltage
2	Cell-3 Voltage
3	Cell-4 Voltage
4	Cell-5 Voltage
5	Shared Slot

Table 5-3. NORMAL Mode Voltage ADC ADSCAN Measurement Loop (setup for a 2s configuration)

Slot Number	Selected Input
0	Cell-1 Voltage
1	Cell-2 Voltage
2	Shared Slot

The additional measurements that are less speed critical use the Shared Slot, which rotates through a series of five less frequent measurements. The completion of one full rotation through all five of these less frequent measurements (one per ADSCAN loop) is termed a FULLSCAN loop. The items measured in the FULLSCAN using the Shared Slot are shown in the table below. This schedule uses 5 ADSCANs to complete one FULLSCAN to provide updated data for all less frequent measurements. The timing of a FULLSCAN loop depends on the timing of the ADSCAN loop and can range from approximately 5.5 ms to approximately 88 ms (and longer based on the ***LOOP_SLOW*** settings described below).

Table 5-4. NORMAL Mode Voltage Schedule - FULLSCAN Shared Slot Usage

Shared Slot Usage	Description
TS	Measurement of TS pin voltage, which can be configured in thermistor mode (with internal pullup enabled and using internal 1.8-V LDO as reference) or general purpose ADCIN mode (with internal pullup disabled and using bandgap reference)
Internal Temperature	Measurement of delta-VBE
Stack	Top of stack voltage (VC5 pin) vs VSS, using resistive divider only switched on during measurement.
VREF	Measurement of the internal REG18 LDO voltage
VSS	Measurement of the VSS pin voltage

The measurement of the internal REG18 LDO voltage (which is set based on VREF2) provides an output code given by REG18 × 32768 × 2 / 5 / VREF1, which results in a nominal value of 19228.

The BQ76905 also includes an option to slow the measurement loop if active power dissipation is more important than speed of data availability. The loop can be slowed by up to 8x in NORMAL mode using the ***Settings:Configuration:Power Config[LOOP_SLOW[1:0]]*** bits, which cause the voltage ADC to insert idle slots to effectively slow the average conversion speed and thus reduces the device's average power dissipation. See below for how these bits control the schedule. The idle slots are inserted in a contiguous group at the end of each active ADSCAN, not interleaved between each active conversion slot, to ensure that cell voltage measurements are taken as closely together as possible. The ***LOOP_SLOW*** setting does not affect the schedule during SLEEP mode.

Table 5-5. LOOP_SLOW Speed Control

LOOP_SLOW[1]	LOOP_SLOW[0]	Loop Speed
0	0	Loop runs at full speed
0	1	Loop runs at half speed (one idle slot included for each active slot)
1	0	Loop runs at quarter speed (three idle slots included for each active slot)
1	1	Loop runs at eighth speed (seven idle slots included for each active slot)

SLEEP Mode Scheduling

When the device is in SLEEP mode, measurements are only taken in a burst every ***Power:Sleep:Voltage Time*** interval. Between these bursts, the ADC remains idle, to save power. When the timer expires, the device takes all measurements in a long burst. These are implemented as shown in the table below. When fewer than 5 cells are being used, the unused cell voltage slots are removed. This results in the SLEEP schedule length in slots = 5 + (number of cells used).

Table 5-6. SLEEP Mode Measurement Schedule (all 5 cells used)

Slot	Description
0	Cell-1 Voltage
1	Cell-2 Voltage
2	Cell-3 Voltage
3	Cell-4 Voltage
4	Cell-5 Voltage
5	TS pin measurement
6	Internal Temperature measurement
7	Stack measurement
8	REG18 measurement
9	VSS measurement

When a burst measurement is complete, the device sets the ADSCAN and FULLSCAN bits in *Alarm Raw Status()* momentarily.

When the device exits SLEEP mode (whether through current detection or command or a protection), it immediately runs a SLEEP mode burst measurement to collect updated data, then begins the NORMAL mode schedule. If a burst measurement is already in progress when the exit is triggered, that burst is completed and then the device begins the NORMAL mode schedule.

Startup Mode Scheduling

When the device first boots from SHUTDOWN or exits DEEPSLEEP or CONFIG_UPDATE modes, a special fast startup schedule is used, which is similar to the SLEEP mode schedule, but with fixed OSR settings, as shown below. This schedule results in approximately 6 ms ADC conversion time, in addition to the time required for the REG18 LDO to power up from SHUTDOWN. The device then transitions to evaluating the protections, so the FETs can be enabled as quickly as possible. This measurement loop and evaluation completion trigger the INITCOMP bit in *Alarm Raw Status()*. If the host intends to manually enable the FET drivers, it can monitor this signal to determine when the startup data is available for reading.

Table 5-7. Startup Mode Measurement Schedule (5s version)

Slot	Description	ADC OSR
0	Cell-1 Voltage	96
1	Cell-2 Voltage	96
2	Cell-3 Voltage	96
3	Cell-4 Voltage	96

Table 5-7. Startup Mode Measurement Schedule (5s version) (continued)

Slot	Description	ADC OSR
4	Cell-5 Voltage	96
5	TS pin measurement	384
6	Internal Temperature measurement	384
7	Stack measurement	96
8	REG18 measurement	96
9	VSS measurement	96

If the device has been configured for a fewer number of cells being used (such as configured for use with only 2 cells being used), the startup sequence is shortened by skipping unused cell measurements. If the device is powering from SHUTDOWN mode, it determines the cell configuration based on the settings read in from OTP. If the device is exiting DEEPSLEEP or CONFIG_UPDATE mode, it uses the cell configuration information previously loaded, either from OTP at power up or modified by the host.

5.1.2 Unused VC Cell Input Pins

If the BQ76905 device is used in a system with fewer than 5 series cells, specific cells must be used for connection to real cells, as shown in Table 5-8. Short out the unused cell inputs on the circuit board. The device only measures and reports those cells designated as real cells. For example, if only two cells are used (which requires cell-1 connected between VC1 - VC0, and cell-2 connected between VC5 - VC4A), the *0x12 Cell 1 Voltage()* command reports the lower cell voltage, while the *0x14 Cell 2 Voltage()* command reports the upper cell voltage.

Table 5-8. Cell Usage

Number of Cell Used (*Vcell Mode* setting)	Cell Connections	Shorted Cells
0, 1, or ≥ 5	VC5–VC4A, VC4B–VC3A, VC3B–VC2, VC2–VC1, VC1–VC0	VC4A–VC4B, VC3A–VC3B
4	VC5–VC4A, VC4B–VC3A, VC2–VC1, VC1–VC0	VC4A–VC4B, VC3A–VC3B, VC3B–VC2
3	VC5–VC4A, VC2–VC1, VC1–VC0	VC4A–VC4B, VC4B–VC3A, VC3A–VC3B, VC3B–VC2
2	VC5–VC4A, VC1–VC0	VC4A–VC4B, VC4B–VC3A, VC3A–VC3B, VC3B–VC2, VC2–VC1

Note

It is important that the differential input for each cell input not fall below –0.3 V (the Absolute Maximum data sheet limit), with the recommended minimum voltage of –0.2 V. Therefore, it is important that the I·R voltage drop across the interconnect resistance does not cause a violation of this requirement.

Short the unused cell input pins to adjacent cell input pins, as shown in Figure 5-1.

It is also important to note that the range of voltages supported by the different VC pins differs depending on the pin. For example, pins VC5, VC4A, and VC4B can only support measurements if their pin voltage is greater than or equal to 2 V. Thus if implementing a 2s system using the top and bottom cell input pins, the upper cell voltage is not measured correctly if the lower cell voltage drops below 2 V, because then VC4A is below 2 V.

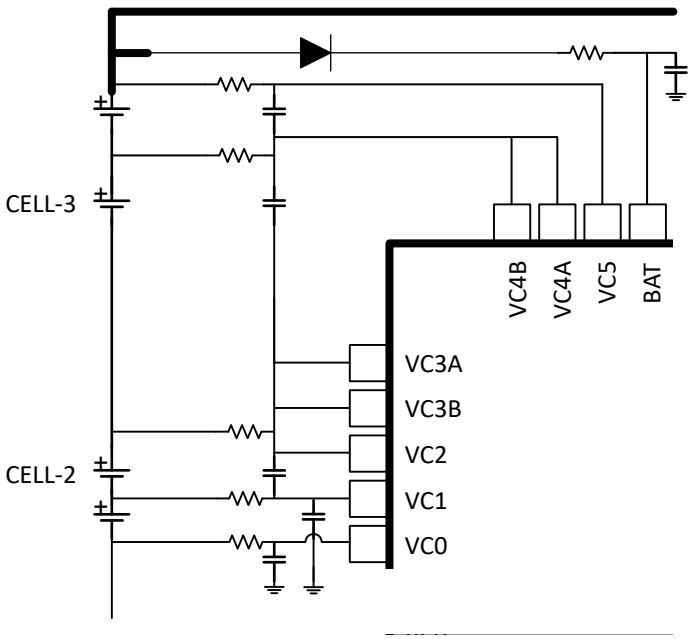

Figure 5-1. Connecting an Unused Cell Input Pin

The ***Settings:Configuration:Vcell Mode*** data memory setting is used to specify which cell inputs are used for actual cells. The device uses this information to disable cell voltage protections associated with inputs which are not used. Voltage measurements are reported in 16-bit format (in units of mV) only for inputs used for real cells.

5.1.3 General Purpose ADCIN Functionality

The TS pin on the BQ76905 device can be used for general purpose ADC input (ADCIN) measurement, if not being used for temperature measurement of a thermistor. When used for ADCIN functionality, the internal VREF1 reference is used by the ADC, and the input range of the ADC is limited to 1.8 V. The digital full-scale range of the ADC is effectively 1.6667 × VREF1, which is approximately 2 V during normal operation.

The ***Settings:Configuration:DA Config[TSMODE]*** data memory bit controls whether the TS pin is used for a thermistor or as a general purpose ADC input. The resulting measurement of the TS pin is available using the *TS Measurement()* command in units of 16-bit ADC counts. The LSB size of the ADC counts is given by VREF1 × 5 / 3 / 32768 ≅ 61 µV.

5.2 Coulomb Counter and Digital Filters

The BQ76905 device monitors pack current using a low-side sense resistor that connects to the SRP and SRN pins through an external RC filter, which must be connected such that a charging current creates a positive voltage on SRP relative to SRN. The device supports a wide range of sense resistor values, such as 1 mΩ or below. The differential voltage between SRP and SRN is digitized by a dedicated integrated coulomb counter ADC, which can digitize voltages over a ±200 mV range. The pins can also support higher positive voltages relative to VSS, which can occur during overcurrent or short circuit in discharge conditions, without damage to the device, although the current is not accurately digitized in this case.

Current Measurement Data

The coulomb counter provides two digital outputs, one of which uses the CC2 digital filter, which generates a 24-bit raw output. The timing and resolution of the CC2 output is programmable, with the output rate also affecting the resolution of the conversion. The effective resolution (defined as the resolution such that the data exhibits 1-sigma variation with ±1 LSB) of the coulomb counter conversions increases with longer conversion time. The conversion time options when the coulomb counter is in full power mode are 366 µs (which results in 13-bit effective resolution), 732 µs (14-bit effective resolution), 1.46 ms (15-bit effective resolution), or 2.93 ms (16-bit

effective resolution). This conversion time is set using the ***Settings:Configuration:DA Config[IADCSPEED1:0]*** configuration bits. In addition, the coulomb counter supports a low power mode, which operates at a 16 times slower rate than the settings listed above, with similar resolution performance at each setting, but with supply current reduced by approximately 55 µA.

This 24-bit CC2 value is reported in the *0x36 Raw Current()* command. This command provides 24 bits of data in the LSBs, which is sign-extended to generate the upper 8 bits of the 32-bit field. While this data provides additional resolution for current measurement if desired,there can be considerable noise in the lower bits, so the data might need further filtering by the host before use. The 32-bit current data has an LSB value of approximately VREF2 / (5 × 2^{23}) ≅ 1.227 V / (5 × 2^{23}) ≅ 29 nV. Note that the data provided by the *0x36 Raw Current()* command is not processed for offset or gain correction.

The 24-bit raw coulomb counter output is further processed, with the result reported in 16-bit format by the *0x3A Current()* command in units of 16-bit userA. The processing consists of first subtracting an offset value (***Calibration:Current:Curr Offset***) from the 24-bit raw ADC result, then multiplying that result by a gain factor (***Calibration:Current:Curr Gain***), dividing the result by 8192, and rounding to 16-bits. The default values of ***Calibration:Current:Curr Offset*** and ***Calibration:Current:Curr Gain*** are trimmed and stored in OTP by TI during manufacturing to provide the final value of *0x3A Current()* in units of mA, assuming a 1 mΩ sense resistor is used. The device loads the trim values to use during operation; the values in use can also be modified by the host in CONFIG_UPDATE mode if desired.

If a different sense resistor value is used, the host can modify the value of ***Calibration:Current:Curr Gain*** to adjust the units of the *0x3A Current()* command, depending on the range of currents expected in the system. Thus the units of each LSB are termed "userA" based on the gain setting. Since the *0x3A Current()* command reports signed 16-bit data, units of mA would only allow reporting of currents between -32768 mA and +32767 mA. If larger currents are expected, then the gain can be adjusted to set the LSB userA to a different value, such as 10 mA or 100 mA, which then allows reporting of currents between -327.68 A and +327.67 A (if userA = 10 mA) or between -3276.8 A and +3276.7 A (if userA = 100 mA).

The device also reports a 16-bit current which is measured primarily for charge integration purposes in *0x3C CC1 Current()*, with units adjustable in similar fashion as the *0x3A Current()*. In this case, the raw data is 16-bit, so the processing consists of first subtracting an offset value (***Calibration:Current:CC1 Offset*** / 256) from the 16-bit raw ADC result, then multiplying that result by a gain factor (***Calibration:Current:CC1 Gain***), dividing the result by 32, and rounding to 16-bits. The default values of ***Calibration:Current:CC1 Offset*** and ***Calibration:Current:CC1 Gain*** are trimmed and stored in OTP by TI during manufacturing to provide the final value of *0x3C CC1 Current()* in units of mA, assuming a 1 mΩ sense resistor is used. The device loads the trim values to use during operation; the values in use can also be modified by the host in CONFIG_UPDATE mode if desired.

The *0x3C CC1 Current()* only operates in NORMAL mode, and generates a sample every 250 ms when the coulomb counter is in full power mode, or every 4 seconds in low power mode (as determined by the ***Settings:Configuration:DA Config[CCMODE1:0]*** setting). The *0x3C CC1 Current()* is used to decide when the device enters SLEEP mode and for accumulated charge integration.

Body Diode Protection

The BQ76905 supports both series and parallel FET configurations. When the CHG and DSG FETs are in series, current can flow through the body diode of a disabled FET when the other FET is enabled. In this configuration, body diode protection is used to turn the disabled FET on when current above a threshold is detected to be flowing through that FET. When the system has separate DSG and CHG paths and parallel FETs, body diode protection is not needed and can be disabled by clearing the ***Settings:Configuration:FET Options[SFET]*** configuration bit.

The body diode protection is implemented in most cases using the digitized current data from the coulomb counter. Except for special cases, the device compares the absolute value of *0x3A Current()* to the body diode protection threshold given by ***Settings:Protection:Body Diode Threshold***. If one FET is disabled and one is

enabled, and the absolute value of *0x3A Current()* exceeds the threshold, and ***[SFET]*** = 0x1, then the disabled FET is enabled.

If ***Settings:Configuration:DA Config[CCMODE1:0]*** = 0x3, then the body diode protection instead uses the wake detector signal to decide whether or not to enable the disabled FET. This means the device uses the wake detector threshold for the body diode protection in these cases, so ***Settings:Protection:Body Diode Threshold*** is not used.

In order to avoid rapid cycling of a FET driver when the current is near the threshold, the FET enabled by body diode protection is not disabled again due to unneeded body diode protection until after a hysteresis time of approximately 240 ms has passed since the FET was initially enabled. This hysteresis does not apply if a protection fault occurs and the device is configured to disable the FET, or if a command to manually disable the FET is sent. In these cases the FET turns off immediately without observing the hysteresis.

Current Measurement Schedule

The schedule for current measurements depends on programmable settings as well as the operating mode of the device (such as whether the device is in SLEEP mode versus NORMAL mode). This programmability, which uses the ***Settings:Configuration:DA Config[CCMODE1:0]***, allows the power dissipation of the device to be reduced if fast current measurements are not required in the system.

Table 5-9. Coulomb Counter Mode Control (*Settings:Configuration:DA Config[CCMODE1:0]*)

CCMODE[1]	CCMODE[0]	Description
0	0	NORMAL mode: Coulomb counter runs continuously, independent of the ***LOOP_SLOW*** or ***CB_LOOP_SLOW*** setting. SLEEP mode: Coulomb counter runs continuously while the voltage ADC is running in SLEEP mode during a burst measurement. It stops at the conclusion of the CC2 measurement underway when the burst measurement completes. Startup mode (at initial powerup from SHUTDOWN or exit of DEEPSLEEP or CONFIG_UPDATE mode): Coulomb counter runs continuously while the voltage ADC is running during the Startup Sequence. It stops at the conclusion of the CC2 measurement underway when the Startup Sequence completes. *0x3C CC1 Current()* and accumulated charge and time integration are updated in NORMAL mode but not in SLEEP mode. Body diode protection uses the coulomb counter CC2 digitized current data.
0	1	NORMAL mode: Coulomb counter runs continuously if ***LOOP_SLOW*** or ***CB_LOOP_SLOW*** is set to the fastest setting. When these parameters are modified to slower settings, the device inserts 1, 3, or 7 idle slots between each current measurement slot, thereby reducing the average output rate of the current measurements. SLEEP mode: Coulomb counter runs continuously while the voltage ADC is running in SLEEP mode during a burst measurement. It stops at the conclusion of the CC2 measurement underway when the burst measurement completes. Startup mode (at initial powerup from SHUTDOWN or exit of DEEPSLEEP or CONFIG_UPDATE mode): Coulomb counter runs continuously while the voltage ADC is running during the Startup Sequence. It stops at the conclusion of the CC2 measurement underway when the Startup Sequence completes. *0x3C CC1 Current()* and accumulated charge and time integration are only updated when in NORMAL and not using a mode that inserts idle slots into the voltage measurement schedule. These are not updated in SLEEP mode. Body diode protection uses the coulomb counter CC2 digitized current data.

Table 5-9. Coulomb Counter Mode Control (*Settings:Configuration:DA Config[CCMODE1:0]*) (continued)

CCMODE[1]	CCMODE[0]	Description
1	0	NORMAL mode: Coulomb counter runs continuously in low power mode (CC1 and CC2 measurements take 16x longer versus in regular full power mode) SLEEP mode: Coulomb counter takes one CC2 measurement at the beginning of each burst measurement using low power mode. Startup mode (at initial powerup from SHUTDOWN or exit of DEEPSLEEP): Coulomb counter takes one CC2 measurement using low power mode at the beginning of the Startup Sequence. *0x3C CC1 Current()* and accumulated charge and time integration are only updated with this setting while in NORMAL mode, they are not updated in SLEEP mode. The *0x3C CC1 Current()* and charge integration is updated every approximately 4 seconds in NORMAL mode using this setting, due to the slower clock rate. The charge integration scales the CC1 Current appropriately when accumulating, to maintain the same units of userA-seconds. Body diode protection uses the coulomb counter CC2 digitized current data.
1	1	Coulomb counter is powered down and does not operate at all. This provides a low power mode if current measurement is not needed. *0x3C CC1 Current()* and accumulated charge and time integration are not available in this mode. In this mode, body diode protection is based on the wake comparator detection threshold, which also serves as the detector to enter/exit SLEEP mode.

Charge Integration

When the *0x3C CC1 Current()* is operating, it is integrated to calculate the accumulated passed charge, with the integrated charge available as a signed 48-bit value from the *0x0004 PASSQ()* subcommand. The first 32-bits contains the 32 LSBs of the accumulated charge in units of userA-seconds, and the next 32-bits contain the upper 16 bits of the 48-bit result sign-extended to fill the 32-bit field. In addition, a timer value with units of 250 ms is available in a 32-bit value from the subcommand, which counts the time the device is in NORMAL mode since the integrator was reset. Neither the time nor the charge integration operate in SLEEP, DEEPSLEEP, or SHUTDOWN modes, only in NORMAL mode and based on the setting of ***Settings:Configuration:DA Config[CCMODE1:0]***. The integrator and timer is reset by sending the *0x0005 RESET_PASSQ()* subcommand. These are also reset upon entering CONFIG_UPDATE mode. When the coulomb counter is in low power mode, it only generates a CC1 current output every 4 seconds, so the charge and time integration is also updated at these intervals. The integration of *0x3C CC1 Current()* is scaled accordingly when in low power mode, to provide accumulated charge using the same units of userA-seconds as in full power mode.

Table 5-10. Accumulated Charge and Time (from *PASSQ()* subcommand)

Subcommand Address	Bytes within Block	Name	Units
0x0004	0 - 3	Accumulated charge lower 32-bits (little-endian)	Lower 32 bits of signed 48-bit result, with the full 48-bit field having units of userA-seconds
	4 - 7	Accumulated charge upper 16-bits sign-extended to a 32-bit field (little-endian)	Upper bits of signed 48-bit result, with the full 48-bit field having units of userA-seconds
	8 - 11	Accumulated Time (little-endian)	32-bit unsigned integer in units of 250 ms

5.3 Internal Temperature Measurement

The BQ76905 device integrates the capability to measure its internal die temperature by digitizing the difference between two internal transistor base-emitter voltages. This voltage difference is measured periodically as part of the measurement loop and is processed to provide a temperature value using the *0x28 Int Temperature()* command in units of °C. This resulting value is used by several protections and decisions within the device, such as the Internal Overtemperature Protection, internal overtemperature shutdown (based on ***Power:Shutdown:Shutdown Temperature***, and cell balancing (based on ***Settings:Cell Balancing:Max Internal Temp***).

The calculation of temperature is performed as follows using the ***Calibration:Temperature:Int Temp Offset*** and ***Calibration:Temperature:Int Temp Gain*** configuration parameters:

$$Int\ Temperature() = \frac{[\ (\text{16-bit ADC counts}) - (\textbf{\textit{Int Temp Offset}})\ ] \times (\textbf{\textit{Int Temp Gain}})}{65536}$$

5.4 Thermistor Temperature Measurement

The BQ76905 device includes an on-chip temperature measurement and can also support measurement of an external thermistor on the TS pin. The device includes an internal trimmed 20-kΩ pullup resistor to bias the thermistor during measurement. The TS pin can be selected for thermistor measurement or general purpose ADCIN measurement using the ***Settings:Configuration:DA Config[TSMODE]*** data memory setting.

When the pin is selected for thermistor measurement, the internal pullup resistor is used to bias the pin during the measurement. In order to provide a high precision result, the device uses the same 1.8 V internal LDO voltage for the ADC reference as is used for biasing the thermistor pullup resistor, thereby implementing a ratiometric measurement that removes the error contribution from the LDO voltage level. Because the pullup resistor is only enabled during the pin measurement, it is recommended to limit the capacitance at this node to less than 4 nF to reduce the effect of incomplete settling when the pullup resistor is biased.

If the pin is selected for general purpose ADCIN measurement, the pullup resistor is not enabled during measurement, and the ADC uses VREF1 for its reference when measuring the pin.

The data is reported using the *TS Measurement()* command, in units of 16-bit ADC counts. The full-scale digital value reflects an analog input level of its reference × 5 / 3. So when the TS pin is measuring a thermistor in ratiometric mode using the 1.8V internal regulator for its reference, the 16-bit LSB is 1.8 V × 5 / 3 / 32768 ≅ 92 µV. When the TS pin is measuring in ADCIN mode using the VREF1 reference, the 16-bit LSB is 1.1962 V × 5 / 3 / 32768 ≅ 61 µV. The processing performed on the ADC data before reporting is shown below, using the ***Calibration:Temperature:TS Offset*** data memory parameter.

$$TS\ Measurement() = (\text{16-bit ADC counts}) - (\textbf{\textit{TS Offset}})$$

5.5 Measurement Calibration

The BQ76905 device includes optional capability for the customer to calibrate offset and gain for the cell voltage measurement, the current measurement, and the internal temperature measurement. It also supports gain calibration for the top-of-stack (TOS) voltage measurement and offset calibration for the TS pin measurement. Table Table 5-11 shows the calibration configuration values provided.

Table 5-11. Calibration Configuration Settings

Name	Description
Calibration:Voltage:Cell 1 Gain	Cell 1 voltage gain calibration value in unsigned 16-bit format
Calibration:Voltage:Cell 2 Gain Delta	Signed 8-bit value which is added to Cell 1 Gain to obtain the Cell 2 Gain calibration value.
Calibration:Voltage:Cell 3 Gain Delta	Signed 8-bit value which is added to Cell 1 Gain to obtain the Cell 3 Gain calibration value.
Calibration:Voltage:Cell 4 Gain Delta	Signed 8-bit value which is added to Cell 1 Gain to obtain the Cell 4 Gain calibration value.
Calibration:Voltage:Cell 5 Gain Delta	Signed 8-bit value which is added to Cell 1 Gain to obtain the Cell 5 Gain calibration value.
Calibration:Voltage:TOS Gain	Top-of-stack (TOS) voltage gain calibration value in unsigned 16-bit format
Calibration:Current:Curr Offset	Current offset calibration value in units of signed 24-bit ADC counts (this is a 16-bit value, so only has range of +/- full-scale raw current range / 256)
Calibration:Current:Curr Gain	Current gain calibration value in unsigned 16-bit format

Table 5-11. Calibration Configuration Settings (continued)

Name	Description
Calibration:Current:CC1 Offset	CC1 Current offset calibration value in units of signed 24-bit ADC counts (this is a 16-bit value, so only has range of +/- full-scale raw current range / 256)
Calibration:Current:CC1 Gain	CC1 Current gain calibration value in unsigned 16-bit format
Calibration:Temperature:TS Offset	TS measurement offset calibration value in units of signed 16-bit ADC counts.
Calibration:Temperature:Int Temp Offset	Internal temperature offset calibration value in units of signed 16-bit ADC counts
Calibration:Temperature:Int Temp Gain	Internal temperature gain calibration value in unsigned 16-bit format

If the host does not overwrite values for the calibration gain or offset configurations, the BQ76905 device uses the factory trim values stored in OTP for each respective setting. When a calibration configuration value is written, the device uses that in place of the respective factory trim value.

Each cell voltage has an associated Cell # Gain value, which is used to scale the raw ADC result to convert it into units of mV. The ***Cell 1 Gain*** is stored directly in data memory, while the remaining Cell # Gain values for cells 2 to 5 are encoded as a delta value versus the ***Cell 1 Gain*** value, as shown below.

$$Cell\ 2\ Gain = (Cell\ 1\ Gain) + (Cell\ 2\ Gain\ Delta) \quad (1)$$

$$Cell\ 3\ Gain = (Cell\ 1\ Gain) + (Cell\ 3\ Gain\ Delta) \quad (2)$$

$$Cell\ 4\ Gain = (Cell\ 1\ Gain) + (Cell\ 4\ Gain\ Delta) \quad (3)$$

$$Cell\ 5\ Gain = (Cell\ 1\ Gain) + (Cell\ 5\ Gain\ Delta) \quad (4)$$

The BQ76905 uses these calibration values to calculate the reported measurements from the raw ADC data as described below.

$$Cell\ \ 1\ \ Voltage() = \frac{[\,(16 - bit\ ADC\ counts) \times (\text{Cell 1 Gain})\,]}{65536} \quad (5)$$

$$Cell\ \ 2\ \ Voltage() = \frac{[\,(16 - bit\ ADC\ counts) \times (\text{Cell 2 Gain})\,]}{65536} \quad (6)$$

$$Cell\ \ 3\ \ Voltage() = \frac{[\,(16 - bit\ ADC\ counts) \times (\text{Cell 3 Gain})\,]}{65536} \quad (7)$$

$$Cell\ \ 4\ \ Voltage() = \frac{[\,(16 - bit\ ADC\ counts) \times (\text{Cell 4 Gain})\,]}{65536} \quad (8)$$

$$Cell\ \ 5\ \ Voltage() = \frac{[\,(16 - bit\ ADC\ counts) \times (\text{Cell 5 Gain})\,]}{65536} \quad (9)$$

$$Stack\ Voltage() = \frac{(16 - bit\ ADC\ counts) \times (\text{TOS Gain})}{16384} \quad (10)$$

$$TS\ Measurement() = (16 - bit\ ADC\ counts) - (\text{TS Offset}) \quad (11)$$

$$Int\ Temperature() = \frac{[\,(16 - bit\ ADC\ counts) - (\text{Int Temp Offset})\,] \times (\text{Int Temp Gain})}{65536} \quad (12)$$

$$CC1\ Current() = \frac{[\,(16 - bit\ ADC\ counts) - (\text{CC1 Offset} / 256)\,] \times (\text{CC1 Gain})}{32} \quad (13)$$

$$Current() = \frac{[\,(24 - bit\ ADC\ counts) - (\text{Curr Offset})\,] \times (\text{Curr Gain})}{8192} \quad (14)$$

The cell voltage calibration is implemented by writing the ***Calibration:Voltage:Cell 1 Gain*** value to 65535 and all ***Calibration:Voltage:Cell # Gain Delta*** values to 0, then applying two precise DC voltages to a cell input (such as 2.5 V and 4.5 V) and averaging multiple raw ADC measurements in 16-bit counts obtained from the *Cell # Voltage()* command for each voltage. The gain is then calculated as:

$$Cell\ \#\ Gain = \frac{65536 \times (Voltage1_{in\ mV} - Voltage2_{in\ mV})}{(16 - bit\ ADC\ Counts)_{Voltage1} - (16 - bit\ ADC\ Counts)_{Voltage2}} \quad (15)$$

The calibration for the TOS measurement gain is implemented by similarly writing the ***Calibration:Voltage:TOS Gain*** value to 16384, then applying two precise DC voltages to the VC5 pin and averaging multiple raw ADC measurements in 16-bit counts obtained from the *0x26 Stack Voltage()* command. Note: one of the voltages can be skipped to reduce calibration time. The gain is then calculated as:

$$TOS\ Gain = \frac{16384 \times (Voltage1_{in\ mV} - Voltage2_{in\ mV})}{(16 - bit\ ADC\ Counts)_{Voltage1} - (16 - bit\ ADC\ Counts)_{Voltage2}} \quad (16)$$

The calibration for the TS pin measurement offset is implemented by similarly first writing the ***Calibration:Temperature:TS Offset*** value to zero. A precise DC voltage can be applied to the TS pin, and the 16-bit ADC counts obtained from the *0x6A TS Measurement()* command. The offset is then calculated as:

$$TS\ Offset = (16 - bit\ ADC\ Counts)_{TS\_Voltage} - \frac{32768 \times 3 \times (TS\_Voltage_{in\ V})}{VREF1 \times 5} \quad (17)$$

Although it is typically not practical in a production environment, the Internal Temperature measurement can be calibrated by first writing the ***Calibration:Temperature:Int Temp Gain*** value to 65535 and ***Calibration:Temperature:Int Temp Offset*** value to zero, then exposing the system to two precise temperatures and averaging multiple raw ADC measurements in 16-bit counts obtained from the *Int Temperature()* command for each temperature. The gain is then calculated as:

$$Int\ Temp\ Gain = \frac{65536 \times (Temp\_1_{in\ °C} - Temp\_2_{in\ °C})}{(16 - bit\ ADC\ Counts)_{Temp\_1} - (16 - bit\ ADC\ Counts)_{Temp\_2}} \quad (18)$$

The offset for the Internal Temperature measurement is calculated using this new value of ***Calibration:Temperature:Int Temp Gain*** as shown below:

$$Int\ Temp\ Offset = (16 - bit\ ADC\ Counts)_{Temp\_1} - \frac{65536 \times (Temp\_1_{in\ °C})}{Int\ Temp\ Gain} \quad (19)$$

The *0x3A Current()* current measurement can be calibrated by applying two precise DC currents and averaging multiple raw ADC measurements in 24-bit counts obtained from the *0x36 Raw Current()* command for each current. The *0x3C CC1 Current()* current measurement, which is used to calculate the charge integration data available from the *0x0004 PASSQ()* command, can be calibrated by applying two precise DC currents and

averaging multiple raw ADC measurements in 16-bit counts obtained from the *0x3C CC1 Current()* command for each current, while the value of ***Calibration:Current:CC1 Gain*** is set to 32.

These gains are then calculated as:

$$CC1\ Gain = \frac{32 \times (Current\_1_{in\ mA} - Current\_2_{in\ mA})}{(16-bit\ ADC\ Counts)_{Current\_1} - (16-bit\ ADC\ Counts)_{Current\_2}} \quad (20)$$

$$Curr\ Gain = \frac{8192 \times (Current\_1_{in\ mA} - Current\_2_{in\ mA})}{(24-bit\ ADC\ Counts)_{Current\_1} - (24-bit\ ADC\ Counts)_{Current\_2}} \quad (21)$$

then quantizing to an integer.

While a current measurement offset ***Calibration:Current:Curr Offset*** can be calculated using one of the two currents measured earlier, a more practical approach is to set the current to zero, and use the average of multiple raw ADC measurements in 24-bit counts obtained from the *0x36 Raw Current()* command as ***Calibration:Current:Curr Offset***, which uses the 16 LSBs from this calculation. The value for ***Calibration:Current:CC1 Offset*** can be obtained by setting the ***Calibration:Current:CC1 Gain*** to 32 and summing 256 samples of *0x3C CC1 Current()*.

A table of example gains and resulting LSB values for various sense resistor values and maximum current levels is shown below (with gains quantized to ensure support for the Max Current listed).

Table 5-12.

Rsense (µΩ)	Max Current (A)	Max Voltage (V)	Min LSB Allowed (mA)	Quantized CC1 Gain	Quantized Current Gain	Quantized CC1 LSB (mA)	Quantized Current LSB (mA)
5000	3	0.015000	0.091553	524	524	0.091618	0.091618
5000	15	0.075000	0.457764	104	104	0.461614	0.461614
5000	40	0.200000	1.220703	39	39	1.230970	1.230970
2000	10	0.020000	0.305176	393	393	0.305393	0.305393
2000	50	0.100000	1.525879	78	78	1.538712	1.538712
2000	100	0.200000	3.051758	39	39	3.077424	3.077424
1000	32.767	0.032767	0.999969	240	240	1.000163	1.000163
1000	50	0.050000	1.525879	157	157	1.528911	1.528911
1000	100	0.100000	3.051758	78	78	3.077424	3.077424
1000	200	0.200000	6.103516	39	39	6.154848	6.154848
500	32.767	0.016384	0.999969	480	480	1.000163	1.000163
500	100	0.050000	3.051758	157	157	3.057822	3.057822
500	250	0.125000	7.629395	62	62	7.743196	7.743196
500	400	0.200000	12.207031	39	39	12.309696	12.309696
250	32.767	0.008192	0.999969	960	960	1.000163	1.000163
250	100	0.025000	3.051758	314	314	3.057822	3.057822
250	250	0.062500	7.629395	125	125	7.681250	7.681250
250	800	0.200000	24.414063	39	39	24.619391	24.619391
100	32.767	0.003277	0.999969	2400	2400	1.000163	1.000163
100	100	0.010000	3.051758	786	786	3.053932	3.053932
100	200	0.020000	6.103516	393	393	6.107864	6.107864
100	327.67	0.032767	9.999695	240	240	10.001628	10.001628
100	500	0.050000	15.258789	157	157	15.289112	15.289112
100	1000	0.100000	30.517578	78	78	30.774239	30.774239
100	2000	0.200000	61.035156	39	39	61.548478	61.548478

Table 5-12. (continued)

Rsense (µΩ)	Max Current (A)	Max Voltage (V)	Min LSB Allowed (mA)	Quantized CC1 Gain	Quantized Current Gain	Quantized CC1 LSB (mA)	Quantized Current LSB (mA)
50	32.767	0.001638	0.999969	4800	4800	1.000163	1.000163
50	100	0.005000	3.051758	1573	1573	3.051991	3.051991
50	250	0.012500	7.629395	629	629	7.632403	7.632403
50	1000	0.050000	30.517578	157	157	30.578225	30.578225
50	2000	0.100000	61.035156	78	78	61.548478	61.548478
50	4000	0.200000	122.070313	39	39	123.096955	123.096955
10	32.767	0.000328	0.999969	24003	24003	1.000038	1.000038
10	100	0.001000	3.051758	7865	7865	3.051991	3.051991
10	250	0.002500	7.629395	3146	3146	7.629977	7.629977
10	1000	0.010000	30.517578	786	786	30.539321	30.539321
10	5000	0.050000	152.587891	157	157	152.891123	152.891123
10	10000	0.100000	305.175781	78	78	307.742388	307.742388
10	20000	0.200000	610.351563	39	39	615.484776	615.484776

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Chapter 6

Protection Subsystem

6.1 Protections Overview

The BQ76905 integrates an extensive protection subsystem which can monitor a variety of parameters, initiate protective actions, and autonomously recover based on conditions. The device also includes a wide range of flexibility, such that the device can be configured to monitor and initiate protective action, but with recovery controlled by the host processor, or such that the device only monitors and alerts the host processor whenever conditions warrant protective action, but with action and recovery fully controlled by the host processor. The protection subsystem includes a suite of individual protections that can be individually enabled and configured, as shown in Table 6-1. The current protections are based on comparator thresholds, while most voltage and temperature protections are based on ADC measurements. Some protection checks are primarily for diagnostic purposes, so the device can be autonomously disabled if a malfunction is detected. The device integrates NFET drivers for low-side CHG and DSG protection FETs, which can be configured in a series or parallel configuration. The FET drivers also support PWM modes of operation, which can be used to implement a precharge or predischarge functionality.

Table 6-1. BQ76905 Protections

Protection	Implementation	Description
Cell Undervoltage	ADC measurement	Detects individual cell voltage below programmed threshold
Cell Overvoltage	ADC measurement	Detects individual cell voltage above programmed threshold
Overcurrent in Charge	Analog comparator	Detects charging current above programmed threshold
Overcurrent in Discharge 1 / 2	Analog comparator	Two levels of detection for discharging current beyond programmed thresholds
Short Circuit in Discharge	Analog comparator	Detects discharging current above programmed threshold
Undertemperature in Charge	ADC measurement	Detects thermistor temperature below programmed threshold limit for charging operation
Overtemperature in Charge	ADC measurement	Detects thermistor temperature above programmed threshold limit for charging operation
Undertemperature in Discharge	ADC measurement	Detects thermistor temperature below programmed threshold limit for discharging operation
Overtemperature in Discharge	ADC measurement	Detects thermistor temperature above programmed threshold limit for discharging operation
Internal Overtemperature	ADC measurement	Detects internal device temperature above programmed threshold
REGOUT LDO Check	Analog comparator	Diagnostic check - detects voltage or temperature fault on REGOUT regulator when enabled

Table 6-1. BQ76905 Protections (continued)

Protection	Implementation	Description
Voltage Reference Check	ADC measurement	Diagnostic check which digitizes the internal 1.8V LDO using the ADC and VREF1, and detects any excessive deviation from the expected result
VSS Check	ADC measurement	Diagnostic check on ADC mux - device digitizes VSS and detects any excessive deviation from the expected result
Host Watchdog	Digital logic	Detects absence of host processor communications

The individual protections are enabled by setting the related ***Settings:Protection:Enabled Protections A – B*** data memory configuration registers. Most protections include a programmable threshold, and when the monitored parameter first exceeds the programmed threshold, a protection alert is asserted. After the parameter remains beyond the threshold for a programmable delay period, a protection status fault is asserted (and the alert is deasserted). The protection alerts are provided by the *0x02 Safety Alert A()* and *0x04 Safety Alert B()* commands, while the protection status faults are provided by the *0x03 Safety Status A()* and *0x05 Safety Status B()* commands, as shown below. Most protections also include a programmable recovery criteria, such that if the parameter no longer exceeds the threshold by some margin, the protection status fault is deasserted. Protection alert and status faults can be mapped to provide an interrupt to the host processor on the ALERT pin, using the *0x62 Alarm Status()*, *0x64 Alarm Raw Status()*, and *0x66 Alarm Enable()* commands.

Table 6-2. Format for 0x02 Safety Alert A()

Bit	Name	Description
7	COV	Cell Overvoltage Safety Alert
6	CUV	Cell Undervoltage Safety Alert
5	SCD	Short Circuit in Discharge Safety Alert
4	OCD1	Overcurrent in Discharge 1 Safety Alert
3	OCD2	Overcurrent in Discharge 2 Safety Alert
2	OCC	Overcurrent in Charge Safety Alert
1-0	RSVD0	Reserved

Table 6-3. Format for 0x03 Safety Status A()

Bit	Name	Description
7	COV	Cell Overvoltage Safety Fault
6	CUV	Cell Undervoltage Safety Fault
5	SCD	Short Circuit in Discharge Safety Fault
4	OCD1	Overcurrent in Discharge 1 Safety Fault
3	OCD2	Overcurrent in Discharge 2 Safety Fault
2	OCC	Overcurrent in Charge Safety Fault
1	CURLATCH	Current Protection Latch Safety Fault
0	REGOUT	REGOUT Safety Fault

Table 6-4. Format for 0x04 Safety Alert B()

Bit	Name	Description
7	OTD	Overtemperature in Discharge Safety Alert
6	OTC	Overtemperature in Charge Safety Alert
5	UTD	Undertemperature in Discharge Safety Alert
4	UTC	Undertemperature in Charge Safety Alert
3	OTINT	Internal Overtemperature Safety Alert

Table 6-4. Format for 0x04 Safety Alert B() (continued)

Bit	Name	Description
2	HWD	Host Watchdog Safety Alert
1	VREF	VREF Measurement Diagnostic Alert
0	VSS	VSS Measurement Diagnostic Alert

Table 6-5. Format for 0x05 Safety Status B()

Bit	Name	Description
7	OTD	Overtemperature in Discharge Safety Fault
6	OTC	Overtemperature in Charge Safety Fault
5	UTD	Undertemperature in Discharge Safety Fault
4	UTC	Undertemperature in Charge Safety Fault
3	OTINT	Internal Overtemperature Safety Fault
2	HWD	Host Watchdog Safety Fault
1	VREF	VREF Measurement Diagnostic Fault
0	VSS	VSS Measurement Diagnostic Fault

The thresholds, delays, and recovery criteria are controlled by individual data memory settings in the ***Protections*** class. For example, the Cell Undervoltage Protection is configured using the ***Protections:Cell Voltage:Cell Undervoltage Protection Threshold***, ***Protections:Cell Voltage:Cell Undervoltage Protection Delay***, and ***Protections:Cell Voltage:Cell Undervoltage Protection Recovery Hysteresis*** data memory settings.

The control of the protection FETs in response to a detected protection event is also configurable, with the device able to operate in a fully autonomous mode, a completely manual mode (controlled through host commands over the serial communications bus), or a combination of the two. Autonomous mode is enabled by setting the ***Settings:Configuration:FET Options[FET_EN]*** data memory configuration bit or sending the *0x0022 FET Enable()* subcommand, which toggles the ***[FET_EN]*** bit. The device can operate in a combined autonomous/manual mode, such that the device can operate autonomously when the host processor does not intervene, but still allows the host to override the autonomous decisions and force FETs on or off based on serial communications. This can be attractive in cases where the host needs autonomous reaction to selected faults, such as a short circuit in discharge event, to provide the fastest protection response, but prefer manual control for other faults, such as cell overtemperature or overvoltage faults. The *0x29 FET Control()* command provides manual FET control capability by the host. If the user is concerned about unauthorized or inadvertent manual FET control by a host, these selected commands can be disabled using the ***Settings:Configuration:FET Options[HOST_FETOFF_EN]*** and ***[HOST_FETON_EN]*** data memory configuration settings. Each protection can be configured whether it autonomously disables the pertinent protection FET using the ***Settings:Protection:CHG FET Protections A***, ***Settings:Protection:DSG FET Protections A***, and ***Settings:Protection:Both FET Protections C*** settings.

6.2 Protection FET Drivers

The BQ76905 integrates low-side CHG and DSG FET drivers, which can directly drive low-side protection NFET transistors. The state of the drivers is reported by the *0x12 Battery Status()[CHG]* and *[DSG]* bits. The device supports both series and parallel FET configurations, providing FET body diode protection when configured for a series FET configuration, if one FET driver is on, and the other FET driver is off. In this case, the DSG driver can be turned on to prevent FET damage if the battery pack is charging while the DSG FET is disabled. Similarly, the CHG driver can be turned on if the pack is discharging while the CHG FET is disabled. For more details, see Body Diode Protection.

The device can be configured for fully autonomous operation, in which case the device autonomously enables the protection FETs if no enabled protection status fault is present which has been configured to control the FETs, and no host command has been issued to force the FET off. Autonomous mode is enabled by setting the ***Settings:Configuration:FET Options[FET_EN]*** or sending the *0x0022 FET Enable()* subcommand, which

toggles the ***[FET_EN]*** bit. If ***[FET_EN]*** = 0, the FETs remains disabled until they are manually enabled by command.

Manual FET control is available using the *0x29 FET Control()* command independent of the setting of ***[FET_EN]***. The format of the *0x29 FET Control()* command is shown below. The bits that force the FETs to be enabled are only available if the ***Settings:Configuration:FET Options[HOST_FETON_EN]*** is set, while the bits that force the FETs to be disabled are only available if the ***Settings:Configuration:FET Options[HOST_FETOFF_EN]*** is set.

Table 6-6. Format for *0x29 FET Control()* Command

Bit	Name	Description
7-4	RSVD	Reserved
3	CHG_OFF	CHG FET driver control. This bit only operates if the ***[HOST_FETOFF_EN]*** bit in data memory is set. 0x0 = CHG FET driver is allowed to turn on if other conditions are met. 0x1 = CHG FET driver is forced off.
2	DSG_OFF	DSG FET driver control. This bit only operates if the ***[HOST_FETOFF_EN]*** bit in data memory is set. 0x0 = DSG FET driver is allowed to turn on if other conditions are met. 0x1 = DSG FET driver is forced off.
1	CHG_ON	CHG FET driver control. This bit only operates if the ***[HOST_FETON_EN]*** bit in data memory is set. 0x0 = CHG FET driver is allowed to turn on if other conditions are met. 0x1 = CHG FET driver is forced on.
0	DSG_ON	DSG FET driver control. This bit only operates if the ***[HOST_FETON_EN]*** bit in data memory is set. 0x0 = DSG FET driver is allowed to turn on if other conditions are met. 0x1 = DSG FET driver is forced on.

Note that body diode protection takes priority over the manual FET commands. If the user does not want body diode protection to take effect in this case, it can be disabled by clearing the ***Settings:Configuration:FET Options[SFET]*** data memory configuration bit.

The BQ76905 includes PWM drive capability on the CHG and DSG FET drivers, which allows them to limit the average current flowing in a charge or discharge mode. The DSG FET driver actively drives the DSG pin high or low, based on the driver control, so can implement relatively fast switching to turn on and off the DSG FET. If a charger is not attached, then the CHG driver can also implement relatively fast switching in PWM mode. If a charger is attached with voltage significantly above the pack voltage (which means the voltage on PACK- is below VSS), then the CHG FET gate voltage is generally driven to approximately VSS + 0.5 V quickly when first disabled, then settles to the lower PACK- voltage at a rate depending on the system capacitance. The drivers are not intended to both be used in PWM mode at the same time, it is recommended to only use one in PWM mode at a time. The *0x6A DSG FET Driver PWM Control()* and *0x6C CHG FET Driver PWM Control()* commands enable the drivers in PWM mode. These commands are only available if the ***Settings:Configuration:FET Options[PWM_EN]*** data memory configuration bit is set.

The BQ76905 provides an option for the device to autonomously disable the CHG FET when the device enters SLEEP mode. The device only enters SLEEP mode when pack current is below a programmable threshold. The DSG FET is generally enabled in this mode, but the CHG FET can be disabled to reduce the power flowing through the gate-source resistor around the CHG FET. When a significant charging or discharging current is detected, the device exits SLEEP mode, returning to NORMAL mode, and then re-enables the CHG FET unless other conditions prevent it. The state of the CHG FET in SLEEP mode is set by the ***Settings:Configuration:FET Options[SLEEPCHG]*** data memory configuration bit.

6.3 Cell Overvoltage Protection

The BQ76905 integrates Cell Overvoltage Protection (COV), monitoring the voltage of every cell using the voltage ADC data, and triggering a COV alert or fault when a cell voltage exceeds the COV threshold. The COV threshold is programmable from 0.0 V to 5.5 V in 1 mV steps and is set by the ***Protections:Cell***

Voltage:Cell Overvoltage Protection Threshold configuration register. The COV protection is enabled using the ***Settings:Protection:Enabled Protections A:[COV]*** configuration bit.

The COV circuitry triggers an alert signal when an overvoltage event is first detected, then triggers a fault after the voltage is measured above the threshold steadily for a programmable number of measurements (ADSCANs). The number of measurements required before the fault is triggered is set by the ***Protections:Cell Voltage:Cell Overvoltage Protection Delay*** configuration register, which ranges from 1 to 255. The time until a fault is triggered is based on the settings for the voltage ADC measurement speeds, which sets the timing for each ADSCAN measurement loop. Note also that during SLEEP mode measurements are only taken every ***Power:Sleep:Voltage Time*** interval, but if any cell voltage is detected above the COV threshold during a SLEEP mode measurement, the device returns to NORMAL mode and continue taking measurements at a more frequent rate until the COV alert has cleared or a COV fault has triggered. The timing of COV delay can be different while cell balancing is active, depending on settings described in Chapter 10.

When a COV fault is triggered, it recovers if the maximum cell voltage drops below the COV threshold by a COV_HYS hysteresis level, which is programmable as 50 mV, 100 mV, or 200 mV, or autonomous recovery can be disabled. The COV_HYS hysteresis level is set by the ***Protections:Cell Voltage:Cell Overvoltage Protection Recovery Hysteresis*** configuration register. If autonomous recovery is disabled, the fault can be recovered manually by the host sending the *0x009B PROT_RECOVERY()* subcommand with the *[VOLTREC]* bit set.

When a COV fault is triggered, the device turns off the CHG FET if configured for autonomous FET control based on setting in ***Settings:Protection:CHG FET Protections A[COV]*** (the DSG FET remains enabled if already enabled). The device recovers (if configured for autonomous FET control) based on all cell voltages being below COV threshold – COV_HYS.

Table 6-7. Overvoltage Protection Operation

Status	Condition	Action
Normal	Max cell voltage ≤ ***Protections:COV:Threshold***	*Safety Alert A()[COV]* = 0
Alert	Max cell voltage > ***Protections:COV:Threshold***	*Safety Alert A()[COV]* = 1
Trip	Max cell voltage > ***Protections:COV:Threshold*** for ***Protections:COV:Delay*** duration	*Safety Alert A()[COV]* = 0 *Safety Status A()[COV]* = 1 and CHG FET can be disabled depending on settings
Recovery	*Safety Status A()[COV]* = 1 and Max cell voltage ≤ ***Protections:COV:Threshold*** - ***Protections:COV:Recovery Hysteresis***	*Safety Status A()[COV]* = 0 and CHG FET can be re-enabled based on settings

6.4 Cell Undervoltage Protection

The BQ76905 integrates Cell Undervoltage Protection (CUV), monitoring the voltage of every cell using the voltage ADC data, and triggering a CUV alert or fault when a cell voltage falls below the CUV threshold. The CUV threshold is programmable from 0.0 V to 5.5 V in 1 mV steps and is set by the ***Protections:Cell Voltage:Cell Undervoltage Protection Threshold*** configuration register. The CUV protection is enabled using the ***Settings:Protection:Enabled Protections A:[CUV]*** configuration bit.

The CUV circuitry triggers an alert signal when an undervoltage event is first detected, then triggers a fault after the voltage is measured below the threshold steadily for a programmable number of measurements (ADSCANs). The number of measurements required before the fault is triggered is set by the ***Protections:Cell Voltage:Cell Undervoltage Protection Delay*** configuration register, which ranges from 1 to 255. The time until a fault is triggered is based on the settings for the voltage ADC measurement speeds, which sets the timing for each ADSCAN measurement loop. During SLEEP mode, measurements are only taken every ***Power:Sleep:Voltage Time*** interval, but if any cell voltage is detected below the CUV threshold during a SLEEP mode measurement, the device returns to NORMAL mode and continues taking measurements at a more frequent rate until the CUV alert has cleared or a CUV fault has triggered. The timing of CUV delay can be different while cell balancing is active, depending on settings described in Chapter 10.

When a CUV fault is triggered, it recovers if the minimum cell voltage rises above the CUV threshold by a CUV_HYS hysteresis level, which is programmable as 50 mV, 100mV, or 200 mV, or autonomous recovery can be disabled. The CUV_HYS hysteresis level is set by the ***Protections:Cell Voltage:Cell Undervoltage Protection Recovery Hysteresis*** configuration register. If autonomous recovery is disabled, the fault can be recovered manually by the host sending the *0x009B PROT_RECOVERY()* subcommand with the *[VOLTREC]* bit set.

When a CUV fault is triggered, the device turns off the DSG FET if configured for autonomous FET control based on setting in ***Settings:Protection:DSG FET Protections A[CUV]*** (the CHG FET remains enabled if already enabled). The device recovers (if configured for autonomous FET control) based on all cell voltages being above CUV threshold + CUV_HYS.

Table 6-8. Undervoltage Protection Operation

Status	Condition	Action
Normal	Min cell voltage ≥ ***Protections:CUV:Threshold***	*Safety Alert A()[CUV]* = 0
Alert	Min cell voltage < ***Protections:CUV:Threshold***	*Safety Alert A()[CUV]* = 1
Trip	Min cell voltage < ***Protections:CUV:Threshold*** for ***Protections:CUV:Delay*** duration	*Safety Alert A()[CUV]* = 0 *Safety Status A()[CUV]* = 1 and DSG FET can be disabled depending on settings
Recovery	*Safety Status A()[CUV]* = 1 and Min cell voltage ≥ ***Protections:CUV:Threshold*** + ***Protections:CUV:Recovery Hysteresis***	*Safety Status A()[CUV]* = 0 and DSG FET can be re-enabled based on settings

6.5 Short Circuit in Discharge Protection

The BQ76905 integrates Short Circuit in Discharge Protection (SCD) using a dedicated comparator that monitors the differential voltage across the SRN - SRP pins and triggers an SCD alert or fault when the voltage exceeds a programmable threshold VSCD. The VSCD threshold is programmable using the ***Protections:Current:Short Circuit in Discharge Protection Threshold*** configuration register, with available settings shown in Table 6-9. The SCD protection is enabled using the ***Settings:Protection:Enabled Protections A:[SCD]*** configuration bit.

Table 6-9. Short Circuit in Discharge Threshold Settings

Setting	Threshold
0	10 mV
1	20 mV
2	40 mV
3	60 mV
4	80 mV
5	100 mV
6	125 mV
7	150 mV
8	175 mV
9	200 mV
10	250 mV
11	300 mV
12	350 mV
13	400 mV
14	450 mV
15	500 mV

The SCD circuitry triggers an alert signal when a short circuit event is first detected, then triggers a fault if it persists after a programmable detection delay, SCD_DLY, which is set by the ***Protections:Current:Short***

Circuit in Discharge Protection Delay configuration register. The fastest setting can result in detection of a short circuit with only comparator delay, which can be <1 µs depending on the overdrive of the threshold. The delay settings are shown in Table 6-10.

Table 6-10. Short Circuit in Discharge Delay Setting

Setting	Nominal Delay
0	Fastest
1	0 to 15 µs
2	15 to 30 µs
3	45 to 60 µs
4	105 to 120 µs
5	225 to 240 µs
6	465 to 480 µs
7	945 to 960 µs
8	1905 to 1920 µs
9	3825 to 3840 µs
10	7665 to 7680 µs

The SCD safety alert is not set in user readable registers until up to 50 µs after the event occurs, even though it was detected and the delay timer already started. When the SCD protection delay is set very short, such as the first three settings, the SCD safety status can actually trigger before the alert becomes visible in the *Alarm Raw Status()* or *Safety Alert A()* registers, and then the alert is cleared by the SCD safety status. When the SCD delay is set to a longer setting, the SCD safety alert is then generally visible.

When an SCD fault is triggered, the device turns off the DSG FET if configured for autonomous FET control in ***Settings:Protection:DSG FET Protections A[SCD]***. The CHG FET can also be disabled autonomously based on setting in ***Settings:Protection:CHG FET Protections A[SCD]***. The device recovers after a programmable delay given by ***Protections:Current:Recovery Time***, which can be set from 1 second to 255 seconds in 1-second steps. A delay setting of 0 disables autonomous recovery based on time. Continual retrying of time-based recovery can be avoided by using the Current Protection Latch feature.

Table 6-11. Short Circuit in Discharge Protection Operation

Status	Condition	Action
Normal	V_{SRN}–V_{SRP} ≤ setting selected by ***Protections:Current:Short Circuit in Discharge Protection Threshold***	*Safety Alert A()[SCD]* = 0. Clear current latch counter if no current protection fault occurs for 5 seconds.
Alert	V_{SRN}–V_{SRP} > setting selected by ***Protections:Current:Short Circuit in Discharge Protection Threshold***	*Safety Alert A()[SCD]* = 1
Trip	V_{SRN}–V_{SRP} > setting selected by ***Protections:Current:Short Circuit in Discharge Protection Threshold*** for ***Protections:Current:Short Circuit in Discharge Protection Delay*** duration.	*Safety Alert A()[SCD]* = 0 *Safety Status A()[SCD]* = 1 Increment current latch counter.
Recovery	*Safety Status A()[SCD]* = 1 and V_{SRN}–V_{SRP} ≤ setting selected by ***Protections:Current:Short Circuit in Discharge Protection Threshold*** for ***Protections:Current:Recovery Time*** duration.	*Safety Status A()[SCD]* = 0 FETs can be re-enabled if conditions allow and not latched off.
Latch Limit	Current latch counter ≥ ***Protections:Current:Latch Limit***	*Safety Status A()[CURLATCH]* = 1 FETs are latched off and not autonomously re-enabled.

Depending on the system configuration, the user can utilize the CHG Detector signal to determine whether the load has been removed from the pack after the FETs have been disabled. For more details on this,

see CHG Detector. In this case, if the load has been removed, then recovery can occur when the *0x009B PROT_RECOVERY()* command is sent from the host with the *[SCDREC]* bit set.

6.6 Overcurrent in Charge Protection

The BQ76905 integrates Overcurrent in Charge Protection (OCC) using a comparator that monitors the differential voltage across the SRP - SRN pins and triggers an OCC alert or fault when the voltage exceeds a programmable threshold VOCC. The VOCC threshold is programmable from 3 mV to 123 mV in 2-mV steps using the ***Protections:Current:Overcurrent in Charge Protection Threshold*** configuration register (threshold = 2 mV × register value - 1 mV). The OCC protection is enabled using the ***Settings:Protection:Enabled Protections A:[OCC]*** configuration bit.

The OCC circuitry triggers an alert signal when an overcurrent in charge event is first detected, then triggers a fault if it persists for a programmable detection delay, OCC_DLY, which can be set as shown below.

Setting	Nominal Delay (ms)
0	Fastest (approximately 0.46 ms)
1 to 64	1.22 ms to 20.435 ms in steps of 0.305 ms
65 to 128	22.875 ms to 176.595 ms in steps of 2.44 ms
129 to 192	181.475 ms to 488.915 ms in steps of 4.88 ms
193 to 255	498.675 ms to 1103.795 ms in steps of 9.77 ms

The delay is set by the ***Protections:Current:Overcurrent in Charge Protection Delay*** configuration register.

When an OCC fault is triggered, the device turns off the CHG FET if configured for autonomous FET control when ***Settings:Protection:CHG FET Protections A[OCC]*** is set. The device recovers after a programmable delay given by ***Protections:Current:Recovery Time*** , which can be set from 1 second to 255 seconds in 1-second steps. A recovery time setting of 0 disables autonomous recovery, in which case recovery only occurs when the *PROT_RECOVERY()* subcommand is sent from the host with the *[OCCREC]* bit set. Continual retrying of time-based recovery can be avoided by using the Current Protection Latch feature.

Table 6-12. Overcurrent in Charge Protection Operation

Status	Condition	Action
Normal	V_{SRP}–V_{SRN} ≤ setting selected by ***Protections:Current:Overcurrent in Charge Protection Threshold***	*Safety Alert A()[OCC]* = 0. Clear current latch counter if no current protection fault occurs for 5 seconds.
Alert	V_{SRP}–V_{SRN} > setting selected by ***Protections:Current:Overcurrent in Charge Protection Threshold***	*Safety Alert A()[OCC]* = 1
Trip	V_{SRP}–V_{SRN} > setting selected by ***Protections:Current:Overcurrent in Charge Protection Threshold*** for ***Protections:Current:Overcurrent in Charge Protection Delay*** duration.	*Safety Alert A()[OCC]* = 0 *Safety Status A()[OCC]* = 1 Increment current latch counter.
Recovery	*Safety Status A()[OCC]* = 1 and V_{SRP}–V_{SRN} ≤ setting selected by ***Protections:Current:Overcurrent in Charge Protection Threshold*** for ***Protections:Current:Recovery Time*** duration.	*Safety Status A()[OCC]* = 0 CHG FET can be re-enabled if conditions allow and it is not latched off.
Latch Limit	Current latch counter ≥ ***Protections:Current:Latch Limit***	*Safety Status A()[CURLATCH]* = 1 CHG FET is latched off and not autonomously re-enabled.

6.7 Overcurrent in Discharge 1 and 2 Protections

The BQ76905 integrates two Overcurrent in Discharge Protections (OCD1, OCD2) using a comparator that monitors the differential voltage across the SRN - SRP pins and triggers an OCD1 or OCD2 alert or fault when the voltage exceeds a programmable threshold VOCD1 and VOCD2, respectively. The VOCD1/2 thresholds are

programmable from 4 mV to 200 mV in 2 mV steps using the ***Protections:Current:Overcurrent in Discharge 1 Protection Threshold*** and ***Protections:Current:Overcurrent in Discharge 2 Protection Threshold*** configuration registers. These two protections operate identically, but can have independent threshold and delay settings. The OCD1 and OCD2 protections are enabled using the ***Settings:Protection:Enabled Protections A:[OCD1]*** and ***[OCD2]*** configuration bits.

The OCD1/2 circuitry triggers an alert signal when an overcurrent in discharge event is first detected, then triggers a fault if it persists for a programmable detection delay, OCD1_DLY or OCD2_DLY, which can be set as shown below.

Setting	Nominal Delay (ms)
0	Fastest (approximately 0.46 ms)
1 to 64	1.22 ms to 20.435 ms in steps of 0.305 ms
65 to 128	22.875 ms to 176.595 ms in steps of 2.44 ms
129 to 192	181.475 ms to 488.915 ms in steps of 4.88 ms
193 to 255	498.675 ms to 1103.795 ms in steps of 9.77 ms

The delay is set by the ***Protections:Current:Overcurrent in Discharge 1 Protection Delay*** and ***Protections:Current:Overcurrent in Discharge 2 Protection Delay*** configuration registers.

When an OCD fault is triggered, the device turns off the DSG FET if configured for autonomous FET control in ***Settings:Protection:DSG FET Protections A[OCD1, OCD2]***. The device recovers after a programmable delay given by ***Protections:Current:Recovery Time***, which can be set from 1 second to 255 seconds in 1-second steps. A recovery time setting of 0 disables autonomous recovery, in which case recovery only occurs when the *PROT_RECOVERY()* command is sent from the host with the appropriate *[OCD1REC]* or *[OCD2REC]* bit set. Continual retrying of time-based recovery can be avoided by using the Current Protection Latch feature.

Table 6-13. Overcurrent in Discharge Protection Operation

Status	Condition	Action
Normal	V_{SRN}–V_{SRP} ≤ setting selected by ***Protections:Current:Overcurrent in Discharge 1 Protection Threshold***	*Safety Alert A()[OCD1]* = 0. Clear current latch counter if no current protection fault occurs for 5 seconds.
Normal	V_{SRN}–V_{SRP} ≤ setting selected by ***Protections:Current:Overcurrent in Discharge 2 Protection Threshold***	*Safety Alert A()[OCD2]* = 0. Clear current latch counter if no current protection fault occurs for 5 seconds.
Alert	V_{SRN}–V_{SRP} > setting selected by ***Protections:Current:Overcurrent in Discharge 1 Protection Threshold***	*Safety Alert A()[OCD1]* = 1
Alert	V_{SRN}–V_{SRP} > setting selected by ***Protections:Current:Overcurrent in Discharge 2 Protection Threshold***	*Safety Alert A()[OCD2]* = 1
Trip	V_{SRP}–V_{SRN} > setting selected by ***Protections:Current:Overcurrent in Discharge 1 Protection Threshold*** for ***Protections:Current:Overcurrent in Discharge 1 Protection Delay*** duration.	*Safety Alert A()[OCD1]* = 0 *Safety Status A()[OCD1]* = 1 Increment current latch counter.
Trip	V_{SRP}–V_{SRN} > setting selected by ***Protections:Current:Overcurrent in Discharge 2 Protection Threshold*** for ***Protections:Current:Overcurrent in Discharge 2 Protection Delay*** duration.	*Safety Alert A()[OCD2]* = 0 *Safety Status A()[OCD2]* = 1 Increment current latch counter.
Recovery	*Safety Status A()[OCD1]* = 1 and V_{SRN}–V_{SRP} ≤ setting selected by ***Protections:Current:Overcurrent in Discharge 1 Protection Threshold*** for ***Protections:Current:Recovery Time*** duration.	*Safety Status A()[OCD1]* = 0 DSG FET can be re-enabled if conditions allow and it is not latched off.
Recovery	*Safety Status A()[OCD2]* = 1 and V_{SRN}–V_{SRP} ≤ setting selected by ***Protections:Current:Overcurrent in Discharge 2 Protection Threshold*** for ***Protections:Current:Recovery Time*** duration.	*Safety Status A()[OCD2]* = 0 DSG FET can be re-enabled if conditions allow and it is not latched off.

Table 6-13. Overcurrent in Discharge Protection Operation (continued)

Status	Condition	Action
Latch Limit	Current latch counter ≥ ***Protections:Current:Latch Limit***	*Safety Status A()[CURLATCH]* = 1 DSG FET is latched off and not autonomously re-enabled.

6.8 Current Protection Latch

The BQ76905 also includes a current protection latch, which prevents the device from continually attempting time-based recovery indefinitely if a short circuit or overcurrent condition persists. Each time an SCD or OCD1 or OCD2 or OCC fault occurs, a latch counter is incremented. If a current protection fault does not occur for 5-sec after re-enabling the pertinent FET, the counter is cleared. If the counter reaches a level of ***Protections:Current:Latch Limit*** (settings of 0, 2, 4, 8, 16, 32, 48, 96, with setting=0 disabling the latch feature), the device disables further autonomous recovery attempts based on time, and the *Safety Status A() [CURLATCH]* bit is set. Recovery can be restarted by the host sending a *PROT_RECOVERY()* command with any of the current protection bits set, which clears the latch counter value, so the device can again attempt recovery.

6.9 CHG Detector

The BQ76905 provides a signal that indicates if the CHG pin voltage is above a level of approximately 2 V. The raw value of this flag can be read through the communications interface, and an alarm can be generated on the ALERT pin whenever the debounced version of this flag changes state, based on device settings. This flag can be used by the system to assist in recovery from a current fault condition.

The CHG Detector signal is enabled and evaluated by logic within the device if ***Settings:Configuration:FET Options[CHGDETEN]*** = 1. The value of the raw CHG Detector output can be read over the serial communications interface at *Alarm Raw Status()[CDRAW].* If the CHG Detector output is stable for a time interval in excess of ***Settings:Configuration:CHG Detector Time*****,** its value is latched into *Battery Status() [CHGDETFLAG],* which is a debounced version of the CHG Detector signal. The *Alarm Status()[CDTOGGLE]* is set whenever the debounced signal (CHGDETFLAG) changes from its previous debounced state. The value of ***Settings:Configuration:CHG Detector Time*** is programmable from 100 ms to 25.5 s in steps of 100 ms

The host can use the *Alarm Enable()[CDTOGGLE]* bit to mask the alarm. When *Alarm Status()[CDTOGGLE]* is set, the host can write a 1 to *Alarm Status()[CDTOGGLE]* to clear the alarm. If ***[CHGDETEN]*** is set, then whenever the CHG Detector output changes state from the debounced latched version, the LFO is wakened to begin timing it (if the LFO is otherwise off in DEEPSLEEP). If in DEEPSLEEP, the LFO can be disabled after timing a new debounced version, based on the setting ***Settings:Configuration:Power Config[DPSLP_LFO]***.

When a current fault occurs in a system, such as a short circuit event, the device generally disables the DSG FET, the CHG FET, or possibly both, depending on settings. The device can be configured to wait a programmed delay then reenable the FETs. If the current fault condition is still present, then a new fault is triggered, and the FETs disabled again. If a fault persists, this cycle of periodically recovering and retriggering a fault can continue indefinitely, which is generally not acceptable.

An alternative is to only allow a limited number of retries, then to disable further retries after that limit is reached. This capability is supported using the Current Protection Latch. This avoids the indefinite cycle of retries, but then can render the pack unusable after a limited number of retries.

If the pack is removable, such as in a power tool, then another option is to keep the FETs disabled until the pack has been removed from the system. In this case, if the CHG driver is disabled and a charger is not connected, then the CHG pin is pulled up to the PACK+ voltage while a load is connected, resulting in the CHG Detector signal being asserted. When the pack is removed from the system (and the charger is still not connected), then the CHG pin generally falls to near the BAT- voltage level, resulting in the CHG Detector signal being deasserted. A host processor within the battery pack can then use this signal to trigger recovery of the pack.

The use of this CHG Detector for load removal depends on the system configuration and is not usable in all cases. Thus, it is important for the pack designer to evaluate whether it is applicable to the system or not.

6.10 Overtemperature in Charge Protection

The BQ76905 device integrates an Overtemperature in Charge (OTC) Protection that digitizes the voltage of an external negative temperature coefficient thermistor on the TS pin using the ADC, and triggers an alert or fault when the digital ADC measurement at the thermistor is less than a programmable threshold VOTC. The thermistor is biased using an on-chip 20-kΩ pullup resistor (which is trimmed in TI factory), which is biased by the internal 1.8-V LDO rail only when the thermistor is being measured (which is the default recommended setting). Alternatively, the pullup resistor can be biased continuously by sending the *0x69 REGOUT_CONTROL()* command with the *[TS_ON]* bit set. The ADC uses this same internal 1.8-V LDO rail as its voltage reference for this measurement, thereby implementing a ratiometric conversion.

The VOTC threshold is programmable from 0 to 13770 16-bit ADC counts in steps of 54 ADC counts using the ***Protections:Temperature:Overtemperature in Charge Protection Threshold*** configuration register. The OTC protection is enabled using the ***Settings:Protection:Enabled Protections B:[OTC]*** configuration bit.

The OTC protection triggers an alert signal when an overtemperature in charge event is first detected, then triggers a fault if this persists after a programmable number of measurements have been taken, OTC_DLY, which can be set from 0 to 255. The delay is set by the ***Protections:Temperature:Overtemperature in Charge Protection Delay*** configuration register. The time interval for measurements will be based on the settings for the voltage and current ADC measurement speeds. Note that during SLEEP mode this protection only operates during the duty-cycled measurement burst every ***Power:Sleep:Voltage Time***, so there can be a longer delay before it triggers an alert. If an alert is triggered, the device will return to NORMAL mode until either the alert is cleared or a fault is triggered.

When an OTC fault is triggered, the device will turn off the CHG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:CHG FET Protections A[OTC]***. The device recovers when the thermistor measurement is greater than or equal to the threshold set by ***Protections:Temperature:Overtemperature in Charge Protection Recovery*** (which has the same threshold range from 0 to 13770 16-bit ADC counts in steps of 54 ADC counts). If the ***Protections:Temperature:Overtemperature in Charge Protection Recovery*** is set to zero, autonomous recovery is disabled, and recovery must be initiated by the host sending the *PROT_RECOVERY()* subcommand with the *[TEMPREC]* bit set.

Table 6-14. Overtemperature in Charge Protection Operation

Status	Condition	Action
Normal	TS pin ADC measurement ≥ ***Protections:Temperature:Overtemperature in Charge Protection Threshold***	*Safety Alert B()[OTC]* = 0
Alert	TS pin ADC measurement < ***Protections:Temperature:Overtemperature in Charge Protection Threshold***	*Safety Alert B()[OTC]* = 1
Trip	TS pin ADC measurement < ***Protections:Temperature:Overtemperature in Charge Protection Threshold*** for ***Protections:Temperature:Overtemperature in Charge Protection Delay*** duration	*Safety Alert B()[OTC]* = 0 *Safety Status B()[OTC]* = 1 and CHG FET can be disabled depending on settings
Recovery	*Safety Status B()[OTC]* = 1 and TS pin ADC measurement ≥ ***Protections:Temperature:Overtemperature in Charge Protection Recovery***	*Safety Status B()[OTC]* = 0 and CHG FET can be re-enabled based on settings

6.11 Overtemperature in Discharge Protection

The BQ76905 device integrates an Overtemperature in Discharge (OTD) Protection that digitizes the voltage of an external negative temperature coefficient thermistor on the TS pin using the ADC, and triggers an alert or fault when the digital ADC measurement at the thermistor is less than a programmable threshold VOTD. The thermistor is biased using an on-chip 20-kΩ pullup resistor (which is trimmed in TI factory), which is biased by the internal 1.8-V LDO rail only when the thermistor is being measured (which is the

default recommended setting). Alternatively, the pullup resistor can be biased continuously by sending the *0x69 REGOUT_CONTROL()* command with the *[TS_ON]* bit set. The ADC uses this same internal 1.8-V LDO rail as its voltage reference for this measurement, thereby implementing a ratiometric conversion.

The VOTD threshold is programmable from 0 to 13770 16-bit ADC counts in steps of 54 ADC counts using the ***Protections:Temperature:Overtemperature in Discharge Protection Threshold*** configuration register. The OTD protection is enabled using the ***Settings:Protection:Enabled Protections B:[OTD]*** configuration bit.

The OTD protection triggers an alert signal when an overtemperature in charge event is first detected, then triggers a fault if this persists after a programmable number of measurements have been taken, OTD_DLY, which can be set from 0 to 255. The delay is set by the ***Protections:Temperature:Overtemperature in Discharge Protection Delay*** configuration register. The time interval for measurements is based on the settings for the voltage and current ADC measurement speeds. Note that during SLEEP mode this protection only operates during the duty-cycled measurement burst every ***Power:Sleep:Voltage Time***, so there can be a longer delay before it triggers an alert. If an alert is triggered, the device returns to NORMAL mode until either the alert is cleared or a fault is triggered.

When an OTD fault is triggered, the device turns off the DSG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:DSG FET Protections A[OTD]***. The device recovers when the thermistor measurement is greater than or equal to the threshold set by ***Protections:Temperature:Overtemperature in Discharge Protection Recovery*** (which has the same threshold range from 0 to 13770 16-bit ADC counts in steps of 54 ADC counts). If the ***Protections:Temperature:Overtemperature in Discharge Protection Recovery*** is set to zero, autonomous recovery is disabled, and recovery must be initiated by the host sending the *PROT_RECOVERY()* subcommand with the *[TEMPREC]* bit set.

Table 6-15. Overtemperature in Discharge Protection Operation

Status	Condition	Action
Normal	TS pin ADC measurement ≥ ***Protections:Temperature:Overtemperature in Discharge Protection Threshold***	*Safety Alert B()[OTD]* = 0
Alert	TS pin ADC measurement < ***Protections:Temperature:Overtemperature in Discharge Protection Threshold***	*Safety Alert B()[OTD]* = 1
Trip	TS pin ADC measurement < ***Protections:Temperature:Overtemperature in Discharge Protection Threshold*** for ***Protections:Temperature:Overtemperature in Discharge Protection Delay*** duration	*Safety Alert B()[OTD]* = 0 *Safety Status B()[OTD]* = 1 and DSG FET can be disabled depending on settings
Recovery	*Safety Status B()[OTD]* = 1 and TS pin ADC measurement ≥ ***Protections:Temperature:Overtemperature in Discharge Protection Recovery***	*Safety Status B()[OTD]* = 0 and DSG FET can be re-enabled based on settings

6.12 Internal Overtemperature Protection

The BQ76905 device integrates an Internal Overtemperature Protection (OTINT) that monitors the internal die temperature using the voltage ADC, and triggers an alert or fault when the internal temperature is greater than a programmable threshold VOTINT.

The VOTINT threshold is programmable from 25°C to 150°C in 1°C steps using the ***Protections:Temperature:Internal Overtemperature Protection Threshold*** configuration register. The OTINT protection is enabled using the ***Settings:Protection:Enabled Protections B:[OTINT]*** configuration bit.

The OTINT protection triggers an alert signal when an internal overtemperature event is first detected, then triggers a fault if it persists after a programmable number of measurements have been taken, OTINT_DLY, which can be set from 0 to 255. The delay is set by the ***Protections:Temperature:Internal Overtemperature Protection Delay*** configuration register. The time interval for measurements is based on the settings for the

voltage, current, and shared slot ADC measurement speeds. Note that during SLEEP mode this protection only operates during the duty-cycled measurement burst every ***Power:Sleep:Voltage Time***, so there can be a longer delay before it triggers an alert. If an alert is triggered, the device returns to NORMAL mode until either the alert is cleared or a fault is triggered.

When an OTINT fault is triggered, the device turns off the DSG and CHG FETs if configured for autonomous FET control, based on the setting in ***Settings:Protection:DSG FET Protections A[OTINT]*** and ***Settings:Protection:CHG FET Protections A[OTINT]***. The device recovers when the temperature is equal or below ***Protections:Temperature:Internal Overtemperature Protection Recovery***. If the ***Protections:Temperature:Internal Overtemperature Protection Recovery*** is set to zero, autonomous recovery is disabled, and recovery must be initiated by the host sending the *PROT_RECOVERY()* subcommand with the *[TEMPREC]* bit set.

Table 6-16. Internal Overtemperature Protection Operation

Status	Condition	Action
Normal	*0x28 Int Temperature()* measurement ≤ ***Protections:Temperature:Internal Overtemperature Protection Threshold***	*Safety Alert B()[OTINT]* = 0
Alert	*0x28 Int Temperature()* measurement > ***Protections:Temperature:Internal Overtemperature Protection Threshold***	*Safety Alert B()[OTINT]* = 1
Trip	*0x28 Int Temperature()* measurement > ***Protections:Temperature:Internal Overtemperature Protection Threshold*** for ***Protections:Temperature:Internal Overtemperature Protection Delay*** duration	*Safety Alert B()[OTINT]* = 0 *Safety Status B()[OTINT]* = 1 and CHG and DSG FETs can be disabled depending on settings
Recovery	*Safety Status B()[OTINT]* = 1 and T*0x28 Int Temperature()* measurement ≤ ***Protections:Temperature:Internal Overtemperature Protection Threshold***	*Safety Status B()[OTINT]* = 0 and CHG and DSG FETs can be re-enabled based on settings

6.13 Undertemperature in Charge Protection

The BQ76905 device integrates an Undertemperature in Charge (UTC) Protection that digitizes the voltage of an external negative temperature coefficient thermistor on the TS pin using the ADC, and triggers an alert or fault when the digital ADC measurement at the thermistor is greater than a programmable threshold VUTC. The thermistor is biased using an on-chip 20-kΩ pullup resistor (which is trimmed in TI factory), which is biased by the internal 1.8-V LDO rail only when the thermistor is being measured (which is the default recommended setting). Alternatively, the pullup resistor can be biased continuously by sending the *0x69 REGOUT_CONTROL()* command with the *[TS_ON]* bit set. The ADC uses this same internal 1.8-V LDO rail as its voltage reference for this measurement, thereby implementing a ratiometric conversion.

The VUTC threshold is programmable from 0 to 19635 16-bit ADC counts in steps of 77 ADC counts using the ***Protections:Temperature:Undertemperature in Charge Protection Threshold*** configuration register. The UTC protection is enabled using the ***Settings:Protection:Enabled Protections B:[UTC]*** configuration bit.

The UTC protection triggers an alert signal when an undertemperature in charge event is first detected, then triggers a fault if it persists after a programmable number of measurements have been taken, UTC_DLY, which can be set from 0 to 255. The delay is set by the ***Protections:Temperature:Undertemperature in Charge Protection Delay*** configuration register. The time interval for measurements is based on the settings for the voltage and current ADC measurement speeds. Note that during SLEEP mode this protection only operates during the duty-cycled measurement burst every ***Power:Sleep:Voltage Time***, so there can be a longer delay before it triggers an alert. If an alert is triggered, the device returns to NORMAL mode until either the alert is cleared or a fault is triggered.

When a UTC fault is triggered, the device turns off the CHG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:CHG FET Protections A[UTC]***. The device recovers when the thermistor measurement is less than or equal to the threshold set

by ***Protections:Temperature:Undertemperature in Charge Protection Recovery*** (which has the same threshold range from 0 to 19635 16-bit ADC counts in steps of 77 ADC counts). If the ***Protections:Temperature:Undertemperature in Charge Protection Recovery*** is set to zero, autonomous recovery is disabled, and recovery must be initiated by the host sending the *PROT_RECOVERY()* subcommand with the *[TEMPREC]* bit set.

Table 6-17. Undertemperature in Charge Protection Operation

Status	Condition	Action
Normal	TS pin ADC measurement ≤ ***Protections:Temperature:Undertemperature in Charge Protection Threshold***	*Safety Alert B()[UTC]* = 0
Alert	TS pin ADC measurement > ***Protections:Temperature:Undertemperature in Charge Protection Threshold***	*Safety Alert B()[UTC]* = 1
Trip	TS pin ADC measurement > ***Protections:Temperature:Undertemperature in Charge Protection Threshold*** for ***Protections:Temperature:Undertemperature in Charge Protection Delay*** duration	*Safety Alert B()[UTC]* = 0 *Safety Status B()[UTC]* = 1 and CHG FET can be disabled depending on settings
Recovery	*Safety Status B()[UTC]* = 1 and TS pin ADC measurement ≤ ***Protections:Temperature:Undertemperature in Charge Protection Recovery***	*Safety Status B()[UTC]* = 0 and CHG FET can be re-enabled based on settings

6.14 Undertemperature in Discharge Protection

The BQ76905 device integrates an Undertemperature in Discharge (UTD) Protection that digitizes the voltage of an external negative temperature coefficient thermistor on the TS pin using the ADC, and triggers an alert or fault when the digital ADC measurement at the thermistor is greater than a programmable threshold VUTD. The thermistor is biased using an on-chip 20-kΩ pullup resistor (which is trimmed in TI factory), which is biased by the internal 1.8-V LDO rail only when the thermistor is being measured (which is the default recommended setting). Alternatively, the pullup resistor can be biased continuously by sending the *0x69 REGOUT_CONTROL()* command with the *[TS_ON]* bit set. The ADC uses this same internal 1.8-V LDO rail as its voltage reference for this measurement, thereby implementing a ratiometric conversion.

The VUTD threshold is programmable from 0 to 19635 16-bit ADC counts in steps of 77 ADC counts using the ***Protections:Temperature:Undertemperature in Discharge Protection Threshold*** configuration register. The UTD protection is enabled using the ***Settings:Protection:Enabled Protections B:[UTD]*** configuration bit.

The UTD protection triggers an alert signal when an undertemperature in discharge event is first detected, then triggers a fault if it persists after a programmable number of measurements have been taken, UTD_DLY, which can be set from 0 to 255. The delay is set by the ***Protections:Temperature:Undertemperature in Discharge Protection Delay*** configuration register. The time interval for measurements is based on the settings for the voltage and current ADC measurement speeds. Note that during SLEEP mode this protection only operates during the duty-cycled measurement burst every ***Power:Sleep:Voltage Time***, so there can be a longer delay before it triggers an alert. If an alert is triggered, the device returns to NORMAL mode until either the alert is cleared or a fault is triggered.

When a UTD fault is triggered, the device turns off the DSG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:DSG FET Protections A[UTD]***. The device recovers when the thermistor measurement is less than or equal to the threshold set by ***Protections:Temperature:Undertemperature in Discharge Protection Recovery*** (which has the same threshold range from 0 to 19635 16-bit ADC counts in steps of 77 ADC counts). If the ***Protections:Temperature:Undertemperature in Discharge Protection Recovery*** is set to zero, autonomous recovery is disabled, and recovery must be initiated by the host sending the *PROT_RECOVERY()* subcommand with the *[TEMPREC]* bit set.

Table 6-18. Undertemperature in Discharge Protection Operation

Status	Condition	Action
Normal	TS pin ADC measurement ≤ ***Protections:Temperature:Undertemperature in Discharge Protection Threshold***	*Safety Alert B()[UTD]* = 0
Alert	TS pin ADC measurement > ***Protections:Temperature:Undertemperature in Discharge Protection Threshold***	*Safety Alert B()[UTD]* = 1
Trip	TS pin ADC measurement > ***Protections:Temperature:Undertemperature in Discharge Protection Threshold*** for ***Protections:Temperature:Undertemperature in Discharge Protection Delay*** duration	*Safety Alert B()[UTD]* = 0 *Safety Status B()[UTD]* = 1 and DSG FET can be disabled depending on settings
Recovery	*Safety Status B()[UTD]* = 1 and TS pin ADC measurement ≤ ***Protections:Temperature:Undertemperature in Discharge Protection Recovery***	*Safety Status B()[UTD]* = 0 and DSG FET can be re-enabled based on settings

6.15 Host Watchdog Protection

The BQ76905 device integrates a Host Watchdog (HWD) Protection that triggers a fault when no valid communications are received for a programmable delay HWD_DLY. The HWD_DLY delay is programmable from 1-sec to 16-sec in 1-sec steps and from 20-sec to 976-sec in 4-sec steps, using the ***Settings:Protection:Host Watchdog Timeout*** configuration register. The HWD protection is enabled using the ***Settings:Protection:Enabled Protections B:[HWD]*** configuration bit.

The *Safety Alert B[HWD]* is asserted when no valid communications are received for a time of HWD_DLY / 2. If no valid communications are received for HWD_DLY, *Safety Status B[HWD]* is asserted. When this occurs, the device turns off the DSG FET, the CHG FET, or both FETs if configured for autonomous FET control, based on settings in ***Settings:Protection:DSG FET Protections A[HWD]*** and ***Settings:Protection:CHG FET Protections A[HWD]***. The device recovers when valid communications are received.

6.16 Cell Open Wire Detection

The BQ76905 device supports detecting a disconnection between a cell in the pack and the cell attachment to the PCB containing BQ76905. Without this check, the voltage at the cell input pin of the BQ76905 device can persist for some time on the board-level capacitor, leading to incorrect voltage readings. The Cell Open Wire detection in the BQ76905 device operates by enabling a small current source from each cell to VSS at programmable intervals. If a cell input pin is floating due to an open wire condition, this current discharges the capacitance, causing the voltage at the pin to slowly drop. This drop in voltage can eventually trigger a Cell Undervoltage protection fault on that particular cell, as well as a Cell Overvoltage protection fault on the cell above it. It is important that the cell undervoltage and overvoltage protections be enabled with appropriate threshold settings for the open wire condition to be detected and the desired reaction initiated.

In NORMAL mode, the cell open wire current is enabled, one cell at a time, one cell approximately every ADSCAN, then disabled for COWNTIME FULLSCAN intervals. The parameter COWNTIME is set by the ***Settings:Protection:Cell Open-Wire NORMAL Check Time*** configuration register, and a setting of 0 disables this check entirely. The current source at each cell is only enabled during the Shared Slot measurement (which is programmable in width from 366 µs to 2.93 ms), except that it skips a Shared Slot being used to measure the stack voltage, to avoid corrupting the stack voltage measurement. Only one current source is enabled in one ADSCAN, so in a 5s system it requires 6 ADSCAN intervals to have the current source at each cell enabled (depending on the skipped slots), then the current sources are all disabled for COWNTIME FULLSCAN intervals, before the loop repeats.

This provides programmability in the average current drawn from ≈2 nA to ≈3 µA in NORMAL mode, based on the typical current source value of 55 µA. During SLEEP mode, the cell open wire current source is enabled immediately following the last burst measurement slot in immediate sequence for each cell in selected burst measurements, for the duration of a Shared Slot per cell. The selection of burst measurements is based on

the ***Settings:Protection:Cell Open-Wire SLEEP Check Time[COWSTIME2:0]***. The cell open-wire currents can be enabled or disabled in SLEEP mode using the ***Settings:Protection:Cell Open-Wire SLEEP Check Time[COWSEN]*** configuration bit.

Table 6-19. Cell Open-Wire SLEEP Check Time Settings

Bit Setting COWSTIME[2:0]	Description
0x0	Current sources are activated once every 8 burst measurements
0x1	Current sources are activated once every 4 burst measurements
0x2	Current sources are activated once every 2 burst measurements
0x3	Current sources are activated once every burst measurement
0x4	Current sources are activated twice every burst measurement
0x5	Current sources are activated four times every burst measurement
0x6	Current sources are activated 8 times every burst measurement
0x7	Current sources are activated 16 times every burst measurement

Note

The cell open wire check can create a cell imbalance, so select the settings appropriately.

The turn-on and turn-off of the cell open-wire current source creates a transient at the cell voltage input, and depending on the RC time constant of the input components used at the VC input pins, the transient can affect the accuracy of the Cell 1 measurement in NORMAL mode, which occurs immediately after the Shared Slot when the current source is enabled. In order to overcome this issue, the BQ76905 includes a programmable delay which is inserted between the end of each Shared Slot and the beginning of the cell measurements, to allow sufficient settling for this transient. This delay can be set from 0 to 64 ms by the ***Settings:Protection:Cell Open-Wire SLEEP Check Time[COWDLY]*** configuration parameter, which has a default of 1 ms.

6.17 Voltage Reference Measurement Diagnostic Protection

The BQ76905 device integrates a diagnostic check on the voltage references used by the device. A regular measurement of the internal 1.8-V LDO voltage is included as part of the standard measurement loop in NORMAL and SLEEP modes. As the ADC mux cycles through its periodic measurement loop, it measures this voltage and compares it to the value expected, in order to implement the Voltage Reference Measurement Diagnostic Protection. Since the ADC uses the VREF1 internal reference, while the internal LDO voltage is based on the VREF2 internal reference, this measurement effectively measures one reference using the other reference. Thus, if one of the two references malfunctions and deviates significantly from its expected value, the resulting measurement result changes and allows detection of this condition. When detected, the device triggers a Voltage Reference Diagnostic Fault and sets *0x03 Safety Status B()[VREF]*, if enabled, and the device can disable FETs based on settings in ***Settings:Protection:Both FET Protections B[VREF]***. The fault can be recovered by the host sending the *0x009B PROT_RECOVERY()[DIAGREC]* subcommand. The expected measurement of the 1.8-V LDO in 16-bit codes is 1.8 V / VREF1 × 2 / 5 × 32768 which is approximately 19228. The diagnostic protection alert is triggered whenever the measured result is below 14592 or above 24320. The diagnostic protection status fault is triggered when this occurs for two consecutive measurements.

6.18 VSS Measurement Diagnostic Protection

The BQ76905 device integrates a regular measurement of the VSS voltage as part of the measurement loop, comparing the resulting value to the expected value, in order to implement the VSS Measurement Diagnostic Protection. If the ADC mux were to malfunction and remain fixed on one particular input, whether that being a cell voltage input, a thermistor, or a diagnostic measurement, this measurement of VSS helps ensure this condition is detected. When detected, the device triggers the VSS Diagnostic Protection Fault and sets *0x03 Safety Status B()[VSS]*, if enabled, and the device can disable FETs based on ***Settings:Protection:Both FET Protections B[VSS]***. The fault can be recovered by the host sending the *0x009B PROT_RECOVERY()[DIAGREC]* subcommand. The expected 16-bit measurement of VSS in 16-bit codes is 0. The diagnostic

protection alert is triggered whenever the 16-bit measurement result is beyond ±1625, which is approximately 99 mV / VREF1 × 3 / 5 × 32767. The diagnostic protection status fault is triggered when this occurs for two consecutive VSS measurements.

6.19 REGOUT Diagnostic Protection

The REGOUT LDO integrated in the BQ76905 device includes circuitry to detect an error condition, such as the regulator is in short circuit current limit, or if the die temperature exceeds approximately 120°C. When an error condition is detected, the device disables the REGOUT LDO, triggers the REGOUT Diagnostic Protection Fault, and sets *0x05 Safety Status A()[REGOUT]*, if enabled. The device can disable FETs based on the setting of ***Settings:Protection:Both FET Protections B[REGOUT]***. When an overtemperature condition is detected, the device can transition to SHUTDOWN mode if ***Settings:Configuration:Power Config[OTSD]*** is set. The fault will be recovered if the cause of the error is removed (such as the short circuit is removed or the regulator temperature falls below the overtemperature threshold). This check operates in DEEPSLEEP mode as well as NORMAL and SLEEP modes.

6.20 LFO Oscillator Integrity Diagnostic Protection

The BQ76905 device integrates a special hardware block that monitors if the LFO stops oscillating or deviates significantly in frequency versus its expected value. If this is detected, the device immediately transitions into SHUTDOWN mode if ***Settings:Configuration:Power Config[LFOWD]*** is set. This check operates in DEEPSLEEP mode as well as NORMAL and SLEEP modes.

6.21 Internal Factory Trim Diagnostic Protection

The BQ76905 device performs a check of the digital trim information within the device at initial power up or after any full reset. If an error is detected during this check, the device immediately transitions to SHUTDOWN mode.

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7.1 *0x00 Control Status()* and *0x12 Battery Status()* Commands

The BQ76905 device includes a *0x00 Control Status()* command, which is primarily intended for legacy bqStudio auto-detection and is not recommended for customer usage. The *0x00 Control Status()* command behaves similarly to 0x3E and 0x3F when written, accepting subcommand addresses. When this command is read back immediately after it has been written, it returns 0xFFA5 once.

The device also includes the *0x12 Battery Status()* command, which reports various status information on the pack, as shown below.

Table 7-1. *0x12 Battery Status()* Bit Definitions

Bit	Name	Description
15	SLEEP	This flag asserts if the device is in SLEEP mode 0x0 = Device is not in SLEEP mode 0x1 = Device is in SLEEP mode
14	DEEPSLEEP	This flag asserts if the device is in DEEPSLEEP mode 0x0 = Device is not in DEEPSLEEP mode 0x1 = Device is in DEEPSLEEP mode
13	SA	This flag asserts if an enabled safety alert is present. 0x0 = Indicates an enabled safety alert is not present 0x1 = Indicates an enabled safety alert is present
12	SS	This flag asserts if an enabled safety fault is present. 0x0 = Indicates an enabled safety fault is not present 0x1 = Indicates an enabled safety fault is present
11-10	SEC1:SEC0	SEC1:0 indicate the present security state of the device. . When in SEALED mode, device configuration cannot be read or written and some commands are restricted. . When in FULLACCESS mode, unrestricted read and write access is allowed and all commands are accepted. 0x0 = 0: Device has not initialized yet. 0x1 = 1: Device is in FULLACCESS mode. 0x2 = 2: Unused. 0x3 = 3: Device is in SEALED mode.
9	RSVD0	Reserved
8	FET_EN	This bit is set when the device is in autonomous FET control mode. The default value of this bit is set by the Settings:FET Options[FET_EN] bit in Data Memory upon exit of CONFIG_UPDATE mode. Its value can be modified during operation using the FET_ENABLE() subcommand. 0x0 = Device is not in autonomous FET control mode, FETs are only enabled through manual command. 0x1 = Device is in autonomous FET control mode, FETs can be enabled by the device if no conditions or commands prevent them being enabled.
7	POR	This bit is set when the device fully resets. It is cleared upon exit of CONFIG_UPDATE mode. It can be used by the host to determine if any register configuration changes were lost due to a reset. 0x0 = Full reset has not occurred since last exit of CONFIG_UPDATE mode. 0x1 = Full reset has occurred since last exit of CONFIG_UPDATE and reconfiguration of any register settings is required.

Table 7-1. *0x12 Battery Status()* Bit Definitions (continued)

Bit	Name	Description
6	SLEEP_EN	This bit indicates whether or not SLEEP mode is allowed based on configuration and commands. The [[Power Config[SLEEP_EN]]] bit sets the default state of this bit. The host can send commands to enable or disable SLEEP mode based on system requirements. When this bit is set, the device can transition to SLEEP mode when other SLEEP criteria are met. 0x0 = SLEEP mode is disabled by the host. 0x1 = SLEEP mode is allowed when other SLEEP conditions are met.
5	CFGUPDATE	This bit indicates whether or not the device is in CONFIG_UPDATE mode. It is set after the SET_CFGUPDATE() subcommand is received and fully processed. Configuration settings can be changed only while this bit is set. 0x0 = Device is not in CONFIG_UPDATE mode. 0x1 = Device is in CONFIG_UPDATE mode.
4	ALERTPIN	This bit indicates whether the ALERT pin is asserted (pulled low). 0x0 = ALERT pin is not asserted (stays in hi-Z mode). 0x1 = ALERT pin is asserted (pulled low).
3	CHG	This bit indicates whether the CHG driver is enabled. 0x0 = CHG driver is disabled. 0x1 = CHG driver is enabled.
2	DSG	This bit indicates whether the DSG driver is enabled. 0x0 = DSG driver is disabled. 0x1 = DSG driver is enabled.
1	CHGDETFLAG	This bit indicates the value of the debounced CHG Detector signal. 0x0 = CHG Detector debounced signal is low. 0x1 = CHG Detector debounced signal is high.
0	RSVD0	Reserved

7.2 LDOs

The BQ76905 contains an integrated 1.8-V LDO (REG18) that provides a regulated 1.8 V supply voltage for the device's internal circuitry and digital logic. The supply current for this LDO is drawn from the BAT pin.

The device also integrates a programmable LDO (REGOUT) for external circuitry, such as a host processor or external transceiver circuitry. The REGOUT LDO takes its input from the REGSRC pin, which is generally expected to be connected to the top-of-stack, or can be generated by a separate DC/DC converter in the system. The REGOUT LDO output voltage can be programmed to 1.8 V, 2.5 V, 3.0 V, 3.3 V, or 5.0 V, and it can provide an output current of up to 20 mA if thermal conditions permit.

The REGOUT LDO voltage level is selected using the ***Settings:Configuration:REGOUT Config[REGCTL_2:0]*** configuration bits as shown below. The LDO is enabled using the ***Settings:Configuration:REGOUT Config[REG_EN]*** configuration bit, and its setting can be modified during operation using the *0x69 REGOUT Control()* command.

The REGOUT LDO can be programmed to either remain disabled or power up automatically whenever the device exits SHUTDOWN mode, depending on OTP configuration. When the REGOUT LDO is disabled, its output is pulled to VSS with an internal resistance of approximately 2.5-kΩ while the device is in NORMAL, SLEEP, or DEEPSLEEP modes. If the LDO is configured based on OTP settings to be powered, then at each later power-up the device autonomously loads the OTP settings and enable the LDO as configured, without requiring communications first.

The REGOUT LDO can also be powered down for a programmable time period, then automatically repowered when the timer expires or any bit in *0x62 Alarm Status()* asserts. For more details on the options available, see the *0x0094 PROG_TIMER()* subcommand.

The BQ76905 is designed to operate properly with a die temperature up to 110°C; therefore, the system design must avoid drawing excessive current from the REGOUT LDO if it could result in the die temperature exceeding this level. For example, with an ambient temperature of 60°C, a stack voltage of 22.5 V, and LDO programmed to an output voltage of 2.5 V, the device dissipates approximately 400 mW when supplying 20 mA of load current. The package thermal impedance can be used to then calculate the resulting die temperature. If this exceeds the device's specified temperature range, the load current must be limited in the system. The BQ76905

REGOUT LDO includes an overtemperature detector, which detects if the die temperature exceeds a level of approximately 120°C and automatically causes the LDO to shutdown. If the ***Settings:Configuration:Power Config[OTSD]*** bit is set, the entire device enters SHUTDOWN mode.

Table 7-2. REGOUT LDO Voltage Settings from *Settings:Configuration:REGOUT Config* and *0x69 REGOUT Control()*

REGCTL[2:0] or REGOUTV[2:0]	REGOUT Voltage (V)
0x0 - 0x3	1.8
0x4	2.5
0x5	3.0
0x6 (default)	3.3
0x7	5.0

7.3 ALERT Pin Operation

The BQ76905 includes functionality to generate an alarm signal at the ALERT pin, which can be used as an interrupt to a host processor. The ALERT pin is an open-drain pin which is pulled low by the device whenever an alarm signal is generated. The alarm signal is an OR of all bits in the *0x62 Alarm Status()* result. The alarm function includes a programmable mask (set using *0x66 Alarm Enable()*), to allow the customer to decide which flags or events can trigger an alarm. The instantaneous, unlatched bits available to trigger an alarm can be read from the *0x64 Alarm Raw Status()* command, these bits are described in the table below.

Table 7-3. Alarm Options

Name	Description
SSA	This bit is set when a bit in *0x03 Safety Status A()* is set
SSB	This bit is set when a bit in *0x05 Safety Status B()* is set
SAA	This bit is set when a bit in *0x02 Safety Alert A()* is set
SAB	This bit is set when a bit in *0x04 Safety Alert B()* is set
XCHG	This bit is set when the CHG FET is off.
XDSG	This bit is set when the DSG FET is off.
SHUTV	Stack voltage is below ***Power:Shutdown:Shutdown Stack Voltage*** or a cell voltage is below ***Power:Shutdown:Shutdown Cell Voltage***.
CB	This bit is set when cell balancing is active.
FULLSCAN	Fullscan Complete. The necessary multiple ADSCANs have been completed to collect the fullscan measurement loop data. This bit in *0x64 Alarm Raw Status()* pulses momentarily each time a fullscan completes.
ADSCAN	Voltage ADSCAN Complete. A single ADC ADSCAN is complete (cell voltages and current are measured on each ADSCAN). This bit in *0x64 Alarm Raw Status()* pulses momentarily each time a cell voltage ADC scan completes.
WAKE	This bit is set when the device is wakened from SLEEP mode.
SLEEP	This bit in *0x64 Alarm Raw Status()* pulses momentarily when the device enters SLEEP mode.
TIMER_ALARM	This bit in *0x64 Alarm Raw Status()* pulses momentarily when the programmable timer expires.
INITCOMP	This bit in *0x64 Alarm Raw Status()* pulses momentarily when the device completes the startup measurement sequence (which occurs as powerup, reset, exit of CONFIG_UPDATE mode, and exit of DEEPSLEEP).
CDRAW / CDTOGGLE	This bit in *0x64 Alarm Raw Status()* is CDRAW, the value of the CHG Detector output. The corresponding bit in *0x62 Alarm Status()* is CDTOGGLE, which is set whenever the debounced version of CDRAW changes state from the previous latched state.

Table 7-3. Alarm Options (continued)

Name	Description
POR	This bit reflects the POR bit in *0x12 Battery Status()*. It is set when the device is first powered up, and is cleared when CONFIG_UPDATE mode is exited. If the host initializes settings at each device power up, monitoring this bit can alert the host that a reset has occurred and the device needs to be reinitialized.

The *0x64 Alarm Raw Status()* command provides the unlatched instantaneous value of each signal listed above. For each signal that is specified by the masking to be included in the alarm, when the bit in *0x64 Alarm Raw Status()* is asserted, the bit is latched into the *0x62 Alarm Status()* register, and the ALERT pin is asserted (pulled low) if any bit in *0x62 Alarm Status()* is asserted. When the host receives the interrupt from the ALERT pin pulled low, the host can read the *0x62 Alarm Status()* register to determine which flag has caused the alarm. The host can then write to the *0x62 Alarm Status()* command with the corresponding bits set, and the corresponding flags are unlatched.

The default alarm mask is set by the ***Settings:Configuration:Default Alarm Mask*** data memory value. This mask can be changed during operation using the *0x66 Alarm Enable()* command, to mask or unmask individual bits from generating an alarm signal.

Several of the bits in *Alarm Raw Status()* only pulse momentarily when an event occurs, so are not intended to be monitored by reading *0x64 Alarm Raw Status()*. This includes *[WAKE]*, *[SLEEP]*, *[ADSCAN]*, *[FULLSCAN]*, *[INITCOMP]*, and *[TIMER_ALARM]*. If these bits are included by mask setting in the *0x62 Alarm Status()*, then the corresponding bits in *0x62 Alarm Status()* latch and remain asserted until cleared by the host.

The host can include the *[ADSCAN]* or *[FULLSCAN]* bits into *0x62 Alarm Status()* to determine when data from a new measurement loop scan is available. Similarly, if the *[WAKE]* and *[SLEEP]* bits are included into *0x62 Alarm Status()*, this allows the host to get a single interrupt on the ALERT pin whenever the device changes from NORMAL to SLEEP mode or from SLEEP to NORMAL mode.

7.4 TS Pin Operation

The TS pin on the BQ76905 device can be connected to an external thermistor for temperature measurement or can be used as a general purpose ADC input (ADCIN mode). When used for thermistor measurement, the thermistor is connected between the TS pin to VSS, and the pin is internally connected to a 20-kΩ trimmed pullup resistor, which is biased by the internal 1.8V LDO (REG18) voltage. The voltage at the TS pin is digitized by the ADC using the same 1.8-V LDO voltage as the ADC reference, thereby implementing a ratiometric measurement. When the pin is configured for ADCIN mode, the 20-kΩ pullup resistor is disconnected, and the ADC uses VREF1 for its reference.

The selection between the two modes is made using the ***Settings:Configuration:DA Config[TSMODE]*** bit. When the bit is set, the TS pin operates in thermistor measurement mode, versus when the bit is cleared it operates in ADCIN mode.

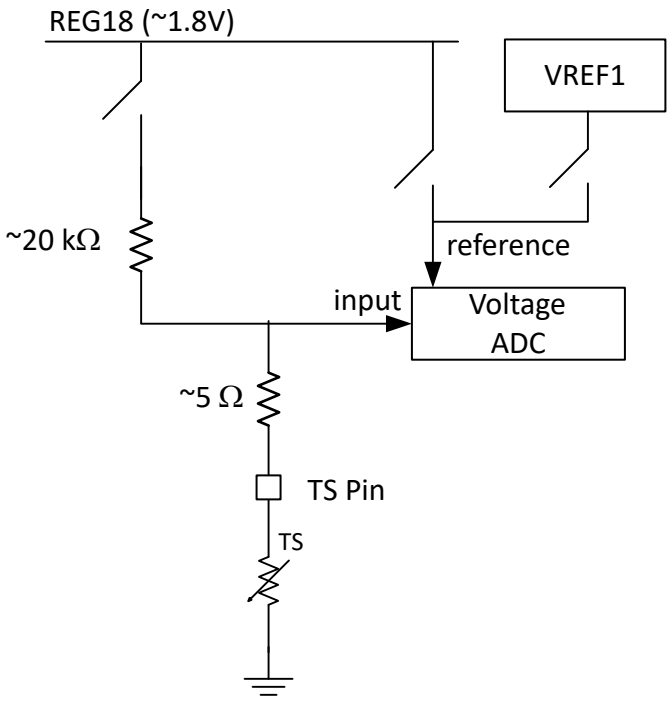

Figure 7-1. BQ76905 TS Pin Configuration

The output of the TS pin ADC measurement is provided by the *0x2A TS Measurement()* command. When the pin is configured for thermistor mode, the LSB size of the resulting data is given by

$1\ LSB_{Thermistor\ Mode} \cong 5 / 3 \times V_{REG18} / 2^{N-1} \approx 5 / 3 \times 1.8\ V / 2^{15} = 92\ \mu V$

When the pin is configured for ADCIN mode, the LSB size of the resulting data is given by

$1\ LSB_{ADCIN\ Mode} \cong 5 / 3 \times V_{REF1} / 2^{N-1} \approx 5 / 3 \times 1.1962\ V / 2^{15} = 61\ \mu V$

When the TS pin is configured for thermistor measurement the device enables the internal pullup resistor only while the pin is being measured (which is the default recommended setting). Alternatively, the pullup resistor can be biased continuously by sending the *0x69 REGOUT_CONTROL()* command with the *[TS_ON]* bit set.

7.5 Programmable Timer

The BQ76905 integrates a programmable timer which can operate in NORMAL, SLEEP, and DEEPSLEEP modes, and supports a time setting from 250 ms to 4 seconds in 250-ms increments, and from 5 seconds up to 243 seconds in 1-second increments. When the timer expires, the *0x64 Alarm Raw Status()[TIMER_ALARM]* bit is pulsed and can generate an alarm on *0x62 Alarm Status()[TIMER_ALARM]* and the ALERT pin, depending on the masking set by *0x66 Alarm Enable()[TIMER_ALARM]*.

The timer can also be configured to automatically disable the REGOUT LDO when it is initiated, and to re-enable the LDO when the timer expires or if any alarm in *0x66 Alarm Enable()* is asserted. The timer is initiated by sending the *0x0094 PROG_TIMER()* subcommand, with parameters described below. The subcommand is accessible in SEALED and FULLACCESS modes.

Table 7-4. *0x0094 PROG_TIMER()* Parameters

Bits	Name	Description
15:12	RSVD0	Reserved, write only 0 to these bits
11	REGOUT_ALARM_WK	0 (default) = Do not re-enable the REGOUT LDO if any bit in *0x62 Alarm Status()* asserts while the timer is running. 1 = If *[REGOUT_SD]*=1 and any bit in *0x62 Alarm Status()* asserts while the timer is running, re-enable the REGOUT LDO based on the setting of *REGOUT Control()*.

Table 7-4. *0x0094 PROG_TIMER()* Parameters (continued)

Bits	Name	Description
10:9	REGOUT_SD_DLY	Delay before REGOUT is disabled when the timer is initiated while REGOUT is powered, and *[REGOUT_SD]*=1. 0x0 (default) = Zero delay. 0x1 = 250ms delay. 0x2 = 1-sec delay. 0x3 = 4-sec delay.
8	REGOUT_SD	0 (default) = do not disable the REGOUT LDO when command is sent. 1 = disable the REGOUT LDO when the timer is initiated, after delay of *[REGOUT_SD_DLY]*. When the timer expires, re-enable the REGOUT LDO based on the setting of *REGOUT Control()*.
7:0	PROG_TMR	Timer value programmable from 250 ms to 4 seconds in 250 ms increments (settings 1 to 16), and from 5 seconds to 243 seconds in 1 second increments (settings 17 to 255). A setting of zero disables the timer. Whenever this field is written with a non-zero value, it initiates the timer.

If the timer is running and the *0x0094 PROG_TIMER()* subcommand is sent with *[PROG_TMR]* = 0x00, then the timer is aborted and the REGOUT LDO is re-enabled if it was initially powered and *[REGOUT_SD]* =1. In this case, however, *0x64 Alarm Raw Status()[TIMER_ALARM]* is not pulsed, so an alarm is not generated.

Note that if *[REGOUT_SD]* =1, then while the timer is running the REGOUT LDO is disabled irrespective of the setting of *REGOUT Control()*.

If the timer is active, the LFO stays powered while the device is in DEEPSLEEP mode, independent of the ***Settings:Configuration:Power Config[DPSLP_LFO]*** data memory setting.

7.6 Device Event Timing

The timing of events in the BQ76905 device varies based on the specific event. Several events and their associated timing are described below. Timings described below do not include the delays related to individual protections, as described in their respective sections.

Table 7-5. Timing of Events

Event Description	Timing
I^2C communications active after initial power-up	< 3 ms
First startup sequence measurements available after initial power-up (*0x64 Alarm Raw Status() [INITCOMP]* is asserted)	8.6 ms
Protections evaluated and FETs enabled after initial power-up (tested using OTP configuration setup to allow autonomous FET control)	8.6 ms
0x62 Alarm Status()[SSA] asserted, ALERT pin asserted due to *0x62 Alarm Status()[SSA]*.	Fast response, in NORMAL or SLEEP modes
Data (including cell voltages, *0x3C CC1 Current()*, *0x3A Current()*, and *0x36 Raw Current()*) calculated after measurements complete.	Fast response, in NORMAL or SLEEP modes
FET turn-off based on enabled protection fault and configured for autonomous FET control.	Fast response, in NORMAL or SLEEP modes
CHG FET turn-on based on current wake detector triggered while in SLEEP mode.	Fast response, in SLEEP mode
Evaluation if SHUTDOWN mode is entered due to temperature beyond ***Power:Shutdown:Shutdown Temperature***	Evaluated after every Internal Temperature measurement in NORMAL mode, or burst measurement in SLEEP mode

Table 7-5. Timing of Events (continued)

Event Description	Timing
0x3C CC1 Current() measurement completes	In NORMAL mode, occurs every 250 ms with *[CCMODE]* = 0 or 1, or every 4 seconds with *[CCMODE]* = 1.

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Chapter 8

Operational Modes

8.1 Overview of Operational Modes

This device supports four operational modes, to support optimized features and power dissipation, with the device able to transition between modes either autonomously or controlled by a host processor.

- NORMAL mode: In this mode, the device performs frequent measurements of system current, cell voltages, internal and thermistor temperature, and various other voltages, operates protections as configured, and provides data and status updates. Battery protections are enabled, and the FET drivers are typically enabled (in the absence of any protection fault).
- SLEEP mode: In this mode, the device performs measurements, calculations, and data updates in adjustable time intervals. Between the measurement intervals, the device is operating in a reduced power state to minimize total average current consumption. Battery protections are still enabled (with modified timing for those using the ADC), and the DSG FET driver (and the CHG FET driver depending on setting) is typically enabled (in the absence of any protection fault).
- DEEPSLEEP mode: In this mode, the FET drivers are disabled, all battery protections are disabled, and no current, voltage, or temperature measurements are taken. The REGOUT LDO can be optionally kept powered, in order to maintain power to external circuitry, such as a host processor. The programmable timer can optionally be used to wake the device and REGOUT LDO after a programmed time interval.
- SHUTDOWN mode: The device is completely disabled (including the internal 1.8 V and REGOUT LDOs), the CHG and DSG FETs are both disabled, all battery protections are disabled, and no measurements are taken. This is the lowest power state of the device, which can be used for shipment or long-term storage. All register settings (other than settings programmed into OTP by TI) are lost when in SHUTDOWN mode.

The device also includes a CONFIG_UPDATE mode, which is used for parameter updates. Transitioning between operational modes is shown in BQ76905 Operational Power Modes.

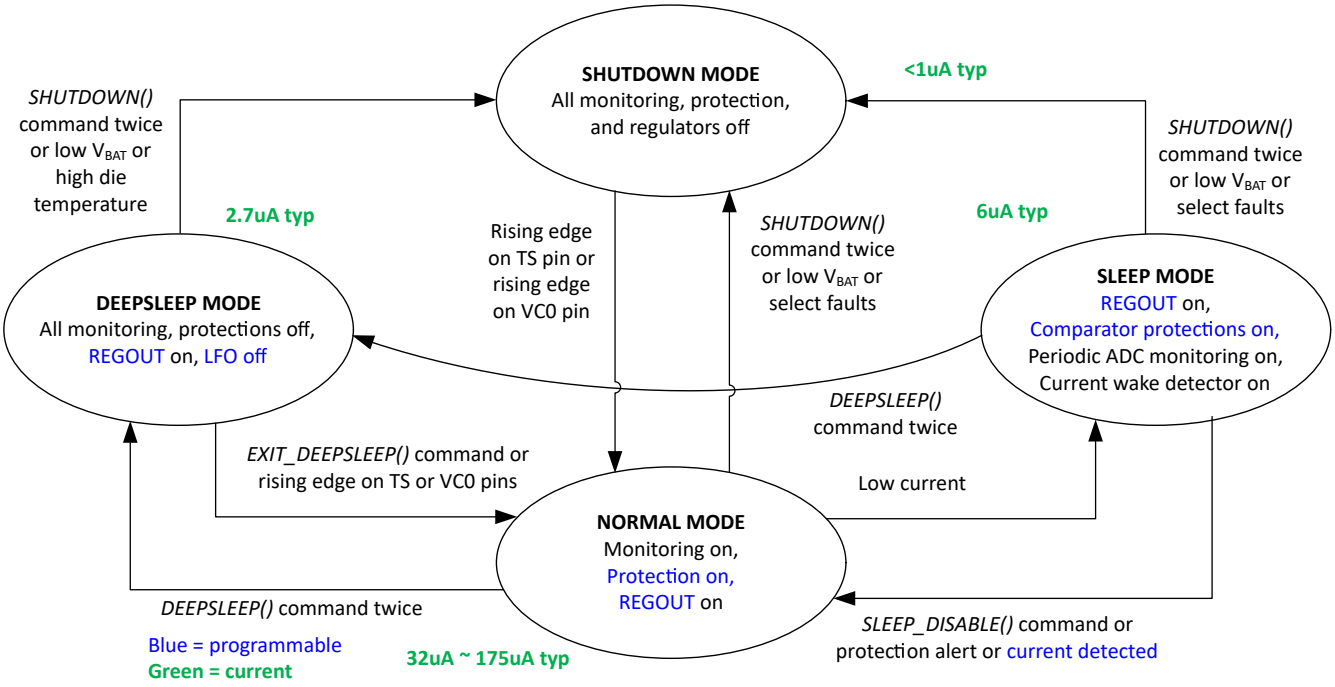

Figure 8-1. BQ76905 Operational Power Modes

8.2 NORMAL Mode

NORMAL mode is the highest performance mode of the device, in which the device is making regular measurements of voltage, current, and temperature, the LFO (low frequency oscillator) is operating, and the internal logic is powered for data processing and control. Full battery protections are operating, based on device configuration settings. Measurements of cell voltages, current, temperature, and other parameters are taken continuously, with timing determined by settings. If measurements are not required at the continuous rate, the ***Settings:Configuration:Power Config[LOOP_SLOW]*** parameter can be used to reduce the measurement rate and also reduce supply current.

The device is generally in NORMAL mode whenever any active charging or discharging is underway. When the current measurement falls below a programmable current threshold given by ***Power:Sleep:Sleep Current***, the system is considered in relax mode, and the device can autonomously transition into SLEEP mode, depending on the configuration. The device includes a current wake detector, which triggers the device to exit SLEEP mode and return to NORMAL mode if a current in excess of a programmable threshold is detected.

8.3 SLEEP Mode

SLEEP mode is a reduced functionality state that can be optionally used to reduce power dissipation when there is little or no system load current or charging in progress, but still provides voltage at the battery pack terminals to keep the system alive. At initial power up, the ***Settings:Configuration:Power Config[SLEEP]*** bit determines whether the device is allowed to enter SLEEP mode. After initialization, SLEEP mode can be allowed or disallowed using the *0x0099 SLEEP_ENABLE()* and *0x009A SLEEP_DISABLE()* subcommands. The *0x12 Battery Status()[SLEEP]* bit indicates whether the device is presently in SLEEP mode or not. The *0x62 Alarm Status()[SLEEP]* and *0x62 Alarm Status()[WAKE]* bits can be used to generate an interrupt to the host when the device operating state changes between SLEEP and NORMAL modes.

When the magnitude of the *0x3C CC1 Current()* measurement falls below a programmable current threshold given by ***Power:Sleep:Sleep Current***, the system is considered in relax mode, and the device autonomously transitions into SLEEP mode, if settings permit. During SLEEP mode, comparator-based protections operate the same as during NORMAL mode. ADC-based current, voltage, and temperature measurements are taken every ***Power:Sleep:Voltage Time*** seconds. When the device is configured such that *0x3C CC1 Current()* is not

available, the device uses the current wake detector to decide when to enter and exit SLEEP mode using the ***Power:Sleep:Wake Comparator Current*** setting.

The device exits SLEEP mode if a protection alert occurs or significant current is detected, or the *0x009A SLEEP_DISABLE()* subcommand is sent. The current is checked by the current wake detector approximately every 2.44 ms and, if it exceeds ***Power:Sleep:Wake Comparator Current*** in magnitude, the device transitions back to NORMAL mode. When exiting based on current flow, the device first runs a SLEEP mode measurement cycle, then restarts the NORMAL mode measurement loop.

The device also includes a 10-second hysteresis on the SLEEP mode entrance, in order to avoid the device quickly entering and exiting SLEEP mode based on a dynamic load. After transitioning from SLEEP mode to NORMAL mode, the device does not enter SLEEP mode again for 10 seconds.

8.4 DEEPSLEEP Mode

The BQ76905 integrates a DEEPSLEEP mode, which is a low power mode that allows the REGOUT LDO and/or the programmable timer to remain powered, but disables most other subsystems. In this mode, the protection FETs are all disabled, so no voltage is provided at the battery pack terminals. All protections are disabled, and all voltage, current, and temperature measurements are disabled. Exceptions to this are the REGOUT Check and LFO Integrity Check, which can still detect a fault, generate a status flag, and can result in the device transitioning to SHUTDOWN mode, depending on settings.

DEEPSLEEP mode can be entered by sending the *0x000F DEEPSLEEP()* subcommand twice in a row within a 4-sec time window. The device exits DEEPSLEEP mode and returns to NORMAL mode if the *0x000E EXIT_DEEPSLEEP()* subcommand is sent, or if a rising edge is generated at the TS pin or VC0 pin. In addition, if the internal 1.8-V LDO goes into power-on-reset (which can occur if the BAT pin voltage falls to an excessively low level) or the internal hardware overtemperature detector detects an excessive die temperature, the device transitions to SHUTDOWN mode.

When the device exits DEEPSLEEP mode, it first completes a Startup Sequence measurement and evaluates conditions relative to enabled protections, to ensure that conditions are acceptable to proceed to NORMAL mode.

The REGOUT LDO maintains its power state when entering DEEPSLEEP mode. The LFO is disabled during DEEPSLEEP mode based on the setting of ***Settings:Configuration:Power Config[DPSLP_LFO]***. If the LFO is powered down, it is wakened by I^2C communications, which can result in a longer than normal clock stretch before the device responds.

Other than the *0x000E EXIT_DEEPSLEEP()* subcommand, communications with the device over the serial interface do not cause it to exit DEEPSLEEP mode. However, because no measurements are taken while in DEEPSLEEP mode, there is no new information available for readout. To collect measurement data without powering the system, the user can do the following:

1. Send the *0x68 FET_CONTROL()* command to keep the FETs disabled.
2. Send the *0x000E EXIT_DEEPSLEEP()* subcommand to transition back into NORMAL mode.
3. Wait for a measurement cycle to complete by monitoring the *0x62 Alarm Status()[ADSCAN]* or *0x62 Alarm Status()[FULLSCAN]* bits.
4. Read the data.
5. Send the *0x000F DEEPSLEEP()* subcommand twice within 4-sec to return to DEEPSLEEP mode.
6. Send the *0x68 FET_CONTROL()* command to unblock the FETs from being enabled when DEEPSLEEP mode is exited in the future.

If the LFO is programmed to be off in DEEPSLEEP mode, I^2C communications cause it to power up at each transaction. To avoid a long clock stretch at every transaction in a short burst of transactions, the LFO includes a hysteresis such that it does not power back down after being wakened in DEEPSLEEP for approximately 25 ms.

8.5 SHUTDOWN Mode

SHUTDOWN mode is the lowest power mode of the BQ76905, which can be used for shipping or long term storage. In this mode, the device loses all register state information (except for what has been programmed into OTP by TI), the internal logic is powered down, the protection FETs are all disabled, so no voltage is provided at the battery pack terminals. All protections are disabled, all voltage, current, and temperature measurements are disabled, and no communications are supported. When the device exits SHUTDOWN mode, it reads any parameters stored in OTP. If the OTP has not been programmed (this is only supported by TI), the device powers up with default settings, and then settings can be changed by the host writing device registers.

Entering SHUTDOWN mode involves a sequence of steps. The sequence can be initiated manually by sending the *0x0010 SHUTDOWN()* subcommand twice within 4 seconds. The device can also be configured to enter SHUTDOWN mode automatically based on the top of stack voltage or the minimum cell voltage. If the top-of-stack voltage falls below ***Power:Shutdown:Shutdown Stack Voltage*** or if the minimum cell voltage falls below ***Power:Shutdown:Shutdown Cell Voltage***, the SHUTDOWN mode sequence is automatically initiated (this is only evaluated in NORMAL or SLEEP modes when measurements are being taken). The shutdown based on cell voltage only applies to cell input pins being used for actual cells, based on settings in ***Settings:Configuration:Vcell Mode***.

While the BQ76905 is in NORMAL mode or SLEEP mode, the device can also be configured to enter SHUTDOWN mode if the internal temperature measurement exceeds ***Power:Shutdown:Shutdown Temperature***.

When the SHUTDOWN mode sequence has been initiated by the *0x0010 SHUTDOWN()* subcommand (twice within 4 seconds) or by stack voltage measured below ***Power:Shutdown:Shutdown Stack Voltage*** or a cell voltage measured below ***Power:Shutdown:Shutdown Cell Voltage***, the device waits for 10 seconds to disable the protection FETs, then proceed toward SHUTDOWN mode. Sending the *0x0010 SHUTDOWN()* subcommand a third time bypasses this delay. When SHUTDOWN mode is initiated in this manner, the device first transitions to NORMAL mode and blocks entrance to SLEEP mode. If the FETs were initially off (such as if the device was in DEEPSLEEP mode), the FETs remain off. At this first transition to NORMAL mode from SLEEP or DEEPSLEEP mode, the device clears the *BatteryStatus()[FET_EN]* bit, so if the FETs are disabled, they are not autonomously re-enabled. The host can send *FET_ENABLE()* to reassert this bit if desired. When the device transitions to NORMAL mode from DEEPSLEEP mode in preparation for entering SHUTDOWN, the device also effectively sets the *FET_CONTROL()[DSG_OFF]* and *[CHG_OFF]* bits, so the FETs remain disabled until the host elects to modify them.

During this 10 second shutdown delay, the device does not abort entering SHUTDOWN if the voltages rise back above the shutdown thresholds. If the host reads the system voltages and prefers to abort the SHUTDOWN entry, it can send either the *0x000E EXIT_DEEPSLEEP()* or the *0x0012 RESET()* commands, and the device restarts with default settings.

When the device is wakened from SHUTDOWN, it requires < 10 ms for the internal circuitry to power up, load settings from OTP memory, perform initial measurements, evaluate those relative to enabled protections, then to enable FETs if conditions allow.

The BQ76905 integrates a hardware overtemperature detection circuit, which determines when the die temperature passes an excessive temperature of approximately 120°C. If this detector triggers, the device automatically begins the sequence to enter SHUTDOWN if the ***Settings:Configuration:Power Config[OTSD]*** configuration bit is set.

The BQ76905 wakes from SHUTDOWN if a voltage is applied at the TS pin above a level of approximately 1 V or a voltage is applied at the VC0 pin above a level of approximately 1.2 V. If the shutdown sequence has been initiated, but the device detects the wakeup criteria is present, then the device stays in a "soft shutdown" state until the wakeup criteria has been removed. While in "soft shutdown", FETs are disabled, and protections and measurements are stopped. The device exits "soft shutdown" when conditions allow the device to continue into SHUTDOWN mode. If the host wants to abort the entry into SHUTDOWN mode, the *EXIT_DEEPSLEEP()* command can be written, and the device restarts operation as if returning from a POR.

8.6 CONFIG_UPDATE Mode

The BQ76905 uses a special CONFIG_UPDATE mode to make changes to the data memory settings. Note that this mode is not available for device versions programmed **and sealed** by TI. Changes made to the data memory settings while the normal measurement and protection functions are in operation can result in unexpected operation or consequences if settings used by the logic change in the midst of operation. When changes to the data memory settings are needed (which generally is only done on the customer manufacturing line or in an offline condition), the host must:

1. Send a command (such as *FET_CONTROL()*) to disable the protection FETs if they are enabled.
2. Place the device into CONFIG_UPDATE mode by sending the *0x0090 SET_CFGUPDATE()* subcommand.
3. Wait for the *0x12 Battery Status()[CFGUPDATE]* flag to set.
4. Modify settings as needed by writing updated data memory settings.
5. Send the *0x0092 EXIT_CFGUPDATE()* command to resume normal operation.

When in CONFIG_UPDATE mode, the device stops normal operation and stops all measurements and protection monitoring (the protection comparator subsystem is disabled). The host can then make changes to data memory settings. After changes are complete, the host then sends the *0x0092 EXIT_CFGUPDATE()* command, at which point the device restarts normal operation using the new data memory settings. As soon as the device enters CONFIG_UPDATE mode, all protection alerts and status faults are cleared. When the device exits CONFIG_UDPATE mode, it performs the startup measurement sequence to determine if any protection faults are present.

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Chapter 9

I²C Serial Communications

9.1 I²C Serial Communications Interface

The I²C serial communications interface in the BQ76905 device acts as a target device and supports rates up to 400 kHz with an optional CRC check. The BQ76905 initially powers up by default with CRC disabled, which is determined by the OTP settings factory programmed by TI. The host can change the CRC mode setting while in CONFIG_UPDATE mode, then the new setting takes effect upon exit of CONFIG_UPDATE mode.

The I²C device address (as an 8-bit value including target address and R/W bit) is set by default as 0x10 (write), 0x11 (read), which can be changed by the ***Settings:Configuration:I2C Address*** configuration setting.

The communications interface includes programmable timeout capability, with the internal I²C bus logic reset when an enabled timeout occurs:

- SCL Short Low Timeout - triggers if SCL stays low for approximately 25 ms. Enabled when ***Settings:Configuration:I2C Config[I2CCSLTO]*** is set.
- SCL Long Low Timeout - triggers if SCL stays low for a duration given by TLLO. TLLO is programmable using ***Settings:Configuration:I2C Config[I2CLLTOT2:0]*** as 0x0 = timeout is disabled, 0x1 = 0.5 sec, 0x2 = 1 sec, 0x3 = 1.5 sec, 0x4 = 2 sec, 0x5 = 2.5 sec, 0x6 = 3 sec, 0x7 = 3.5 sec. To use this timeout, ***Settings:Configuration:I2C Config[I2CLLTO]*** must be cleared.

An I²C write transaction is shown in I²C Write. Block writes are allowed by sending additional data bytes before the Stop. The I²C logic auto-increments the register address after each data byte. The shaded regions show when the device can clock stretch.

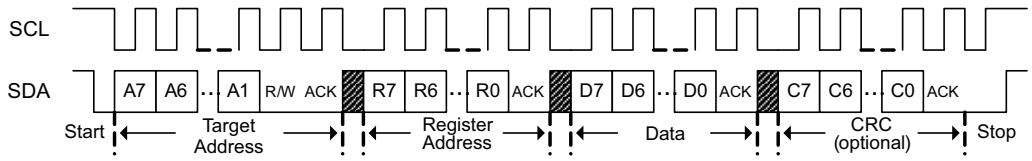

Figure 9-1. I²C Write

The CRC check is enabled by setting the ***Settings:Configuration:I2C Config[CRC]*** data memory bit. When enabled, the CRC is calculated as follows:

- The CRC is reset after each data byte and after each stop.
- In a single-byte write transaction, the CRC is calculated over the target address, register address, and data.
- In a block write transaction, the CRC for the first data byte is calculated over the target address, register address, and data. The CRC for subsequent data bytes is calculated over the data byte only.

The CRC polynomial is $x^8 + x^2 + x + 1$, and the initial value is 0.

When the target detects an invalid CRC, the I²C target NACKs the CRC, which causes the I²C target to go to an idle state.

I²C Read with Repeated Start shows a read transaction using a Repeated Start. The shaded regions show when the device can clock stretch.

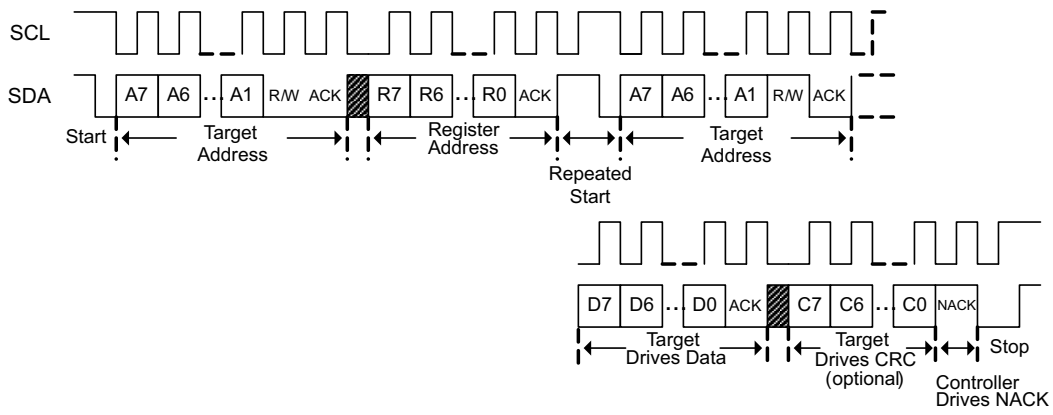

Figure 9-2. I²C Read with Repeated Start

I²C Read without Repeated Start shows a read transaction where a Repeated Start is not used, for example if not available in hardware. For a block read, the controller ACKs each data byte except the last and continues to clock the interface. The I²C block auto-increments the register address after each data byte. The shaded regions show when the device can clock stretch.

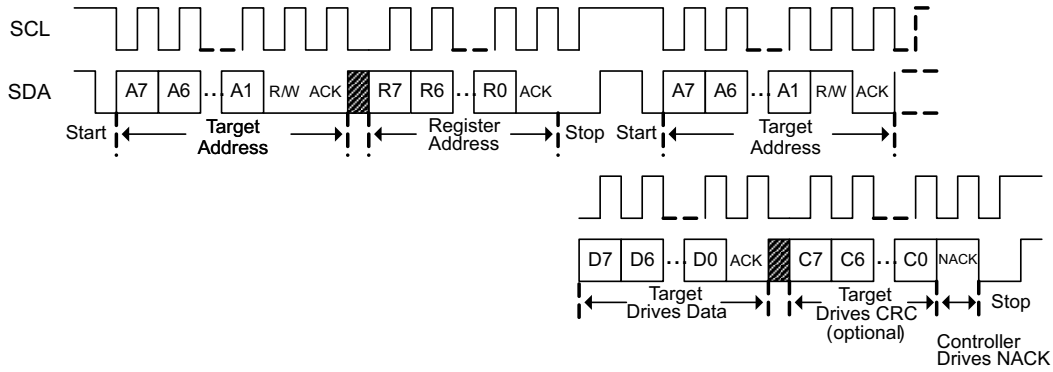

Figure 9-3. I²C Read without Repeated Start

When enabled, the CRC for a read transaction is calculated as follows:

- The CRC is reset after each data byte and after each stop.
- In a single-byte read transaction using a repeated start, the CRC is calculated beginning at the first start and includes the target address, the register address, then the target address with read bit set, then the data byte.
- In a single-byte read transaction using a stop after the initial register address, the CRC is reset after the stop and only includes the target address with read bit set and the data byte.
- In a block read transaction using repeated starts, the CRC for the first data byte is calculated beginning at the first start and includes the target address, the register address, then the target address with read bit set, then the data byte. The CRC for subsequent data bytes is calculated over the data byte only.
- In a block read transaction using a stop after the initial register address, the CRC is reset after the stop and only includes the target address with read bit set and the first data byte. The CRC for subsequent data bytes is calculated over the data byte only.

The CRC polynomial is $x^8 + x^2 + x + 1$, and the initial value is 0.

When the controller detects an invalid CRC, the I²C controller NACKs the CRC, which causes the I²C target to go to an idle state.

Chapter 10
Cell Balancing

10.1 Cell Balancing

The BQ76905 supports passive cell balancing by bypassing the current of a selected cell during charging or at rest, using either integrated bypass switches between cells, or external bypass FETs or BJTs. Balancing must be initiated and controlled manually from a host processor.

Adjacent as well as non-adjacent cells can be balanced. Balancing is controlled using the *0x0083 CB_ACTIVE_CELLS()* subcommand sent by the host. When balancing is initiated using this subcommand, the device starts a timer and begins balancing the specified cells for up to 20 seconds. The timer is reset if a new balancing subcommand is issued. This is included as a precaution, in case the host processor initiated balancing but then stopped communication with the BQ76905, so that balancing does not continue indefinitely. The host can write 0x00 to the subcommand to disable balancing. When this subcommand is read, it reports a bit mask of which cells are being actively balanced.

The *0x0083 CB_ACTIVE_CELLS()* subcommand is accessible in SEALED mode, to avoid the need for the pack to be unsealed in the field in order to initiate balancing. If balancing is not used, writes to this subcommand can be disabled by setting the ***Settings:Cell Balancing:Balancing Configuration[CB_NO_CMD]*** configuration bit.

The device disables balancing if the ADC measurement of a thermistor (if the TS pin is configured for thermistor measurement) is above ***Settings:Cell Balancing:Min Temp Threshold*** (the threshold for the minimum temperature) or below ***Settings:Cell Balancing:Max Temp Threshold*** (the threshold for the maximum temperature) or the internal die temperature of the device exceeds a programmable threshold set by ***Settings:Cell Balancing:Max Internal Temp***. However, the customer must still carefully analyze the thermal effect of the balancing on the device in system. Based on the planned ambient temperature of the device during operation and the thermal properties of the package, the maximum power must be calculated that can be dissipated within the device and still ensure operation remains within the recommended operating temperature range. The cell balancing configuration can then be determined such that the device power remains below this level by reducing the number of cells being balanced simultaneously, or by reducing the balancing current of each cell by appropriate selection of the external resistance in series with each cell.

Cell Balancing Timing

Due to the current that flows into the cell input pins on the BQ76905 while balancing is active, cell voltage measurements cannot be made without disabling balancing temporarily. Therefore, the timing for measurement of cell voltages and evaluation of cell voltage protections by the device is modified during balancing. While balancing of any cell is active, the balancing FETs are disabled temporarily during each ADSCAN while the cell voltages are being measured, as well as during the Shared Slot measurement.

In order to meet the need for regular measurements while cell balancing is underway, the ***Settings:Configuration:Power Config[CB_LOOP_SLOW[1:0]]*** configuration bits modify the cell voltage measurement timing when cell balancing is active, to increase the average balancing current. This modification involves replacing the measurements in selected ADSCANs with idle slots of the same width, to allow balancing to remain active a higher percentage of the time.

If ***CB_LOOP_SLOW[1:0]*** = 0b00, the voltage measurements in every other ADSCAN are replaced with idle slots of the same time duration. This allows balancing to be enabled during an entire "idle" ADSCAN. Balancing remains off during the "active" ADSCAN when voltage measurements are enabled. Therefore this setting

allows balancing to be enabled almost 50% of the time (balancing is disabled one slot before any voltage measurement, thus is off for all slots of the "active" ADSCAN and for one slot in the "idle" ADSCAN just before the "active" ADSCAN begins).

If ***CB_LOOP_SLOW[1:0]*** = 0b01, the voltage measurements in three of every four ADSCANs are replaced with idle slots of the same time duration. This allows balancing to be enabled during each "idle" ADSCAN. Balancing remains off during the "active" ADSCAN that still has voltage measurements enabled. Therefore this setting allows balancing to be enabled approximately 75% of the time (balancing is disabled one slot before any voltage measurement, thus is off for all slots of the "active" ADSCAN and for one slot in the "idle" ADSCAN just before the "active" ADSCAN).

If ***CB_LOOP_SLOW[1:0]*** = 0b10, the voltage measurements in seven of every eight ADSCANs are replaced with idle slots of the same time duration. This allows balancing to be enabled during each "idle" ADSCAN. Balancing remains off during the "active" ADSCAN that still has voltage measurements enabled. Therefore this setting allows balancing to be enabled approximately 87% of the time (balancing is disabled one slot before any voltage measurement, thus is off for all slots of the "active" ADSCAN and for one slot in the "idle" ADSCAN just before the "active" ADSCAN).

If ***CB_LOOP_SLOW[1:0]*** = 0b11, the voltage measurements in 15 of every 16 ADSCANs are replaced with idle slots of the same time duration. This allows balancing to be enabled during each "idle" ADSCAN. Balancing remains off during the "active" ADSCAN that still has voltage measurements enabled. Therefore this setting allows balancing to be enabled approximately 92% of the time (balancing is disabled one slot before any voltage measurement, thus is off for all slots of the "active" ADSCAN and for one slot in the "idle" ADSCAN just before the "active" ADSCAN).

The timing of COV and CUV protection checks that use cell voltage measurement data is also modified due to the reduced frequency of measurements.

When a command is sent to initiate cell balancing, the device first completes any ADSCAN presently in operation before it enables balancing.

Table 10-1. Cell Balancing Loop Slow Down Settings

CB_LOOP_SLOW[1]	CB_LOOP_SLOW[0]	Description
0	0	Measurements are skipped in one of every two ADSCANs.
0	1	Measurements are skipped in three of every four ADSCANs.
1	0	Measurements are skipped in seven of every eight ADSCANs.
1	1	Measurements are skipped in 15 of every 16 ADSCANs.

The ***LOOP_SLOW*** and ***CB_LOOP_SLOW*** settings operate independently. The ***LOOP_SLOW*** setting determines the speed of the regular measurement loop while balancing is not active. The ***CB_LOOP_SLOW*** setting determines the speed of the regular measurement loop only while balancing is active (the two settings do not combine together during balancing).

If a CUV or COV alert is detected while balancing is active, the device immediately disables balancing, and the schedule returns to the original NORMAL mode schedule.

While balancing is active, the device remains in NORMAL mode and does not enter SLEEP mode. If the device is in SLEEP mode and a command is sent to start balancing, the device first transitions to NORMAL mode. Commands to start balancing while the device is in DEEPSLEEP are ignored. When the device enters DEEPSLEEP mode, any balancing underway is terminated.

When the *0x0083 CB_ACTIVE_CELLS()* subcommand is sent, the intended cells to be balanced can be read back, even though the balancing has not started yet (it starts at the end of the in-progress ADSCAN). This allows the host to confirm the command sent was accepted by the device. When balancing actually begins, the *0x64*

AlarmRawStatus()[CB] bit is asserted, and it is deasserted when balancing is disabled. So this can be monitored for more precise timing on when the balancing FET is enabled and disabled. Note that this bit does not reflect the brief time periods when balancing is disabled to allow measurements to run; it continues to be asserted during these periods.

At the time cell balancing is disabled (either indefinitely or periodically to allow regular cell voltage measurements), there is a voltage transient generated that can affect several nearby cell input pins, due to the resistor and capacitor network at those pins. If a cell measurement occurs too quickly after cell balancing has been disabled, the accuracy of the cell voltage measurement can be impacted. In order to address this potential issue, the device includes a programmable delay implemented each time cell balancing is disabled before any cell voltage measurements are taken. This delay is set by ***Settings:Cell Balancing:Balancing Configuration[CBDLY2:0]*** from zero to 64 ms. This delay increases the time between successive active measurement loops.

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11.1 Direct Commands

11.1.1 Direct Commands Table

Command	Name	Units	Type	Access	Description
0x02	Safety Alert A	Hex	H1	Sealed: R Full Access: R	Provides individual alert signals when enabled safety alerts have triggered. Bit descriptions can be found in Safety Alert A Register.
0x03	Safety Status A	Hex	H1	Sealed: R Full Access: R	Provides individual fault signals when enabled safety faults have triggered. Bit descriptions can be found in Safety Status A Register.
0x04	Safety Alert B	Hex	H1	Sealed: R Full Access: R	Provides individual alert signals when enabled safety alerts have triggered. Bit descriptions can be found in Safety Alert B Register.
0x05	Safety Status B	Hex	H1	Sealed: R Full Access: R	Provides individual fault signals when enabled safety faults have triggered. Bit descriptions can be found in Safety Status B Register.
0x12	Battery Status	Hex	H2	Sealed: R Full Access: R	Provides flags related to battery status. Bit descriptions can be found in Battery Status Register.
0x14	Cell 1 Voltage	mV	I2	Sealed: R Full Access: R	16-bit voltage on cell 1.
0x16	Cell 2 Voltage	mV	I2	Sealed: R Full Access: R	16-bit voltage on cell 2.
0x18	Cell 3 Voltage	mV	I2	Sealed: R Full Access: R	16-bit voltage on cell 3.
0x1A	Cell 4 Voltage	mV	I2	Sealed: R Full Access: R	16-bit voltage on cell 4.
0x1C	Cell 5 Voltage	mV	I2	Sealed: R Full Access: R	16-bit voltage on cell 5.
0x22	REG18 Voltage	16-bit ADC codes	I2	Sealed: R Full Access: R	Internal 1.8V regulator voltage measured using bandgap reference, used for diagnostic of VREF1 vs VREF2.
0x24	VSS Voltage	16-bit ADC codes	I2	Sealed: R Full Access: R	Measurement of VSS using ADC, used for diagnostic of ADC input mux
0x26	Stack Voltage	mV	U2	Sealed: R Full Access: R	16-bit voltage on top of stack
0x28	Int Temperature	°C	I2	Sealed: R Full Access: R	This is the most recent measured internal die temperature.
0x2A	TS Measurement	16-bit ADC codes	I2	Sealed: R Full Access: R	ADC measurement of the TS pin.
0x36	Raw Current	24-bit ADC codes sign-extended for 32-bit format	I4	Sealed: R Full Access: R	32-bit raw current measurement
0x3A	Current	userA	I2	Sealed: R Full Access: R	16-bit CC2 current measurement
0x3C	CC1 Current	userA	I2	Sealed: R Full Access: R	16-bit CC1 current measurement

Command	Name	Units	Type	Access	Description
0x62	Alarm Status	Hex	H2	Sealed: R/W Full Access: R/W	Latched signal used to assert the ALERT pin. Write a bit high to clear the latched bit. Bit descriptions can be found in Alarm Status Register.
0x64	Alarm Raw Status	Hex	H2	Sealed: R Full Access: R	Unlatched value of flags which can be selected to be latched (using Alarm Enable()) and used to assert the ALERT pin. Bit descriptions can be found in Alarm Raw Status Register.
0x66	Alarm Enable	Hex	H2	Sealed: R/W Full Access: R/W	Mask for Alarm Status(). Can be written to change during operation to change which alarm sources are enabled. The default value of this parameter is set by Settings:Configuration:Default Alarm Mask. Bit descriptions can be found in Alarm Enable Register.
0x68	FET CONTROL	Hex	H1	Sealed: R/W Full Access: R/W	FET Control: Allows host control of individual FET drivers. Bit descriptions can be found in FET CONTROL Register.
0x69	REGOUT CONTROL	Hex	H1	Sealed: R/W Full Access: R/W	REGOUT Control: Changes voltage regulator settings. Bit descriptions can be found in REGOUT CONTROL Register.
0x6A	DSG FET Driver PWM Control	Hex	H2	Sealed: R/W Full Access: R/W	Controls the PWM mode of the DSG FET driver. Values are not used until the second byte is written. Bit descriptions can be found in DSG FET Driver PWM Control Register.
0x6C	CHG FET Driver PWM Control	Hex	H2	Sealed: R/W Full Access: R/W	Controls the PWM mode of the CHG FET driver. Values are not used until the second byte is written. Bit descriptions can be found in CHG FET Driver PWM Control Register.

11.2 Bit field Definitions for Direct Commands

11.2.1 Safety Alert A Register

7	6	5	4	3	2	1	0
COV	CUV	SCD	OCD1	OCD2	OCC	RSVD0_1	RSVD0_0

Description: Provides individual alert signals when enabled safety alerts have triggered.

Table 11-1. Safety Alert A Register Field Descriptions

Bit	Field	Description
7	COV	Cell Overvoltage Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
6	CUV	Cell Undervoltage Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
5	SCD	Short Circuit in Discharge Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
4	OCD1	Overcurrent in Discharge 1 Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
3	OCD2	Overcurrent in Discharge 2 Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
2	OCC	Overcurrent in Charge Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered

11.2.2 Safety Status A Register

7	6	5	4	3	2	1	0
COV	CUV	SCD	OCD1	OCD2	OCC	CURLATCH	REGOUT

Description: Provides individual fault signals when enabled safety faults have triggered.

Table 11-2. Safety Status A Register Field Descriptions

Bit	Field	Description
7	COV	Cell Overvoltage Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
6	CUV	Cell Undervoltage Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
5	SCD	Short Circuit in Discharge Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
4	OCD1	Overcurrent in Discharge 1 Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
3	OCD2	Overcurrent in Discharge 2 Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
2	OCC	Overcurrent in Charge Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
1	CURLATCH	Current Protection Latch Safety Fault 0 = Indicates the number of attempted current protection recoveries has not yet exceeded the latch count. 1 = Indicates the number of attempted current protection recoveries has exceeded the latch count, and autorecovery based on time is disabled.
0	REGOUT	REGOUT Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered

11.2.3 Safety Alert B Register

7	6	5	4	3	2	1	0
OTD	OTC	UTD	UTC	OTINT	HWD	VREF	VSS

Description: Provides individual alert signals when enabled safety alerts have triggered.

Table 11-3. Safety Alert B Register Field Descriptions

Bit	Field	Description
7	OTD	Overtemperature in Discharge Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered

Table 11-3. Safety Alert B Register Field Descriptions (continued)

Bit	Field	Description
6	OTC	Overtemperature in Charge Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
5	UTD	Undertemperature in Discharge Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
4	UTC	Undertemperature in Charge Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
3	OTINT	Internal Overtemperature Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
2	HWD	Host Watchdog Safety Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
1	VREF	VREF Measurement Diagnostic Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered
0	VSS	VSS Measurement Diagnostic Alert 0 = Indicates protection alert has not triggered 1 = indicates protection alert has triggered

11.2.4 Safety Status B Register

7	6	5	4	3	2	1	0
OTD	OTC	UTD	UTC	OTINT	HWD	VREF	VSS

Description: Provides individual fault signals when enabled safety faults have triggered.

Table 11-4. Safety Status B Register Field Descriptions

Bit	Field	Description
7	OTD	Overtemperature in Discharge Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
6	OTC	Overtemperature in Charge Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
5	UTD	Undertemperature in Discharge Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
4	UTC	Undertemperature in Charge Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
3	OTINT	Internal Overtemperature Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
2	HWD	Host Watchdog Safety Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered

Table 11-4. Safety Status B Register Field Descriptions (continued)

Bit	Field	Description
1	VREF	VREF Measurement Diagnostic Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered
0	VSS	VSS Measurement Diagnostic Fault 0 = Indicates protection fault has not triggered 1 = indicates protection fault has triggered

11.2.5 Battery Status Register

15	14	13	12	11	10	9	8
SLEEP	DEEPSLEEP	SA	SS	SEC_1	SEC_0	RSVD0	FET_EN
7	6	5	4	3	2	1	0
POR	SLEEP_EN	CFGUPDATE	ALERTPIN	CHG	DSG	CHGDETFLAG	RSVD0

Description: Provides flags related to battery status.

Table 11-5. Battery Status Register Field Descriptions

Bit	Field	Description
15	SLEEP	This flag asserts if the device is in SLEEP mode 0 = Device is not in SLEEP mode 1 = Device is in SLEEP mode
14	DEEPSLEEP	This flag asserts if the device is in DEEPSLEEP mode 0 = Device is not in DEEPSLEEP mode 1 = Device is in DEEPSLEEP mode
13	SA	This flag asserts if an enabled safety alert is present. 0 = Indicates an enabled safety alert is not present 1 = Indicates an enabled safety alert is present
12	SS	This flag asserts if an enabled safety fault is present. 0 = Indicates an enabled safety fault is not present 1 = Indicates an enabled safety fault is present
11–10	SEC_1–SEC_0	SEC1:0 indicate the present security state of the device. When in SEALED mode, device configuration cannot be read or written and some commands are restricted. When in FULLACCESS mode, unrestricted read and write access is allowed and all commands are accepted. 0 = 0: Device has not initialized yet. 1 = 1: Device is in FULLACCESS mode. 2 = 2: Unused. 3 = 3: Device is in SEALED mode.
8	FET_EN	This bit is set when the device is in autonomous FET control mode. The default value of this bit is set by the Settings:FET Options[FET_EN] bit in Data Memory upon exit of CONFIG_UPDATE mode. Its value can be modified during operation using the FET_ENABLE() subcommand. 0 = Device is not in autonomous FET control mode, FETs are only enabled through manual command. 1 = Device is in autonomous FET control mode, FETs can be enabled by the device if no conditions or commands prevent them being enabled.

Table 11-5. Battery Status Register Field Descriptions (continued)

Bit	Field	Description
7	POR	This bit is set when the device fully resets. It is cleared upon exit of CONFIG_UPDATE mode. It can be used by the host to determine if any RAM configuration changes were lost due to a reset. 0 = Full reset has not occurred since last exit of CONFIG_UPDATE mode. 1 = Full reset has occurred since last exit of CONFIG_UPDATE and reconfiguration of any RAM settings is required.
6	SLEEP_EN	This bit indicates whether or not SLEEP mode is allowed based on configuration and commands. The***Settings:Configuration:Power Config[SLEEP_EN]*** bit sets the default state of this bit. The host can send commands to enable or disable SLEEP mode based on system requirements. When this bit is set, the device can transition to SLEEP mode when other SLEEP criteria are met. 0 = SLEEP mode is disabled by the host. 1 = SLEEP mode is allowed when other SLEEP conditions are met.
5	CFGUPDATE	This bit indicates whether or not the device is in CONFIG_UPDATE mode. It is set after the SET_CFGUPDATE() subcommand is received and fully processed. Configuration settings can be changed only while this bit is set. 0 = Device is not in CONFIG_UPDATE mode. 1 = Device is in CONFIG_UPDATE mode.
4	ALERTPIN	This bit indicates whether the ALERT pin is asserted (pulled low). 0 = ALERT pin is not asserted (stays in hi-Z mode). 1 = ALERT pin is asserted (pulled low).
3	CHG	This bit indicates whether the CHG driver is enabled. 0 = CHG driver is disabled. 1 = CHG driver is enabled.
2	DSG	This bit indicates whether the DSG driver is enabled. 0 = DSG driver is disabled. 1 = DSG driver is enabled.
1	CHGDETFLAG	This bit indicates the value of the debounced CHG Detector signal. 0 = CHG Detector debounced signal is low. 1 = CHG Detector debounced signal is high.

11.2.6 Alarm Status Register

15	14	13	12	11	10	9	8
SSA	SSB	SAA	SAB	XCHG	XDSG	SHUTV	CB
7	6	5	4	3	2	1	0
FULLSCAN	ADSCAN	WAKE	SLEEP	TIMER_ALARM	INITCOMP	CDTOGGLE	POR

Description: Latched signal used to assert the ALERT pin. Write a bit high to clear the latched bit.

Table 11-6. Alarm Status Register Field Descriptions

Bit	Field	Description
15	SSA	This bit is latched when a bit in Safety Status A() is set, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set

Table 11-6. Alarm Status Register Field Descriptions (continued)

Bit	Field	Description
14	SSB	This bit is latched when a bit in Safety Status B() is set, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
13	SAA	This bit is latched when a bit in Safety Alert A() is set, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
12	SAB	This bit is latched when a bit in Safety Alert B() is set, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
11	XCHG	This bit is latched when the CHG driver is disabled, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
10	XDSG	This bit is latched when the DSG driver is disabled, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
9	SHUTV	This bit is latched when either a cell voltage has been measured below Shutdown Cell Voltage, or the stack voltage has been measured below Shutdown Stack Voltage. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
8	CB	This bit is latched when cell balancing is active, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
7	FULLSCAN	This bit is latched when a full scan is complete (including cell voltages, top-of-stack voltage, temperature, and diagnostic measurements), and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
6	ADSCAN	This bit is latched when a voltage ADC measurement scan is complete (this includes the cell voltage measurements and one additional measurement), and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
5	WAKE	This bit is latched when the device is wakened from SLEEP mode, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
4	SLEEP	This bit is latched when the device enters SLEEP mode, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set

Table 11-6. Alarm Status Register Field Descriptions (continued)

Bit	Field	Description
3	TIMER_ALARM	This bit is latched when the programmable timer expires, and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
2	INITCOMP	This bit is latched when the device completes the startup measurement sequence (which runs after an initial powerup, after a device reset, when the device exits CONFIG_UPDATE mode, and when it exits DEEPSLEEP mode) and the bit is included in the mask. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
1	CDTOGGLE	This bit is latched when the debounced CHG Detector signal is different from the last debounced value. 0 = Flag is not set 1 = Flag is set
0	POR	This bit is latched when the POR bit in Battery Status is asserted. 0 = Flag is not set 1 = Flag is set

11.2.7 Alarm Raw Status Register

15	14	13	12	11	10	9	8
SSA	SSB	SAA	SAB	XCHG	XDSG	SHUTV	CB
7	6	5	4	3	2	1	0
FULLSCAN	ADSCAN	WAKE	SLEEP	TIMER_ALARM	INITCOMP	CDRAW	POR

Description: Unlatched value of flags which can be selected to be latched (using Alarm Enable()) and used to assert the ALERT pin.

Table 11-7. Alarm Raw Status Register Field Descriptions

Bit	Field	Description
15	SSA	This bit is set when a bit in Safety Status A() is set. 0 = Flag is not set 1 = Flag is set
14	SSB	This bit is set when a bit in Safety Status B() is set. 0 = Flag is not set 1 = Flag is set
13	SAA	This bit is set when a bit in Safety Alert A() is set. 0 = Flag is not set 1 = Flag is set
12	SAB	This bit is set when a bit in Safety Alert B() is set. 0 = Flag is not set 1 = Flag is set
11	XCHG	This bit is set when the CHG driver is disabled. 0 = Flag is not set 1 = Flag is set
10	XDSG	This bit is set when the DSG driver is disabled. 0 = Flag is not set 1 = Flag is set

Table 11-7. Alarm Raw Status Register Field Descriptions (continued)

Bit	Field	Description
9	SHUTV	This bit is set when either a cell voltage has been measured below Shutdown Cell Voltage, or the stack voltage has been measured below Shutdown Stack Voltage. The bit is cleared when written with a "1". A bit set here causes the ALERT pin to be asserted low. 0 = Flag is not set 1 = Flag is set
8	CB	This bit is set when cell balancing is active. 0 = Flag is not set 1 = Flag is set
7	FULLSCAN	This bit pulses high briefly when a full scan is complete (including cell voltages, top-of-stack voltage, temperature, and diagnostic measurements).
6	ADSCAN	This bit pulses high briefly when a voltage ADC measurement scan is complete (this includes the cell voltage measurements and one additional measurement).
5	WAKE	This bit pulses high briefly when the device is wakened from SLEEP mode.
4	SLEEP	This bit pulses high briefly when the device enters SLEEP mode. 0 = Flag is not set 1 = Flag is set
3	TIMER_ALARM	This bit pulses high briefly when the programmable timer expires.
2	INITCOMP	This bit pulses high briefly when the device has completed the startup measurement sequence (after powerup or reset or exit of CONFIG_UPDATE mode or exit of DEEPSLEEP).
1	CDRAW	This bit is set when the CHG Detector output is set, indicating that the CHG pin has been detected above a level of approximately 2 V. 0 = CHG Detector output is not set 1 = CHG Detector output is set
0	POR	This bit is set if the POR bit in Battery Status is asserted. 0 = Flag is not set 1 = Flag is set

11.2.8 Alarm Enable Register

15	14	13	12	11	10	9	8
SSA	SSB	SAA	SAB	XCHG	XDSG	SHUTV	CB
7	6	5	4	3	2	1	0
FULLSCAN	ADSCAN	WAKE	SLEEP	TIMER_ALARM	INITCOMP	CDTOGGLE	POR

Description: Mask for Alarm Status(). Can be written to change during operation to change which alarm sources are enabled. The default value of this parameter is set by Settings:Configuration:Default Alarm Mask.

Table 11-8. Alarm Enable Register Field Descriptions

Bit	Field	Description
15	SSA	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
14	SSB	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()

Table 11-8. Alarm Enable Register Field Descriptions (continued)

Bit	Field	Description
13	SAA	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
12	SAB	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
11	XCHG	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
10	XDSG	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
9	SHUTV	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
8	CB	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
7	FULLSCAN	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
6	ADSCAN	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
5	WAKE	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
4	SLEEP	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
3	TIMER_ALARM	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
2	INITCOMP	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
1	CDTOGGLE	Setting this bit allows the internally determined value of CDTOGGLE to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. This flag is set whenever the debounced CHG Detector signal differs from the previous debounced value. 0 = The CDTOGGLE signal is not included in Alarm Status() 1 = The CDTOGGLE signal is included in Alarm Status()

Table 11-8. Alarm Enable Register Field Descriptions (continued)

Bit	Field	Description
0	POR	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()

11.2.9 FET CONTROL Register

7	6	5	4	3	2	1	0
RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	CHG_OFF	DSG_OFF	CHG_ON	DSG_ON

Description: FET Control: Allows host control of individual FET drivers.

Table 11-9. FET CONTROL Register Field Descriptions

Bit	Field	Description
3	CHG_OFF	CHG FET driver control. This bit only operates if the HOST_FETOFF_EN bit in data memory is set. 0 = CHG FET driver is allowed to turn on if other conditions are met. 1 = CHG FET driver is forced off.
2	DSG_OFF	DSG FET driver control. This bit only operates if the HOST_FETOFF_EN bit in data memory is set. 0 = DSG FET driver is allowed to turn on if other conditions are met. 1 = DSG FET driver is forced off.
1	CHG_ON	CHG FET driver control. This bit only operates if the HOST_FETON_EN bit in data memory is set. 0 = CHG FET driver is allowed to turn on if other conditions are met. 1 = CHG FET driver is forced on.
0	DSG_ON	DSG FET driver control. This bit only operates if the HOST_FETON_EN bit in data memory is set. 0 = DSG FET driver is allowed to turn on if other conditions are met. 1 = DSG FET driver is forced on.

11.2.10 REGOUT CONTROL Register

7	6	5	4	3	2	1	0
RSVD0_2	RSVD0_1	RSVD0_0	TS_ON	REG_EN	REGOUTV_2	REGOUTV_1	REGOUTV_0

Description: REGOUT Control: Changes voltage regulator settings.

Table 11-10. REGOUT CONTROL Register Field Descriptions

Bit	Field	Description
4	TS_ON	Control for TS pullup to stay biased continuously. 0 = TS pullup resistor is not continuously connected. 1 = TS pullup resistor is continuously connected.
3	REG_EN	REGOUT LDO enable. 0 = REGOUT LDO is disabled 1 = REGOUT LDO is enabled

Table 11-10. REGOUT CONTROL Register Field Descriptions (continued)

Bit	Field	Description
2–0	REGOUTV_2–REGOUTV_0	REGOUT LDO voltage control. 0 = REGOUT LDO is set to 1.8V 1 = REGOUT LDO is set to 1.8V 2 = REGOUT LDO is set to 1.8V 3 = REGOUT LDO is set to 1.8V 4 = REGOUT LDO is set to 2.5 V 5 = REGOUT LDO is set to 3.0 V 6 = REGOUT LDO is set to 3.3 V 7 = REGOUT LDO is set to 5 V

11.2.11 DSG FET Driver PWM Control Register

15	14	13	12	11	10	9	8
DSGPWMEN	DSGPWMON_6	DSGPWMON_5	DSGPWMON_4	DSGPWMON_3	DSGPWMON_2	DSGPWMON_1	DSGPWMON_0
7	6	5	4	3	2	1	0
DSGPWMOFF_7	DSGPWMOFF_6	DSGPWMOFF_5	DSGPWMOFF_4	DSGPWMOFF_3	DSGPWMOFF_2	DSGPWMOFF_1	DSGPWMOFF_0

Description: Controls the PWM mode of the DSG FET driver. Values are not used until the second byte is written.

Table 11-11. DSG FET Driver PWM Control Register Field Descriptions

Bit	Field	Description
15	DSGPWMEN	DSG FET driver PWM mode control 0 = DSG FET driver PWM mode is disabled 1 = DSG FET driver PWM mode is enabled
14–8	DSGPWMON_6–DSGPWMON_0	Time the DSG FET driver is enabled when PWM mode is enabled. Settings from 30.52 µs to 3.876 ms in steps of 30.52 µs A setting of 0 disables PWM mode, such that this command has no effect.
7–0	DSGPWMOFF_7–DSGPWMOFF_0	Time the DSG FET driver is disabled each cycle when PWM mode is enabled. Settings from 122.1 µs to 31.128 ms in steps of 122.1 µs A setting of 0 disables PWM mode, such that this command has no effect.

11.2.12 CHG FET Driver PWM Control Register

15	14	13	12	11	10	9	8
CHGPWMEN	CHGPWMON_6	CHGPWMON_5	CHGPWMON_4	CHGPWMON_3	CHGPWMON_2	CHGPWMON_1	CHGPWMON_0
7	6	5	4	3	2	1	0
CHGPWMOFF_7	CHGPWMOFF_6	CHGPWMOFF_5	CHGPWMOFF_4	CHGPWMOFF_3	CHGPWMOFF_2	CHGPWMOFF_1	CHGPWMOFF_0

Description: Controls the PWM mode of the CHG FET driver. Values are not used until the second byte is written.

Table 11-12. CHG FET Driver PWM Control Register Field Descriptions

Bit	Field	Description
15	CHGPWMEN	CHG FET driver PWM mode control 0 = CHG FET driver PWM mode is disabled 1 = CHG FET driver PWM mode is enabled
14–8	CHGPWMON_6–CHGPWMON_0	Time the CHG FET driver is enabled when PWM mode is enabled. Settings from 30.52 µs to 3.876 ms in steps of 30.52 µs A setting of 0 disables PWM mode, such that this command has no effect.
7–0	CHGPWMOFF_7–CHGPWMOFF_0	Time the CHG FET driver is disabled each cycle when PWM mode is enabled. Settings from 488.4 µs to 124.512 ms in steps of 488.4 µs A setting of 0 disables PWM mode, such that this command has no effect.

11.3 Command-only Subcommands

Table of Command-only Subcommands

Command	Name	Access	Description
0x0005	RESET_PASSQ	Sealed: W Full Access: W	This command resets the accumulated charge and timer
0x000E	EXIT_DEEPSLEEP	Sealed: W Full Access: W	This command is sent to exit DEEPSLEEP mode.
0x000F	DEEPSLEEP	Sealed: W Full Access: W	This command is sent to enter DEEPSLEEP mode. Must be sent twice in a row within 4s to take effect
0x0010	SHUTDOWN	Sealed: W Full Access: W	This command is sent to start SHUTDOWN sequence. Must be sent twice in a row within 4s to take effect. If sent a third time, the shutdown delay is skipped
0x0012	RESET	Sealed: — Full Access: W	This command is sent to reset the device
0x0022	FET_ENABLE	Sealed: — Full Access: W	This command is sent to toggle the FET_EN bit in Battery Status(). FET_EN=0 means manual FET control. FET_EN=1 means autonomous device FET control
0x0030	SEAL	Sealed: — Full Access: W	This command is sent to place the device in SEALED mode
0x0090	SET_CFGUPDATE	Sealed: — Full Access: W	This command is sent to place the device in CONFIG_UPDATE mode
0x0092	EXIT_CFGUPDATE	Sealed: — Full Access: W	This command is sent to exit CONFIG_UPDATE mode
0x0099	SLEEP_ENABLE	Sealed: W Full Access: W	This command is sent to allow the device to enter SLEEP mode
0x009A	SLEEP_DISABLE	Sealed: W Full Access: W	This command is sent to block the device from entering SLEEP mode

11.4 Subcommands with Data

Subcommands Table

Command	Name	Access	Offset	Data	Units	Type	Description
0x0001	DEVICE_NUMBER	Sealed: R Full Access: R	0	DEVICE NUMBER	Hex	H2	The DEVICE_NUMBER subcommand reports the device number that identifies the product. The data is returned in little-endian format. Bit descriptions can be found in DEVICE NUMBER Register.

Command	Name	Access	Offset	Data	Units	Type	Description
0x0002	FW_VERSION	Sealed: R Full Access: R	0	FW VERSION	Hex	H6	The FW_VERSION subcommand returns three 16-bit word values. Bytes 0-1: Device Number (Big-Endian): Device number in big-endian format for compatibility with legacy products. Bytes 3-2: Firmware Version (Big-Endian): Device firmware major and minor version number (Big-Endian). Bytes 5-4: Build Number (Big-Endian): Firmware build number in big-endian, binary coded decimal format for compatibility with legacy products. Bit descriptions can be found in FW VERSION Register.
0x0003	HW_VERSION	Sealed: R Full Access: R	0	HW VERSION	Hex	H2	Hardware Version: Reports the device hardware version number Bit descriptions can be found in HW VERSION Register.
0x0004	PASSQ	Sealed: R Full Access: R	0	PASSQLSB	0.25-userA-sec	U4	Accumulated charge lower 32-bits (little-endian byte-by-byte). Lower 32 bits of signed 48-bit result, with the full 48-bit field having units of userA-seconds.
			4	PASSQMSB	0.25-userA-sec	I4	Accumulated charge upper 16-bits sign-extended to a 32-bit field (little-endian byte-by-byte). Upper bits of signed 48-bit result, with the full 48-bit field having units of userA-seconds.
			8	PASSTIME	250ms	U4	Accumulated Time (little-endian byte-by-byte), 32-bit unsigned integer in units of 250 ms.
0x0035	SECURITY_KEYS	Sealed: — Full Access: W	0	SECURITY KEYS	Hex	H4	Security key that must be sent to transition from SEALED to FULLACCESS mode. The subcommand includes two 16-bit words Bit descriptions can be found in SECURITY KEYS Register.
0x0083	CB_ACTIVE_CELLS	Sealed: R Full Access: R/W	0	CB ACTIVE CELLS	Hex	H1	Cell balancing active cells: When read, reports a bit mask of which cells are being actively balanced. When written, starts balancing on the specified cells. Write 0x00 to disable balancing Bit descriptions can be found in CB ACTIVE CELLS Register.
0x0094	PROG_TIMER	Sealed: R Full Access: R/W	0	PROG TIMER	Hex	H2	Programmable timer, which allows the REGOUT LDO to be disabled and wakened after a programmed time or by alarm Bit descriptions can be found in PROG TIMER Register.
0x009b	PROT_RECOVERY	Sealed: R Full Access: R/W	0	PROT RECOVERY	Hex	H1	This command enables the host to allow recovery of selected protection faults Bit descriptions can be found in PROT RECOVERY Register.

11.5 Bit field Definitions for Subcommands

11.5.1 DEVICE NUMBER Register

15	14	13	12	11	10	9	8
DEVNUM_15	DEVNUM_14	DEVNUM_13	DEVNUM_12	DEVNUM_11	DEVNUM_10	DEVNUM_9	DEVNUM_8
7	6	5	4	3	2	1	0

DEVNUM_7	DEVNUM_6	DEVNUM_5	DEVNUM_4	DEVNUM_3	DEVNUM_2	DEVNUM_1	DEVNUM_0

Description: The DEVICE_NUMBER subcommand reports the device number that identifies the product. The data is returned in little-endian format.

Table 11-13. DEVICE NUMBER Register Field Descriptions

Bit	Field	Description
15–0	DEVNUM_15–DEVNUM_0	Reports the device number that identifies the product. The data is returned in little-endian format.

11.5.2 FW VERSION Register

47	46	45	44	43	42	41	40
FVBLDNUM_15	FVBLDNUM_14	FVBLDNUM_13	FVBLDNUM_12	FVBLDNUM_11	FVBLDNUM_10	FVBLDNUM_9	FVBLDNUM_8
39	38	37	36	35	34	33	32
FVBLDNUM_7	FVBLDNUM_6	FVBLDNUM_5	FVBLDNUM_4	FVBLDNUM_3	FVBLDNUM_2	FVBLDNUM_1	FVBLDNUM_0
31	30	29	28	27	26	25	24
FVFWVER_15	FVFWVER_14	FVFWVER_13	FVFWVER_12	FVFWVER_11	FVFWVER_10	FVFWVER_9	FVFWVER_8
23	22	21	20	19	18	17	16
FVFWVER_7	FVFWVER_6	FVFWVER_5	FVFWVER_4	FVFWVER_3	FVFWVER_2	FVFWVER_1	FVFWVER_0
15	14	13	12	11	10	9	8
FVDEVNUM_15	FVDEVNUM_14	FVDEVNUM_13	FVDEVNUM_12	FVDEVNUM_11	FVDEVNUM_10	FVDEVNUM_9	FVDEVNUM_8
7	6	5	4	3	2	1	0
FVDEVNUM_7	FVDEVNUM_6	FVDEVNUM_5	FVDEVNUM_4	FVDEVNUM_3	FVDEVNUM_2	FVDEVNUM_1	FVDEVNUM_0

Description: The FW_VERSION subcommand returns three 16-bit word values. Bytes 0-1: Device Number (Big-Endian): Device number in big-endian format for compatibility with legacy products. Bytes 3-2: Firmware Version (Big-Endian): Device firmware major and minor version number (Big-Endian). Bytes 5-4: Build Number (Big-Endian): Firmware build number in big-endian, binary coded decimal format for compatibility with legacy products

Table 11-14. FW VERSION Register Field Descriptions

Bit	Field	Description
47–32	FVBLDNUM_15–FVBLDNUM_0	Build Number (Big-Endian): Firmware build number in big-endian, binary coded decimal format for compatibility with legacy products
31–16	FVFWVER_15–FVFWVER_0	Firmware Version (Big-Endian): Device firmware major and minor version number (Big-Endian)
15–0	FVDEVNUM_15–FVDEVNUM_0	Device Number (Big-Endian): Device number in big-endian format for compatibility with legacy products

11.5.3 HW VERSION Register

15	14	13	12	11	10	9	8
HWVER_15	HWVER_14	HWVER_13	HWVER_12	HWVER_11	HWVER_10	HWVER_9	HWVER_8
7	6	5	4	3	2	1	0
HWVER_7	HWVER_6	HWVER_5	HWVER_4	HWVER_3	HWVER_2	HWVER_1	HWVER_0

Description: Hardware Version: Reports the device hardware version number

Table 11-15. HW VERSION Register Field Descriptions

Bit	Field	Description
15–0	HWVER_15–HWVER_0	Hardware Version: Reports the device hardware version number.

11.5.4 SECURITY KEYS Register

31	30	29	28	27	26	25	24
FAKEY2_6_15	FAKEY2_6_14	FAKEY2_6_13	FAKEY2_6_12	FAKEY2_6_11	FAKEY2_6_10	FAKEY2_6_9	FAKEY2_6_8
23	22	21	20	19	18	17	16
FAKEY2_6_7	FAKEY2_6_6	FAKEY2_6_5	FAKEY2_6_4	FAKEY2_6_3	FAKEY2_6_2	FAKEY2_6_1	FAKEY2_6_0
15	14	13	12	11	10	9	8
FAKEY1__15	FAKEY1__14	FAKEY1__13	FAKEY1__12	FAKEY1__11	FAKEY1__10	FAKEY1__9	FAKEY1__8
7	6	5	4	3	2	1	0
FAKEY1__7	FAKEY1__6	FAKEY1__5	FAKEY1__4	FAKEY1__3	FAKEY1__2	FAKEY1__1	FAKEY1__0

Description: Security key that must be sent to transition from SEALED to FULLACCESS mode. The subcommand includes two 16-bit words

Table 11-16. SECURITY KEYS Register Field Descriptions

Bit	Field	Description
31–16	FAKEY2_6_15–FAKEY2_6_0	Full Access Key Step 2: This is the second word of the security key that must be sent to transition from SEALED to FULLACCESS mode. Do not choose a word identical to a subcommand address or the same as the first word. It must be sent within 5 seconds of the first word of the key and with no other commands in between.
15–0	FAKEY1__15–FAKEY1__0	Full Access Key Step 1: This is the first word of the security key that must be sent to transition from SEALED to FULLACCESS mode. Do not choose a word identical to a subcommand address.

11.5.5 CB ACTIVE CELLS Register

7	6	5	4	3	2	1	0

CBCELLS_7	CBCELLS_6	CBCELLS_5	CBCELLS_4	CBCELLS_3	CBCELLS_2	CBCELLS_1	CBCELLS_0

Description: Cell balancing active cells: When read, reports a bit mask of which cells are being actively balanced. When written, starts balancing on the specified cells. Write 0x00 to disable balancing

Table 11-17. CB ACTIVE CELLS Register Field Descriptions

Bit	Field	Description
7–0	CBCELLS_7–CBCELLS_0	Cell balancing active cells: When read, reports a bit mask of which cells are being actively balanced. When written, starts balancing on the specified cells. Write 0x00 to turn balancing off. Bit 7 is reserved, read/write 0 to this bit Bit 6 is reserved, read/write 0 to this bit Bit 5 corresponds to the fifth active cell Bit 4 corresponds to the fourth active cell Bit 3 corresponds to the third active cell Bit 2 corresponds to the second active cell Bit 1 corresponds to the first active cell (connected between VC1 and VC0) Bit 0 is reserved, read/write 0 to this bit

11.5.6 PROG TIMER Register

15	14	13	12	11	10	9	8
RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	REGOUT_ALARM_WK	REGOUT_SD_DLY_1	REGOUT_SD_DLY_0	REGOUT_SD
7	6	5	4	3	2	1	0
PROG_TMR_7	PROG_TMR_6	PROG_TMR_5	PROG_TMR_4	PROG_TMR_3	PROG_TMR_2	PROG_TMR_1	PROG_TMR_0

Description: Programmable timer, which allows the REGOUT LDO to be disabled and wakened after a programmed time or by alarm

Table 11-18. PROG TIMER Register Field Descriptions

Bit	Field	Description
11	REGOUT_ALARM_WK	Control to determine if REGOUT is wakened when an Alarm Status() bit asserts. 0 = Do not re-enable the REGOUT LDO if any bit in Alarm Status() asserts while the timer is running (default). 1 = If [REGOUT_SD]=1 and any bit in Alarm Status() asserts while the timer is running, reenable the REGOUT LDO based on the setting of *REGOUT Control()*.
10–9	REGOUT_SD_DLY_1–REGOUT_SD_DLY_0	Delay before REGOUT is disabled when the timer is initiated while REGOUT is powered, and [REGOUT_SD]=1. 0 = Zero delay (default). 1 = 250ms delay. 2 = 1-sec delay. 3 = 4-sec delay
8	REGOUT_SD	Control to determine if REGOUT is disabled when the command is sent. 0 = do not disable the REGOUT LDO when command is sent (default). 1 = disable the REGOUT LDO when the timer is initiated, after delay of [REGOUT_SD_DLY]. When the timer expires, re-enable the REGOUT LDO based on the status of *REGOUT Control()*.

Table 11-18. PROG TIMER Register Field Descriptions (continued)

Bit	Field	Description
7–0	PROG_TMR_7–PROG_TMR_0	Timer value programmable from 250 ms to 4 seconds in 250 ms increments (settings 1 to 16), and from 5 seconds to 243 seconds in 1 second increments (settings 17 to 255). A setting of zero disables the timer. Whenever this field is written with a non-zero value, it initiates the timer.

11.5.7 PROT RECOVERY Register

7	6	5	4	3	2	1	0
VOLTREC	DIAGREC	SCDREC	OCD1REC	OCD2REC	OCCREC	TEMPREC	RSVD0

Description: This command enables the host to allow recovery of selected protection faults

Table 11-19. PROT RECOVERY Register Field Descriptions

Bit	Field	Description
7	VOLTREC	Cell Overvoltage or Cell Undervoltage fault recovery 0 = Recovery of an COV/CUV fault is not triggered 1 = Recovery of an COV/CUV fault is triggered.
6	DIAGREC	Recovery for a VSS or VREF fault from Safety Status B() 0 = Recovery of a VSS or VREF fault is not triggered 1 = Recovery of a VSS or VREF fault is triggered.
5	SCDREC	Short Circuit in Discharge fault recovery 0 = Recovery of an SCD fault is not triggered 1 = Recovery of an SCD fault is triggered.
4	OCD1REC	Overcurrent in Discharge 1 fault recovery 0 = Recovery of an OCD1 fault is not triggered 1 = Recovery of an OCD1 fault is triggered.
3	OCD2REC	Overcurrent in Discharge 2 fault recovery 0 = Recovery of an OCD2 fault is not triggered 1 = Recovery of an OCD2 fault is triggered.
2	OCCREC	Overcurrent in Charge fault recovery 0 = Recovery of an OCC fault is not triggered 1 = Recovery of an OCC fault is triggered.
1	TEMPREC	Temperature fault recovery 0 = Recovery of a temperature fault is not triggered 1 = Recovery of a temperature fault is triggered.

12.1 Calibration

12.1.1 Calibration:Voltage

12.1.1.1 Calibration:Voltage:Cell 1 Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 1 Gain	U2	0	65535	0x0	—

Description: The Cell 1 Gain is used to scale the Cell 1 voltage ADC measurements for reporting in mV.

12.1.1.2 Calibration:Voltage:Cell 2 Gain Delta

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 2 Gain Delta	I1	-128	127	0x0	—

Description: The Cell 2 Gain Delta is added to the Cell 1 Gain value to obtain the Cell 2 Gain. The Cell 2 Gain is multiplied by the Cell 2 voltage ADC measurements for reporting in mV.

12.1.1.3 Calibration:Voltage:Cell 3 Gain Delta

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 3 Gain Delta	I1	-128	127	0x0	—

Description: The Cell 3 Gain Delta is added to the Cell 1 Gain value to obtain the Cell 3 Gain. The Cell 3 Gain is multiplied by the Cell 3 voltage ADC measurements for reporting in mV.

12.1.1.4 Calibration:Voltage:Cell 4 Gain Delta

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 4 Gain Delta	I1	-128	127	0x0	—

Description: The Cell 4 Gain Delta is added to the Cell 1 Gain value to obtain the Cell 4 Gain. The Cell 4 Gain is multiplied by the Cell 4 voltage ADC measurements for reporting in mV.

12.1.1.5 Calibration:Voltage:Cell 5 Gain Delta

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 5 Gain Delta	I1	-128	127	0x0	—

Description: The Cell 5 Gain Delta is added to the Cell 1 Gain value to obtain the Cell 5 Gain. The Cell 5 Gain is multiplied by the Cell 5 voltage ADC measurements for reporting in mV.

12.1.1.6 Calibration:Voltage:Stack Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Stack Gain	U2	0	65535	0x0	—

Description: Gain value used to scale the stack voltage ADC measurements for reporting in mV.

This value is multiplied by the upper 16-bits of the stack voltage ADC result.

12.1.2 Calibration:Current

12.1.2.1 Calibration:Current:Curr Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Current	Curr Gain	U2	0	65535	0x0	—

Description: Gain value used to scale the coulomb counter CC2 measurement after the Curr Offset is subtracted, for reporting in userA

12.1.2.2 Calibration:Current:Curr Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Current	Curr Offset	I2	–32768	32767	0x0	—

Description: Offset value subtracted from the coulomb counter CC2 measurement before scaling by Curr Gain to report result in userA.

12.1.2.3 Calibration:Current:CC1 Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Current	CC1 Gain	U2	0	65535	0x0	—

Description: Gain value used to scale the coulomb counter CC1 measurement after the CC1 Offset is subtracted, for reporting in userA

12.1.2.4 Calibration:Current:CC1 Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Current	CC1 Offset	I2	–32768	32767	0x0	—

Description: Offset value subtracted from the coulomb counter CC1 measurement before scaling by CC1 Gain to report result in userA

12.1.3 Calibration:Temperature

12.1.3.1 Calibration:Temperature:TS Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Temperature	TS Offset	I2	–32768	32767	0x0	—

Description: Offset value subtracted from the TS pin ADC measurement before result is reported

12.1.3.2 Calibration:Temperature:Int Temp Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Temperature	Int Temp Gain	U2	0	65535	0x0	—

Description: Internal temperature gain value used to scale the internal temperature ADC measurement after the Int Temp Offset is subtracted, for reporting in degrees Celsius

12.1.3.3 Calibration:Temperature:Int Temp Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Temperature	Int Temp Offset	I2	–32768	32767	0x0	—

Description: Internal temperature offset value subtracted from the internal temperature ADC measurement before scaling by Int Temp Gain, to report result in degrees Celsius

12.2 Settings

12.2.1 Settings:Configuration

12.2.1.1 Settings:Configuration:Power Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	Power Config	H1	0x00	0xFF	0x01	Hex

7	6	5	4	3	2	1	0
LOOP_SPEED_1	LOOP_SPEED_0	CB_LOOP_SPEED_1	CB_LOOP_SPEED_0	OTSD	LFOWD	DPSLP_LFO	SLEEP_EN

Description: This register contains several settings that affect the power of the device

Table 12-1. Power Config Register Field Descriptions

Bit	Field	Default	Description
7–6	LOOP_SPEED_1–LOOP_SPEED_0	0	Sets normal ADC scan loop speed by inserting current-only measurements after each voltage and temperature scan loop. This setting is used while cell balancing is not active. 0 = Full speed 1 = Half speed 2 = Quarter speed 3 = Eighth speed
5–4	CB_LOOP_SPEED_1–CB_LOOP_SPEED_0	0	Sets ADC scan loop speed while cell balancing is active by inserting idle slots after each voltage and temperature scan loop. This can be used to slow down voltage measurements while balancing to increase the duty-cycle, since balancing must be paused during measurement of the cell. 0 = Full speed 1 = Half speed 2 = Quarter speed 3 = Eighth speed
3	OTSD	0	Determines whether the device shuts down if the die HW overtemperature detector triggers a fault. 0 = Do not shutdown when the HW OT triggers 1 = Device enters shutdown when the HW OT triggers
2	LFOWD	0	Determines whether the device shuts down if the LFO watchdog triggers a fault. 0 = Do not shutdown the device when an LFO watchdog fault occurs. 1 = Shutdown the device when an LFO watchdog fault occurs.
1	DPSLP_LFO	0	Determines whether or not to disable the Low Frequency Oscillator in DEEPSLEEP mode to conserve power. 0 = Disable the Low Frequency Oscillator in DEEPSLEEP mode (recommended) 1 = Enable the Low Frequency Oscillator in DEEPSLEEP mode
0	SLEEP_EN	1	Sets the default value of BatteryStatus()[SLEEP_EN] which enables or disables SLEEP mode. After initialization, SLEEP_EN can still be changed via the SLEEP_ENABLE and SLEEP_DISABLE subcommands. 0 = Disable SLEEP mode by default 1 = Enable SLEEP mode by default

12.2.1.2 Settings:Configuration:REGOUT Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	REGOUT Config	H1	0x00	0xFF	0x08	Hex

7	6	5	4	3	2	1	0
RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	REG_EN	REGCTL_2	REGCTL_1	REGCTL_0

Description: This register contains settings to control the REGOUT voltage regulator

Table 12-2. REGOUT Config Register Field Descriptions

Bit	Field	Default	Description
3	REG_EN	1	Default value of enable for REG_EN. This value is used upon exit of CONFIG_UPDATE mode, but can be modified during operation using the REGOUT Control() command. 0 = REGOUT is not enabled (default) 1 = REGOUT is enabled
2–0	REGCTL_2–REGCTL_0	0	Default value for the REGOUT LDO settings. This value is used upon exit of CONFIG_UPDATE mode, but can be modified during operation using the REGOUT Control() command. 0 = Set to 1.8V 1 = Set to 1.8V 2 = Set to 1.8V 3 = Set to 1.8V 4 = Set to 2.5V 5 = Set to 3.0V 6 = Set to 3.3V (default) 7 = Set to 5V

12.2.1.3 Settings:Configuration:I2C Address

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	I2C Address	H1	0x00	0x7F	0x08	Hex

7	6	5	4	3	2	1	0
RSVD0	I2CADDR_6	I2CADDR_5	I2CADDR_4	I2CADDR_3	I2CADDR_2	I2CADDR_1	I2CADDR_0

Description: This register sets the I^2C address for the serial communications interface

Table 12-3. I2C Address Register Field Descriptions

Bit	Field	Default	Description
6–0	I2CADDR_6–I2CADDR_0	8	7-bit I^2C Address. 0 = The device uses address 0x08.All other values are used as the address directly.

12.2.1.4 Settings:Configuration:I2C Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	I2C Config	H2	0x0000	0xFFFF	0x3400	Hex

15	14	13	12	11	10	9	8
I2CCSLTO	I2CCSHTO	I2CCSHTOT_1	I2CCSHTOT_0	I2CLLTO	I2CLLTOT_2	I2CLLTOT_1	I2CLLTOT_0

7	6	5	4	3	2	1	0
RSVD0_5	RSVD0_4	RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	I2CBBTO	CRC

Description: This register includes configuration settings for the I²C address for the serial communications interface

Table 12-4. I2C Config Register Field Descriptions

Bit	Field	Default	Description
15	I2CCSLTO	0	SCL Short Low Timeout, times out I²C logic if SCL is detected low for ~25ms 0 = Timeout is not enabled (default) 1 = Timeout is enabled
14	I2CCSHTO	0	SCL Short High Timeout, times out I²C logic if SCL is detected high for duration given by I²CCSHTOT1:0 0 = Timeout is not enabled (default) 1 = Timeout is enabled
13–12	I2CCSHTOT_1–I2CCSHTOT_0	3	SCL Short High Timeout Duration 0 = Timeout occurs after 64 ms 1 = Timeout occurs after 512 ms 2 = Timeout occurs after 1 ms 3 = Timeout occurs after 15 ms (default)
11	I2CLLTO	0	Long Low Timeout, times out I²C logic if SCL or SCL and SDA are detected low for duration given by I²CLLTOT 0 = Timeout occurs if SCL is detected low for duration I²CLLTOT (default) 1 = Timeout occurs if both SCL and SDA are detected low for duration I²CLLTOT
10–8	I2CLLTOT_2–I2CLLTOT_0	4	Long Low Timeout Duration 0 = Timeout is disabled 1 = Timeout occurs after 0.5 seconds 2 = Timeout occurs after 1 seconds 3 = Timeout occurs after 1.5 seconds 4 = Timeout occurs after 2 seconds (default) 5 = Timeout occurs after 2.5 seconds 6 = Timeout occurs after 3 seconds 7 = Timeout occurs after 3.5 seconds
1	I2CBBTO	0	I²C Bus Busy Timeout, times out I²C logic if a transaction is detected longer than the duration given by I²CLLTOT2:0 0 = Timeout is not enabled (default) 1 = Timeout is enabled
0	CRC	0	Controls whether the I²C serial communications interface uses CRC. 0 = CRC is not used (default) 1 = CRC is enabled

12.2.1.5 Settings:Configuration:DA Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	DA Config	H2	0x0000	0xFFFF	0x0000	Hex

15	14	13	12	11	10	9	8
RSVD0_6	RSVD0_5	RSVD0_4	RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	TSMODE
7	6	5	4	3	2	1	0
CCMODE_1	CCMODE_0	CVADCSPEED_1	CVADCSPEED_0	IADCSPEED_1	IADCSPEED_0	SSADCSPEED_1	SSADCSPEED_0

Description: This register includes configuration settings related to the device data acquisition.

Table 12-5. DA Config Register Field Descriptions

Bit	Field	Default	Description
8	TSMODE	0	This bit controls whether the TS pin is used for external thermistor measurement or as a general purpose ADC input. 0 = TS pin is used for external thermistor measurement, with the internal pullup resistor enabled during measurement, and the ADC used in ratiometric mode, using the internal REG18 LDO voltage for the pullup resistor bias and for the ADC reference. 1 = TS pin is used for general purpose ADC voltage measurement, with the internal pullup resistor disabled during measurement, and the ADC using the internal bandgap for its reference.
7–6	CCMODE_1–CCMODE_0	0	Selects coulomb counter mode. Note that CC1 Current() and accumulated charge integration only operates in modes where the coulomb counter is running continuously (0x00 NORMAL mode, or 0x01 NORMAL mode while no idle slots are being introduced, or 0x02 NORMAL mode) 0 = NORMAL mode: Coulomb counter runs continuously, independent of the LOOP_SLOW or CB_LOOP_SLOW setting. SLEEP mode: Coulomb counter run continuously while the voltage ADC is running in SLEEP mode during a burst measurement. It stops at the conclusion of the measurement underway when the burst measurement completes. Startup mode (at initial powerup from SHUTDOWN or exit of DEEPSLEEP): Coulomb counter runs continuously while the voltage ADC is running during the Startup Sequence. It stops at the conclusion of the measurement underway when the Startup Sequence completes (default) 1 = NORMAL mode: Coulomb counter runs continuously if LOOP_SLOW or CB_LOOP_SLOW is set to the fastest setting. When these parameters are modified to slower settings, the device inserts 1, 3, or 7 idle slots between each current measurement slot, thereby reducing the average output rate of the current measurements. SLEEP mode: Coulomb counter run continuously while the voltage ADC is running in SLEEP mode during a burst measurement. It stops at the conclusion of the measurement underway when the burst measurement completes. Startup mode (at initial powerup from SHUTDOWN or exit of DEEPSLEEP): Coulomb counter runs continuously while the voltage ADC is running during the Startup Sequence. It stops at the conclusion of the measurement underway when the Startup Sequence completes. 2 = NORMAL mode: Coulomb counter runs continuously in low power mode (so only takes ~4 µA instead of ~60 µA).SLEEP mode: SLEEP mode: Coulomb counter takes one measurement at the beginning of each burst measurement using its low power mode. Startup mode (at initial powerup from SHUTDOWN or exit of DEEPSLEEP): Coulomb counter takes one measurement using its low power mode at the beginning of the Startup Sequence. 3 = Coulomb counter is powered down and does not operate at all. This provides a low power mode for customers who do not need current measurement.
5–4	CVADCSPEED_1–CVADCSPEED_0	0	Selects ADC conversion speed for cell voltage measurements. Higher speed results in higher noise in conversions. 0 = 2.93 ms per conversion (default) 1 = 1.46 ms per conversion 2 = 732 µs per conversion 3 = 366 µs per conversion
3–2	IADCSPEED_1–IADCSPEED_0	0	Selects ADC conversion speed for current measurements. Higher speed results in higher noise in conversions. 0 = 2.93 ms per conversion (default) 1 = 1.46 ms per conversion 2 = 732 µs per conversion 3 = 366 µs per conversion

Table 12-5. DA Config Register Field Descriptions (continued)

Bit	Field	Default	Description
1–0	SSADCSPEED_1–SSADCSPEED_0	0	Selects ADC conversion speed for Shared Slot measurements. Higher speed results in higher noise in conversions. 0 = 2.93 ms per conversion (default) 1 = 1.46 ms per conversion 2 = 732 µs per conversion 3 = 366 µs per conversion

12.2.1.6 Settings:Configuration:Vcell Mode

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	Vcell Mode	H1	0x00	0x05	0x0	Hex

7	6	5	4	3	2	1	0
RSVD0_4	RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	VCELL_2	VCELL_1	VCELL_0

Description: Not every system uses all of the cell input pins. If the system has fewer cells than the device supports, some VC input pins must be shorted together. To prevent action being taken for cell undervoltage conditions on pins that are shorted, set these bits appropriately.

Table 12-6. Vcell Mode Register Field Descriptions

Bit	Field	Default	Description
2–0	VCELL_2–VCELL_0	0	Not every system uses all of the cell input pins. If the system has fewer cells than the device supports, some VC input pins must be shorted together. To prevent action being taken for cell undervoltage conditions on pins that are shorted, set these bits appropriately. 0 = All cell inputs are used for actual cells. 1 = All cell inputs are used for actual cells. 2 = Two actual cells are in use (VC5-VC4A, VC1-VC0), unused cell pins can be shorted to an adjacent cell pin at the device or connected through RC to the cells. 3 = Three actual cells are in use (VC5-VC4A, VC2-VC1, VC1-VC0), unused cell pins can be shorted to an adjacent cell pin at the device or connected through RC to the cells. 4 = Four actual cells are in use (VC5-VC4A, VC4B-VC3A, VC2-VC1, VC1-VC0), unused cell pins can be shorted to an adjacent cell pin at the device or connected through RC to the cells. 5 = All cell inputs are used for actual cells.

12.2.1.7 Settings:Configuration:Default Alarm Mask

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	Default Alarm Mask	H2	0x0000	0xFFFF	0xC200	Hex

15	14	13	12	11	10	9	8
SSA	SSB	SAA	SAB	XCHG	XDSG	SHUTV	CB

7	6	5	4	3	2	1	0
FULLSCAN	ADSCAN	WAKE	SLEEP	TIMER_ALARM	INITCOMP	CDTOGGLE	POR

Description: This parameter sets the default value of the AlarmEnable() register. The default value is reloaded at reset (if programmed into OTP) and at exit of CONFIG_UPDATE mode

Table 12-7. Default Alarm Mask Register Field Descriptions

Bit	Field	Default	Description
15	SSA	1	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
14	SSB	1	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
13	SAA	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
12	SAB	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
11	XCHG	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
10	XDSG	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
9	SHUTV	1	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
8	CB	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
7	FULLSCAN	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
6	ADSCAN	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
5	WAKE	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
4	SLEEP	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
3	TIMER_ALARM	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()

Table 12-7. Default Alarm Mask Register Field Descriptions (continued)

Bit	Field	Default	Description
2	INITCOMP	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()
1	CDTOGGLE	0	Setting this bit allows the internally determined value of CDTOGGLE to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. This flag is set whenever the debounced CHG Detector signal differs from the previous debounced value. 0 = The CDTOGGLE signal is not included in Alarm Status() 1 = The CDTOGGLE signal is included in Alarm Status()
0	POR	0	Setting this bit allows the corresponding bit in Alarm Raw Status() to be mapped to the corresponding bit in Alarm Status() and to control the ALERT pin. 0 = This bit in Alarm Raw Status() is not included in Alarm Status() 1 = This bit in Alarm Raw Status() is included in Alarm Status()

12.2.1.8 Settings:Configuration:FET Options

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	FET Options	H1	0x00	0xFF	0x18	Hex

7	6	5	4	3	2	1	0
CHGDETEN	HOST_FETOFF_EN	HOST_FETON_EN	SLEEPCHG	SFET	FET_EN	PWM_EN	PROTRCVR

Description: This bit field includes settings related to the FET driver operation

Table 12-8. FET Options Register Field Descriptions

Bit	Field	Default	Description
7	CHGDETEN	0	The CHG Detector block is enabled and provides an output signal to the Alarm logic. 0 = CHG Detector block is disabled 1 = CHG Detector block is enabled
6	HOST_FETOFF_EN	0	Some systems need the ability to override the device's FET control and force the FETs to turn off through commands. If that functionality is not needed, it can be disabled to prevent commands from turning the FETs off. 0 = Host FET turnoff control commands are ignored 1 = Host FET turnoff control commands are allowed
5	HOST_FETON_EN	0	Some systems need the ability to override the device's FET control and force the FETs to turn on through commands. If that functionality is not needed, it can be disabled to prevent commands from turning the FETs on. 0 = Host FET turn-on control commands are ignored 1 = Host FET turn-on control commands are allowed
4	SLEEPCHG	1	The CHG FET can be disabled while in SLEEP mode to conserve power. This bit configures whether or not to allow the CHG FET to be enabled in SLEEP mode. 0 = CHG FET is turned off in SLEEP mode 1 = CHG FET can be enabled in SLEEP mode
3	SFET	1	The device supports both series and parallel FET configurations. When the CHG and DSG FETs are in series, current can flow through the body diode of one of the FETs when the other is enabled. In this configuration, body diode protection is used to turn the FET on when current above a threshold is detected to be flowing through that FET. When the system has separate DSG and CHG paths and parallel FETs, body diode protection is not needed and can be disabled. 0 = Parallel FET mode: Body diode protection is disabled 1 = Series FET mode: Body diode protection is enabled

Table 12-8. FET Options Register Field Descriptions (continued)

Bit	Field	Default	Description
2	FET_EN	0	This is the default value of the bit which enables or disables device autonomous control of the FET drivers. If autonomous FET control is disabled, the device is in FET Test mode, in which the FET states are entirely controlled by the FET Control command. This is typically used during manufacturing to test FET circuitry or manual host control. Note that the FETs can still be enabled for body diode protection in FET Test mode. This bit is loaded into the active state upon exit of CONFIG_UPDATE mode. The active state in use is provided by BatteryStatus([FET_EN]) and can be toggled during operation using the FET_ENABLE() subcommand. 0 = Autonomous FET control is disabled by default upon exit of CONFIG_UPDATE mode. FET Test mode is enabled. Device does not turn on FETs unless FET Control command instructs it to do so. 1 = Autonomous FET control is enabled by default upon exit of CONFIG_UPDATE mode. FET Test mode is disabled. FET Control commands can still be used, based on the settings of HOST_FETOFF_EN and HOST_FETON_EN.
1	PWM_EN	0	This bit enables or disables the capability for the host to use the FET driver PWM modes. 0 = Host PWM commands are ignored. 1 = How PWM commands are accepted.
0	PROTRCVR	0	This bit enables or disables the capability to manually recover faults using the PROT_RECOVERY() subcommand. 0 = PROT_RECOVERY() subcommand cannot be used in SEALED mode. 1 = PROT_RECOVERY() subcommand can be used in SEALED mode.

12.2.1.9 Settings:Configuration:Charge Detector Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	Charge Detector Time	U1	0	255	1	100ms

Description: This value sets the debounce timing used for the Charge Detect signal. The debounce delay is programmable in units of 100 ms, from 0 to 25.5 seconds

12.2.2 Settings:Cell Balancing

12.2.2.1 Settings:Cell Balancing:Balancing Configuration

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Balancing	Balancing Configuration	H1	0x00	0xFF	0x02	Hex

7	6	5	4	3	2	1	0
RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	CBDLY_2	CBDLY_1	CBDLY_0	CB_NO_CMD

Description: This bit field includes settings to control the cell balancing operation

Table 12-9. Balancing Configuration Register Field Descriptions

Bit	Field	Default	Description
3–1	CBDLY_2–CBDLY_0	1	This setting determines the delay from when cell balancing is disabled before cell measurements begin, to allow voltage transients at the cell input pins to settle. 0 = No delay 1 = 1 ms delay 2 = 2 ms delay 3 = 4 ms delay 4 = 8 ms delay 5 = 16 ms delay 6 = 32 ms delay 7 = 64 ms delay
0	CB_NO_CMD	0	This bit enables blocking writes to the CB_ACTIVE_CELLS() subcommand if host-controlled balancing is not desired. Readback of cell balancing status using this command is always enabled. 0 = Writes to CB_ACTIVE_CELLS() are accepted. 1 = Writes to CB_ACTIVE_CELLS() are ignored.

12.2.2.2 Settings:Cell Balancing:Min Temp Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Balancing	Min Temp Threshold	U1	0	255	255	256-LSBs

Description: When the measurement of the TS pin configured for a thermistor is above this value, cell balancing is not allowed. Value ranges from 0 to 32512 in steps of 256 16-bit ADC codes. When using an NTC, this value corresponds to the low temperature limit

12.2.2.3 Settings:Cell Balancing:Max Temp Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Balancing	Max Temp Threshold	U1	0	255	0	256 LSBs

Description: When the measurement of the TS pin configured for a thermistor is below this value, cell balancing is not allowed. Value ranges from 0 to 32512 in steps of 256 16-bit ADC codes. When using an NTC, this value corresponds to the high temperature limit.

12.2.2.4 Settings:Cell Balancing:Max Internal Temp

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Balancing	Max Internal Temp	I1	–128	127	85	°C

Description: When the internal temperature is above this value, cell balancing is not allowed. Units are in °C signed

12.2.3 Settings:Protection

12.2.3.1 Settings:Protection:Enabled Protections A

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	Enabled Protections A	H1	0x00	0xFF	0xA1	Hex

7	6	5	4	3	2	1	0
COV	CUV	SCD	OCD1	OCD2	OCC	CURLATCH	REGOUT

Description: This bit field enables or disables various protections. Protections that are enabled set their corresponding Safety Status flags when a fault is detected.

Settings:Protection:CHG FET Protections A, Settings:Protection:DSG FET Protections A, and Settings:Protection:Both FET Protections B must be appropriately configured to control the FET action taken when these faults are detected.

Table 12-10. Enabled Protections A Register Field Descriptions

Bit	Field	Default	Description
7	COV	1	Cell Overvoltage Protection 0 = Disabled 1 = Enabled
6	CUV	0	Cell Undervoltage Protection 0 = Disabled 1 = Enabled
5	SCD	1	Short circuit in discharge protection 0 = Disabled 1 = Enabled
4	OCD1	0	Overcurrent in discharge protection 1 0 = Disabled 1 = Enabled
3	OCD2	0	Overcurrent in discharge protection 2 0 = Disabled 1 = Enabled
2	OCC	0	Overcurrent in charge protection 0 = Disabled 1 = Enabled
1	CURLATCH	0	Current latch protection 0 = Disabled 1 = Enabled
0	REGOUT	1	REGOUT safety check 0 = Disabled 1 = Enabled

12.2.3.2 Settings:Protection:Enabled Protections B

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	Enabled Protections B	H1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
RSVD0_1	RSVD0_0	OTD	OTC	UTD	UTC	OTINT	HWD

Description: This bit field enables or disables various protections. Protections that are enabled set their corresponding Safety Status flags when a fault is detected. Settings:Protection:CHG FET Protections A, Settings:Protection:DSG FET Protections A, and Settings:Protection:Both FET Protections B must be appropriately configured to control the FET action taken when these faults are detected.

Table 12-11. Enabled Protections B Register Field Descriptions

Bit	Field	Default	Description
5	OTD	0	Overtemperature in Discharge Protection 0 = Disabled 1 = Enabled
4	OTC	0	Overtemperature in Charge Protection 0 = Disabled 1 = Enabled

Table 12-11. Enabled Protections B Register Field Descriptions (continued)

Bit	Field	Default	Description
3	UTD	0	Undertemperature in Discharge Protection 0 = Disabled 1 = Enabled
2	UTC	0	Undertemperature in Charge Protection 0 = Disabled 1 = Enabled
1	OTINT	0	Internal Overtemperature Protection 0 = Disabled 1 = Enabled
0	HWD	0	Host Watchdog Protection 0 = Disabled 1 = Enabled

12.2.3.3 Settings:Protection:DSG FET Protections A

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	DSG FET Protections A	H1	0x00	0xFF	0xFF	Hex

7	6	5	4	3	2	1	0
CUV	SCD	OCD1	OCD2	HWD	OTD	UTD	OTINT

Description: This bit field configures which protections disable the DSG FET.

Table 12-12. DSG FET Protections A Register Field Descriptions

Bit	Field	Default	Description
7	CUV	1	Cell Undervoltage Protection 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
6	SCD	1	Short circuit in discharge protection 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
5	OCD1	1	Overcurrent in discharge protection 1 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
4	OCD2	1	Overcurrent in discharge protection 2 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
3	HWD	1	Host Watchdog Protection 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
2	OTD	1	Overtemperature in Discharge Protection 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
1	UTD	1	Undertemperature in Discharge Protection 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
0	OTINT	1	Internal Overtemperature Protection 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.

12.2.3.4 Settings:Protection:CHG FET Protections A

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	CHG FET Protections A	H1	0x00	0xFF	0xEF	Hex

7	6	5	4	3	2	1	0
COV	SCD	OCC	RSVD0	HWD	OTC	UTC	OTINT

Description: This bit field configures which protections disable the CHG FET.

Table 12-13. CHG FET Protections A Register Field Descriptions

Bit	Field	Default	Description
7	COV	1	Cell Overvoltage Protection 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
6	SCD	1	Short Circuit in Discharge Protection 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
5	OCC	1	Overcurrent in Charge Protection 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
3	HWD	1	Host Watchdog Protection 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
2	OTC	1	Overtemperature in Charge Protection 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
1	UTC	1	Undertemperature in Charge Protection 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
0	OTINT	1	Internal Overtemperature Protection 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.

12.2.3.5 Settings:Protection:Both FET Protections B

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	Both FET Protections B	H1	0x00	0xFF	0x06	Hex

7	6	5	4	3	2	1	0
RSVD0_4	RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	VREF	VSS	REGOUT

Description: This bit field configures which protections disable Both FETs.

Table 12-14. Both FET Protections B Register Field Descriptions

Bit	Field	Default	Description
2	VREF	1	VREF Measurement Check 0 = Both FETs are not disabled when protection is triggered. 1 = Both FETs are disabled when protection is triggered.
1	VSS	1	VSS Measurement Check 0 = Both FETs are not disabled when protection is triggered. 1 = Both FETs are disabled when protection is triggered.

Table 12-14. Both FET Protections B Register Field Descriptions (continued)

Bit	Field	Default	Description
0	REGOUT	0	REGOUT flag 0 = Both FETs are not disabled when protection is triggered. 1 = Both FETs are disabled when protection is triggered.

12.2.3.6 Settings:Protection:Body Diode Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	Body Diode Threshold	I2	0	32767	64	userA

Description: This register sets the current threshold at which the device enables the FET driver to protect the body diode.

To minimize power dissipation in the FET body diode, the FET is turned on when reverse current is detected and the other FET is on.

When measured discharge current is greater in magnitude than Settings:Protection:Body Diode Threshold and the DSG FET is on, the CHG FET is turned on.

When measured charge current is greater than Settings:Protection:Body Diode Threshold and the CHG FET is on, the DSG FET is turned on.

When in parallel FET mode (Settings:FET:FET Options[SFET] = 0), body diode protection is disabled and a FET is not turned on in response to reverse current.

12.2.3.7 Settings:Protection:Cell Open Wire NORMAL Check Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	Cell Open Wire NORMAL Check Time	U1	0	255	0x0	FULLSCAN intervals

Description: This register sets the timing for the cell open-wire checks in NORMAL mode.

In order to detect a broken connection between a cell in the stack and the PCB, the device periodically enables a current from each enabled cell input to VSS.

0 = Cell open-wire check is disabled in NORMAL mode, current is not enabled.

All other values = Cell open-wire check is enabled for one measurement slot per ADSCAN per cell, then is disabled for the number of FULLSCANs given by this value in NORMAL mode.

12.2.3.8 Settings:Protection:Cell Open Wire SLEEP Check Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	Cell Open Wire SLEEP Check Time	H1	0x00	0xFF	0x10	Hex

7	6	5	4	3	2	1	0
RSVD0	COWDLY_2	COWDLY_1	COWDLY_0	COWSEN	COWSTIME_2	COWSTIME_1	COWSTIME_0

Description: This register sets the timing for the cell open-wire checks in SLEEP mode

Table 12-15. Cell Open Wire SLEEP Check Time Register Field Descriptions

Bit	Field	Default	Description
6–4	COWDLY_2–COWDLY_0	1	This setting determines the delay from when the cell open-wire current is disabled before cell measurements begin in NORMAL mode, to allow voltage transients at the cell input pins to settle. 0 = No delay 1 = 1 ms delay 2 = 2 ms delay 3 = 4 ms delay 4 = 8 ms delay 5 = 16 ms delay 6 = 32 ms delay 7 = 64 ms delay
3	COWSEN	0	Enable cell open-wire checks during SLEEP mode. 0 = Cell open-wire checks are disabled in SLEEP mode. 1 = Cell open-wire checks are enabled in SLEEP mode.
2–0	COWSTIME_2–COWSTIME_0	0	In order to detect a broken connection between a cell in the stack and the PCB, the device periodically enables a current from each enabled cell input to VSS. 0 = Current sources are activated once every 8 burst measurements. 1 = Current sources are activated once every 4 burst measurements. 2 = Current sources are activated once every 2 burst measurements. 3 = Current sources are activated once every burst measurement. 4 = Current sources are activated twice every burst measurement. 5 = Current sources are activated 4 times every burst measurement. 6 = Current sources are activated 8 times every burst measurement. 7 = Current sources are activated 16 times every burst measurement.

12.2.3.9 Settings:Protection:Host Watchdog Timeout

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	Host Watchdog Timeout	U1	0	255	0x0	Varying

Description: This register sets the timing for the Host Watchdog timing. If communications are not received for this many seconds, the Host Watchdog Fault is triggered. The Host Watchdog Alert is triggered when the timer reaches half of the timeout.

0 to 15: 1 to 16 sec in 1-second steps

16 to 255: 20 to 976-sec in 4-second steps

12.3 Protections

12.3.1 Protections:Cell Voltage

12.3.1.1 Protections:Cell Voltage:Cell Undervoltage Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Cell Voltage	Cell Undervoltage Protection Threshold	I2	0	5500	2500	mV

Description: This parameter sets the Cell Undervoltage Protection threshold in units of mV.

Minimum value = 0 (setting for 0 V)

Maximum value = 5500 (setting for 5.5 V)

12.3.1.2 Protections:Cell Voltage:Cell Undervoltage Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Cell Voltage	Cell Undervoltage Protection Delay	U1	0	255	10	ADSCAN intervals

Description: This parameter sets the Cell Undervoltage Protection delay. Units are the number of ADSCAN measurements taken (timing depends on the measurement speed settings and can be longer in SLEEP mode) and can range from 1 to 255.

12.3.1.3 Protections:Cell Voltage:Cell Undervoltage Protection Recovery Hysteresis

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Cell Voltage	Cell Undervoltage Protection Recovery Hysteresis	H1	0x00	0x03	0x02	Hex

7	6	5	4	3	2	1	0
RSVD0_5	RSVD0_4	RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	CUVRCVR_1	CUVRCVR_0

Description: This parameter sets the Cell Undervoltage Protection recovery hysteresis threshold. The minimum cell voltage must be greater than or equal to the CUV threshold plus this hysteresis to recover from a CUV condition

Table 12-16. Cell Undervoltage Protection Recovery Hysteresis Register Field Descriptions

Bit	Field	Default	Description
1–0	CUVRCVR_1–CUVRCVR_0	2	This parameter sets the Cell Undervoltage Protection recovery hysteresis threshold. The minimum cell voltage must be greater than or equal to the CUV threshold plus this hysteresis to recover from a CUV condition. 0 = no autonomous recovery 1 = 50mV 2 = 100mV 3 = 200mV

12.3.1.4 Protections:Cell Voltage:Cell Overvoltage Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Cell Voltage	Cell Overvoltage Protection Threshold	I2	0	5500	4200	mV

Description: This parameter sets the Cell Overvoltage Protection threshold in units of mV.

Minimum value = 0 (setting for 0 V)

Maximum value = 5500 (setting for 5.5 V)

12.3.1.5 Protections:Cell Voltage:Cell Overvoltage Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Cell Voltage	Cell Overvoltage Protection Delay	U1	0	255	10	ADSCAN intervals

Description: This parameter sets the Cell Overvoltage Protection delay. Units are the number of ADSCAN measurements taken (timing depends on the measurement speed settings and can be longer in SLEEP mode) and can range from 1 to 255.

12.3.1.6 Protections:Cell Voltage:Cell Overvoltage Protection Recovery Hysteresis

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Cell Voltage	Cell Overvoltage Protection Recovery Hysteresis	H1	0x00	0x03	0x02	Hex

7	6	5	4	3	2	1	0
RSVD0_5	RSVD0_4	RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	COVRCVR_1	COVRCVR_0

Description: This parameter sets the Cell Overvoltage Protection recovery hysteresis threshold. The maximum cell voltage must be less than or equal to the COV threshold minus this hysteresis to recover from a COV condition

Table 12-17. Cell Overvoltage Protection Recovery Hysteresis Register Field Descriptions

Bit	Field	Default	Description
1–0	COVRCVR_1–COVRCVR_0	2	This parameter sets the Cell Overvoltage Protection recovery hysteresis threshold. The maximum cell voltage must be less than or equal to the COV threshold minus this hysteresis to recover from a COV condition. 0 = no autonomous recovery 1 = 50mV 2 = 100mV 3 = 200mV

12.3.2 Protections:Current

12.3.2.1 Protections:Current:Overcurrent in Charge Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Overcurrent in Charge Protection Threshold	U1	2	62	2	2mV

Description: This parameter sets the Overcurrent in Charge Protection threshold in units of 2mV.

Minimum value = 2 (setting for 4 mV)

Maximum value = 62 (setting for 124 mV)

12.3.2.2 Protections:Current:Overcurrent in Charge Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Overcurrent in Charge Protection Delay	U1	0	255	58	Varying

Description: This parameter sets the Overcurrent in Charge Protection delay.

0x00 = Fastest delay (~0.46 ms)

0x01 - 0x40 = 1.22 ms to 20.435 ms in steps of 0.305 ms

0x41 - 0x80 = 22.875 ms to 176.595 ms in steps of 2.44 ms

0x81 - 0xC0 = 181.475 ms to 488.915 ms in steps of 4.88 ms

0xC1 - 0xFF = 498.675 ms to 1103.795 ms in steps of 9.77 ms

12.3.2.3 Protections:Current:Overcurrent in Discharge 1 Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Overcurrent in Discharge 1 Protection Threshold	U1	2	100	4	2mV

Description: This parameter sets the Overcurrent in Discharge 1 Protection threshold in units of 2mV.

Minimum value = 2 (setting for 4 mV)

Maximum value = 100 (setting for 200 mV)

12.3.2.4 Protections:Current:Overcurrent in Discharge 1 Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Overcurrent in Discharge 1 Protection Delay	U1	0	255	6	—

Description: This parameter sets the Overcurrent in Discharge 1 Protection delay.

0x00 = Fastest delay (~0.46 ms)

0x01 - 0x40 = 1.22 ms to 20.435 ms in steps of 0.305 ms

0x41 - 0x80 = 22.875 ms to 176.595 ms in steps of 2.44 ms

0x81 - 0xC0 = 181.475 ms to 488.915 ms in steps of 4.88 ms

0xC1 - 0xFF = 498.675 ms to 1103.795 ms in steps of 9.77 ms

12.3.2.5 Protections:Current:Overcurrent in Discharge 2 Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Overcurrent in Discharge 2 Protection Threshold	U1	2	100	3	2mV

Description: This parameter sets the Overcurrent in Discharge 2 Protection threshold in units of 2mV.

Minimum value = 2 (setting for 4 mV)

Maximum value = 100 (setting for 200 mV)

12.3.2.6 Protections:Current:Overcurrent in Discharge 2 Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Overcurrent in Discharge 2 Protection Delay	U1	0	255	19	—

Description: This parameter sets the Overcurrent in Discharge 2 Protection delay.

0x00 = Fastest delay (~0.46 ms)

0x01 - 0x40 = 1.22 ms to 20.435 ms in steps of 0.305 ms

0x41 - 0x80 = 22.875 ms to 176.595 ms in steps of 2.44 ms

0x81 - 0xC0 = 181.475 ms to 488.915 ms in steps of 4.88 ms

0xC1 - 0xFF = 498.675 ms to 1103.795 ms in steps of 9.77 ms

12.3.2.7 Protections:Current:Short Circuit in Discharge Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Short Circuit in Discharge Protection Threshold	H1	0x00	0xFF	0x0	Varying

7	6	5	4	3	2	1	0
RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	SCDTHR_3	SCDTHR_2	SCDTHR_1	SCDTHR_0

Description: This parameter sets the Short Circuit in Discharge Protection threshold for the sense resistor voltage

Table 12-18. Short Circuit in Discharge Protection Threshold Register Field Descriptions

Bit	Field	Default	Description
3–0	SCDTHR_3–SCDTHR_0	0	This parameter sets the Short Circuit in Discharge Protection threshold for the sense resistor voltage. 0 = 10 mV 1 = 20 mV 2 = 40 mV 3 = 60 mV 4 = 80 mV 5 = 100 mV 6 = 125 mV 7 = 150 mV 8 = 175 mV 9 = 200 mV 10 = 250 mV 11 = 300 mV 12 = 350 mV 13 = 400 mV 14 = 450 mV 15 = 500 mV

12.3.2.8 Protections:Current:Short Circuit in Discharge Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Short Circuit in Discharge Protection Delay	H1	0x00	0x0A	0x01	Varying

7	6	5	4	3	2	1	0
RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	SCDDLY_3	SCDDLY_2	SCDDLY_1	SCDDLY_0

Description: This parameter sets the Short Circuit in Discharge Protection delay

Table 12-19. Short Circuit in Discharge Protection Delay Register Field Descriptions

Bit	Field	Default	Description
3–0	SCDDLY_3–SCDDLY_0	1	This parameter sets the delay before the fault is triggered. 0 = Fastest 1 = 15 µs 2 = 31 µs 3 = 61 µs 4 = 122 µs 5 = 244 µs 6 = 488 µs 7 = 977 µs 8 = 1953 µs 9 = 3906 µs 10 = 7797 µs

12.3.2.9 Protections:Current:Latch Limit

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Latch Limit	H1	0x00	0x07	0x0	Varying

7	6	5	4	3	2	1	0
RSVD0_4	RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	CURRLAT_2	CURRLAT_1	CURRLAT_0

Description: This parameter configures the number of retries for recovery of the SCD, OCD1, OCD2, or OCC before the FETs are latched as disabled.

Table 12-20. Latch Limit Register Field Descriptions

Bit	Field	Default	Description
2–0	CURRLAT_2–CURRLAT_0	0	This parameter configures the number of retries for recovery of the SCD, OCD1, OCD2, or OCC before the FETs are latched as disabled. If the protection does not retrigger within 5-sec after a recovery, the counter will be reset to 0. 0 = Latching is disabled 1 = 2 retries before FETs are latched disabled 2 = 4 retries before FETs are latched disabled 3 = 8 retries before FETs are latched disabled 4 = 16 retries before FETs are latched disabled 5 = 32 retries before FETs are latched disabled 6 = 48 retries before FETs are latched disabled 7 = 96 retries before FETs are latched disabled

12.3.2.10 Protections:Current:Recovery Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Current	Recovery Time	U1	0	255	5	Seconds

Description: This parameter configures the delay after which current protections recover.

Programmable from 1 second to 255 seconds in 1-second steps.

0x0 = Disable auto recovery

12.3.3 Protections:Temperature

12.3.3.1 Protections:Temperature:Overtemperature in Charge Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Overtemperature in Charge Protection Threshold	U1	0	255	55	54-LSBs

Description: This parameter configures the threshold for the Overtemperature in Charge Protection. The protection is triggered when the TS measurement is below this threshold.

This sets the threshold measured at the TS pin from 0 to 13770 in steps of 54 16-bit ADC codes.

12.3.3.2 Protections:Temperature:Overtemperature in Charge Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Overtemperature in Charge Protection Delay	U1	0	255	15	Measurements

Description: This parameter configures the delay for the Overtemperature in Charge Protection in units of numbers of measurements.

The settings are from 0 (fastest) to 255 measurements.

12.3.3.3 Protections:Temperature:Overtemperature in Charge Protection Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Overtemperature in Charge Protection Recovery	U1	0	255	63	54-LSBs

Description: This parameter configures the recovery threshold for the Overtemperature in Charge Protection. The protection recovers when the TS measurement is above this threshold.

This sets the threshold measured at the TS pin from 0 to 13770 in steps of 54 16-bit ADC codes.

12.3.3.4 Protections:Temperature:Undertemperature in Charge Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Undertemperature in Charge Protection Threshold	U1	0	255	147	77-LSBs

Description: This parameter configures the threshold for the Undertemperature in Charge Protection. The protection is triggered when the TS measurement is above this threshold.

This sets the threshold measured at the TS pins from 0 to 19635 in steps of 77 16-bit ADC codes.

12.3.3.5 Protections:Temperature:Undertemperature in Charge Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Undertemperature in Charge Protection Delay	U1	0	255	15	Measurements

Description: This parameter configures the delay for the Undertemperature in Charge Protection in units of numbers of measurements.

The settings are from 0 (fastest) to 255 measurements.

12.3.3.6 Protections:Temperature:Undertemperature in Charge Protection Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Undertemperature in Charge Protection Recovery	U1	0	255	134	77-LSBs

Description: This parameter configures the recovery threshold for the Undertemperature in Charge Protection. The protection recovers when the TS measurement falls below this threshold.

This sets the threshold measured at the TS pins from 0 to 19635 in steps of 77 16-bit ADC codes.

12.3.3.7 Protections:Temperature:Overtemperature in Discharge Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Overtemperature in Discharge Protection Threshold	U1	0	255	48	54-LSBs

Description: This parameter configures the threshold for the Overtemperature in Discharge Protection. The protection is triggered when the TS measurement is below this threshold.

This sets the threshold measured at the TS pin from 0 to 13770 in steps of 54 16-bit ADC codes.

12.3.3.8 Protections:Temperature:Overtemperature in Discharge Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Overtemperature in Discharge Protection Delay	U1	0	255	15	Measurements

Description: This parameter configures the delay for the Overtemperature in Discharge Protection in units of numbers of measurements.

The settings are from 0 (fastest) to 255 measurements.

12.3.3.9 Protections:Temperature:Overtemperature in Discharge Protection Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Overtemperature in Discharge Protection Recovery	U1	0	255	55	54-LSBs

Description: This parameter configures the recovery threshold for the Overtemperature in Discharge Protection. The protection recovers when the TS measurement rises above this threshold.

This sets the threshold measured at the TS pin from 0 to 13770 in steps of 54 16-bit ADC codes.

12.3.3.10 Protections:Temperature:Undertemperature in Discharge Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Undertemperature in Discharge Protection Threshold	U1	0	255	147	77-LSBs

Description: This parameter configures the threshold for the Undertemperature in Discharge Protection.

This sets the threshold measured at the TS pins from 0 to 19635 in steps of 77 16-bit ADC codes.

12.3.3.11 Protections:Temperature:Undertemperature in Discharge Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Undertemperature in Discharge Protection Delay	U1	0	255	15	Measurements

Description: This parameter configures the delay for the Undertemperature in Discharge Protection in units of numbers of measurements.

The settings are from 0 (fastest) to 255 measurements.

12.3.3.12 Protections:Temperature:Undertemperature in Discharge Protection Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Undertemperature in Discharge Protection Recovery	U1	0	255	134	77-LSBs

Description: This parameter configures the recovery threshold for the Undertemperature in Discharge Protection.

This sets the threshold measured at the TS pins from 0 to 19635 in steps of 77 16-bit ADC codes.

12.3.3.13 Protections:Temperature:Internal Overtemperature Protection Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Internal Overtemperature Protection Threshold	U1	25	150	105	°C

Description: This parameter configures the threshold for the Internal Overtemperature Protection.

The settings set the temperature threshold from 25°C to 150°C in 1°C steps.

12.3.3.14 Protections:Temperature:Internal Overtemperature Protection Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Internal Overtemperature Protection Delay	U1	0	255	15	Measurements

Description: This parameter configures the delay for the Internal Overtemperature Protection in units of numbers of measurements.

The settings are from 0 (fastest) to 255 measurements.

12.3.3.15 Protections:Temperature:Internal Overtemperature Protection Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Temperature	Internal Overtemperature Protection Recovery	U1	25	150	100	°C

Description: This parameter configures the recovery threshold for the Internal Overtemperature Protection.

The settings set the temperature recovery threshold from 25°C to 150°C in 1°C steps.

12.4 Power

12.4.1 Power:Sleep

12.4.1.1 Power:Sleep:Sleep Current

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Sleep	Sleep Current	I2	0	32767	64	userA

Description: Configures the current threshold above which the device does not enter SLEEP mode. If a current magnitude is measured above this value during a periodic measurement in SLEEP mode, SLEEP mode is exited

12.4.1.2 Power:Sleep:Voltage Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Sleep	Voltage Time	U1	0	255	5	Seconds

Description: This parameter sets how often the device wakes to measure voltages and temperatures while in SLEEP mode.

Units in seconds (unsigned), except a setting of 0 results in measurements every 250 ms.

12.4.1.3 Power:Sleep:Wake Comparator Current

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Sleep	Wake Comparator Current	U1	1	10	1	500uV

Description: This parameter sets the Wake Comparator Current threshold (designated as voltage across the sense resistor) in units of 500 µV. This includes a check in both directions and causes the device to exit SLEEP and return to NORMAL mode whenever the absolute value of the current detected exceeds the threshold.

Threshold = 500 µV × (setting)

Note

The minimum setting is 1 (500 µV), meaning 500 mA across 1 mΩ. The maximum setting is 10 (5 mV).

12.4.2 Power:Shutdown

12.4.2.1 Power:Shutdown:Shutdown Cell Voltage

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Shutdown	Shutdown Cell Voltage	I2	0	5500	0x0	mV

Description: Configures the cell voltage threshold at which the device enters SHUTDOWN mode after a 10-second delay. This threshold does not apply to VC pins not configured for use with actual cells.

0 = Cell-Voltage-based shutdown disabled

All other values = Cell voltage shutdown threshold in mV (signed)

12.4.2.2 Power:Shutdown:Shutdown Stack Voltage

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Shutdown	Shutdown Stack Voltage	U2	0	65535	0x0	mV

Description: Configures the stack voltage threshold at which the device enters SHUTDOWN mode after a 10-second delay.

0 = Top-of-Stack-Voltage-based shutdown disabled

All other values = Top-of-stack voltage shutdown threshold in mV (unsigned)

12.4.2.3 Power:Shutdown:Shutdown Temperature

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Shutdown	Shutdown Temperature	U1	0	150	0x0	°C

Description: Configures the internal temperature threshold at which the device shuts down.

0 = Shutdown based on measured internal temperature disabled

All other values = Shutdown Internal Temperature threshold in °C (unsigned)

12.4.2.4 Power:Shutdown:Auto Shutdown Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Shutdown	Auto Shutdown Time	U1	0	255	0x0	Minutes

Description: As a countermeasure to inadvertent wake from SHUTDOWN, the device can be configured to automatically enter SHUTDOWN again after a number of minutes defined by this parameter.

If valid communications occur, or if charge current or discharge current above the SLEEP current threshold is detected before this time expires, automatic shutdown is canceled.

If none of those events occur, after this time expires, the device re-enters SHUTDOWN mode.

0 = Auto-shutdown feature is disabled.

All other values = Auto-shutdown occurs after this many minutes if it is not canceled (unsigned).

12.5 Security

12.5.1 Security:Settings

12.5.1.1 Security:Settings:Security Settings

Class	Subclass	Name	Type	Min	Max	Default	Unit
Security	Settings	Security Settings	H1	0x00	0x07	0x0	Hex

7	6	5	4	3	2	1	0

RSVD0_4	RSVD0_3	RSVD0_2	RSVD0_1	RSVD0_0	SEAL	LOCK_CFG	PERM_SEAL

Description: These bits configure the security settings of the device

Table 12-21. Security Settings Register Field Descriptions

Bit	Field	Default	Description
2	SEAL	0	Setting this bit causes the device to enter SEALED mode when reset (if saved in OTP) or exiting CONFIG_UPDATE mode. In production systems, this bit is generally set for security purposes. 0 = Device does not default to SEALED mode. 1 = Device default state is SEALED.
1	LOCK_CFG	0	Setting this bit prevents entry into CONFIG_UPDATE mode. This prevents further modifications to the device configuration after CONFIG_UPDATE mode is exited. 0 = Configuration parameters can be changed in CONFIG_UPDATE mode. 1 = Configuration parameters cannot be changed, CONFIG_UPDATE mode cannot be entered.
0	PERM_SEAL	0	Setting this bit prevents unsealing the device once it is sealed. If this is not programmed to OTP, this setting is lost on a full reset and the device is again able to unseal. 0 = The device can be unsealed by sending the correct security keys. 1 = The device cannot be unsealed.

12.5.1.2 Security:Settings:Full Access Key Step 1

Class	Subclass	Name	Type	Min	Max	Default	Unit
Security	Settings	Full Access Key Step 1	H2	0x0000	0xFFFF	0x0414	Hex

15	14	13	12	11	10	9	8
FAKEY_15	FAKEY_14	FAKEY_13	FAKEY_12	FAKEY_11	FAKEY_10	FAKEY_9	FAKEY_8
7	6	5	4	3	2	1	0
FAKEY_7	FAKEY_6	FAKEY_5	FAKEY_4	FAKEY_3	FAKEY_2	FAKEY_1	FAKEY_0

Description: -

This is the first word of the security key that must be sent to transition from SEALED to FULLACCESS mode. Do not choose a word identical to a subcommand address

Table 12-22. Full Access Key Step 1 Register Field Descriptions

Bit	Field	Default	Description
15–0	FAKEY_15–FAKEY_0	1044	

12.5.1.3 Security:Settings:Full Access Key Step 2

Class	Subclass	Name	Type	Min	Max	Default	Unit
Security	Settings	Full Access Key Step 2	H2	0x0000	0xFFFF	0x3672	Hex

15	14	13	12	11	10	9	8
FAKEY_15	FAKEY_14	FAKEY_13	FAKEY_12	FAKEY_11	FAKEY_10	FAKEY_9	FAKEY_8
7	6	5	4	3	2	1	0
FAKEY_7	FAKEY_6	FAKEY_5	FAKEY_4	FAKEY_3	FAKEY_2	FAKEY_1	FAKEY_0

Description:

This is the second word of the security key that must be sent to transition from SEALED to FULLACCESS mode. Do no choose a word identical to a subcommand address or the same as the first word.

It must be sent within 5 seconds of the first word of the key and with no other commands in between.

Table 12-23. Full Access Key Step 2 Register Field Descriptions

Bit	Field	Default	Description
15–0	FAKEY_15–FAKEY_0	13938	

12.6 Data Memory Summary

Data Memory Table

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Calibration	Voltage	0x9000	Cell 1 Gain	U2	0	65535	0x0	—
Calibration	Voltage	0x9002	Stack Gain	U2	0	65535	0x0	—
Calibration	Voltage	0x9004	Cell 2 Gain Delta	I1	–128	127	0x0	—
Calibration	Voltage	0x9005	Cell 3 Gain Delta	I1	–128	127	0x0	—
Calibration	Voltage	0x9071	Cell 4 Gain Delta	I1	–128	127	0x0	—
Calibration	Voltage	0x9072	Cell 5 Gain Delta	I1	–128	127	0x0	—
Calibration	Current	0x9006	Curr Gain	U2	0	65535	0x0	—
Calibration	Current	0x9008	Curr Offset	I2	–32768	32767	0x0	—
Calibration	Current	0x900A	CC1 Gain	U2	0	65535	0x0	—
Calibration	Current	0x900C	CC1 Offset	I2	–32768	32767	0x0	—
Calibration	Temperature	0x900E	TS Offset	I2	–32768	32767	0x0	—
Calibration	Temperature	0x9010	Int Temp Gain	U2	0	65535	0x0	—
Calibration	Temperature	0x9012	Int Temp Offset	I2	–32768	32767	0x0	—
Settings	Configuration	0x9014	Power Config	H1	0x00	0xFF	0x01	Hex
Settings	Configuration	0x9015	REGOUT Config	H1	0x00	0xFF	0x08	Hex
Settings	Configuration	0x9016	I2C Address	H1	0x00	0x7F	0x08	Hex
Settings	Configuration	0x9017	I2C Config	H2	0x0000	0xFFFF	0x3400	Hex
Settings	Configuration	0x9019	DA Config	H2	0x0000	0xFFFF	0x0000	Hex
Settings	Configuration	0x901B	Vcell Mode	H1	0x00	0x05	0x0	Hex
Settings	Configuration	0x901C	Default Alarm Mask	H2	0x0000	0xFFFF	0xC200	Hex
Settings	Configuration	0x901E	FET Options	H1	0x00	0xFF	0x18	Hex
Settings	Configuration	0x901F	Charge Detector Time	U1	0	255	1	100ms
Settings	Cell Balancing	0x9020	Balancing Configuration	H1	0x00	0xFF	0x02	Hex
Settings	Cell Balancing	0x9021	Min Temp Threshold	U1	0	255	255	256-LSBs
Settings	Cell Balancing	0x9022	Max Temp Threshold	U1	0	255	0	256 LSBs
Settings	Cell Balancing	0x9023	Max Internal Temp	I1	–128	127	85	°C
Settings	Protection	0x9024	Enabled Protections A	H1	0x00	0xFF	0xA1	Hex
Settings	Protection	0x9025	Enabled Protections B	H1	0x00	0xFF	0x00	Hex
Settings	Protection	0x9026	DSG FET Protections A	H1	0x00	0xFF	0xFF	Hex
Settings	Protection	0x9027	CHG FET Protections A	H1	0x00	0xFF	0xEF	Hex
Settings	Protection	0x9028	Both FET Protections B	H1	0x00	0xFF	0x06	Hex
Settings	Protection	0x9029	Body Diode Threshold	I2	0	32767	64	userA
Settings	Protection	0x902B	Cell Open Wire NORMAL Check Time	U1	0	255	0x0	FULLSCAN intervals
Settings	Protection	0x902C	Cell Open Wire SLEEP Check Time	H1	0x00	0xFF	0x10	Hex
Settings	Protection	0x902D	Host Watchdog Timeout	U1	0	255	0x0	Varying

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Protections	Cell Voltage	0x902E	Cell Undervoltage Protection Threshold	I2	0	5500	2500	mV
Protections	Cell Voltage	0x9030	Cell Undervoltage Protection Delay	U1	0	255	10	ADSCAN intervals
Protections	Cell Voltage	0x9031	Cell Undervoltage Protection Recovery Hysteresis	H1	0x00	0x03	0x02	Hex
Protections	Cell Voltage	0x9032	Cell Overvoltage Protection Threshold	I2	0	5500	4200	mV
Protections	Cell Voltage	0x9034	Cell Overvoltage Protection Delay	U1	0	255	10	ADSCAN intervals
Protections	Cell Voltage	0x9035	Cell Overvoltage Protection Recovery Hysteresis	H1	0x00	0x03	0x02	Hex
Protections	Current	0x9036	Overcurrent in Charge Protection Threshold	U1	2	62	2	2mV
Protections	Current	0x9037	Overcurrent in Charge Protection Delay	U1	0	255	58	Varying
Protections	Current	0x9038	Overcurrent in Discharge 1 Protection Threshold	U1	2	100	4	2mV
Protections	Current	0x9039	Overcurrent in Discharge 1 Protection Delay	U1	0	255	6	—
Protections	Current	0x903A	Overcurrent in Discharge 2 Protection Threshold	U1	2	100	3	2mV
Protections	Current	0x903B	Overcurrent in Discharge 2 Protection Delay	U1	0	255	19	—
Protections	Current	0x903C	Short Circuit in Discharge Protection Threshold	H1	0x00	0xFF	0x0	Varying
Protections	Current	0x903D	Short Circuit in Discharge Protection Delay	H1	0x00	0x0A	0x01	Varying
Protections	Current	0x903E	Latch Limit	H1	0x00	0x07	0x0	Varying
Protections	Current	0x903F	Recovery Time	U1	0	255	5	Seconds
Protections	Temperature	0x9040	Overtemperature in Charge Protection Threshold	U1	0	255	55	54-LSBs
Protections	Temperature	0x9041	Overtemperature in Charge Protection Delay	U1	0	255	15	Measurements
Protections	Temperature	0x9042	Overtemperature in Charge Protection Recovery	U1	0	255	63	54-LSBs
Protections	Temperature	0x9043	Undertemperature in Charge Protection Threshold	U1	0	255	147	77-LSBs
Protections	Temperature	0x9044	Undertemperature in Charge Protection Delay	U1	0	255	15	Measurements
Protections	Temperature	0x9045	Undertemperature in Charge Protection Recovery	U1	0	255	134	77-LSBs
Protections	Temperature	0x9046	Overtemperature in Discharge Protection Threshold	U1	0	255	48	54-LSBs
Protections	Temperature	0x9047	Overtemperature in Discharge Protection Delay	U1	0	255	15	Measurements
Protections	Temperature	0x9048	Overtemperature in Discharge Protection Recovery	U1	0	255	55	54-LSBs
Protections	Temperature	0x9049	Undertemperature in Discharge Protection Threshold	U1	0	255	147	77-LSBs
Protections	Temperature	0x904A	Undertemperature in Discharge Protection Delay	U1	0	255	15	Measurements
Protections	Temperature	0x904B	Undertemperature in Discharge Protection Recovery	U1	0	255	134	77-LSBs
Protections	Temperature	0x904C	Internal Overtemperature Protection Threshold	U1	25	150	105	°C
Protections	Temperature	0x904D	Internal Overtemperature Protection Delay	U1	0	255	15	Measurements
Protections	Temperature	0x904E	Internal Overtemperature Protection Recovery	U1	25	150	100	°C

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Power	Sleep	0x904F	Sleep Current	I2	0	32767	64	userA
Power	Sleep	0x9051	Voltage Time	U1	0	255	5	Seconds
Power	Sleep	0x9052	Wake Comparator Current	U1	1	10	1	500uV
Power	Shutdown	0x9053	Shutdown Cell Voltage	I2	0	5500	0x0	mV
Power	Shutdown	0x9055	Shutdown Stack Voltage	U2	0	65535	0x0	mV
Power	Shutdown	0x9057	Shutdown Temperature	U1	0	150	0x0	°C
Power	Shutdown	0x9058	Auto Shutdown Time	U1	0	255	0x0	Minutes
Security	Settings	0x9059	Security Settings	H1	0x00	0x07	0x0	Hex
Security	Settings	0x905A	Full Access Key Step 1	H2	0x0000	0xFFFF	0x0414	Hex
Security	Settings	0x905C	Full Access Key Step 2	H2	0x0000	0xFFFF	0x3672	Hex

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2023	*	Initial Release

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