User's Guide

TPS546D24S 2-Phase SWIFT™ Step-Down Converter Evaluation Module User's Guide

ABSTRACT

The TPS546D24SEVM-2PH evaluation module (EVM) is a two-phase buck converter with two TPS546D24S devices. The TPS546D24S device is a stackable synchronous buck with PMBus® interface that can operate from a nominal 2.95-V to 16-V supply. The device allows programming and monitoring through the PMBus interface.

Two TPS546D24S devices are configured as a two-phase buck converter in factory default. Output current is evenly distributed in the two devices; both the negative and positive output terminals are connected together.

Table of Contents

List of Figures

List of Tables

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1 Description

The TPS546D24SEVM-2PH is a two-phase buck design using two stacked TPS546D24S devices. The TPS546D24SEVM-2PH is designed for a nominal 12-V bus and to produce a regulated 0.8-V output at up to 80 A of load current. The TPS546D24SEVM-2PH is designed to demonstrate stacking operation of the TPS546D24S in a two-phase, low-output voltage application while providing a number of test points to evaluate the performance of the devices. The TPS546D24SEVM-2PH can be modified to single-phase buck converters by changing the components assembled. See *Tip and Barrel Measurement* for more information on single-phase configuration.

1.1 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TPS546D24SEVM-2PH. Observe all safety precautions.

⚠	**Warning**	The TPS546D24SEVM-2PH circuit module may become hot during operation due to dissipation of heat. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.
⚠	**Caution**	Do not leave the EVM powered when unattended.

WARNING

The circuit module has signal traces, components, and component leads on the bottom of the board. This may result in exposed voltages, hot surfaces, or sharp edges. Do not reach under the board during operation.

CAUTION

The circuit module may be damaged by over temperature. To avoid damage, monitor the temperature during evaluation and provide cooling, as needed, for your system environment.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than 1 power supply, check your equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to your equipment.

CAUTION

The communication interface is not isolated on the EVM. Be sure no ground potential exists between the computer and the EVM. Also be aware that the computer is referenced to the battery- potential of the EVM.

1.2 Typical Applications

The TPS546D24S device is designed for the following applications:

- High-density power solutions
- Wireless infrastructure
- Switcher
- Router network
- Server
- Storage
- Smart power systems

1.3 Features

This EVM has the following features:

- Regulated 0.8-V output up to 80-A_{DC} steady-state output current
- The output voltage is marginable and trimmable using the PMBus interface
  - Programmable UVLO, soft start, and enable through the PMBus interface
  - Programmable overcurrent warning and fault limits and programmable response to faults via the PMBus interface
  - Programmable overvoltage and undervoltage warning and fault limits and programmable response to faults via the PMBus interface
  - Programmable turn-on and turn-off delays
- Convenient test points for probing critical waveforms

2 Electrical Performance Specifications

Table 2-1 lists the electrical performance specifications in room temperature (20 to 25°C). Characteristics are given for an input voltage of VIN = 12 V, unless otherwise specified.

Table 2-1. TPS546D24SEVM-2PH Electrical Performance Specifications

Parameter	Test Conditions	MIN	TYP	MAX	Unit
Input Characteristics					
Input voltage range, V_{IN}		5	12	16	V
Full load input current	I_{OUT} = 80 A		6.4		A
Full load input current	V_{IN} = 5 V, I_{OUT} = 80 A		15.6		A
No load input current	I_{OUT} = 0 A, switching enabled		130		mA
Enable switching threshold	Set by default resistor divider, JP2_P1 and JP2_P2 pins 3 and 4 shorted		5.26		V
Disable switching threshold	Set by default resistor divider, JP2_P1 and JP2_P2 pins 3 and 4 shorted		4.75		V
Output Characteristics					
Output voltage, V_{OUT}			0.8		V
Output load current, I_{OUT}		0		80	A
Output voltage regulation	Line Regulation: V_{IN} = 5 V to 16 V		0.1%		
	Load Regulation: I_{OUT} = 0 A to 80 A		0.1%		
Output voltage ripple	I_{OUT} = 80 A		5		mVpp
Output voltage undershoot	I_{OUT} = 20-A to 60-A step at 1 A/µs		70		mV
Output voltage overshoot	I_{OUT} = 60-A to 20-A step at 100 A/µs		70		mV
Output overcurrent fault threshold	Phase current limit setting of U1_P1 programmed by MSEL2		52		A
	Phase current limit setting of U1_P2 programmed by MSEL2		52		A
Systems Characteristics					
Switching frequency	Programmed by MSEL1		550		kHz
Full load efficiency, V_{OUT} (1)	I_{OUT} = 80 A		84.8%		
Operating case temperature	I_{OUT} = 80 A, 10 minute soak		80		°C
Loop bandwidth	I_{OUT} = 40 A		30.3		kHz
Phase margin			93.5		°
PMBus Interface and Pin-Strapping					
U1_P1 PMBus address	Programmed by NVM and ADRSEL		36		Decimal
U1_P1 Voltage reference	Default setting of VOUT_COMMAND programmed by VSEL		800		mV
U1_P1 Soft-start time (TON_RISE)	Default setting of TON_RISE programmed by MSEL2		3		ms

(1) The efficiency is measured using the test points listed in Table 6-2 to minimize the effect of DC drops caused by onboard copper traces.

3 Schematic

Figure 3-1 through Figure 3-3 illustrate the TPS546D24SEVM-2PH schematics.

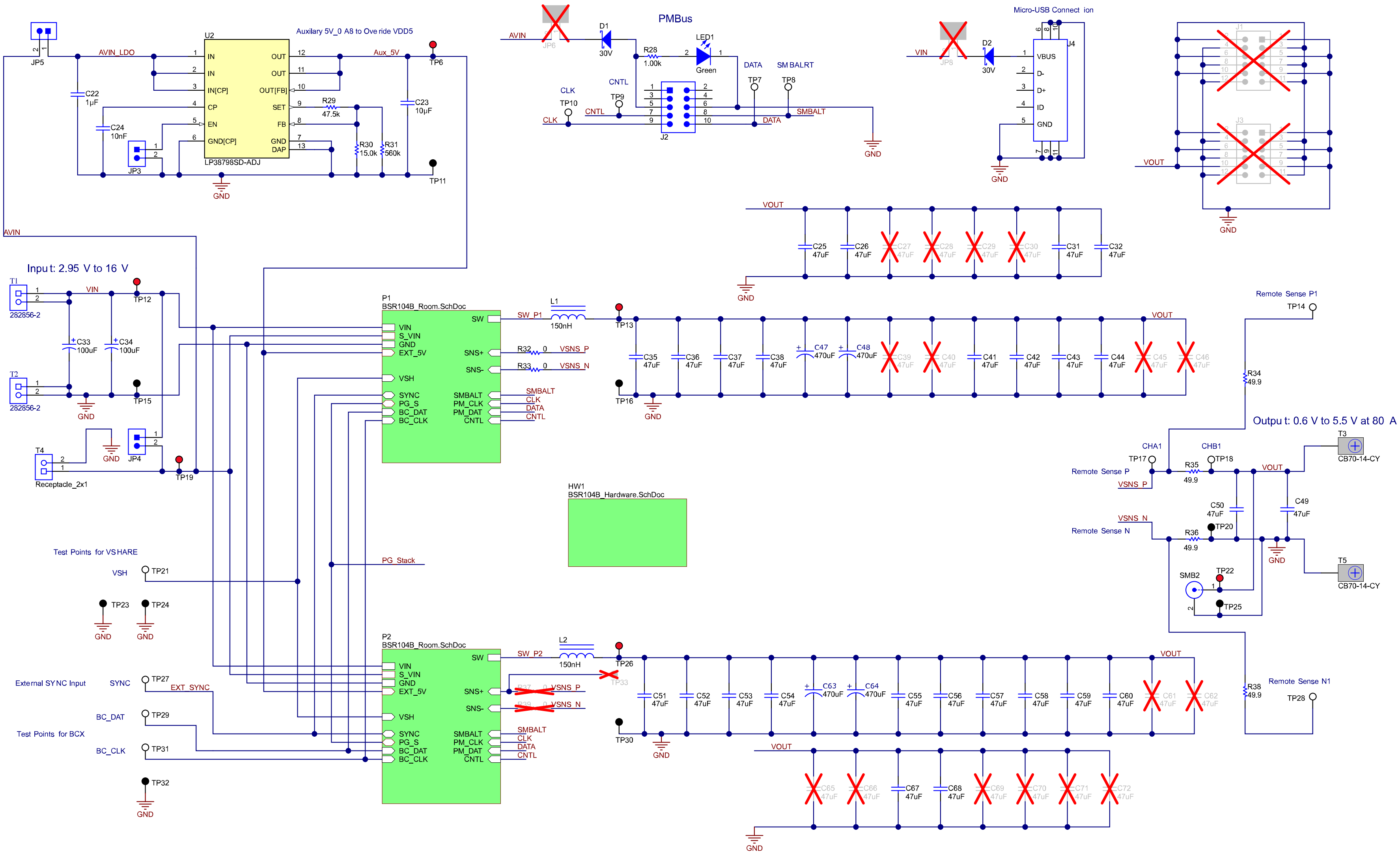
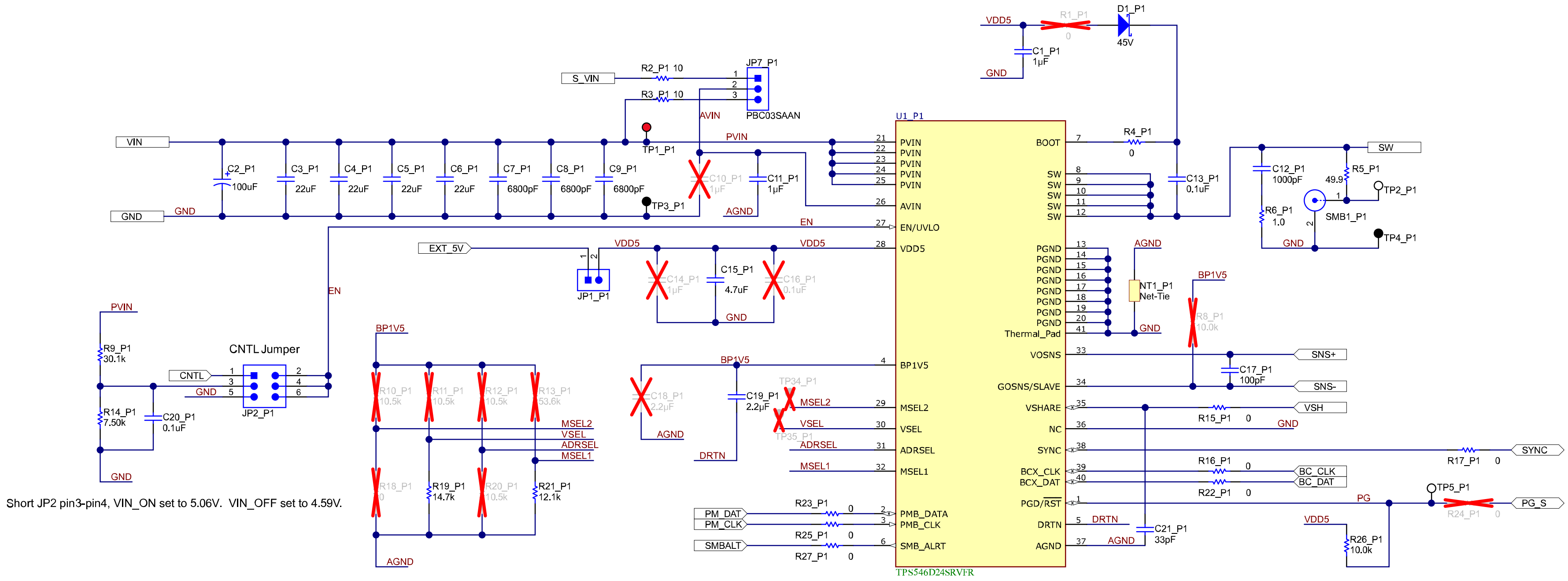


Figure 3-1. TPS546D24SEVM-2PH Schematic Page 1



Short JP2 pin3-pin4, VIN_ON set to 5.06V. VIN_OFF set to 4.59V.

Figure 3-2. TPS546D24SEVM-2PH Schematic Page 2 (U1_P1 Controller)

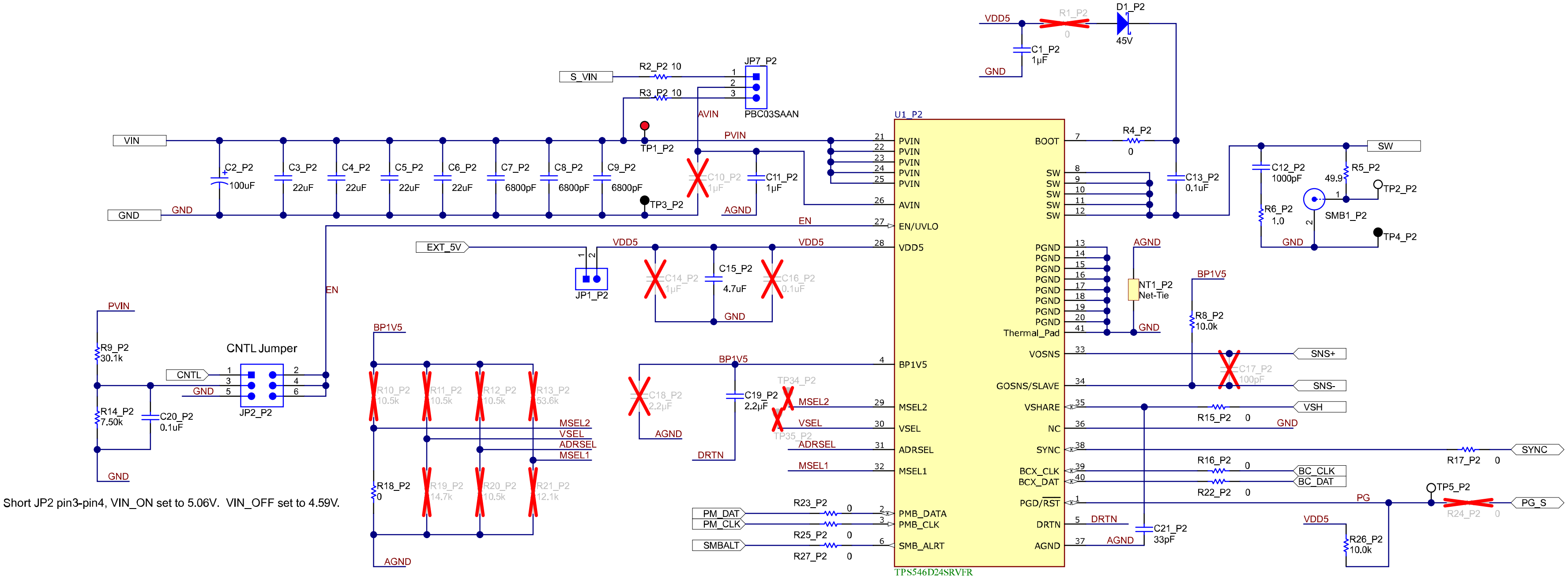


Figure 3-3. TPS546D24SEVM-2PH Schematic Page 3 (U1_P2 Follower)

4 Test Setup

4.1 Test and Configuration Software

To change any of the default configuration parameters on the EVM through PMBus, obtain the *TI Fusion Digital Power Designer* software.

4.1.1 Description

The *TI Fusion Digital Power Designer* is the graphical user interface (GUI) used to configure and monitor the Texas Instruments TPS546D24S power converter installed on this evaluation module. The application uses the PMBus protocol to communicate with the controller over serial bus by way of a TI USB adapter described in Section 4.2.6.

4.1.2 Features

Some of the tasks you can perform with the GUI include:

- Turn on or off the power supply output, either through the hardware control line or the PMBus operation command.
- Monitor real-time data. Items such as input voltage, output voltage, output current, die temperature, and warnings and faults that are continuously monitored and displayed by the GUI.
- Configure common operating characteristics such as V_{OUT} trim and margin, UVLO, soft-start time, warning and fault thresholds, fault response, and on and off modes.

4.2 Test Equipment

4.2.1 Voltage Source

The input voltage source V_{IN} must be a 0-V to 20-V variable DC source capable of supplying a minimum of 16 ADC to support 80-A load with 5-V input. Connect input VIN and GND to T1 and T2. If the output voltage of the EVM is increased, the power supply can need to be capable of supplying more current.

4.2.2 Multimeters

TI recommends using two separate multimeters: one meter to measure V_{IN} and the other to measure V_{OUT}.

4.2.3 Output Load:

TI recommends a variable electronic load for the test setup. To test the full load current this EVM supports, the load must be capable of sinking at least 80 A.

4.2.4 Oscilloscope

When using an oscilloscope to measure the switching node voltage or voltage ripple, measure using a *Tip-and-Barrel* method as Figure 4-1 shows, or better.

4.2.5 Fan:

During prolonged operation at high loads, it can be necessary to provide forced air cooling with a small fan aimed at the EVM. Maintain the surface temperature of the devices on the EVM below their rated temperature.

4.2.6 USB-to-GPIO Interface Adapter:

A communications adapter is required between the EVM and the host computer. This EVM is designed to use TI's USB-to-GPIO or USB-to-GPIO2 Adapter. Purchase this adapter at http://www.ti.com/tool/usb-to-gpio2.

4.2.7 Recommended Wire Gauge

- Input VIN and GND to T1 and T2 (GND) (12-V input) – The recommended wire size is AWG #12, with the total length of wire less than 2 feet (1 foot input, 1 foot return).
- Output T3 and GND T5 (0.8-V output) – The minimum recommended wire size is AWG #10, with the total length of wire less than 2 feet (1 foot output, 1 foot return). A thicker wire gauge can be required to minimize the voltage drop the wires.

4.3 Tip and Barrel Measurement

Figure 4-1 illustrates the tip and barrel measurement for switching node waveform on TP2_P1 with TP4_P1 or TP2_P2 with TP4_P2.

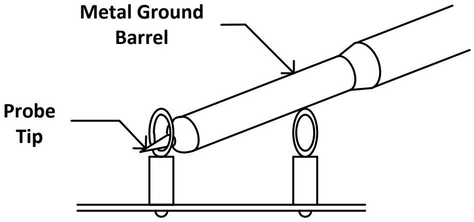


Figure 4-1. Tip and Barrel Measurement

4.4 List of Test Points, Jumpers, and Connectors

Table 4-1 lists the test point functions.

Table 4-1. Test Point Functions

Test Point	Type	Name	Description
TP1_P1	T-H Loop	PVIN_P1	PVIN pin voltage of U1_P1 device measurement point
TP1_P2	T-H Loop	PVIN_P2	PVIN pin voltage of U1_P2 device measurement point
TP2_P1	T-H Loop	SW_P1	Switching node of output rail phase 1 measurement point, reference to TP4_P1
TP2_P2	T-H Loop	SW_P2	Switching node of output rail phase 2 measurement point, reference to TP4_P2
TP3_P1	T-H Loop	GND_P1	GND pin voltage of U1_P1 device measurement point
TP3_P2	T-H Loop	GND_P2	GND pin voltage of U1_P2 device measurement point
TP4_P1	T-H Loop	GND_P1	GND reference for switch node measurement of U1_P1
TP4_P2	T-H Loop	GND_P2	GND reference for switch node measurement of U1_P2
TP5_P1	T-H Loop	PG_S_P1	PGOOD signal of phase 1
TP5_P2	T-H Loop	PG_S_P2	PGOOD signal of phase 2
TP6	T-H Loop	AUX_5V	External 5-V measurement point for VDD5
TP7	T-H Loop	DATA	DATA signal on J2 header
TP8	T-H Loop	SMBALRT	SMBALERT signal on J2 header
TP9	T-H Loop	CNTL	CNTL signal on J2 header
TP10	T-H Loop	CLK	CLK signal on J2 header
TP11	T-H Loop	GND	GND reference
TP12	T-H Loop	PVIN	VIN+ measurement point
TP13	T-H Loop	VOUT_P1	U1_P1 output voltage measurement point for efficiency, reference to TP16
TP14	T-H Loop	Remote SNS+	OUTPUT remote sense + voltage point
TP15	T-H Loop	GND	VIN- measurement point
TP16	T-H Loop	GND_P1	U1_P1 output voltage referencing GND for efficiency measurement
TP17	T-H Loop	CH_A	OUTPUT for small signal loop gain measurements (B/A setup)
TP18	T-H Loop	CH_B	INPUT for small signal loop gain measurements (B/A setup)
TP19	T-H Loop	Ext_AVIN	AVIN measurement point
TP20	T-H Loop	GND	GND reference
TP21	T-H Loop	VSHARE	VSHARE measurement point. Sensitive signal.
TP22	T-H Loop	VOUT	VOUT + measurement point
TP23	T-H Loop	GND	GND reference
TP24	T-H Loop	GND	GND reference
TP25	T-H Loop	GND	VOUT - measurement point
TP26	T-H Loop	VOUT_P2	U1_P2 output voltage measurement point for efficiency, reference to TP30
TP27	T-H Loop	SYNC	Synchronization connection between U1_P1 and U1_P2. External SYNC input.

Table 4-1. Test Point Functions (continued)

Test Point	Type	Name	Description
TP28	T-H Loop	Remote SNS-	OUTPUT remote sense - voltage point
TP29	T-H Loop	BC_DAT	Data for back-channel communications between stacked devices
TP30	T-H Loop	GND_P2	U1_P2 output voltage referencing GND for efficiency measurement
TP31	T-H Loop	BC_CLK	Clock for back-channel communications between stacked devices
TP32	T-H Loop	GND	GND reference
TP33	T-H Loop	VOSNS_P2	VOSNS measurement point for U1_P2
TP34_P1, TP34_P2	T-H Loop	MSEL2_P1, MSEL2_P2	MSEL2 measurement point for U1_P1 and U1_P2
TP35_P1, TP35_P2	T-H Loop	VSEL_P1, VSEL_P2	VSEL measurement point for U1_P1 and U1_P2

Table 4-2 lists the EVM jumpers.

Table 4-2. Jumpers

Jumper	Type	Name	Description
JP1_P1, JP1_P2	Header, 100 mil, 2 × 1	EXT_5.1V_P1, EXT_5.1V_P2	Short to connect VDD5 of U1_P1 or U1_P2 to the 5.1 V from U2
JP2_P1, JP2_P2	Header, 100 mil, 3 × 2	CNTL_SEL1, CNTL_SEL2	U1_P1 and U1_P2 EN/UVLO pin selections
JP3	Header, 100 mil, 2 × 1	EN to GND	Short to disable the auxiliary 5 V
JP4	Header, 100 mil, 2 × 1	AVIN-PVIN	Short to connect to connect AVIN input to PVIN
JP5	Header, 100 mil, 2 × 1	AVIN-LDO	Short to connect to connect AVIN input to U2 input
JP6	Header, 100 mil, 2 × 1	PMBus3.3V-AVIN	Short to connect USB-to-GPIO 3.3V to AVIN
JP7_P1, JP7_P2	Header, 100 mil, 3 × 1	AVIN-U1_P1, AVIN-U1_P2	U1_P1 and U1_P2 AVIN input source selections
JP8	Header, 100 mil, 2 × 1	Micro_USB-PVIN	Short to connect PVIN to Micro USB connector

Table 4-3 lists the options for the EN/UVLO pin selections on JP2_P1 and JP2_P2.

Table 4-3. JP2_P1 and JP2_P2 Selections

Shunt Position	Selection
pin 1 to 2 shorted	PMBus adaptor control signal
pin 3 to 4 shorted	Resistor divider to PVIN
pin 5 to 6 shorted	EN/UVLO short to ground

Table 4-4 lists the options for the EN/UVLO pin selections on JP2_P1 and JP2_P2.

Table 4-4. JP7_P1 and JP7_P2 Selections

Shunt Position	Selection
pin 1 to 2 shorted	AVIN pin connected to AVIN input through 10-Ω resistor. Use this selection when testing with a split rail input.
pin 2 to 3 shorted	AVIN pin connected to PVIN through 10-Ω resistor

Table 4-5 lists the EVM connector functions.

Table 4-5. Connector Functions

Connector	Type	Name	Description
J1	Header, 100 mil, 6 × 2	N/A	Do not use
J2	Header, 100 mil, 5 × 2	PMBus connector	PMBus socket for TI FUSION adaptor
J3	Header, 100 mil, 6 × 2	N/A	Do not use
J4	Micro USB	Micro USB	Micro USB connector to power EVM from a 5 V USB source

Table 4-5. Connector Functions (continued)

Connector	Type	Name	Description
T1	Terminal block, 2 × 1	PVIN	VIN+ connector
T2	Terminal block, 2 × 1	GND	VIN– connector
T3	Terminal 90A Lug	VOUT	VOUT+ connector
T4	Terminal block, 2 × 1	Ext_AVIN	External AVIN connector
T5	Terminal 90A Lug	GND	VOUT– connector

4.5 Evaluating Single Phase Operation

The default configuration of the EVM is for 2-phase operation. For a single-phase operation, modify the EVM as follows:

1. Short MSEL2 of U1_P1 to GND to program single-phase operation by populating R18_P1 with a 0-Ω resistor.
2. If U1_P2 is left populated, disconnect VSHARE of U1_P2 (Follower) device from U1_P1 (Controller) by depopulating R15_P1 (this is a 0-Ω resistor and can be used for MSEL2 pin of U1_P1 in the previous step).
3. If U1_P2 is left populated, disable U1_P2 by moving the JP2_P2 jumper to position 5-6 (GND).

Note

This modification leaves the AVIN (pin 26) of U1_P2 powered, if no-load leakage current or light-light efficiency measurement is important, the U1_P2 AVIN pin must also be disconnected from the input supply. Disconnect U1_P2 (Follower) AVIN from V_{IN} by removing the jumper from JP7_P2.

4.6 Evaluating Split Rail Input

The default configuration of the EVM is for single rail input. Split rail input enables operation with 3.3V PVIN. For split rail operation configure the jumpers on the EVM as follows:

1. Open JP4 to disconnect AVIN from PVIN.
2. Move the jumper JP7_P1 and JP7_P2 to position 1-2 to disconnect the AVIN pin from the PVIN pins.
3. Apply the AVIN input to T4. 4-V or greater AVIN is required to bring the VDD5 voltage high enough to enable conversion.
4. If operation with 3.3-V PVIN is needed and the CNTL Jumpers (JP2_P1 and JP2_P2) are in position 3-4, the resistor divider at the EN/UVLO must be changed. Alternately move the CNTL Jumpers to position 1-2 and use the control signal to enable conversion or use the ON_OFF_CONFIG and OPERATION commands to enable conversion.

4.7 Configuring EVM to Overdrive VDD5

The EVM has an external LDO (U2) that can be used to overdrive VDD5. The output of this LDO is set for 5.1 V by default. This LDO is useful to minimize the power dissipation in the TPS546D24S IC when using a single rail input. Overdriving VDD5 moves the loss from the internal LDO of the TPS546D24S to the external LDO (U2). To use this LDO, configure the jumpers on the EVM as follows:

1. Short JP4 and JP5 to connect the input of the LDO to the input supply.
2. Open JP3 to enable the LDO.
3. Short JP1_P1 and JP1_P2 to connect the LDO output to the VDD5 pin.
4. Ensure the VDD5 output of the TPS546D24S is set below the external LDO output voltage.

5 EVM Configuration Using the Fusion GUI

The TPS546D24S IC leaves the factory pre-configured. The factory default settings for the parameters can be found in the datasheet. If configuring the EVM to settings other than the factory defaults, use the software described in *Test and Configuration Software*. Make sure to have the input voltage applied to the EVM prior to launching the software so that the TPS546D24S can respond to the GUI and the GUI can recognize the device. The default configuration for the EVM to stop converting is set by the EN/UVLO resistor divider to a nominal input voltage of 4.75 V; therefore if necessary to avoid any converter activity during configuration, an input voltage less than 4.75 V must be applied. TI recommends an input voltage of 3.3 V.

5.1 Configuration Procedure

1. Adjust the input supply to provide 3.3 VDC, current limited to 1 A.
2. Apply the input voltage to the EVM. See Section 4.2 for connections and test setup.
3. Launch the Fusion GUI software. See the screen shots in Section 10 for more information.
4. Configure the EVM operating parameters as desired.

By default the pinstrap resistors configure U1_P1 as the stack controller and U1_P2 as the stack follower.

6 Test Procedure

6.1 Line and Load Regulation and Efficiency Measurement Procedure

1. Set up the EVM as Section 4.2 and Section 6.2 describe.
2. Set the electronic load to draw 0 A_{DC}.
3. Increase V_{IN} from 0 V to 12 V using voltage meter to measure input voltage.
4. Use the other voltage meter to measure output voltage V_{OUT}.
5. Vary the load from 0 to 80 A_{DC}. V_{OUT} must remain in regulation as defined in Table 2-1.
6. Vary V_{IN} from 5 V to 16 V. V_{OUT} must remain in regulation as defined in Table 2-1.
7. Decrease the load to 0 A.
8. Decrease V_{IN} to 0 V.

6.2 Efficiency Measurement Test Points

To evaluate the efficiency of the power train (device and inductor), make sure to measure the voltages at the correct location. This action is necessary because otherwise the measurements include losses that are not related to the power train itself. Losses incurred by the voltage drop in the copper traces and in the input and output connectors are not related to the efficiency of the power train, which must not be included in efficiency measurements.

Input current can be measured at any point in the input wires, and output current can be measured anywhere in the output wires of the output being measured.

Table 6-1 shows the measurement points for input voltage and output voltage. VIN and VOUT are measured to calculate the efficiency. Using these measurement points results in efficiency measurements that excluded losses due to the wires and connectors.

Table 6-1. Test Points for Efficiency Measurements

Test Point	Node Name	Description	Comment
TP12	PVIN	Input voltage measurement point for VIN+	The pair of test points are connected to the PVIN/PGND pins of U1_P1. The voltage drop between input terminal to the device pins is included for efficiency measurement.
TP15	PGND	Input voltage measurement point for VIN– (GND)	
TP22	VOUT	Output voltage measurement point for VOUT+	The pair of test points are connected near the output terminals. The voltage drop from the output point of the inductor to the output terminals is included for efficiency measurement.
TP25	GND	Output voltage measurement point for VOUT– (GND)	

For more accurate efficiency measurements of the power train, remove the voltage drop between the power train and the terminals from the measurement. Using the test points in Table 6-2 reduces these losses. To average the voltages at each test point so that only one meter is needed for PVIN and VOUT, add some resistance between the each test point and the meter. For the measurements taken in this user's guide, a 1.5-kΩ resistor was added in series with each test point. Using these test points reduced the measured power loss at 80 A load by approximately 0.5 W. This power is lost in the copper traces of the PCB.

Table 6-2. Test Points for Better Efficiency Measurements

Test Point	Node Name	Description	Comment
TP1_P1	PVIN_P1	Input voltage measurement point for VIN+	This pair of test points are connected to PVIN and PGND near the pins of U1_P1
TP4_P1	GND_P1	Input voltage measurement point for VIN– (PGND)	
TP1_P2	PVIN_P2	Input voltage measurement point for VIN+	This pair of test points are connected to PVIN and PGND near the pins of U1_P2
TP4_P2	GND_P2	Input voltage measurement point for VIN– (PGND)	
TP13	VOUT_P1	Output voltage measurement point for VOUT+	This pair of test points are connected to VOUT and GND near the output inductor for U1_P1
TP16	GND_P1	Output voltage measurement point for VOUT– (GND)	
TP26	VOUT_P2	Output voltage measurement point for VOUT+	This pair of test points are connected to VOUT and GND near the output inductor for U1_P2
TP30	GND_P2	Output voltage measurement point for VOUT– (GND)	

6.3 Control Loop Gain and Phase Measurement Procedure

The TPS546D24SEVM-2PH includes a 49.9-Ω series resistor in the feedback loop for V_{OUT}. The resistor is accessible at the test points TP17 and TP18 for loop response analysis. These test points must be used during loop response measurements as the perturbation injecting points for the loop . See the description in Table 6-3.

Table 6-3. List of Test Points for Loop Response Measurements

Test Point	Node Name	Description	Comment
TP18	CH_B	Input to feedback divider of V_{OUT}	The amplitude of the perturbation at this node must be limited to less than 30 mV
TP17	CH_A	Resulting output of V_{OUT}	Bode can be measured by a network analyzer with a CH_B/CH_A configuration

Measure the loop response with the following procedure:

1. Set up the EVM as described in Section 4.2.
2. For V_{OUT}, connect the isolation transformer of the network analyzer from TP18 to TP17.
3. Connect the input signal measurement probe to TP18. Connect the output signal measurement probe to TP17.
4. Connect the ground leads of both probe channels to TP20.
5. On the network analyzer, measure the Bode as TP18/TP17 (In/Out).

7 Performance Data and Typical Characteristic Curves

Figure 7-1 through Figure 7-4 present typical performance curves for the TPS546D24SEVM-2PH. The input voltage is 12 V and the oscilloscope measurements use 20 MHz bandwidth limiting unless otherwise noted.

7.1 Efficiency

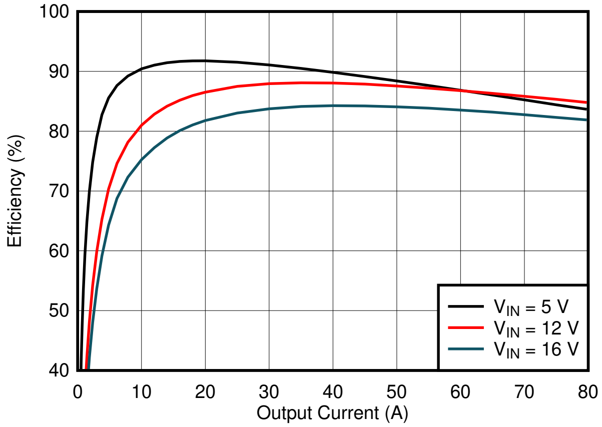


Figure 7-1. Efficiency, V_{OUT} Measured Using TP13, TP16, TP26 and TP30

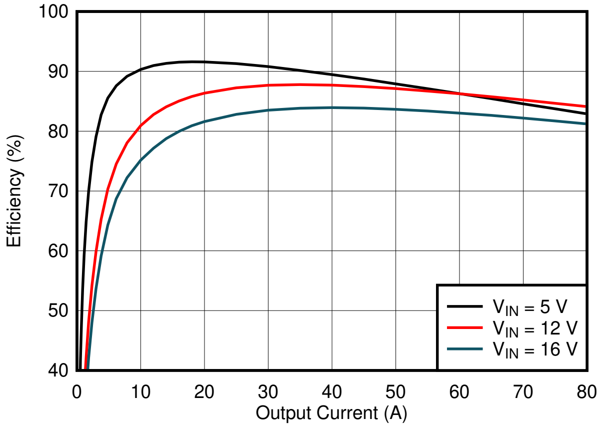


Figure 7-2. Efficiency, V_{OUT} Measured Using TP22 and TP25

7.2 Load and Line Regulation (Measured Between TP22 and TP25)

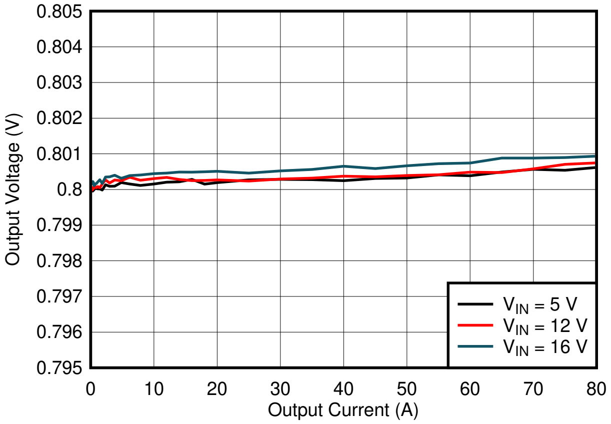


Figure 7-3. Load Regulation

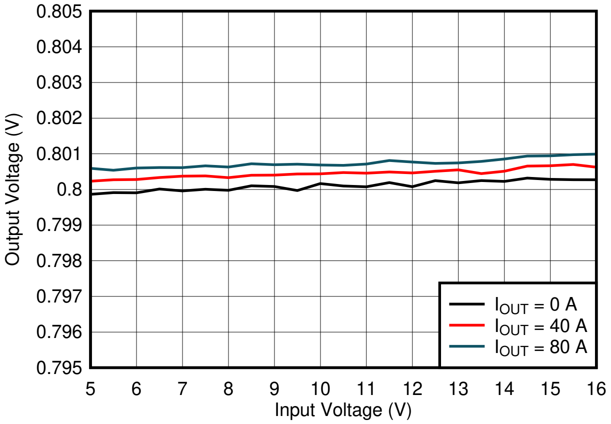
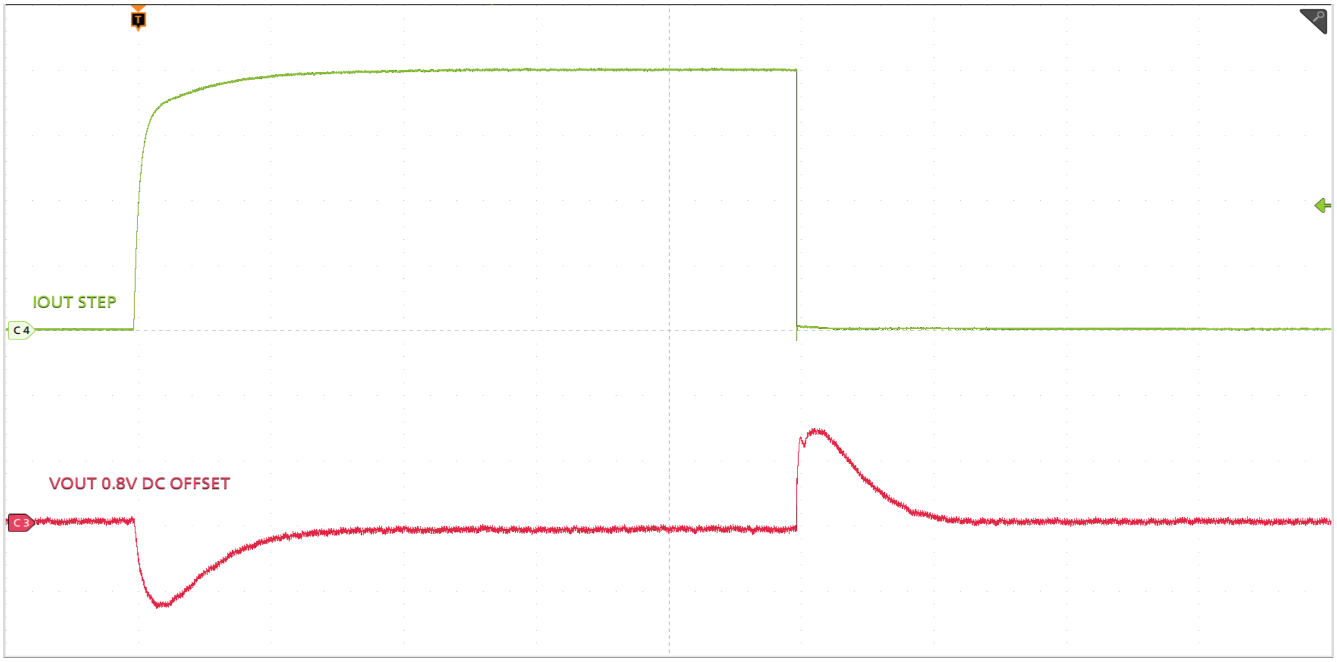


Figure 7-4. Line Regulation

7.3 Transient Response

Figure 7-5 shows the transient response waveform with a 20-A to 60-A transient at 1 A/μs



Timescale = 100 μs/div, CH4 = I_{OUT} STEP at 10 A/div, CH3 = V_{OUT} at 50 mV/division

Figure 7-5. Transient Response

7.4 Control Loop Bode Plot

Figure 7-6 is the control loop bode plot.

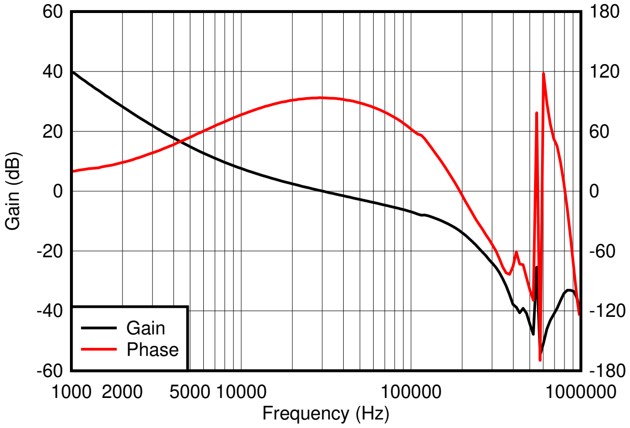
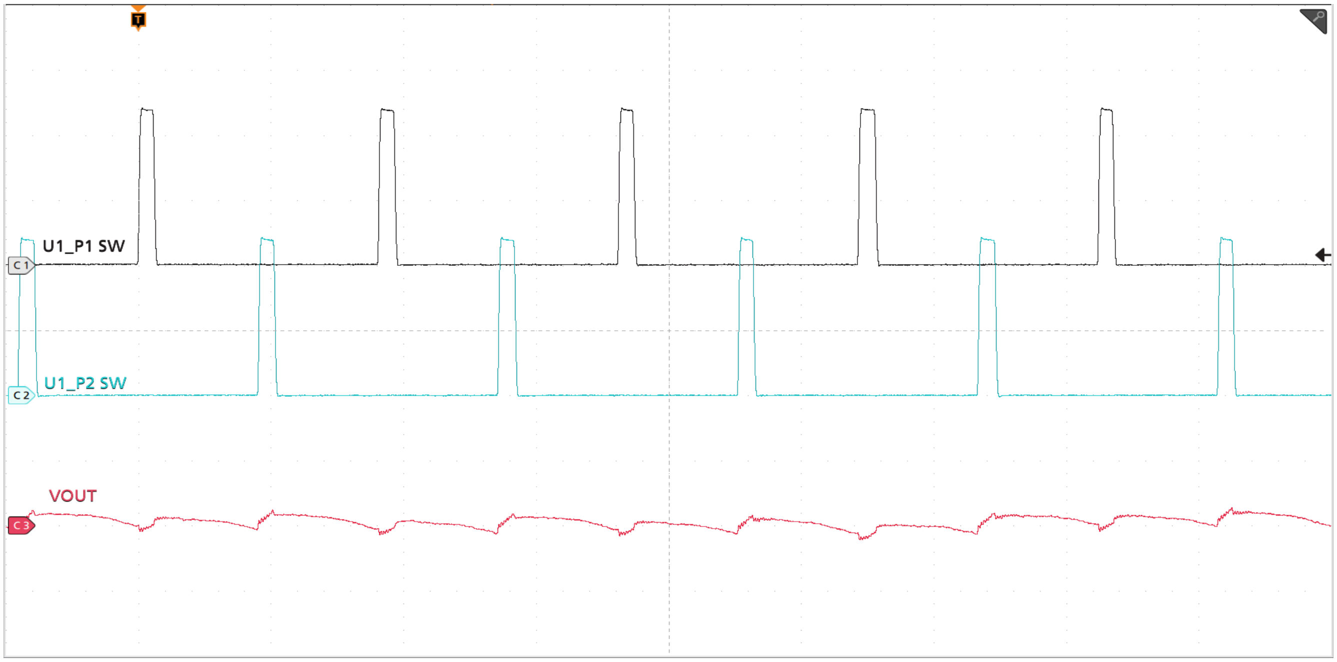


Figure 7-6. Bode Plot at 0.8-V Output at 12 V_{IN}, 20-A Load

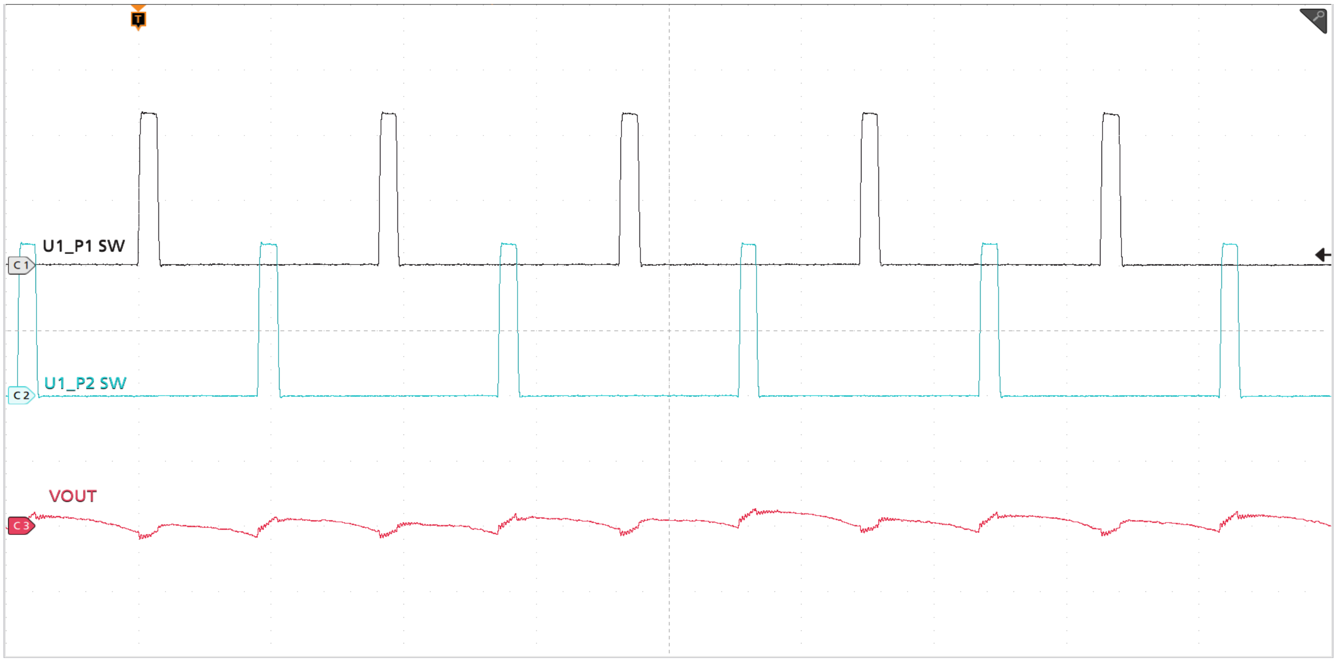
7.5 Output Ripple

Figure 7-7 and Figure 7-8 show the output ripple waveforms at 0-A and 80-A load.



Timescale = 1 μs/div, CH1 = SW1 at 5 V/div, CH2 = SW2 at 5 V/div, CH3 = V_{OUT} at 10 mV/div

Figure 7-7. Output Ripple With 0-A Load

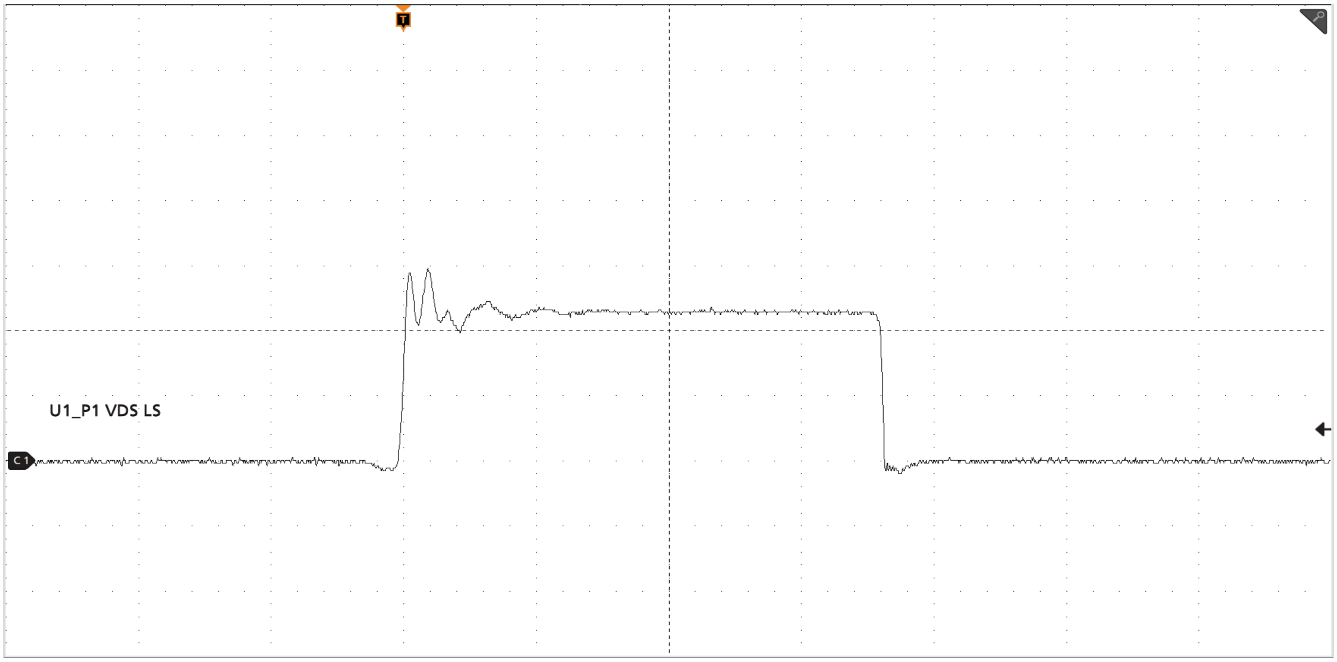


Timescale = 1 μs/div, CH1 = SW1 at 5 V/div, CH2 = SW2 at 5 V/div, CH3 = V_{OUT} at 10 mV/div

Figure 7-8. Output Ripple With 80-A Load

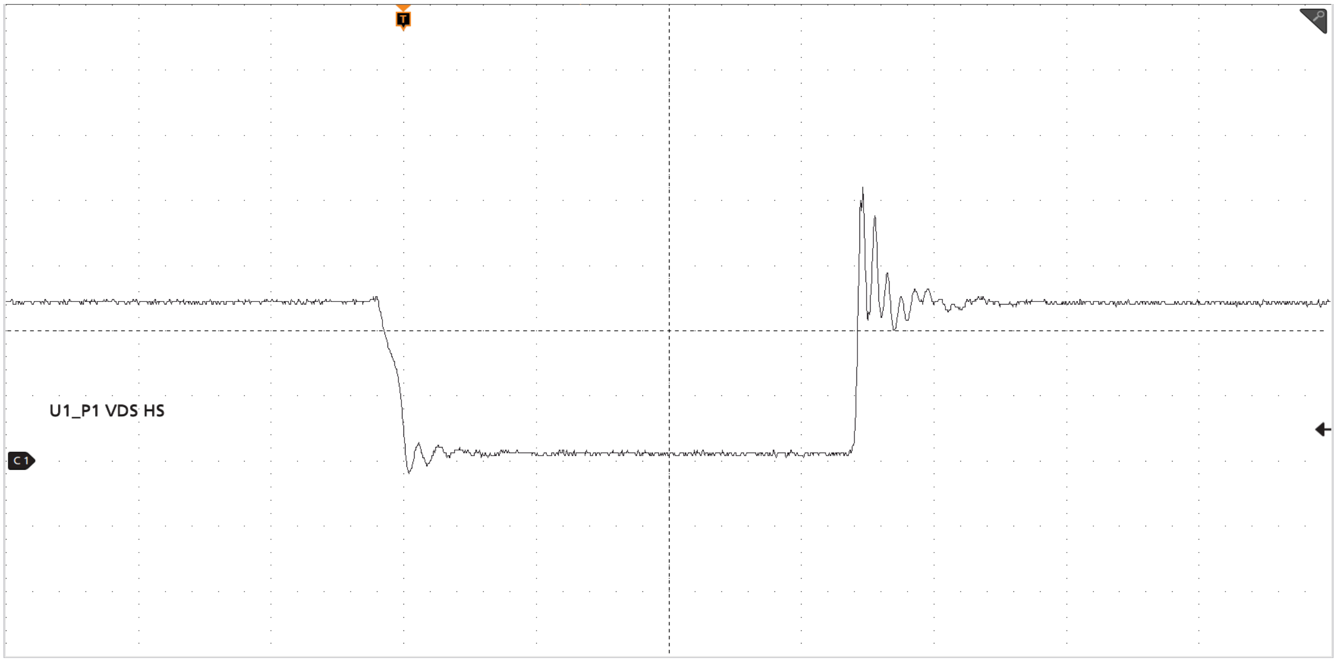
7.6 Power MOSFET Drain-Source Voltage

Figure 7-9 and Figure 7-10 show the low-side and high-side MOSFET drain-source voltage (V_{DS}) at 80-A load. The voltage is measured with 1-GHz bandwidth and at the solder mask openings near the U1_P1 IC using a 1-GHz differential probe.



Timescale = 40 ns/div, CH1 = Low-side V_{DS} at 5 V/div

Figure 7-9. Low-side MOSFET V_{DS}

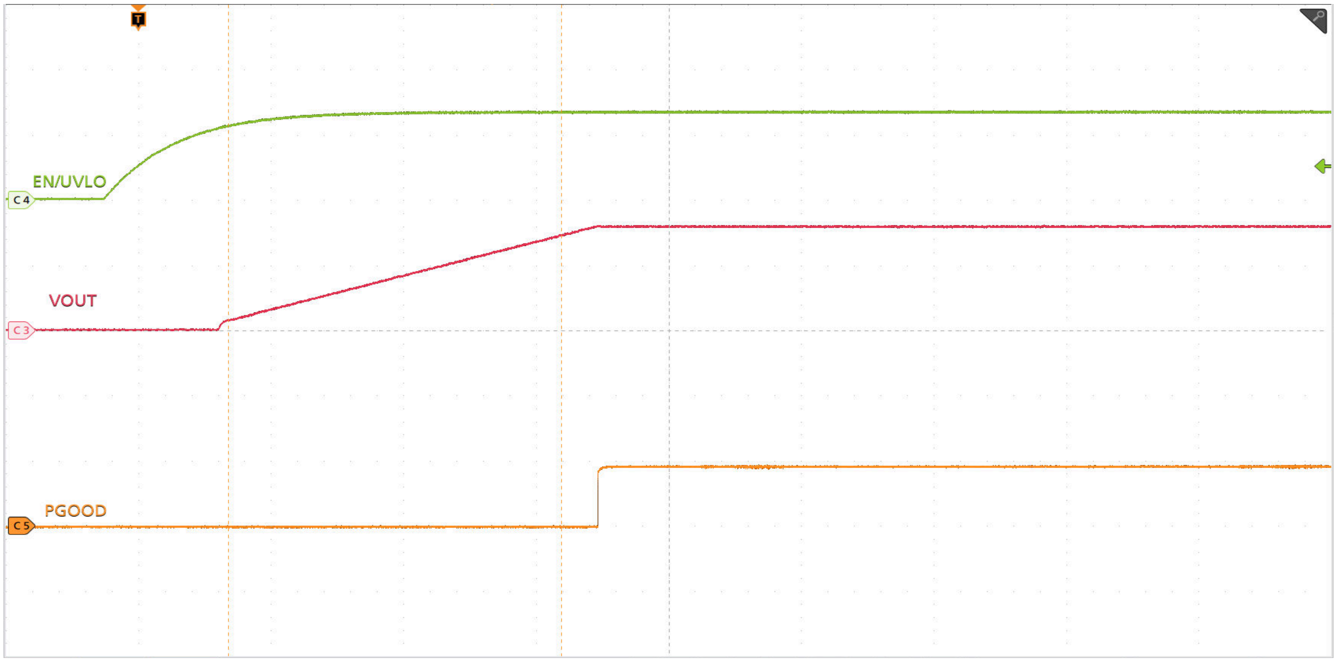


Timescale = 40 ns/div, CH1 = High-side V_{DS} at 5 V/div

Figure 7-10. High-side MOSFET V_{DS}

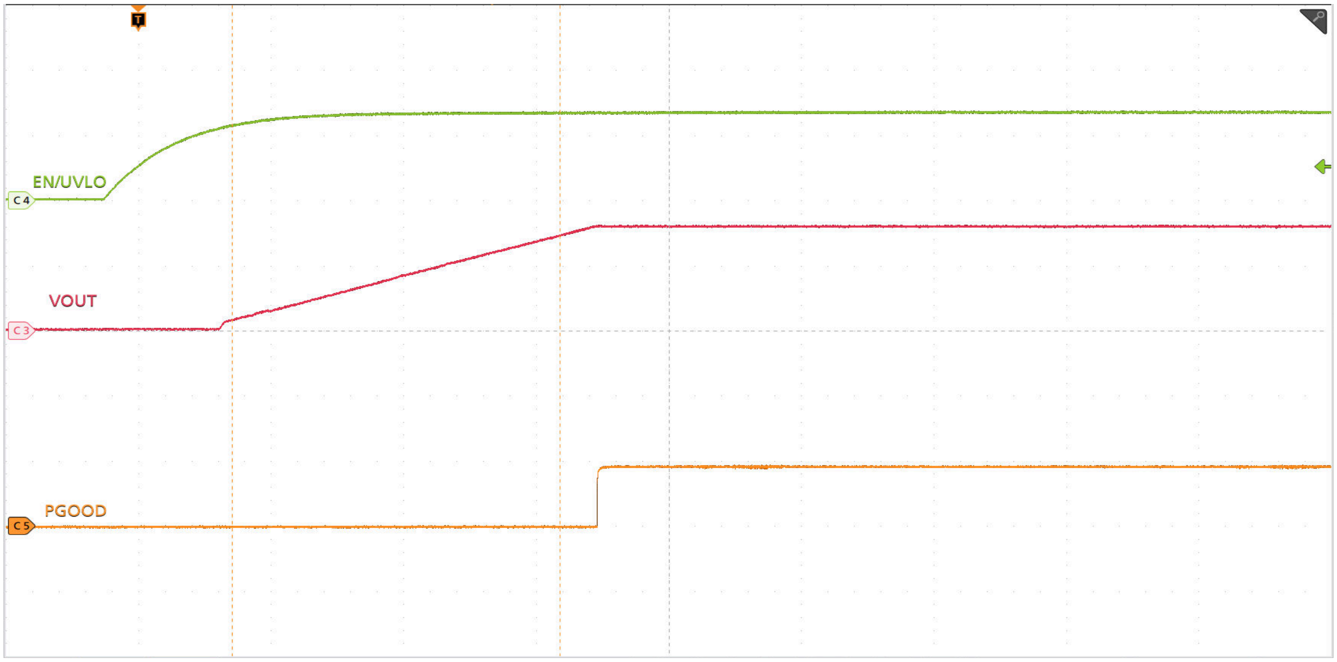
7.7 Control On

Figure 7-11 and Figure 7-12 illustrate the start-up from control on waveforms at 0-A and 80-A output.



Timescale = 1 ms/div, CH3 = V_{OUT} at 500mV/div, CH4 = EN/UVLO at 2 V/div, CH5 = PGOOD at 5 V/div

Figure 7-11. Start-Up From Control, 0-A Load

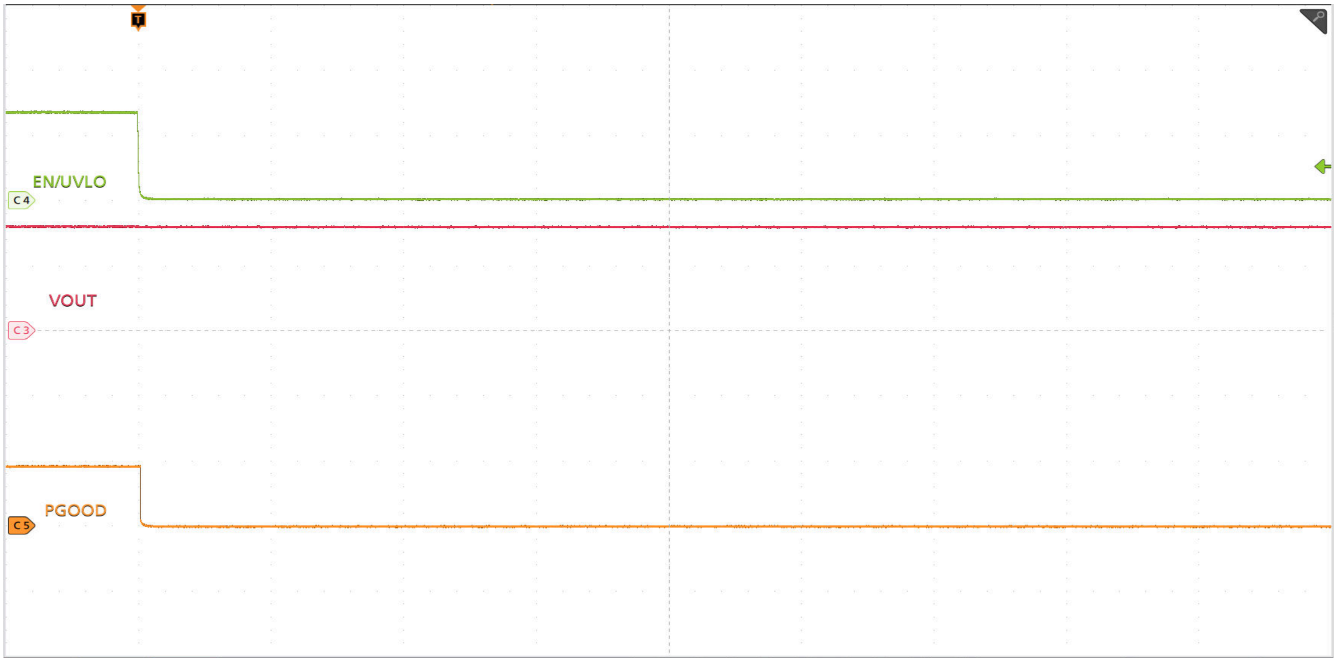


Timescale = 1 ms/div, CH3 = V_{OUT} at 500mV/div, CH4 = EN/UVLO at 2 V/div, CH5 = PGOOD at 5 V/div

Figure 7-12. Start-Up From Control, 80-A CC Load

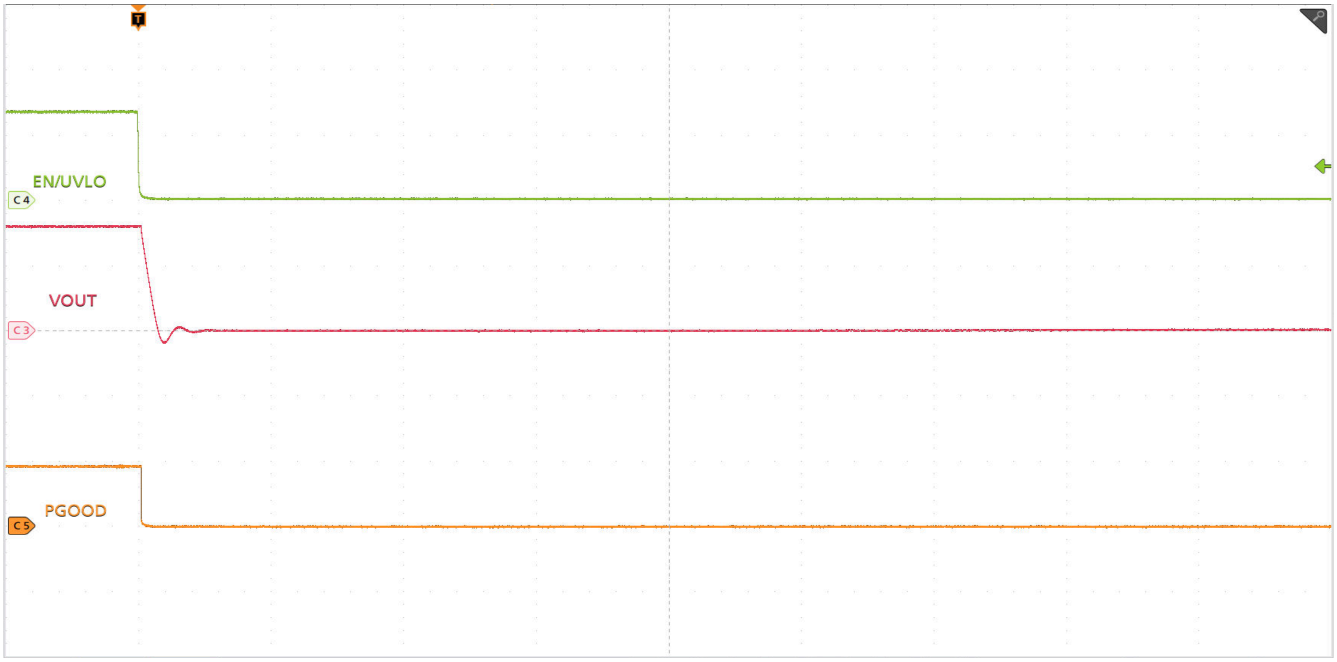
7.8 Control Off

Figure 7-13 and Figure 7-14 illustrate the control off waveforms at 0-A and 20-A outputs, respectively.



Timescale = 1 ms/div, CH3 = V_{OUT} at 500mV/div, CH4 = EN/UVLO at 2 V/div, CH5 = PGOOD at 5 V/div

Figure 7-13. Shutdown From Control, 0-A Load

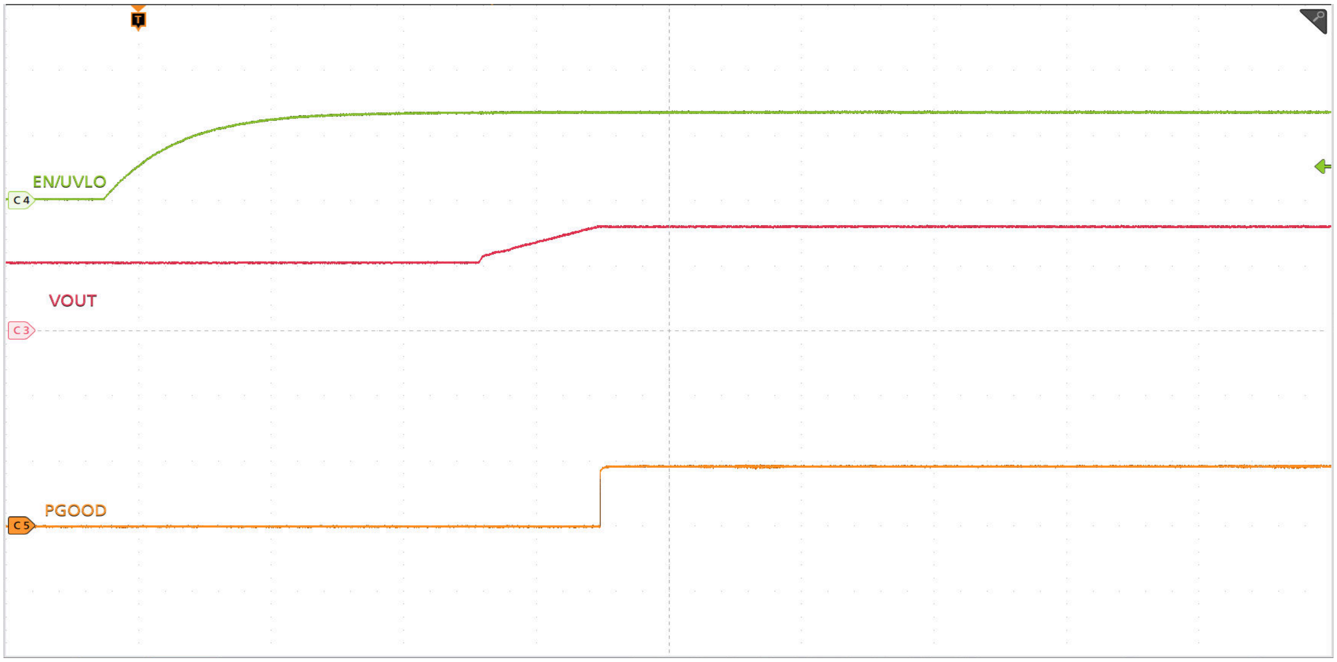


Timescale = 1 ms/div, CH3 = V_{OUT} at 500mV/div, CH4 = EN/UVLO at 2 V/div, CH5 = PGOOD at 5 V/div

Figure 7-14. Shutdown From Control, 20-A CC Load

7.9 Control On With Pre-biased Output

Figure 7-15 illustrates the control on waveforms with a pre-biased output voltage.

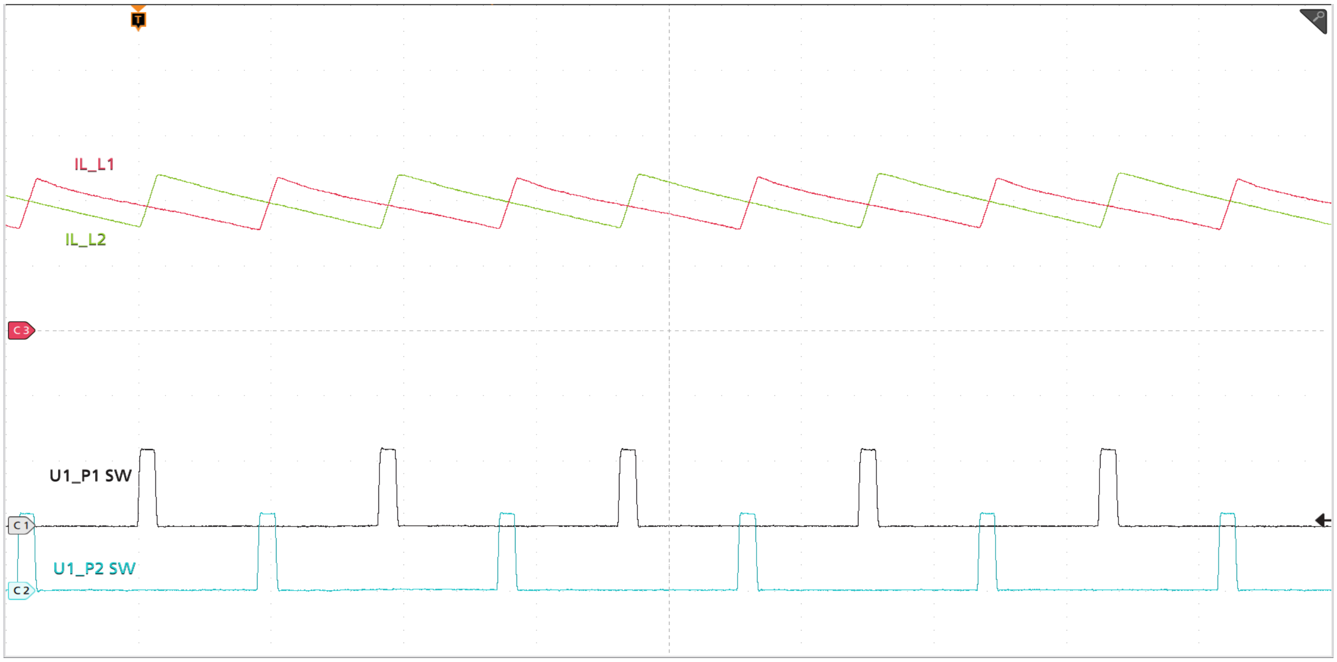


Timescale = 1 ms/div, CH3 = V_{OUT} at 500mV/div, CH4 = EN/UVLO at 2 V/div, CH5 = PGOOD at 5 V/div

Figure 7-15. Start-Up From Control With Pre-biased Output

7.10 Current Sharing Between Two Phases

Figure 7-16 illustrates the current sharing between two phases.

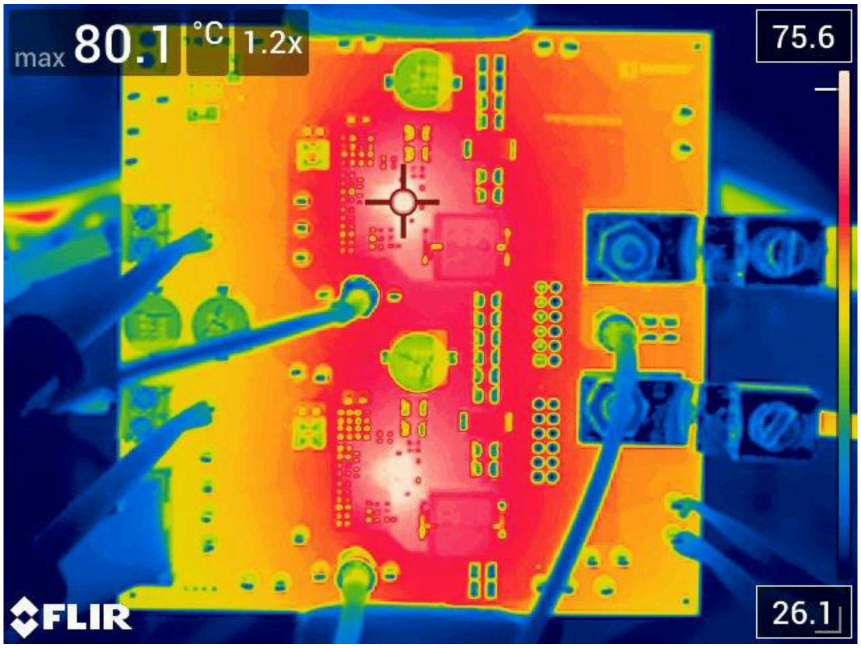


Timescale = 1 µs/div, CH1 = SW1 at 10 V/div, CH2 = SW2 at 10 V/div, CH3 = IL1 at 10 A/div, CH4 = IL2 at 10 A/div

Figure 7-16. Inductor Current and Switch Node Waveform, 40-A Load

7.11 Thermal Image

Figure 7-17 shows the TPS546D24SEVM-2PH thermal image.



V_{IN} = 12 V, I_{OUT} = 80 A

Figure 7-17. Thermal Image

8 EVM Assembly Drawing and PCB Layout

Figure 8-1 through Figure 8-8 show the design of the TPS546D24SEVM-2PH printed circuit board.

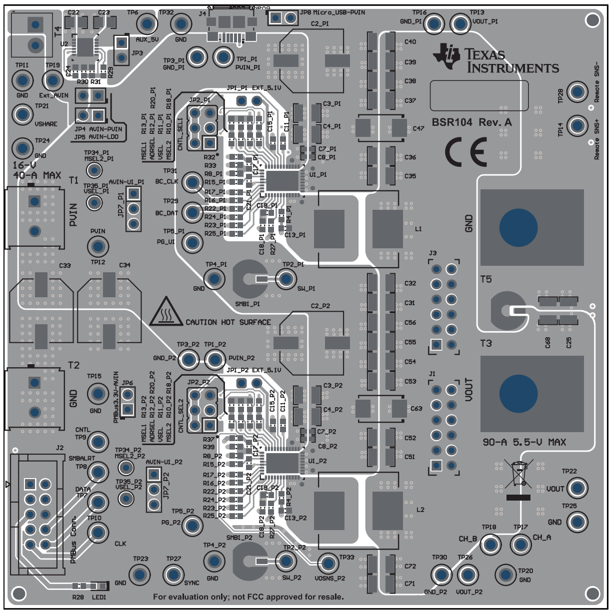


Figure 8-1. TPS546D24SEVM-2PH Top Side Component View (Top View)

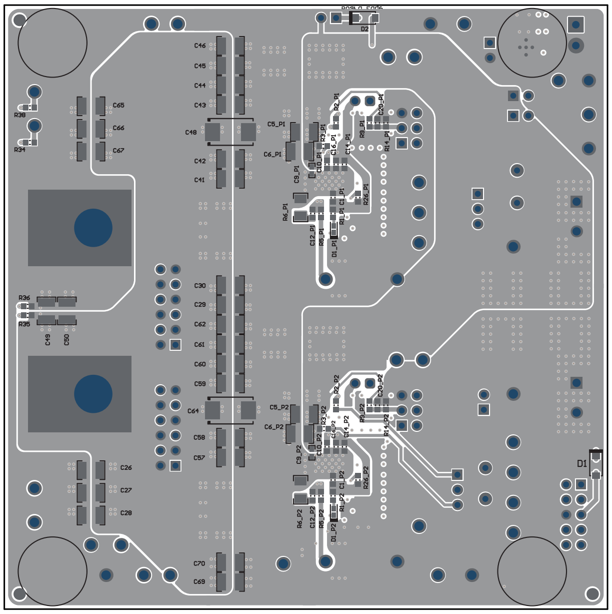


Figure 8-2. TPS546D24SEVM-2PH Bottom Side Component View (Bottom View)

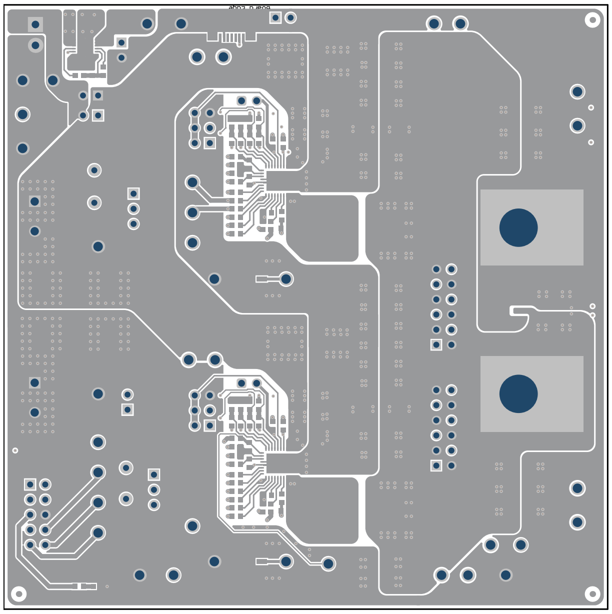


Figure 8-3. TPS546D24SEVM-2PH Top Copper (Top View)

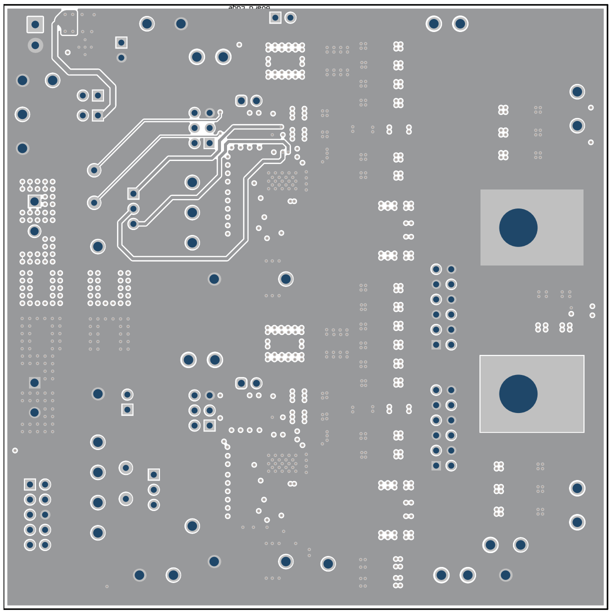


Figure 8-4. TPS546D24SEVM-2PH Internal Layer 1 (Top View)

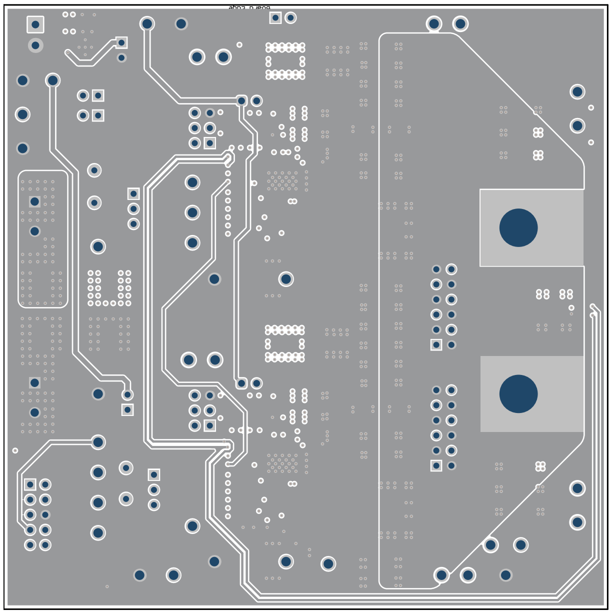


Figure 8-5. TPS546D24SEVM-2PH Internal Layer 2 (Top View)

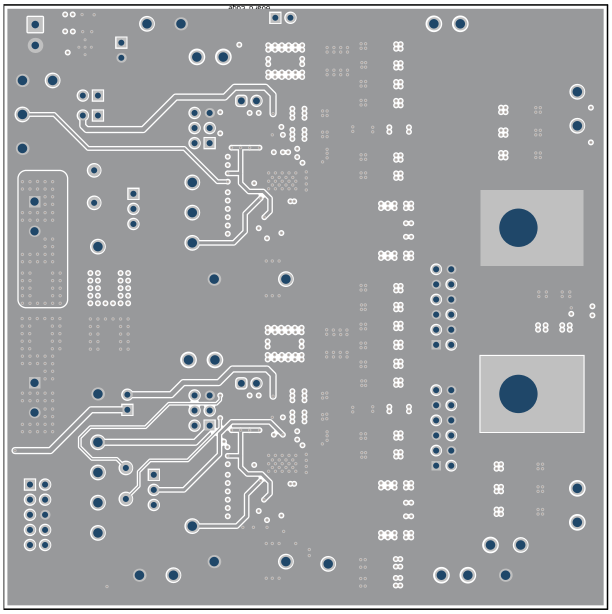


Figure 8-6. TPS546D24SEVM-2PH Internal Layer 3 (Top View)

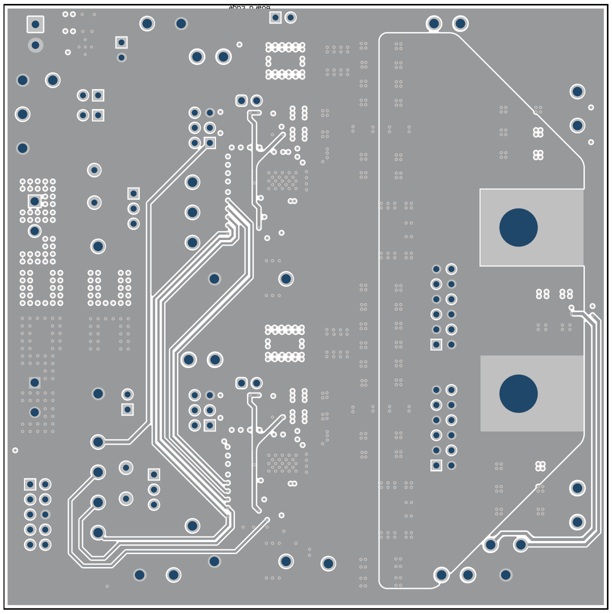


Figure 8-7. TPS546D24SEVM-2PH Internal Layer 4 (Top View)

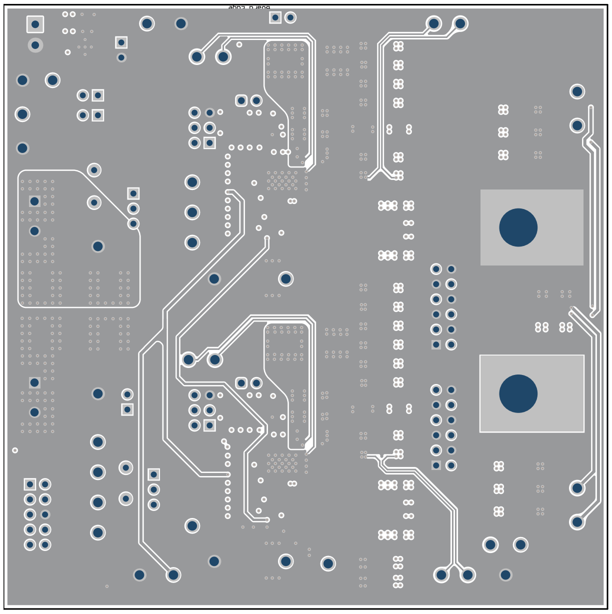


Figure 8-8. TPS546D24SEVM-2PH Internal Layer 5 (Top View)

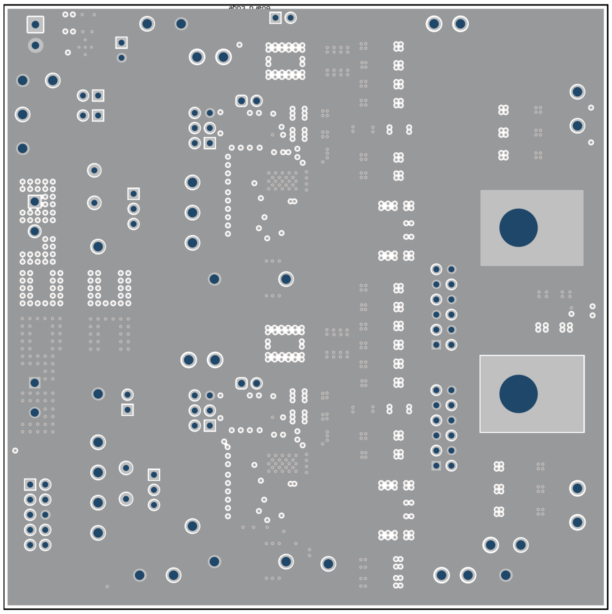


Figure 8-9. TPS546D24SEVM-2PH Internal Layer 6 (Top View)

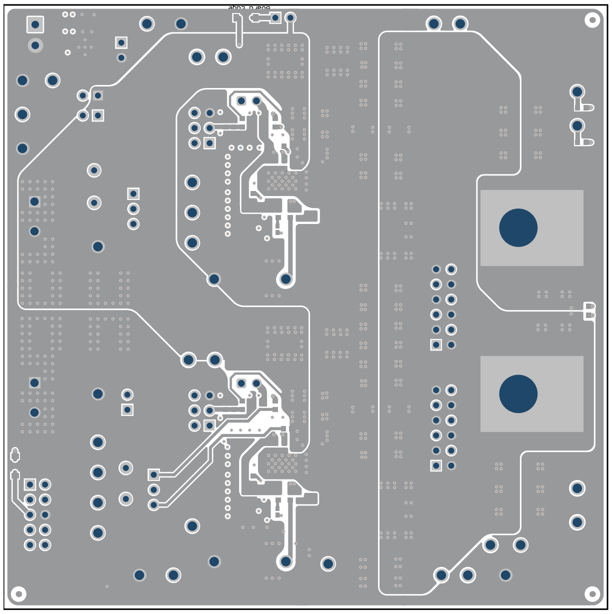


Figure 8-10. TPS546D24SEVM-2PH Internal Bottom Layer (Top View)

9 Bill of Materials

Table 9-1 lists the BOM for the TPS546D24SEVM-2PH.

Table 9-1. TPS546D24SEVM-2PH Bill of Materials

Designator[(1)]	Quantity	Value	Description	Package	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		BSR104	Any
C1_P1, C1_P2, C11_P1, C11_P2	4	1 uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet
C2_P1, C2_P2, C33, C34	4	100 uF	CAP, AL, 100 uF, 35 V, +/- 20%, 0.15 ohm, SMD	SMT Radial G	EEE-FC1V101P	Panasonic
C3_P1, C3_P2, C4_P1, C4_P2, C5_P1, C5_P2, C6_P1, C6_P2	8	22 uF	CAP, CERM, 22 uF, 25 V, +/- 10%, X6S, 1210	1210	GRM32EC81E226KE15L	MuRata
C7_P1, C7_P2, C8_P1, C8_P2, C9_P1, C9_P2	6	6800 pF	CAP, CERM, 6800 pF, 50 V, +/- 10%, X7R, 0402	0402	GRM155R71H682KA88D	MuRata
C12_P1, C12_P2	2	1000 pF	CAP, CERM, 1000 pF, 100 V, +/- 5%, X7R, 0603	0603	06031C102JAT2A	AVX
C13_P1, C13_P2, C20_P1, C20_P2	4	0.1 uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	0603	C0603C104K5RACTU	Kemet
C15_P1, C15_P2	2	4.7 uF	CAP, CERM, 4.7 uF, 10 V, +/- 10%, X5R, 0603	0603	C0603C475K8PACTU	Kemet
C17_P1	1	100 pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H101JA01D	MuRata
C19_P1, C19_P2	2	2.2 uF	CAP, CERM, 2.2 uF, 16 V, +/- 10%, X7R, 0603	0603	EMK107BB7225KA-T	Taiyo Yuden
C21_P1, C21_P2	2	33 pF	CAP, CERM, 33 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	C0603C330J5GACTU	Kemet
C22	1	1 uF	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0805	0805	C0805C105K5RACTU	Kemet
C23	1	10 uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X7R, 0805	0805	C2012X7R1A106M125AC	TDK
C24	1	0.01 uF	CAP, CERM, 0.01 µF, 100 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	GCM188R72A103KA37J	MuRata
C25, C26, C31, C32, C35, C36, C37, C38, C41, C42, C43, C44, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C67, C68	26	47 uF	CAP, CERM, 47 uF, 10 V, +/- 10%, X7R, 1210	1210	GRM32ER71A476KE15L	MuRata
C47, C48, C63, C64	4	470 uF	CAP, Tantalum Polymer, 470 uF, 6.3 V, +/- 20%, 0.01 ohm, 7343-40 SMD	7343-40	6TPF470MAH	Panasonic
D1, D2	2	30 V	Diode, Schottky, 30 V, 2 A, AEC-Q101, SOD-123FL	SOD-123FL	MBR230LSFT1G	ON Semiconductor
D1_P1, D1_P2	2	45 V	Diode, Schottky, 45 V, 0.75 A, SOD-523	SOD-523	BAS 52-02V H6327	Infineon Technologies
H1, H2	2		Machine Screw Pan Philips 10-32		PMSSS 102 0050 PH	B&F Fastener Supply
H3, H4, H5, H6	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
H7, H8	2		Machine Screw Nut, Hex, 3/8', Stn, Steel, 10-32		HNSS 102	B&F Fastener Supply
H9, H10	2		Washer, Split Lock, #10		1477	Keystone
J2	1		Header (shrouded), 100mil, 5x2, Gold, TH	5x2 Shrouded header	5103308-1	TE Connectivity
J4	1		Connector, Receptacle, Micro-USB Type B, R/A, Bottom Mount SMT	MICRO USB CONN, R/A	1981568-1	TE Connectivity
JP1_P1, JP1_P2	2		Header, 2.54 mm, 2x1, Gold, TH	Header, 2.54mm, 2x1, TH	61300211121	Wurth Elektronik
JP2_P1, JP2_P2	2		Header, 100mil, 3x2, Gold, TH	Sullins 100mil, 2x3, 230 mil above insulator	PBC03DAAN	Sullins Connector Solutions
JP3, JP4, JP5	3		Header, 100mil, 2x1, Tin, TH	Header, 2x1, 100mil, TH	5-146278-2	TE Connectivity

Table 9-1. TPS546D24SEVM-2PH Bill of Materials (continued)

Designator[1]	Quantity	Value	Description	Package	Part Number	Manufacturer
JP7_P1, JP7_P2	2		Header, 100mil, 3x1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
L1, L2	2	150 nH	Inductor, Shielded, Ferrite, 150 nH, 55 A, 0.00015 ohm, SMD	SMD 13.46x8.0x12.95mm	SLC1480-151MLB	Coilcraft
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
LED1	1	Green	LED, Green, SMD	LED_0603	150060GS75000	Wurth Elektronik
R2_P1, R2_P2, R3_P1, R3_P2	4	10	RES, 10, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310R0JNEA	Vishay-Dale
R4_P1, R4_P2, R15_P1, R15_P2, R16_P1, R16_P2, R17_P1, R17_P2, R18_P2, R22_P1, R22_P2, R23_P1, R23_P2, R25_P1, R25_P2, R27_P1, R27_P2, R32, R33	19	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEY0R00V	Panasonic
R5_P1, R5_P2, R34, R35, R36, R38	6	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060349R9FKEA	Vishay-Dale
R6_P1, R6_P2	2	1.0	RES, 1.0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	CRCW12061R00JNEA	Vishay-Dale
R8_P2, R26_P1, R26_P2	3	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R9_P1, R9_P2	2	30.1k	RES, 30.1 k, 1%, 0.1 W, 0603	0603	RC0603FR-0730K1L	Yageo
R14_P1, R14_P2	2	7.50k	RES, 7.50 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF7501V	Panasonic
R19_P1	1	14.7k	RES, 14.7 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3EKF1472V	Panasonic
R21_P1	1	12.1k	RES, 12.1 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060312K1FKEA	Vishay-Dale
R28	1	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
R29	1	47.5k	RES, 47.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060347K5FKEA	Vishay-Dale
R30	1	15.0k	RES, 15.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060315K0FKEA	Vishay-Dale
R31	1	560k	RES, 560 k, 1%, 0.1 W, 0603	0603	RC0603FR-07560KL	Yageo
SH-JP1, SH-JP2, SH-JP3, SH-JP4, SH-JP5, SH-JP6	6	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
SMB1_P1, SMB1_P2, SMB2	3		Connector, Receptacle, 50 ohm, TH	SMB Connector	SMBR004D00	JAE Electronics
T1, T2	2		Therminal Block, 5 mm, 2-pole, Tin, TH	TH, 2-Leads, Body 10x10mm, Pitch 5mm	282856-2	TE Connectivity
T3, T5	2		Terminal 90-A Lug	CB70-14-CY	CB70-14-CY	Panduit
T4	1		Terminal Block, 3.5mm Pitch, 2x1, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
TP1_P1, TP1_P2, TP6, TP12, TP13, TP19, TP22, TP26	8		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
TP2_P1, TP2_P2, TP5_P1, TP5_P2, TP7, TP8, TP9, TP10, TP14, TP17, TP18, TP21, TP27, TP28, TP29, TP31	16		Test Point, Multipurpose, White, TH	White Multipurpose Testpoint	5012	Keystone
TP3_P1, TP3_P2, TP4_P1, TP4_P2, TP11, TP15, TP16, TP20, TP23, TP24, TP25, TP30, TP32	13		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone
U1_P1, U1_P2	2		2.95-16 V 40 A PMBUS Stackable Synchronous Buck Converter, RVF0040A (LQFN-CLIP-40)	RVF0040A	TPS546D24SRVFR	Texas Instruments
U2	1		800-mA Ultra-Low-Noise, High-PSRR LDO, DNT0012B (WSON-12)	DNT0012B	LP38798SD-ADJ/NOPB	Texas Instruments

Table 9-1. TPS546D24SEVM-2PH Bill of Materials (continued)

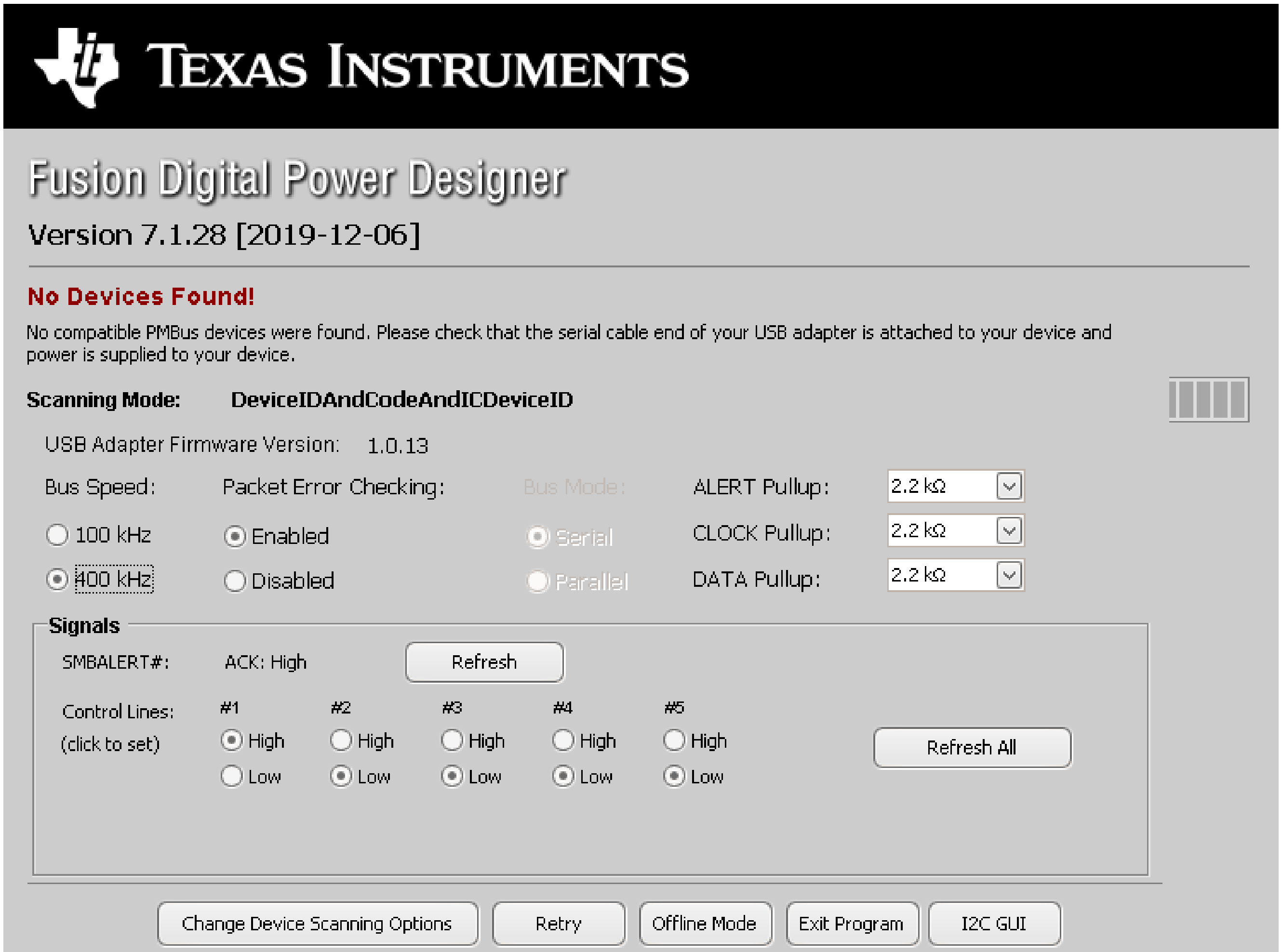
Designator[1]	Quantity	Value	Description	Package	Part Number	Manufacturer
C10_P1, C10_P2, C14_P1, C14_P2	0	1 uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet
C16_P1, C16_P2	0	0.1 uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	0603	C0603C104K5RACTU	Kemet
C17_P2	0	100 pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H101JA01D	MuRata
C18_P1, C18_P2	0	2.2 uF	CAP, CERM, 2.2 uF, 16 V, +/- 10%, X7R, 0603	0603	EMK107BB7225KA-T	Taiyo Yuden
C27, C28, C29, C30, C39, C40, C45, C46, C61, C62, C65, C66, C69, C70, C71, C72	0	47 uF	CAP, CERM, 47 uF, 10 V, +/- 10%, X7R, 1210	1210	GRM32ER71A476KE15L	MuRata
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J1, J3	0		Receptacle, 2.54mm, 6x2, Gold, TH	Receptacle, 2.54mm, 6x2, TH	SSQ-106-03-G-D	Samtec
JP6, JP8	0		Header, 100mil, 2x1, Tin, TH	Header, 2x1, 100mil, TH	5-146278-2	TE Connectivity
R1_P1, R1_P2, R18_P1, R24_P1, R24_P2, R37, R39	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEY0R00V	Panasonic
R8_P1	0	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R10_P1, R10_P2, R11_P1, R11_P2, R12_P1, R12_P2, R20_P1, R20_P2	0	10.5k	RES, 10.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K5FKEA	Vishay-Dale
R13_P1, R13_P2	0	53.6k	RES, 53.6 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060353K6FKEA	Vishay-Dale
R19_P2	0	14.7k	RES, 14.7 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3EKF1472V	Panasonic
R21_P2	0	12.1k	RES, 12.1 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060312K1FKEA	Vishay-Dale
TP33	0		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
TP34_P1, TP34_P2, TP35_P1, TP35_P2	0		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone

(1) Unless otherwise noted, all parts can be substituted with equivalents.

10 Using the Fusion GUI

10.1 Opening the Fusion GUI

The Fusion GUI must include *IC_DEVICE_ID* in the scanning mode to find TPS546D24S. The EVM needs power to be recognized by the Fusion GUI. See Section 5 for the recommended procedure. Figures in this section can use screen shots showing other TPS546x24x family devices to illustrate the use of the FUSION GUI with the TPS546D24SEVM-2PH when those functions are similar.



Fusion Digital Power Designer

Version 7.1.28 [2019-12-06]

No Devices Found!

No compatible PMBus devices were found. Please check that the serial cable end of your USB adapter is attached to your device and power is supplied to your device.

Scanning Mode: **DeviceIDAndCodeAndICDeviceID**

USB Adapter Firmware Version: 1.0.13

Bus Speed: ○ 100 kHz ● 400 kHz

Packet Error Checking: ● Enabled ○ Disabled

Bus Mode: ● Serial ○ Parallel

ALERT Pullup: 2.2 kΩ

CLOCK Pullup: 2.2 kΩ

DATA Pullup: 2.2 kΩ

Signals

SMBALERT#: ACK: High

Control Lines: (click to set)

	#1	#2	#3	#4	#5
High	●	○	○	○	○
Low	○	●	●	●	●

Figure 10-1. Select Device Scanning Mode

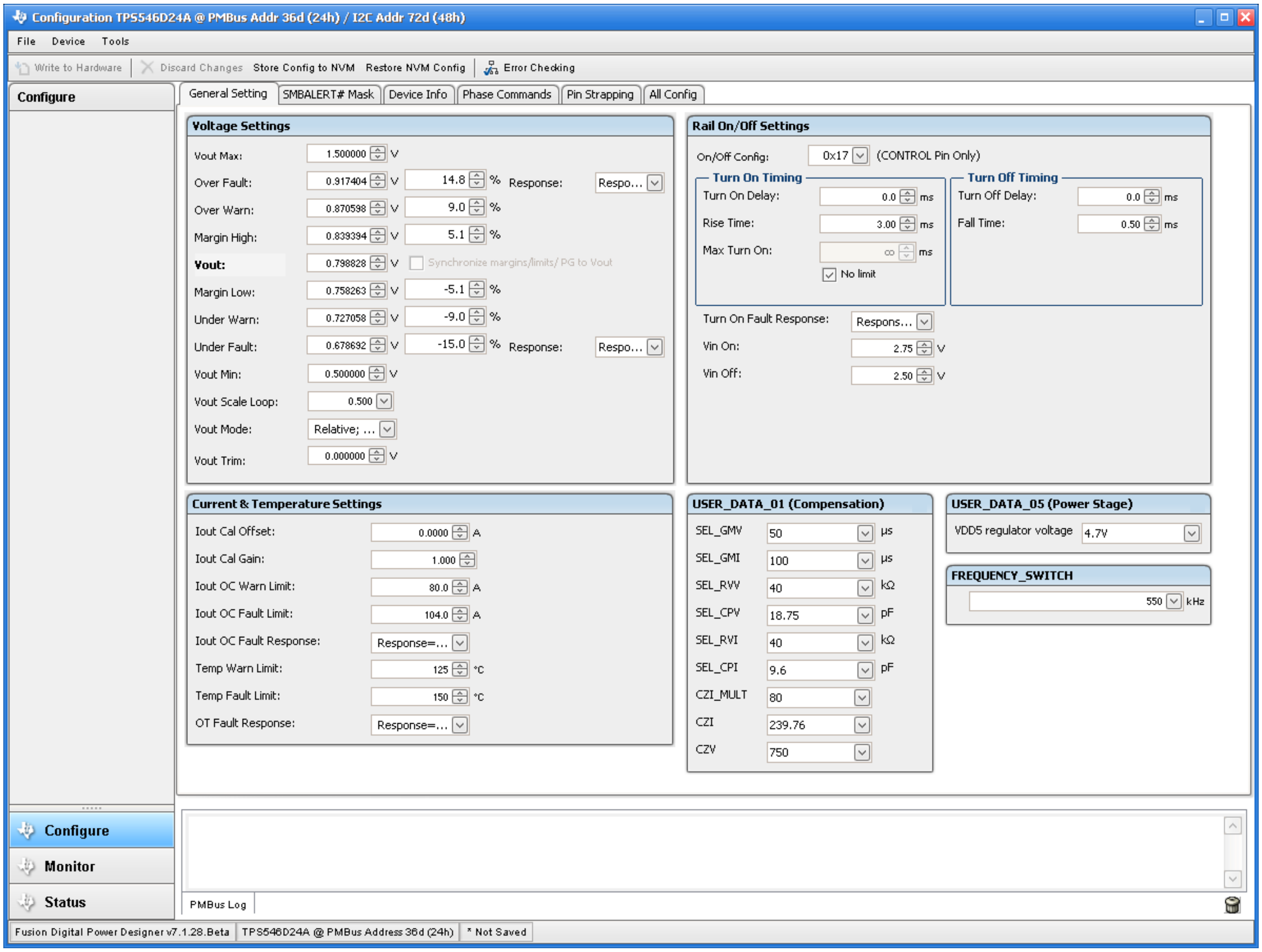
10.2 General Settings

Figure 10-2 shows the *General Settings* that can be used to configure the following:

- Vout settings, power-good limits, and margin voltages
- OC Fault, OC Warn and Fault response
- OT Fault, OT Warn (Die Temperature) and Fault response
- Vin on and off UVLO
- On and Off Config
- Soft Start (Output rise time), other Turn-On Timing and Turn-Off Timing
- Switching frequency
- Compensation

After clicking *Write to Hardware* to make changes to one or more configurable parameters, the changes can be committed to nonvolatile memory by clicking *Store Config to NVM*. This action prompts a pop-up, and if confirmed, the changes are committed to nonvolatile memory to store all the modifications in non-volatile memory.

Both the Stack Controller device (U1_P1) and the Stack Follower device (U1_P2) are tied to same bus interface. In a two-phase stacking system, the stack controller receives and responds to all PMBus communication and follower devices do not need to be connected to the PMBus. If the stack controller receives commands which require updates to the PMBus values of one or all of the followers, the stack controller relays these commands to the followers. All commands on this tab are for PHASE = 0xFF.



Voltage Settings

Vout Max: 1.500000 V
Over Fault: 0.917404 V 14.8 % Response: Respo…
Over Warn: 0.870598 V 9.0 %
Margin High: 0.839394 V 5.1 %
Vout: 0.798828 V ☐ Synchronize margins/limits/ PG to Vout
Margin Low: 0.758263 V -5.1 %
Under Warn: 0.727058 V -9.0 %
Under Fault: 0.678692 V -15.0 % Response: Respo…
Vout Min: 0.500000 V
Vout Scale Loop: 0.500
Vout Mode: Relative; …
Vout Trim: 0.000000 V

Rail On/Off Settings

On/Off Config: 0x17 (CONTROL Pin Only)

Turn On Timing
Turn On Delay: 0.0 ms
Rise Time: 3.00 ms
Max Turn On: ∞ ms
☑ No limit

Turn Off Timing
Turn Off Delay: 0.0 ms
Fall Time: 0.50 ms

Turn On Fault Response: Respons…
Vin On: 2.75 V
Vin Off: 2.50 V

Current & Temperature Settings

Iout Cal Offset: 0.0000 A
Iout Cal Gain: 1.000
Iout OC Warn Limit: 80.0 A
Iout OC Fault Limit: 104.0 A
Iout OC Fault Response: Response=…
Temp Warn Limit: 125 °C
Temp Fault Limit: 150 °C
OT Fault Response: Response=…

USER_DATA_01 (Compensation)

SEL_GMV 50 µs
SEL_GMI 100 µs
SEL_RVV 40 kΩ
SEL_CPV 18.75 pF
SEL_RVI 40 kΩ
SEL_CPI 9.6 pF
CZI_MULT 80
CZI 239.76
CZV 750

USER_DATA_05 (Power Stage)

VDD5 regulator voltage 4.7V

FREQUENCY_SWITCH

550 kHz

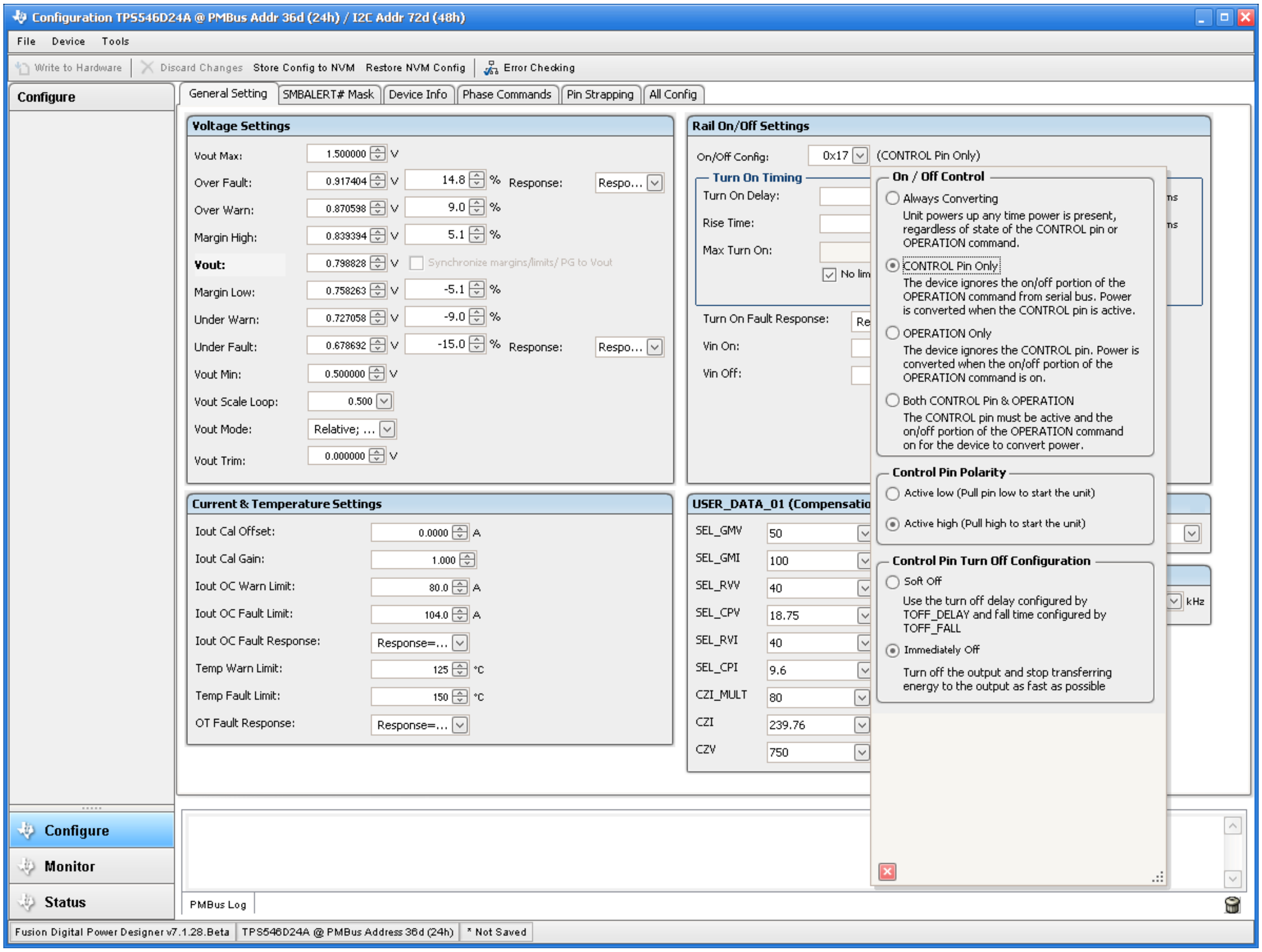
Fusion Digital Power Designer v7.1.28.Beta | TPS546D24A @ PMBus Address 36d (24h) | * Not Saved

Figure 10-2. General Settings

Some commands require the

10.3 Changing ON_OFF_CONFIG

Changing the *On and Off Config* prompts a pop-up window with details of the options shown in Figure 10-3. This pop-up gives multiple options on what turns on and off power conversion. By default the TPS546D24S is configured to *CONTROL Pin Only*. This pin is the EN/UVLO pin.



Voltage Settings

Vout Max: 1.500000 V
Over Fault: 0.917404 V 14.8 % Response: Respo...
Over Warn: 0.870598 V 9.0 %
Margin High: 0.839394 V 5.1 %
Vout: 0.798828 V ☐ Synchronize margins/limits/ PG to Vout
Margin Low: 0.758263 V -5.1 %
Under Warn: 0.727058 V -9.0 %
Under Fault: 0.678692 V -15.0 % Response: Respo...
Vout Min: 0.500000 V
Vout Scale Loop: 0.500
Vout Mode: Relative; ...
Vout Trim: 0.000000 V

Current & Temperature Settings

Iout Cal Offset: 0.0000 A
Iout Cal Gain: 1.000
Iout OC Warn Limit: 80.0 A
Iout OC Fault Limit: 104.0 A
Iout OC Fault Response: Response=...
Temp Warn Limit: 125 °C
Temp Fault Limit: 150 °C
OT Fault Response: Response=...

Rail On/Off Settings

On/Off Config: 0x17 (CONTROL Pin Only)

Turn On Timing
Turn On Delay:
Rise Time:
Max Turn On:
☑ No lim
Turn On Fault Response: Re
Vin On:
Vin Off:

USER_DATA_01 (Compensatio

SEL_GMV 50
SEL_GMI 100
SEL_RVV 40
SEL_CPV 18.75
SEL_RVI 40
SEL_CPI 9.6
CZI_MULT 80
CZI 239.76
CZV 750

On / Off Control

○ Always Converting
Unit powers up any time power is present, regardless of state of the CONTROL pin or OPERATION command.

● CONTROL Pin Only
The device ignores the on/off portion of the OPERATION command from serial bus. Power is converted when the CONTROL pin is active.

○ OPERATION Only
The device ignores the CONTROL pin. Power is converted when the on/off portion of the OPERATION command is on.

○ Both CONTROL Pin & OPERATION
The CONTROL pin must be active and the on/off portion of the OPERATION command on for the device to convert power.

Control Pin Polarity

○ Active low (Pull pin low to start the unit)
● Active high (Pull high to start the unit)

Control Pin Turn Off Configuration

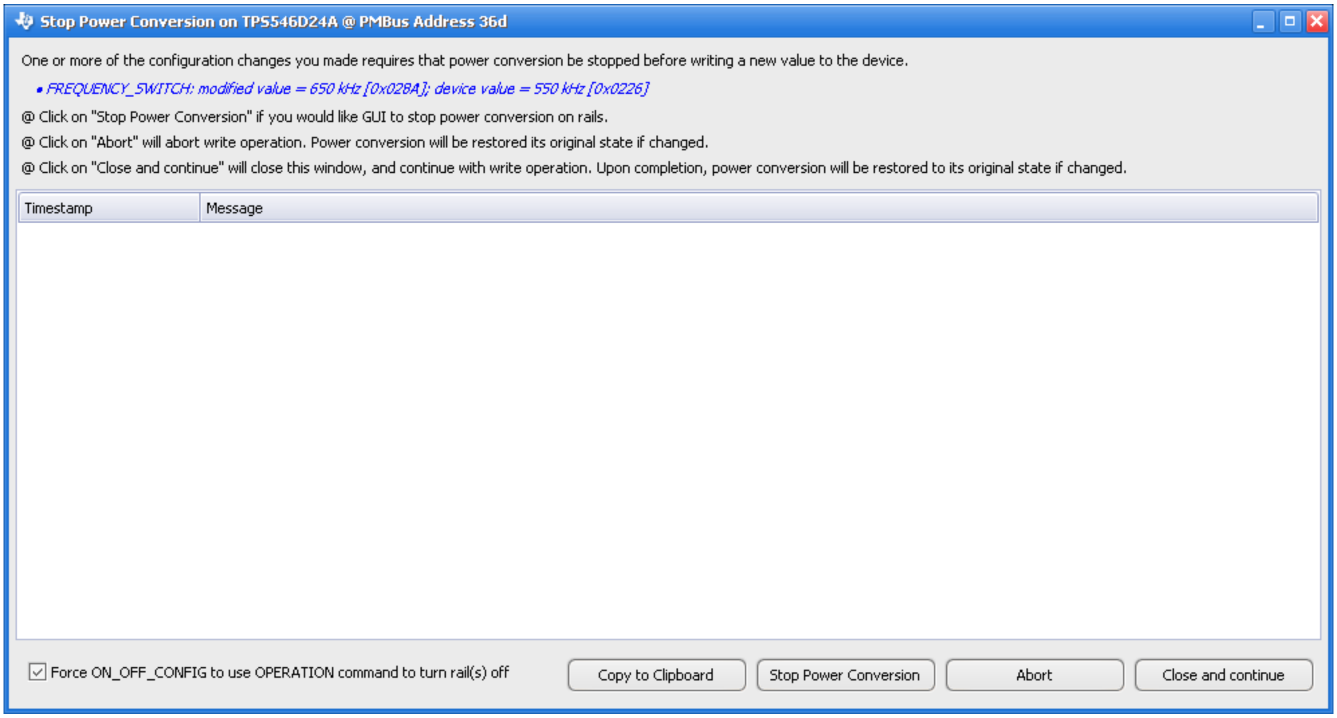
○ Soft Off
Use the turn off delay configured by TOFF_DELAY and fall time configured by TOFF_FALL

● Immediately Off
Turn off the output and stop transferring energy to the output as fast as possible

Figure 10-3. Configure – ON_OFF_CONFIG

10.4 Pop-up for Some Commands While Conversion is Enabled

Some commands cause a pop-up like the one shown in Figure 10-4 when trying to change them while conversion is enabled. The settings in the GUI which cause this pop-up include *FREQUENCY_SWITCH*, *USER_DATA_01 (Compensation)*, *Vout Mode* and *Vout Scale Loop*. To change these settings to a new value, click on *Stop Power Conversion* then *Close and continue*. The GUI automatically disables conversion, write the new value, and enable conversion again.


Stop Power Conversion on TPS546D24A @ PMBus Address 36d

One or more of the configuration changes you made requires that power conversion be stopped before writing a new value to the device.

- *FREQUENCY_SWITCH: modified value = 650 kHz [0x028A]; device value = 550 kHz [0x0226]*

@ Click on "Stop Power Conversion" if you would like GUI to stop power conversion on rails.
@ Click on "Abort" will abort write operation. Power conversion will be restored its original state if changed.
@ Click on "Close and continue" will close this window, and continue with write operation. Upon completion, power conversion will be restored to its original state if changed.

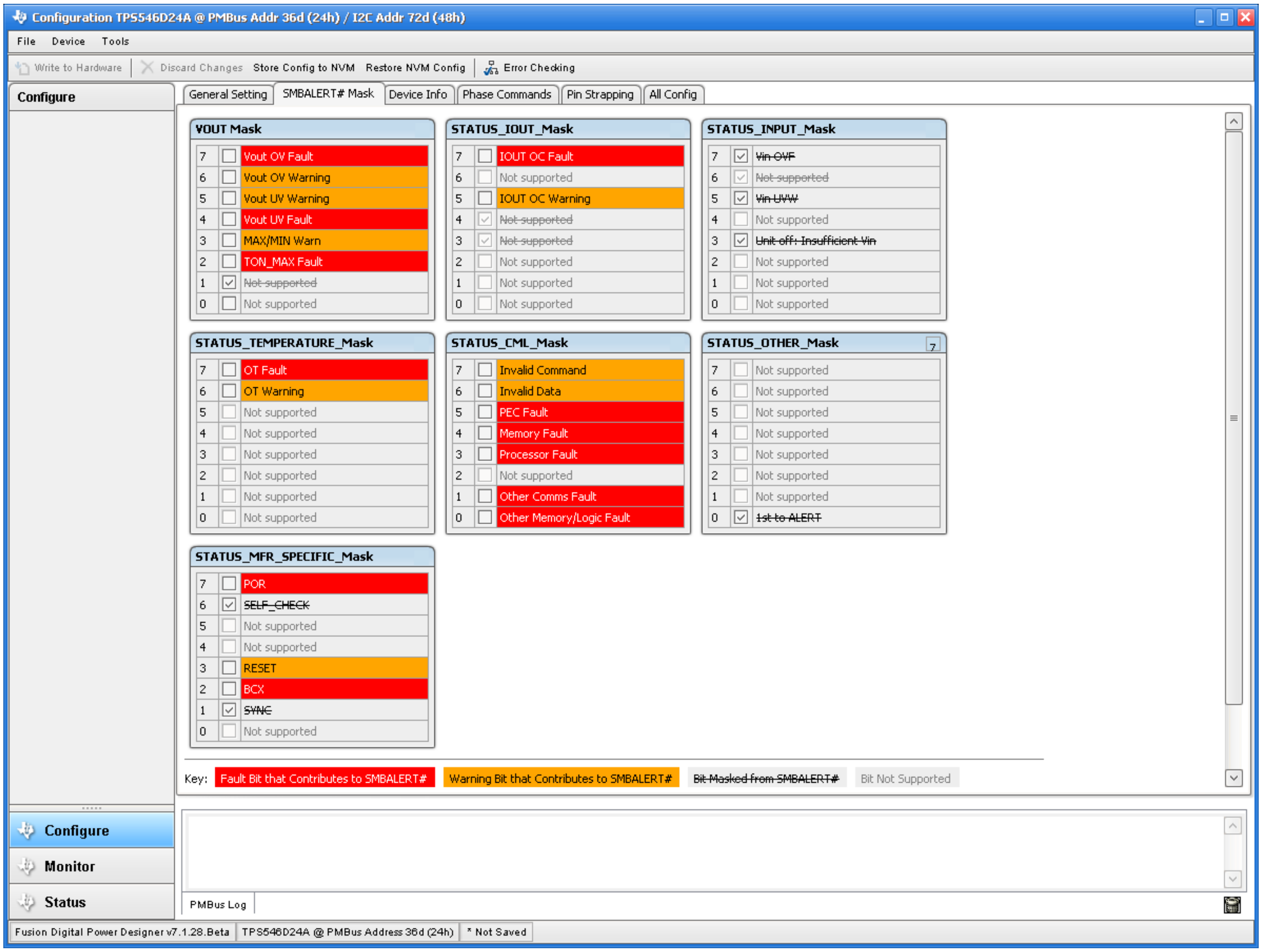
Timestamp	Message

☑ Force ON_OFF_CONFIG to use OPERATION command to turn rail(s) off

Figure 10-4. Pop-up When Trying to Change FREQUENCY_SWITCH with Conversion Enabled

10.5 SMBALERT# Mask

The sources of SMBALERT which can be masked are found and configured on the *SMBALERT # Mask* tab (Figure 10-5).



VOUT Mask

7	☐	Vout OV Fault
6	☐	Vout OV Warning
5	☐	Vout UV Warning
4	☐	Vout UV Fault
3	☐	MAX/MIN Warn
2	☐	TON_MAX Fault
1	☑	~~Not supported~~
0	☐	Not supported

STATUS_IOUT_Mask

7	☐	IOUT OC Fault
6	☐	Not supported
5	☐	IOUT OC Warning
4	☑	~~Not supported~~
3	☑	~~Not supported~~
2	☐	Not supported
1	☐	Not supported
0	☐	Not supported

STATUS_INPUT_Mask

7	☑	~~Vin OVF~~
6	☑	~~Not supported~~
5	☑	~~Vin UVW~~
4	☐	Not supported
3	☑	~~Unit off: Insufficient Vin~~
2	☐	Not supported
1	☐	Not supported
0	☐	Not supported

STATUS_TEMPERATURE_Mask

7	☐	OT Fault
6	☐	OT Warning
5	☐	Not supported
4	☐	Not supported
3	☐	Not supported
2	☐	Not supported
1	☐	Not supported
0	☐	Not supported

STATUS_CML_Mask

7	☐	Invalid Command
6	☐	Invalid Data
5	☐	PEC Fault
4	☐	Memory Fault
3	☐	Processor Fault
2	☐	Not supported
1	☐	Other Comms Fault
0	☐	Other Memory/Logic Fault

STATUS_OTHER_Mask

7	☐	Not supported
6	☐	Not supported
5	☐	Not supported
4	☐	Not supported
3	☐	Not supported
2	☐	Not supported
1	☐	Not supported
0	☑	~~1st to ALERT~~

STATUS_MFR_SPECIFIC_Mask

7	☐	POR
6	☑	~~SELF_CHECK~~
5	☐	Not supported
4	☐	Not supported
3	☐	RESET
2	☐	BCX
1	☑	~~SYNC~~
0	☐	Not supported

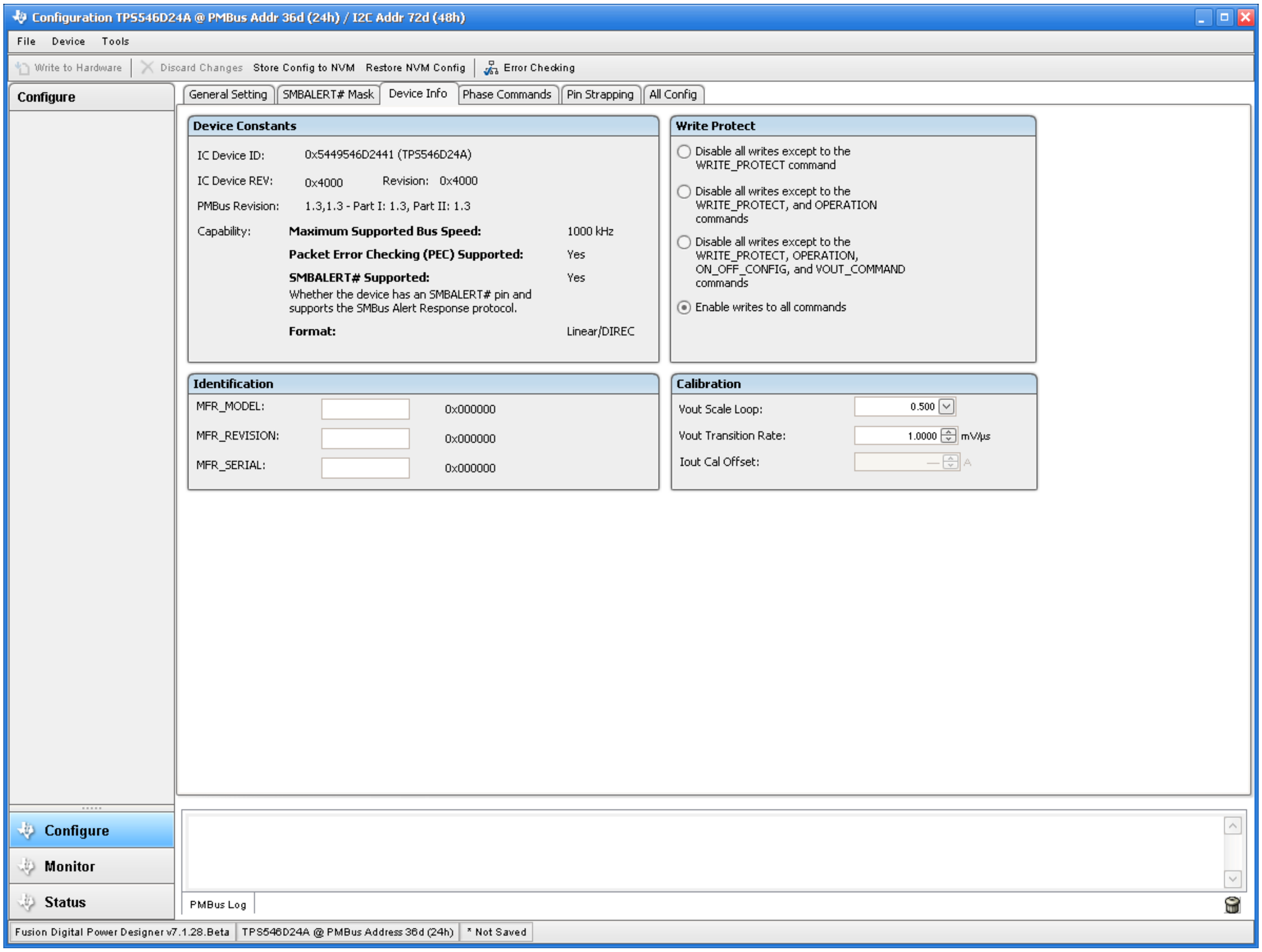
Key: Fault Bit that Contributes to SMBALERT# | Warning Bit that Contributes to SMBALERT# | ~~Bit Masked from SMBALERT#~~ | Bit Not Supported

Fusion Digital Power Designer v7.1.28.Beta | TPS546D24A @ PMBus Address 36d (24h) | * Not Saved

Figure 10-5. Configure – SMBALERT # Mask

10.6 Device Info

The device information, Write Protection options, the configuration of *Vout Scale Loop*, *Vout Transition Rate*, and *Iout Cal Offset* are found on the *Device Info* tab (see Figure 10-6).



Device Constants

IC Device ID: 0x5449546D2441 (TPS546D24A)
IC Device REV: 0x4000 Revision: 0x4000
PMBus Revision: 1.3,1.3 - Part I: 1.3, Part II: 1.3

Capability:		
	Maximum Supported Bus Speed:	1000 kHz
	Packet Error Checking (PEC) Supported:	Yes
	SMBALERT# Supported: Whether the device has an SMBALERT# pin and supports the SMBus Alert Response protocol.	Yes
	Format:	Linear/DIREC

Write Protect

○ Disable all writes except to the WRITE_PROTECT command
○ Disable all writes except to the WRITE_PROTECT, and OPERATION commands
○ Disable all writes except to the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG, and VOUT_COMMAND commands
● Enable writes to all commands

Identification

MFR_MODEL: 0x000000
MFR_REVISION: 0x000000
MFR_SERIAL: 0x000000

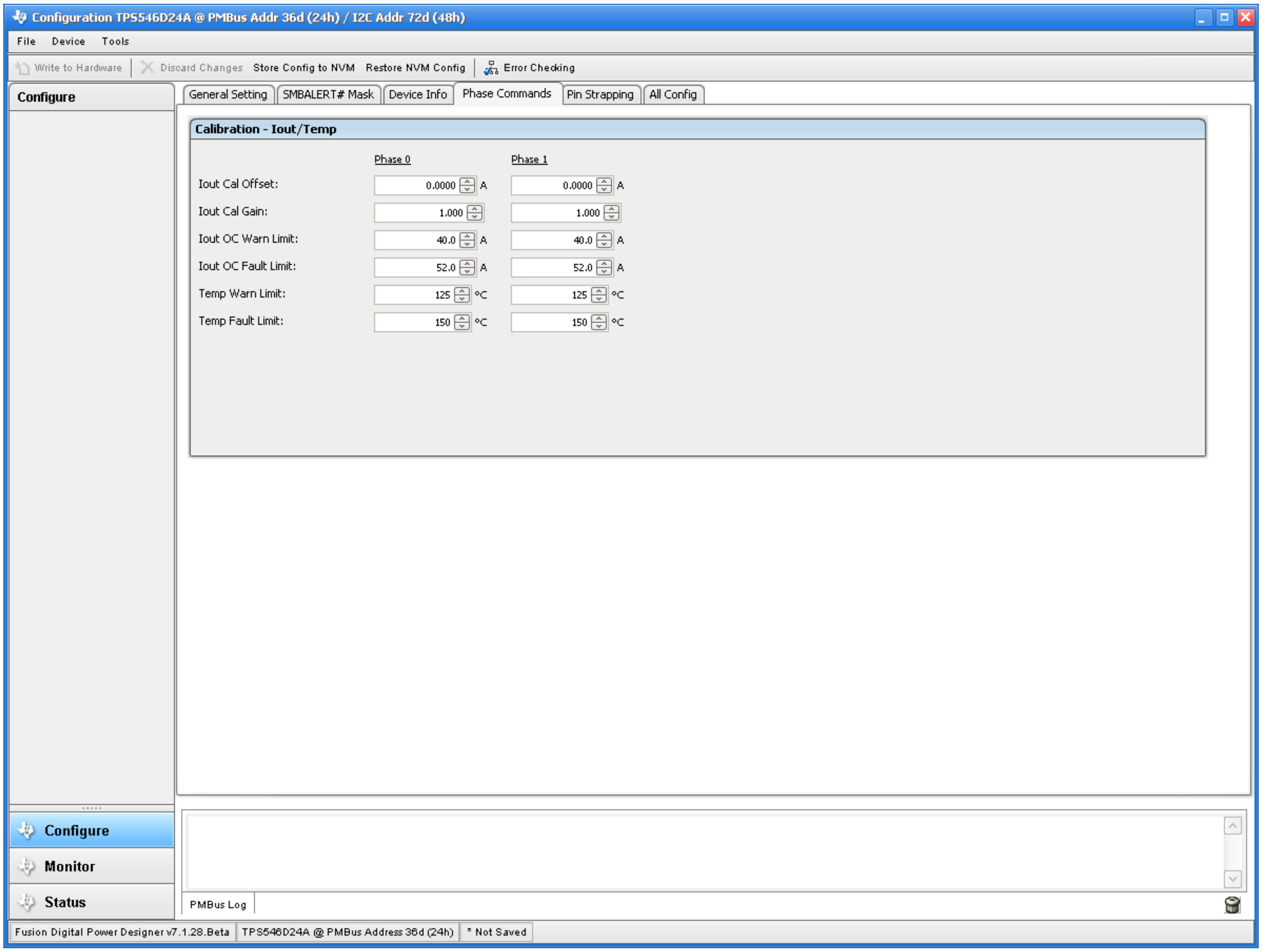
Calibration

Vout Scale Loop: 0.500
Vout Transition Rate: 1.0000 mV/µs
Iout Cal Offset: — A

Figure 10-6. Configure – Device Info

10.7 Phase Commands

Use the *Phase Command* tab (see Figure 10-7) to calibrate the *IOUT/Temp* of each phase.

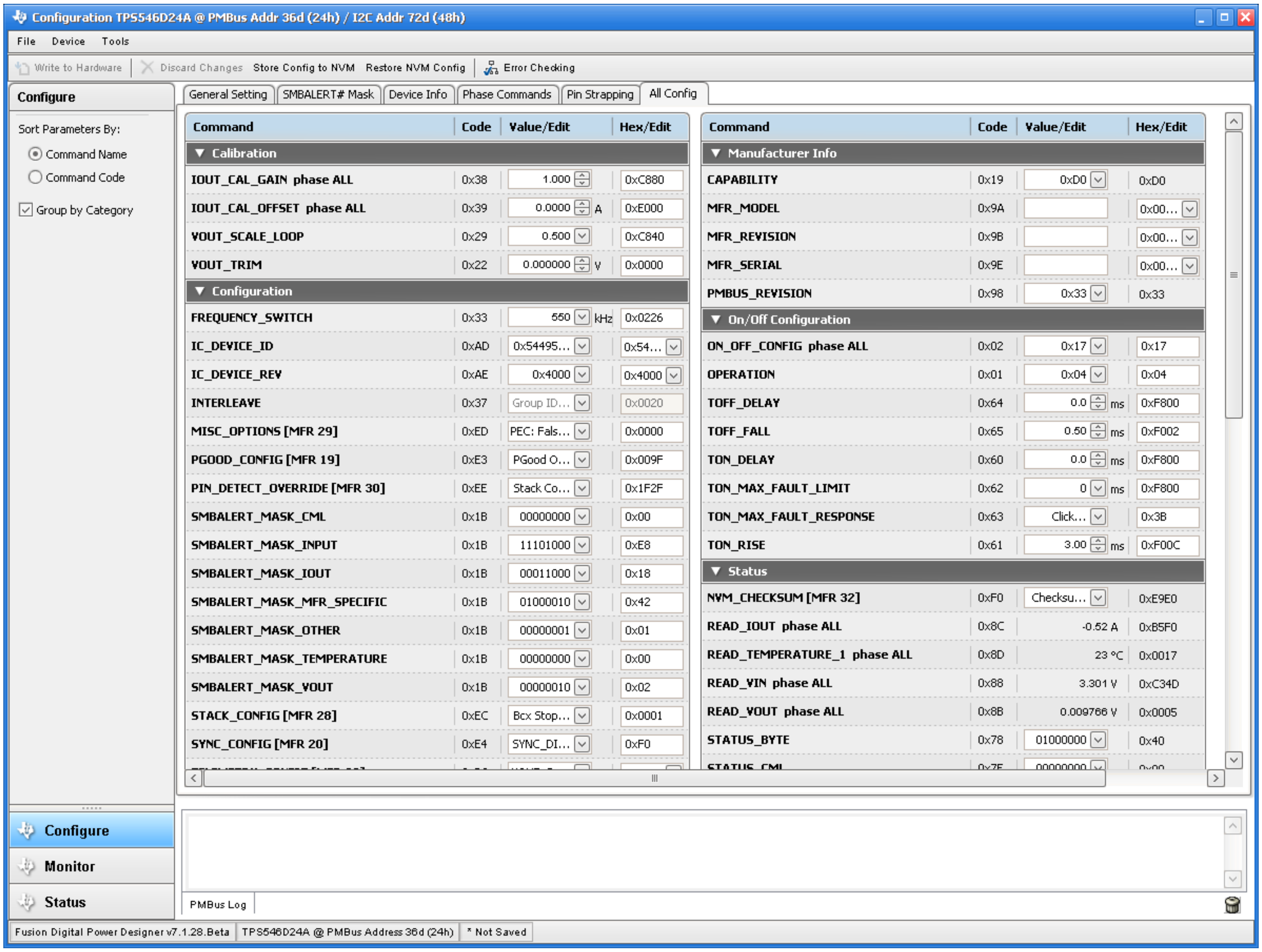


	Phase 0	Phase 1
Iout Cal Offset:	0.0000 A	0.0000 A
Iout Cal Gain:	1.000	1.000
Iout OC Warn Limit:	40.0 A	40.0 A
Iout OC Fault Limit:	52.0 A	52.0 A
Temp Warn Limit:	125 °C	125 °C
Temp Fault Limit:	150 °C	150 °C

Figure 10-7. Phase Commands

10.8 All Config

Use the *All Config* tab (Figure 10-8) to configure all of the configurable parameters, which also shows other details like Hex encoding.



Configuration TPS546D24A @ PMBus Addr 36d (24h) / I2C Addr 72d (48h)

Sort Parameters By:
● Command Name
○ Command Code
☑ Group by Category

Command	Code	Value/Edit	Hex/Edit
▼ Calibration			
IOUT_CAL_GAIN phase ALL	0x38	1.000	0xC880
IOUT_CAL_OFFSET phase ALL	0x39	0.0000 A	0xE000
VOUT_SCALE_LOOP	0x29	0.500	0xC840
VOUT_TRIM	0x22	0.000000 V	0x0000
▼ Configuration			
FREQUENCY_SWITCH	0x33	550 kHz	0x0226
IC_DEVICE_ID	0xAD	0x54495…	0x54…
IC_DEVICE_REV	0xAE	0x4000	0x4000
INTERLEAVE	0x37	Group ID…	0x0020
MISC_OPTIONS [MFR 29]	0xED	PEC: Fals…	0x0000
PGOOD_CONFIG [MFR 19]	0xE3	PGood O…	0x009F
PIN_DETECT_OVERRIDE [MFR 30]	0xEE	Stack Co…	0x1F2F
SMBALERT_MASK_CML	0x1B	00000000	0x00
SMBALERT_MASK_INPUT	0x1B	11101000	0xE8
SMBALERT_MASK_IOUT	0x1B	00011000	0x18
SMBALERT_MASK_MFR_SPECIFIC	0x1B	01000010	0x42
SMBALERT_MASK_OTHER	0x1B	00000001	0x01
SMBALERT_MASK_TEMPERATURE	0x1B	00000000	0x00
SMBALERT_MASK_VOUT	0x1B	00000010	0x02
STACK_CONFIG [MFR 28]	0xEC	Bcx Stop…	0x0001
SYNC_CONFIG [MFR 20]	0xE4	SYNC_DI…	0xF0

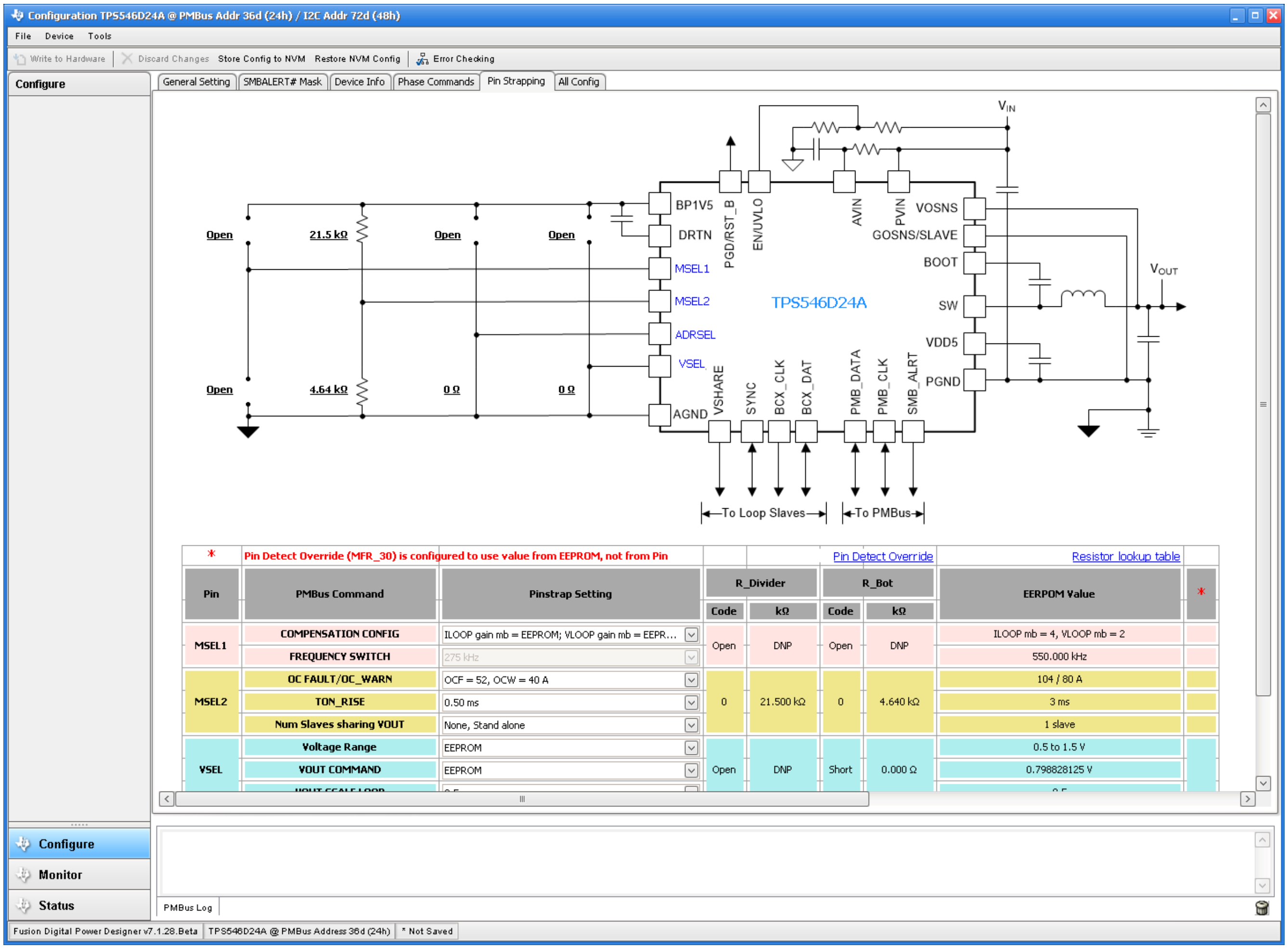
Command	Code	Value/Edit	Hex/Edit
▼ Manufacturer Info			
CAPABILITY	0x19	0xD0	0xD0
MFR_MODEL	0x9A		0x00…
MFR_REVISION	0x9B		0x00…
MFR_SERIAL	0x9E		0x00…
PMBUS_REVISION	0x98	0x33	0x33
▼ On/Off Configuration			
ON_OFF_CONFIG phase ALL	0x02	0x17	0x17
OPERATION	0x01	0x04	0x04
TOFF_DELAY	0x64	0.0 ms	0xF800
TOFF_FALL	0x65	0.50 ms	0xF002
TON_DELAY	0x60	0.0 ms	0xF800
TON_MAX_FAULT_LIMIT	0x62	0 ms	0xF800
TON_MAX_FAULT_RESPONSE	0x63	Click…	0x3B
TON_RISE	0x61	3.00 ms	0xF00C
▼ Status			
NVM_CHECKSUM [MFR 32]	0xF0	Checksu…	0xE9E0
READ_IOUT phase ALL	0x8C	-0.52 A	0xB5F0
READ_TEMPERATURE_1 phase ALL	0x8D	23 °C	0x0017
READ_VIN phase ALL	0x88	3.301 V	0xC34D
READ_VOUT phase ALL	0x8B	0.009766 V	0x0005
STATUS_BYTE	0x78	01000000	0x40
STATUS_CML	0x7E	00000000	0x00

Fusion Digital Power Designer v7.1.28.Beta | TPS546D24A @ PMBus Address 36d (24h) | * Not Saved

Figure 10-8. Configure – All Config

10.9 Pin Strapping

Use the *Pin Strapping* tab (Figure 10-8) to aid in selection of external pin strapping resistors used to program some of the PMBus commands at power-up. The *EEPROM Value* column shows the values currently configured to the related PMBus commands.



* Pin Detect Override (MFR_30) is configured to use value from EEPROM, not from Pin

Pin Detect Override

Resistor lookup table

Pin	PMBus Command	Pinstrap Setting	R_Divider		R_Bot		EERPOM Value	*
			Code	kΩ	Code	kΩ		
MSEL1	COMPENSATION CONFIG	ILOOP gain mb = EEPROM; VLOOP gain mb = EEPR...	Open	DNP	Open	DNP	ILOOP mb = 4, VLOOP mb = 2	
	FREQUENCY SWITCH	275 kHz					550.000 kHz	
MSEL2	OC FAULT/OC_WARN	OCF = 52, OCW = 40 A	0	21.500 kΩ	0	4.640 kΩ	104 / 80 A	
	TON_RISE	0.50 ms					3 ms	
	Num Slaves sharing VOUT	None, Stand alone					1 slave	
VSEL	Voltage Range	EEPROM	Open	DNP	Short	0.000 Ω	0.5 to 1.5 V	
	VOUT COMMAND	EEPROM					0.798828125 V	

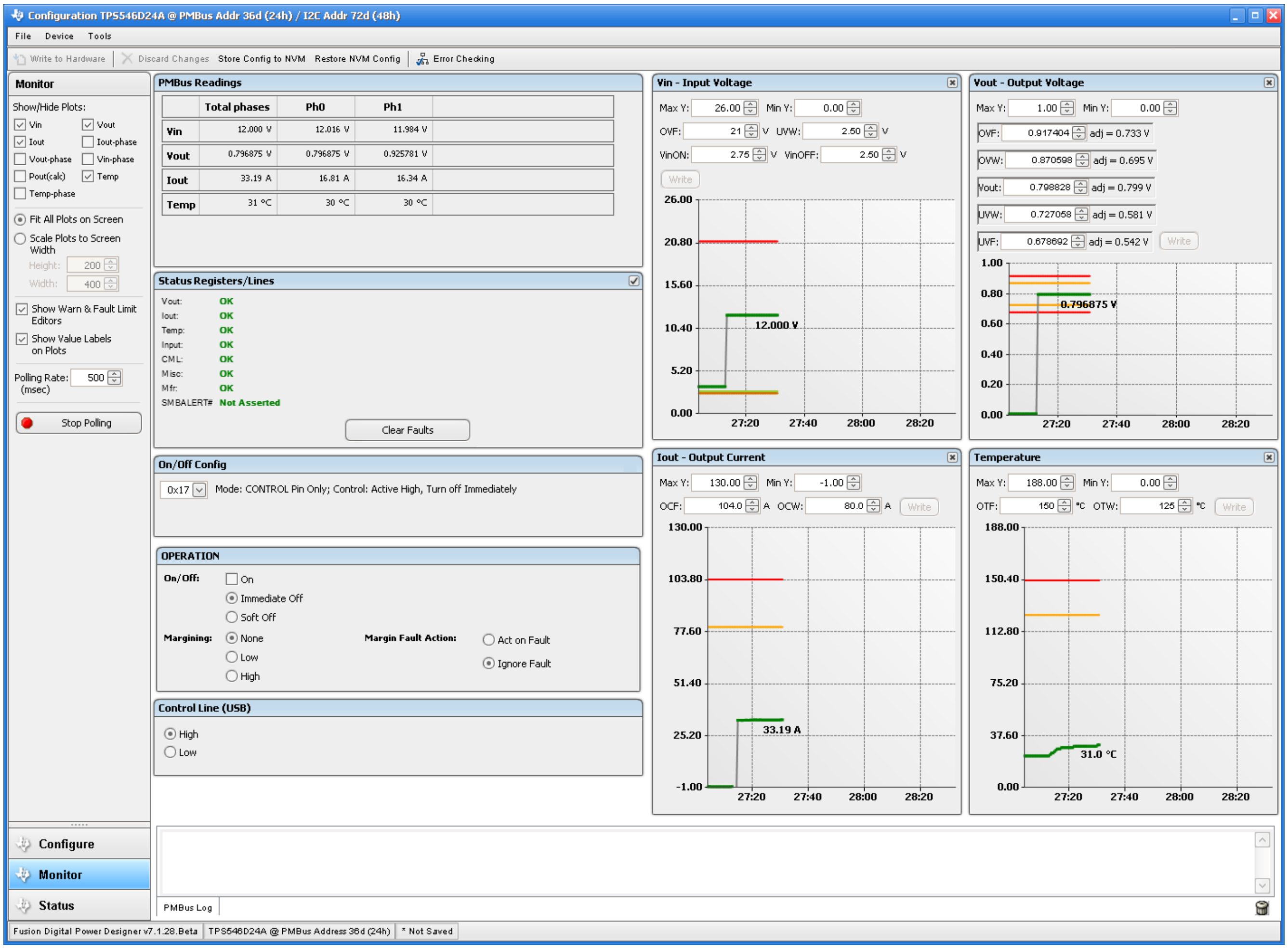
Figure 10-9. Configure – Pin Strapping

10.10 Monitor

When the *Monitor* screen (Figure 10-10) is selected, the screen changes to display real-time data of the parameters that are measured by the device. This screen provides access to:

- Graphs of *Vout*, *Iout*, *Vin*, *Pout*, and *Temperature*
- *Start and Stop Polling* which turns ON or OFF the realtime display of data
- Quick access to *On and Off Config*
- Control pin activation and *OPERATION* command
- Margin control
- Clear Fault: Selecting ***Clear Faults*** clears any prior fault flags.

With two devices stacked together, the *Iout* reading is the total load supported by both devices. There is also an *Iout* which shows the current in each phase.



Configuration TPS546D24A @ PMBus Addr 36d (24h) / I2C Addr 72d (48h)

Monitor

Show/Hide Plots:
☑ Vin ☑ Vout
☑ Iout ☐ Iout-phase
☐ Vout-phase ☐ Vin-phase
☐ Pout(calc) ☑ Temp
☐ Temp-phase

● Fit All Plots on Screen
○ Scale Plots to Screen Width
Height: 200
Width: 400

☑ Show Warn & Fault Limit Editors
☑ Show Value Labels on Plots

Polling Rate: (msec) 500

PMBus Readings

	Total phases	Ph0	Ph1
Vin	12.000 V	12.016 V	11.984 V
Vout	0.796875 V	0.796875 V	0.925781 V
Iout	33.19 A	16.81 A	16.34 A
Temp	31 °C	30 °C	30 °C

Status Registers/Lines

Vout:	OK
Iout:	OK
Temp:	OK
Input:	OK
CML:	OK
Misc:	OK
Mfr:	OK
SMBALERT#	Not Asserted

On/Off Config

0x17 Mode: CONTROL Pin Only; Control: Active High, Turn off Immediately

OPERATION

On/Off: ☐ On ● Immediate Off ○ Soft Off
Margining: ● None ○ Low ○ High
Margin Fault Action: ○ Act on Fault ● Ignore Fault

Control Line (USB)

● High
○ Low

Vin - Input Voltage

Max Y: 26.00 Min Y: 0.00
OVF: 21 V UVW: 2.50 V
VinON: 2.75 V VinOFF: 2.50 V

Vout - Output Voltage

Max Y: 1.00 Min Y: 0.00
OVF: 0.917404 adj = 0.733 V
OVW: 0.870598 adj = 0.695 V
Vout: 0.798828 adj = 0.799 V
UVW: 0.727058 adj = 0.581 V
UVF: 0.678692 adj = 0.542 V

Iout - Output Current

Max Y: 130.00 Min Y: -1.00
OCF: 104.0 A OCW: 80.0 A

Temperature

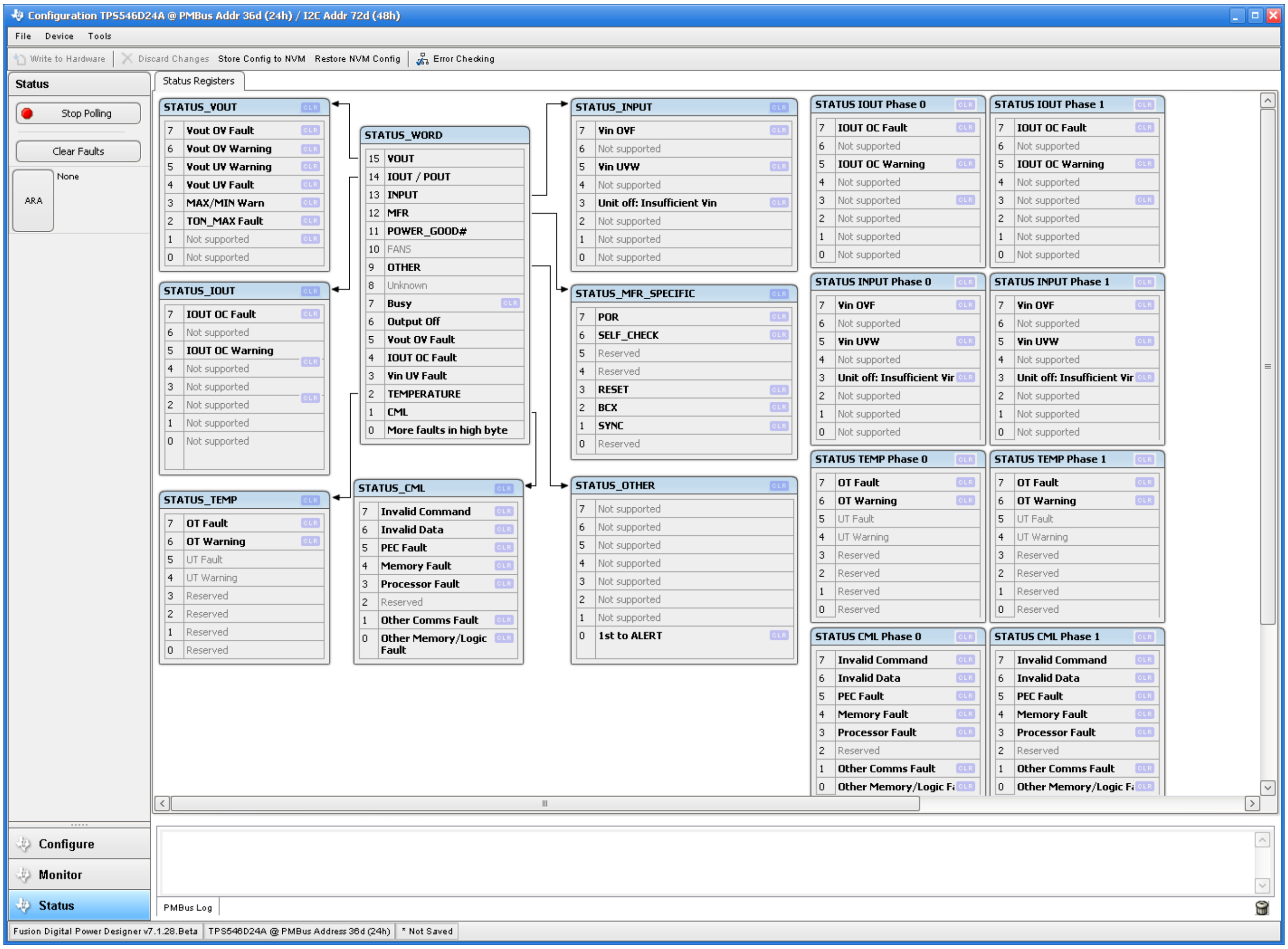
Max Y: 188.00 Min Y: 0.00
OTF: 150 °C OTW: 125 °C

Fusion Digital Power Designer v7.1.28.Beta | TPS546D24A @ PMBus Address 36d (24h) | * Not Saved

Figure 10-10. Monitor Screen

10.11 Status

Selecting *Status* screen from lower left corner (Figure 10-11) shows the status of the device.



STATUS_VOUT	
7	Vout OV Fault
6	Vout OV Warning
5	Vout UV Warning
4	Vout UV Fault
3	MAX/MIN Warn
2	TON_MAX Fault
1	Not supported
0	Not supported

STATUS_IOUT	
7	IOUT OC Fault
6	Not supported
5	IOUT OC Warning
4	Not supported
3	Not supported
2	Not supported
1	Not supported
0	Not supported

STATUS_TEMP	
7	OT Fault
6	OT Warning
5	UT Fault
4	UT Warning
3	Reserved
2	Reserved
1	Reserved
0	Reserved

STATUS_WORD	
15	VOUT
14	IOUT / POUT
13	INPUT
12	MFR
11	POWER_GOOD#
10	FANS
9	OTHER
8	Unknown
7	Busy
6	Output Off
5	Vout OV Fault
4	IOUT OC Fault
3	Vin UV Fault
2	TEMPERATURE
1	CML
0	More faults in high byte

STATUS_CML	
7	Invalid Command
6	Invalid Data
5	PEC Fault
4	Memory Fault
3	Processor Fault
2	Reserved
1	Other Comms Fault
0	Other Memory/Logic Fault

STATUS_INPUT	
7	Vin OVF
6	Not supported
5	Vin UVW
4	Not supported
3	Unit off: Insufficient Vin
2	Not supported
1	Not supported
0	Not supported

STATUS_MFR_SPECIFIC	
7	POR
6	SELF_CHECK
5	Reserved
4	Reserved
3	RESET
2	BCX
1	SYNC
0	Reserved

STATUS_OTHER	
7	Not supported
6	Not supported
5	Not supported
4	Not supported
3	Not supported
2	Not supported
1	Not supported
0	1st to ALERT

STATUS IOUT Phase 0	
7	IOUT OC Fault
6	Not supported
5	IOUT OC Warning
4	Not supported
3	Not supported
2	Not supported
1	Not supported
0	Not supported

STATUS IOUT Phase 1	
7	IOUT OC Fault
6	Not supported
5	IOUT OC Warning
4	Not supported
3	Not supported
2	Not supported
1	Not supported
0	Not supported

STATUS INPUT Phase 0	
7	Vin OVF
6	Not supported
5	Vin UVW
4	Not supported
3	Unit off: Insufficient Vir
2	Not supported
1	Not supported
0	Not supported

STATUS INPUT Phase 1	
7	Vin OVF
6	Not supported
5	Vin UVW
4	Not supported
3	Unit off: Insufficient Vir
2	Not supported
1	Not supported
0	Not supported

STATUS TEMP Phase 0	
7	OT Fault
6	OT Warning
5	UT Fault
4	UT Warning
3	Reserved
2	Reserved
1	Reserved
0	Reserved

STATUS TEMP Phase 1	
7	OT Fault
6	OT Warning
5	UT Fault
4	UT Warning
3	Reserved
2	Reserved
1	Reserved
0	Reserved

STATUS CML Phase 0	
7	Invalid Command
6	Invalid Data
5	PEC Fault
4	Memory Fault
3	Processor Fault
2	Reserved
1	Other Comms Fault
0	Other Memory/Logic F

STATUS CML Phase 1	
7	Invalid Command
6	Invalid Data
5	PEC Fault
4	Memory Fault
3	Processor Fault
2	Reserved
1	Other Comms Fault
0	Other Memory/Logic F

Figure 10-11. Status Screen

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス· インスツルメンツ株式会社
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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*
   - 8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.
   - 8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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